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Additional Documents for Major Projects, Internship

PRINCIPAL
RV COLLEGE OF ENGINEERING
BENGALURU - 560 059

DEPARTMENT OF CIVIL ENGINEERING
R V COLLEGE OF ENGINEERING,
BENGALURU – 560059

BATCH LIST OF STUDENTS FOR EXTENSIVE SURVEY CAMP (12CV74)– JUNE 2018

Sl. No.	USN	Student Name	Gender	Batch No.
1	1RV15CV001	AASTHA RANI	F	
2	1RV15CV022	CHETHAN K S	M	
3	1RV15CV040	KUSHAL RUNTHALA	M	
4	1RV15CV066	PRIYANKA C	F	
5	1RV15CV078	SACHIN S ISHWARAPPAGOL	M	Batch No. 1
6	1RV15CV103	SUJITH S CHINDANUR	M	
7	1RV15CV124	ANIMESH SINGH	M	
8	1RV16CV400	ABHIJITH K K	M	
9	1RV16CV416	PRASHANTH ACHARYA	M	
1	1RV15CV002	ABHIJEET VERMA	M	
2	1RV15CV023	CHETHAN S	M	
3	1RV15CV041	L VINYAS	M	
4	1RV15CV127	AYESHA LEENA MUTALIB	F	
5	1RV15CV080	SAHANA B GANGAL	F	Batch No. 2
6	1RV15CV104	SUMANTH LINGRAJ KUDRIMANI	M	
7	1RV15CV125	ASHAM HUSAIN	M	
8	1RV16CV401	ABHISHEK L	M	
9	1RV16CV417	RAGHAVENDRA K G	M	
1	1RV15CV003	ABHIJITTH S	M	
2	1RV15CV024	DEEKSHITH P R	M	
3	1RV15CV042	LAKSHYA NIDHI	M	
4	1RV15CV061	PRAJWAL ALABURU	M	
5	1RV15CV081	SALONI DUGAR	F	Batch No. 3
6	1RV15CV105	SUSHMITA MADIVALESH MURADI	F	
7	1RV15CV126	ASHWANI KUMAR SINGH	M	
8	1RV16CV402	MUJAWAR AHMEDRAZA MOULALI	M	
9	1RV16CV418	RAVUTAPPA KOLAKAR	M	
1	1RV15CV004	ACHINTYA JACHAK	M	
2	1RV15CV025	DEEPANSHU SWAMI	M	
3	1RV15CV044	MAHAVIR ASTIGIKAR	M	
4	1RV15CV062	PRAKHAR SAXENA	M	
5	1RV15CV083	SANDEEP KUMAR	M	Batch No. 4
6	1RV15CV107	T S PRAJWAL	M	
7	1RV15CV129	DIVYANSHU RAJ	M	
8	1RV16CV403	AJJAYYA K P	M	
9	1RV16CV419	SADDAMHUSEN SONAR	M	

1	1RV15CV005	ADITHYA S N	M	
2	1RV15CV026	DEVANABANDA KESAVA REDDY	M	
3	1RV15CV046	MOHAMMED ASAD ULLAH ALAM	M	
4	1RV15CV063	PRASHANT KISHLAY	M	
5	1RV15CV084	SANDEEP SHANTHINATH PATIL	M	Batch No. 5
6	1RV15CV108	SAGAR T	M	
7	1RV15CV130	KUMAR SIDDHANT	M	
8	1RV16CV404	DILEEPA N	M	
9	1RV16CV420	SOHAIL P KHAN	M	

1	1RV15CV006	AKASH M	M	
2	1RV15CV027	FARUQANWAR MYAGERI	M	
3	1RV15CV047	MOIDIN AFSAN	M	
4	1RV15CV064	PRATIK A VASANAD	M	
5	1RV15CV085	SANGAMESH GANGAVATI	M	Batch No. 6
6	1RV15CV110	TEJA SAI KRISHNA MANIKONDA	M	
7	1RV15CV131	MOHAMMAD ASIF	M	
8	1RV16CV405	GANESH NADIGA D	M	
9	1RV16CV421	TEJASHWINI I Y	F	

1	1RV15CV007	AKASH MADANLAL AGARWAL	M	
2	1RV15CV028	G PRANAV BHARADWAJ	M	
3	1RV15CV049	MRITYUNJAY KUMAR	M	
4	1RV15CV065	PRAVEEN M OSWAL	M	
5	1RV15CV086	SANGAMESH RAGHOJI	M	Batch No.7
6	1RV15CV111	UDAY MISHRA	M	
7	1RV13CV097	RITESH KUMAR	M	
8	1RV16CV406	GURURAJ KURLE	M	
9	1RV16CV422	UDAY B K	M	

1	1RV15CV008	AMEENA LUBNA MUTALIB U	F	
2	1RV15CV029	GAURAV KUMAR SINGH	M	
3	1RV15CV051	NANDISH MAHESH BHATE	M	
4	1RV15CV067	R P ROSHAN	M	
5	1RV15CV087	SANJANA S	F	Batch No. 8
6	1RV15CV112	VAISHAK	M	
7	1RV14CV012	ANU S PRASAD	M	
8	1RV16CV407	KOUSHIK SADANAND NAYAK	M	
9	1RV16CV423	VEERESH TURMARI	M	

1	1RV15CV009	ANAND BASAPPA DODADANNAVAR	M	
2	1RV15CV030	GAUTHAM P PEETA	M	
3	1RV15CV052	NAVEEN K	M	
4	1RV15CV068	RACHAMALLU CHAITHANYA	F	
5	1RV15CV089	SAURABH SHRIVASTAVA	M	Batch No. 9
6	1RV15CV113	VENKATESH BABU	M	
7	1RV14CV037	JUNAID KHAN	M	

8	1RV16CV408	LAVANYA S	F	
9	1RV16CV424	VINUTHA H	F	

1	1RV15CV010	ANIKET SINGH	M	
2	1RV15CV031	GOURISH M NADUGADDI	M	
3	1RV15CV053	NIKHIL GURUSWAMY	M	
4	1RV15CV069	RAJ VEDHANTH G	M	
5	1RV15CV090	SAURABH SINGH KUSHWAHA	M	Batch No. 10
6	1RV15CV114	VENKATESH PRASAD V	M	
7	1RV14CV044	KISHAN M N	M	
8	1RV16CV409	MADHUSUDHAN S	M	
9	1RV16CV425	VIVEKANANDAREDDY	M	

1	1RV15CV011	ANKIT KUMAR	M	
2	1RV15CV032	HARSH S JAIN	M	
3	1RV15CV054	NIKUNJ OSTWAL	M	
4	1RV15CV070	RAJAT VERMA	M	
5	1RV15CV092	SHASHANK S	M	Batch No. 11
6	1RV15CV115	VIGNESH M S	M	
7	1RV14CV062	NAVEEN ALMAJE	M	
8	1RV16CV410	MAHIBOOB H KOTWAL	M	
9	1RV16CV426	YASARANEES NADAF	M	

1	1RV15CV012	ANKITH GOWDA H Y	M	
2	1RV15CV033	HARSHITHA N	F	
3	1RV15CV055	NIPUN K H	M	
4	1RV15CV071	RAJU H V	M	
5	1RV15CV096	SHREYANSH BAID	M	Batch No. 12
6	1RV15CV116	VIJAYANAND PATIL	M	
7	1RV14CV064	NIHAL SATISH	M	
8	1RV16CV412	NAMIT KUMAR A	M	
9	1RV13CV400	CHANDRAKANTH	M	

1	1RV15CV016	ASHRUT KUMAR GAUTAM	M	
2	1RV15CV034	ISHAN BAKSHI	M	
3	1RV15CV056	NITHIN M M	M	
4	1RV15CV072	RAMINENI RISHI KRISHNA	M	
5	1RV15CV097	SHUBHAM KUMAR AGARWAL	M	Batch No. 13
6	1RV15CV117	VINAY KUMAR H S	M	
7	1RV14CV118	VAISHAK B H	M	
8	1RV16CV413	NIHAL D MASUR	M	
9	1RV13CV403	MAHESH M	M	

1	1RV15CV018	BALJIT SINGH KARNAVAT	M	
2	1RV15CV035	JASTI HARSHA VARDHAN	M	
3	1RV15CV057	POORNIMA N	F	
4	1RV15CV073	RANJITH R N	M	Batch No. 14

5	1RV15CV099	SHYAM RAMJI	M	Batch No. 14
6	1RV15CV118	VINAY KUMAR I G	M	
7	1RV12CV072	ADISHWAR SINGH	M	
8	1RV16CV414	PANKAJ KIRAN	M	

1	1RV15CV019	BHARGAV	M	Batch No. 15
2	1RV15CV036	K V S PAVAN BHARADWAJ	M	
3	1RV15CV058	PRACHEER PRANAY	M	
4	1RV15CV074	RAUNAQ SABOO	M	
5	1RV15CV100	SIDDHARTH B S	M	
6	1RV15CV120	VISHWANATH B	M	
7	1RV13CV001	ABHAY TIWARI	M	
8	1RV16CV415	PRABHU	M	

1	1RV15CV020	CHANDRA MOHAN R	M	Batch No. 16
2	1RV15CV037	KARTHIK R	M	
3	1RV15CV059	PRADEEP D	M	
4	1RV15CV075	ROHIT KABRA	M	
5	1RV15CV101	SRINIVAS R J	M	
6	1RV15CV121	VISIKHO ALBERT	M	
7	1RV15CV422	SOUDHAMINI D	F	
8	1RV13CV409	RAGHAVENDRA S	M	

1	1RV15CV021	CHETAN SANGANNA TUNGALAD	M	Batch No. 17
2	1RV15CV038	K G PUNYA KEERTHISH	M	
3	1RV15CV060	PRADEEP K KARANDI	M	
4	1RV15CV076	ROHITH S	M	
5	1RV15CV102	SRUJHANA P	F	
6	1RV15CV123	ABHISHEK MINOCHA	M	
7	1RV15CV413	MAHENDRA H K	M	
8	1RV13CV411	YALLALING	M	

R.V. College of Engineering, Bengaluru – 59

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Department of Industrial Engineering and Management

Course: Major Project Code: 12IM81

Project Batches – 2018-19

Batch	USN	Name of the student	Project Title	Place of Work	Internal Guide	External Guide
1	1RV15IM040	Rakshith Srujan	Productivity Improvement in Cutting Section of Garment Manufacturing Industry	Aditya Birla Fashion and Retail Ltd., Bengaluru	Prof. Shobha.N.S	Mohamed Rafi (Cluster Head), Abhilash (Factory Head)
	1RV15IM034	Pallavi.M				
2	1RV14IM065	Yash Chaudhary	Quality Improvement Study to Increase Production Volume	Precision Drawell Pvt Ltd, Nagpur, Maharashtra	Prof.Vivekanand S Gogi Prof.B. Nandini	Srikanth Dange, Production Manager
	1RV15IM039	Raghav K				
3	1RV15IM020	Harith Talikota	Engineering Change Process Improvement	Ather Energy, Bengaluru	Prof.B. Nandini	Mr. Arindam Bannerjee, Director, Process Excellence
4	1RV15IM036	Phani T Kethana	Improvement Studies on Fiber Optic Cable Assembly	Amphenol FCi, Bannerghatta, Bengaluru	Prof. Shobha.N.S	Mr. Harish R E, Assistant Manager
	1RV15IM006	Adhyayan				
	1RV15IM053	Siddha				
	1RV15IM065	Sagarika R				
5	1RV15IM025	Malavika Menon	Application of Six Sigma Methodology to Non-Standard Royalty Payments	Cisco Systems India Pvt Ltd.	Dr.K.N. Subramanya	Mr. Rishi Singh, Manager- Software & Cloud GSM
6	1RV15IM051	Shwetha Kini	Transformation of Supplier Enrollment for Global Supplier Management	Cisco Systems India Pvt Ltd.	Dr.K.N. Subramanya	Ms. Neha Sharma, Project Specialist
7	1RV15IM043	Saloni Agarwal	Cost Estimation of Parts During Various Phases of Development Cycle	Mercedes Benz R&D, Bengaluru	Dr.Sunil R Y	Mr.Abhinav Dhakar, Senior Design Engineer

Batch	USN	Name of the student	Project Title	Place of Work	Internal Guide	External Guide
8	1RV15IM064	Komal Chhajer	Development of Methodology to Validate Brake Hose Deformations in the Braking System of cars	Mercedes Benz R&D, Bengaluru	Dr.Vikram. N.B	Mr. Bharadwaj P, Product Design Engineer
9	1RV15IM030	Nakul Agarwal	Production Planning and Improving Productivity of Cutting Section of a Garment Industry	Gokaldas Exports, Bengaluru	Prof. Prashant.V Dr.Rajeswara Rao.K.V.S	Mr. Gururaj. P Sr. Industrial Engineer
	1RV15IM056	Sumangal Bhaiya				
10	1RV15IM005	Adarsh Gouli	Enhancing the Customer Satisfaction by Improving the Patient Call Handling System	Narayana Nethralaya, Bengaluru	Prof.B. Nandini	Dr.Bindu, Chief operations Officer, Narayana Nethralaya, Bengaluru
	1RV15IM028	Mohammed Akeef				
	1RV15IM029	Nagdev A R				
	1RV15IM013	Bharath S N				
11	1RV15IM033	P R Anusha	Design and Development of an Intelligent Prototype for Quality Improvement in a Garment Manufacturing Unit	Aditya Birla Fashion and Retail Ltd., Bengaluru	Dr.Rajeswara Rao.K.V.S	Padma Priya , Head of Quality
	1RV15IM023	Likitha R				
	1RV15IM022	Karthik.S				
12	1RV15IM057	Sumedh Atul Bang	Digitalization of Education Loan Origination and Credit Decisioning	Kuliza Technologies Pvt Ltd, Bengaluru	Dr.N.S. Narahari	Uday Kiran reddy M , Director-Delivery
13	1RV15IM004	Aby Babu	Exploratory Study of Bio-Medical Waste Management System	m.Verve, Bengaluru	Dr.Ramaa.A	Mr. Harsha Marigowda, Founder and Business Development Head
	1RV15IM045	Sanket S				
14	1RV15IM032	Nithin Joshy	Development of a Smart Waste Collection Bin and System in Hospitals	m.Verve, Bengaluru	Prof. Bhaskar.M.G Dr.C.K. Nagendra Guptha	Mr. Harsha Marigowda, Founder and Business Development Head
	1RV15IM035	Pavan B				
	1RV15IM011	Arpith C Patil				
15	1RV15IM027	Mayank Sagar	Market Basket Analysis and Recommendation Engine for Effective Target Marketing Using Prescriptive Analytics	MiQ Digital India Pvt Ltd., Bengaluru	Prof. V. Ravishankar	Ms. Rupsha Majumder, Regional Analysis Lead, West & Mid - West US

Batch	USN	Name of the student	Project Title	Place of Work	Internal Guide	External Guide
16	1RV15IM002	Abhash Singhal	Improving the Overall Productivity and Quality of the Operations, Production and Packaging in a Pharmaceutical Industry	Bal Pharma Ltd., Bengaluru	Prof.Varna	Mr. Prithesh, HR Head
	1RV15IM014	D Aniruddh				
	1RV15IM017	Gaurav Jain				
17	1RV15IM015	Deshpande Srivatsa	Robotic Process Automation for Data Extraction from Management of Information System	KPMG	Dr.M.N. VijayaKumar	Mr. Jayant Singh, Manager
18	1RV15IM046	Sejal Srikant B	Design and Development of Tractor Mounted Sugarcane Harvesting Machine	Shri Prabhulingeshwar Sugars & Chemicals ltd. Jamakhandi, Bagalkot	Dr.M.N. VijayaKumar	Mr.Kyadhi, Head of Mechanical & Design Department
	1RV15IM061	Veerupakshayya				
	1RV16IM410	Veeresh Ashok H				
19	1RV16IM400	Kishan Kumar	Design and Development of Bicycle Operated Water Purification System	RVCE	Dr.Rajeswara Rao.K.V.S	–
	1RV16IM401	Krishnanda Naik				
	1RV16IM405	Shailesh M R				
	1RV16IM406	Shamanth R S				
20	1RV15IM003	Abhilash C R	Design and Development of Exoskeleton for Lower Extremities	RVCE	Dr.N.S. Narahari	–
	1RV15IM024	M Abdul Haq				
	1RV15IM055	Sriraksha M				
	1RV15IM058	Tanay Bysani				
21	1RV15IM041	Rohan Kumar	Financial Portfolio Optimisation using Multi Armed Bandit Algorithm	RVCE	Dr.Ramaa.A Prof.Archana.M.S	–
	1RV15IM048	Shivam Tyagi				
	1RV15IM062	Vineet Dash				
	1RV16IM403	Raghavendra P				
22	1RV15IM007	Aditya Batham	Redesign of Last Mile Delivery	RVCE	Dr.K.N. Subramanya	–
	1RV15IM016	Dibyansh Jalan				
	1RV15IM059	Tarun Narayan				
	1RV15IM060	Tejas Kumar				

Batch	USN	Name of the student	Project Title	Place of Work	Internal Guide	External Guide
23	1RV15IM031	Nishchitha M	Predictive Analytics for the Optimal Level Setting for the Fabrication of Thin Film Solar Cells	RVCE	Dr.C.K. Nagendra Guptha	Dr. T K Subramanyam, HOD, Interdisciplinary Research Centre, RVCE
	1RV15IM044	Samyukta R				
	1RV15IM052	Shwetha R				
	1RV14IM066	Shimnaz Ramzan				
24	1RV14IM049	Shivamani N P	Ergonomic Redesign of Paint Brush for Pre Painting Activities	RVCE	Prof.Vivekanand S Gogi Dr.N.S. Narahari	–
	1RV13IM065	Nandishwar S P				
	1RV14IM015	Gavisiddana G				
	1RV15IM406	Sandeep M				
25	1RV15IM026	Manoj K Y	Redesign and Development of Standing Frame for Physically Challenged Children	RVCE in Collaboration with R V College of Physiotherapy.	Dr.C.K. Nagendra Guptha	Dr. Pallavi Wajapay Dr. Sneha
	1RV16IM404	Raufmiyya				
	1RV16IM402	Manu Kiran H K				
	1RV15IM009	Akshay G Shetty				

Internship (Placement)	10
Project (Inhouse)	6
Project (Industry)	9
Total No. of project batches	**25**

Internship (Placement)	13
Project (Inhouse)	24
Project (Industry)	27
Total No. of Students	**64**

R.V. College of Engineering, Bengaluru – 59
(Autonomous Institution affiliated to VTU, Belagavi)
Department of Computer Science and Engineering
Course: Major Project Code: 12IM81

UG PROJECT ACADEMIC YEAR 2020-21

Batch No	Name of the Student	USN	Organization Name	Project Title	Internal Guide
1	Akash P	1RV17EC008	In-House	Deep Compressive Sensing of Image and Video systems	Dr. M Uttara Kumari
	Shashank C Mouli	1RV17EC138			
2	Nandini Mittal	1RV17EC085		Design and Implementation of decision level sensor fusion for classification of signatures	Dr. M. Uttara Kumari
3	DINDUKURTHI K SRAVANI	1RV17EC042		Design and Implementation of Footstep and Vehical Classification System using Deep Learning Algorithms	Prof. Sujata D. Badiger
	Kavya G	1RV17EC060			
	Y Sai Deepak Reddy	1RV17EC186			
4	Tanushree G V	1RV17EC172		Collision avoidance for unmanned surface vehicle	Dr. Nethravathi K.A
	Fadiyah mukhtar	1RV17EC187			
	SHEIKH SAQIB FAYAZ	1RV17EC142			
5	ADVAITH ASHWIN HARISH	1RV17EC006		Obstacle detection in autonomous vehicles using 3D LIDAR point cloud data	Dr. Nethravathi K.A
	M LIKITHA	1RV17EC066			
	N SAI SUMANTH	1RV17EC082			
	REMIDI ROHITH REDDY	1RV17EC122			
6	Ashuthosh N Bhat	1RV17EC025		Channel characterization and measurement of different parameters using LoRa technology for wireless underground channel network	Dr. Nethravathi K A
	Shreyans Gomes	1RV17EC146			
	Shyamanth R H	1RV17EC151			
7	Nidhi S Nair	1RV17EC090		Automatic Image Annotation using Computer Vision	Dr. PN JAYANTHI
	Aditi Modi	1RV17EC005			
	Mishma Toppo	1RV17EC076			
8	Nagesh B	1RV17EC084	QUALCOMM	Machine Learning for Audio Applications	Dr. M. Uttara Kumari
9	Sinchana G	1RV17EC154	Walmart labs	IR portal backend optimization using Sonarqube	Dr. Nethravathi K A
10	Deepika Anantharaman	1RV17EC037	DRDO (Defense Research and Development Organization)	Optimization of Irregular Sub Arrays for efficient Digital Beamforming in Large Phased Arrays	Dr. Nethravathi K.A
11	Srivaths JM	1RV17EC164	HPE - Aruba	Unified Communication and Collaboration Management	Dr. K S Geetha
12	Monica Eswar	1RV17EC195	HPE Aruba	Automation of Route convergence measurement of BGP with BFD	Dr. K S Geetha
13	Pradyumna C	1RV17EC013	Bosch	Vehicle Tracking without GPS	Dr.Nethravathi
14	Harshitha K	1RV17EC051	HPE	Design and Development of Smart City IoT Solution	Prof Sujata D Badiger
15	Darshan Haragi L	1RV16EC048	In-House	Infrastructure Optimization in Kubernetes Cluster	Prof. Sahana B
	Mahith S	1RV15EC078			
	Kushal Kalyan P M	1RV16EC080			
16	Pranshu Chaurasia	1RV17EC107		Comparison between FACS Humanoid Head Design and Symbolic Humanoid Head for Low-Cost Humanoid Design	Prof. Arunkumar P Chavan
	Preetham R	1RV17EC109			
	Prabuddh M	1RV17EC101			
17	Deekshith Nayak	1RV17EC035	Endurance International Group	Migrating a Stateful Service to Openshift by using Operators	Dr. H V Ravish Aradhya
18	Ankitha	1RV17EC017	Samsung Semiconductor India Research	ISP CoreSIM framework for Design Verification	Dr. H V Ravish Aradhya
19	Prakash S Bhat	1RV17EC105	Sandvine	Internet traffic categorization, shaping and whitelisting based on IP Geolocation technology	Dr. Ramya S
20	Shriya Barpanda	1RV17EC149	Cisco	Controller Service and Kong API Gateway for Controller Framework	Dr. Ramya S
21	Sudheendra Hegde	1RV17EC167	Cisco Systems (India) Pvt. Ltd.	Configuration Change Notification Using Syslog Messages	Dr. Ramya S
22	Arpitha O Naik	1RV17EC023	Qualcomm	Integration and design verification of the IP cores on a SoC	Prof. Arunkumar Chavan
23	Elizabeth Kuruvilla	1RV17EC044			

24	Rohan Antony Viji	1RV17EC127	FANUC INDIA PVT LTD	Design and Implementation of Industrial Robots for Factory Automation	Prof. Arunkumar Chavan
25	AKSHAY.M.S	1RV13EC015	In-House	Automated terrain surveying using a remote controlled robot	Dr. Nagaraj Bhat
	MAMATA	1RV15EC413			
	PRAJWAL	1RV16EC114			
26	Hamsa G	1RV18EC406		Computer Vision Based IoT Enabled Grape Fruit Disease Detection and Monitoring System	Prof. Mahendra B M
	Nayana V	1RV18EC413			
	Shahista Kousar	1RV18EC427			
27	Darshan S Gowda	1RV18EC403		Grape Morbidity Detection and Medication	Prof. Mahendra B M
	Karthik S S	1RV18EC408			
	Kiran V	1RV18EC409			
	Saurabh Kumar	1RV18EC425			
28	PAURUSH GUPTHA	1RV17EC097	o9 Solutions	Time Series Forecasting to predict Stock trends	Dr. Nagaraj Bhat
	RISHIKESH NANDA	1RV17EC125			
	SAGAR.T	1RV17EC133			
29	Rakshata Karligannavar	1RV17EC119	Hewlett Packard Enterprise	Design and Development of A Federated Service	Dr.Nagaraj Bhat
	Varsha Kulkarni	1RV17EC177	Hewlett Packard Enterprise	Automated deployment and configuration of NetworkOrchestrator for monitoring and managing SAN	
30	Roshni Sen	1RV17EC128	Rakuten	Design and Development of NFC-Enabled Rakuten Pay Mobile Application	Dr. Nagaraj Bhat
31	Sonali Ajit Karki	1RV17EC159	Cisco	Router Components Cataloging System	Dr. Kiran V
32	Sowjanya M	1RV17EC160	Cisco Systems	Design and Implementation of a Simulator for Routers	Dr. Kiran V
33	Niveditha.V.K	1RV17EC096	CISCO	Designing a tool for automatic software upgrade in data centers	Dr. Kiran.V
34	Prajwal S Telkar	1RV17EC104	Cisco Systems	Implementation of routing process on NLP part of LINA in Firepower Threat Defense	Dr. Kiran V
35	RAHUL RAJ D N	1RV17EC116	CISCO	Decoupling Signaling and Media Planes into different containers	Dr. Kiran V
36	Rakshak Udupa T S	1RV17EC118	In-House	BIST with Adaptive Low Power TPG and Optimized ORA for a Start-Up Sequence Controller of a Mammography Machine	Prof. Namita P
	Shashank K Holla	1RV17EC139			
37	Mahesh Bhat K	1RV17EC069		Design of ATPG Simulation Tool with UI	Prof. Namita P
38	Siddharth P	1RV15EC148		Design and development of Electronic nose for Explosive Chemical Detection.	Prof. Neeta Malvi
	Shashank S	1RV16EC144			
	Saketh Saran M	1RV16EC139			
	Shreyas BM	1RV15EC140			
39	Abhinav S	1RV17EC003		Design of Trans Impedance Amplifier	Dr. Nithin M
	Nithin Kumar B G	1RV17EC094			
40	Bishwapa Sanyal	1RV17EC193	Microchip Technology	Verification of Firmware based NVMe Host	Prof. Namita P
41	NISCHITH T R	1RV17EC093	Ansys		Prof. Namita P
42	Spoorthi G Gojanur	1RV17EC161	Qualcomm	UPF based Design and Synthesis of Low Power Techniques in a SoC having DVFS and Power Islands	Dr. Shylashree N
43	Ananth G S	1RV17EC194	Texas Instruments	Characterization Of ADC And PMBus In Power ICs In a Test Environment Using Eagle Tester	Dr. Shylashree N
44	Sarvesh Shashidhar	1RV17EC137	AthenaHealth	Technological Solutions for Healthcare Industry	Dr. Shylashree N
	Rakshit J C	1RV17EC120			
45	FIRDOSH A D	1RV18EC404	ColorTokens	Automation in testing for network security	Prof. Neeta Malvi
46	Manoj Naik	1RV17EC073	Colortokens		
47	SHRIDHAR P PRABHU	1RV17EC148	Colortokens		
48	Sohan S A	1RV17EC158	ColorTokens		
49	SHIVANS GUPTA	1RV17EC143		Design and Development of Hybrid Algorithm for Interactive Recolouring of Wall.	Dr. Abhay Deshpande
	Sachin Goyal	1RV17EC131			
	Faizan Munazeer	1RV17EC045			
50	G.V. Keerthi	1RV17EC046		Comprehensive Monitoring And Remote Control Of Therapeutic	Dr. Abhay Deshpande
	Ramya. N	1RV17EC121			

50	Suchitra. N. S	1RV17EC166	In-House	Exoskeleton For Muscular Dystrophy Physiotherapy	Dr. Abhay Deshpande
	Ramya. B	1RV18EC420			
51	Singa Reddy Bhagya Lakshmi	1RV17EC155		Design and development of an algorithm to detect and diagnose the Parkinson's disease	Dr. Abhay Deshpande
	Siri S Gowda	1RV17EC156			
	Trisha A	1RV17EC174			
52	Nitin Kumar Ojha	1RV17EC095		Solar Powered Agribot with Multiple operations	Dr. Abhay Deshpande
	Manjunath G	1RV17EC071			
53	SHUBHANKAR	1RV16EC155		Detection and Classification Of Malicious URLs and Websites	Dr. Prakash Biswagar
	SIDDHARTHA BHAUMIK	1RV16EC156			
54	SHIVANSH BISHEN	1RV17EC144		Signature Image Hiding in Colour Image using Steganography and Cryptography based on Digital Signature Concepts	Dr. Prakash Biswagar
	Saloni Rao	1RV16EC140			
	Paurav Malik	1RV16EC107			
55	Amisha Singh	1RV17EC011		Prevention of phishing attacks on online voting systems using Visual Cryptography	Dr. Prakash Biswagar
	Nandini S	1RV17EC086			
	Pawana S	1RV17EC098			
	Supriya C	1RV17EC169			
56	Dhanush U	1RV17EC038		Secure File Transfer over Virtual Machine Instances using Hybrid Encryption Technique	Dr. Prakash Biswagar
	Prasannasai S H	1RV17EC108			
	Raghavendra H M	1RV17EC112			
	Sandur Shreesha	1RV17EC136			
57	Anilkumar M G	1RV18EC400		Detection of Diseases in Arecanut using Conventional Neural Networks	Dr. Abhay Deshpande
	Karibasaveshwara TG	1RV18EC407			
	Pavan HK	1RV18EC416			
	Sainath Urankar	1RV18EC422			
58	Neha Suresh	1RV17EC087	IISc	Predicting Groundnut plant disease using CNN models	Prof. Roopa J
59	Nikhil Chandra BS	1RV17EC091	Cypress Semiconductors	Design and Development of Contactless Liquid Level Sensing using CapSense®	Prof. Roopa J
60	Anubhav Dinkar	1RV17EC019	Nutanix		Dr. Prakash Biswagar
61	RANJITH A C	1RV17EC423	In-House	Modeling and Simulation of Battery Management System for Electric Vehicles	Dr. KARIYAPPA B S
	SACHIN K M	1RV17EC426			
	RAVI P BHOVI	1RV14EC126			
62	MANJUNATHA R	1RV17EC072		Implementation of sparse techniques for mimo channel estimation	Dr. P N Jayanthi
	AKASH	1RV17EC007			
	S RAMITH	1RV17EC130			
	SOURAB M	1RV16EC161			
63	NAGARJUN J	1RV14EC093		Design and Analysis of E and F Shaped MSPA	Dr. P N Jayanthi
	NEELANSH GUPTA	1RV14EC096			
	VARUN S	1RV14EC179			
	VINAY RAJASHEKAR	1RV16EC182			
64	Bhargav N	1RV17EC028	Epsilon	Real time office Seat Management System	Dr Jayanthi P N
65	Abhayakumara S Basutakara	1RV17EC001	Athenahealth		Dr. Jayanthi P N
66	Juhie Fadnavis	1RV17EC054	Qualcomm	Physical Design Implementation of a Hard Macro in a DDR Subsystem of a Snapdragon SoC	Dr. B.S. Kariyappa
67	Lavanya B S	1RV18EC410	In-House	Kannada script Analysis in E-Governance	Prof. Rajith B. K
	Anusha D	1RV18EC401			
	Shivanad Rugi	1RV18EC410			
68	Prachii K.	1RV17EC102	Outdu Mediatech		Dr. Shushrutha K S
69	Udbhav Vikas	1RV17EC175	o9 solutions	Demand Planning Solution for Cosmetic Industry using o9 Platform	Prof. Rohini Hallikar
	Karthik Sunil	1RV17EC057			
70	Ankith Kumar Rathore B	1RV17EC016	Signaltron (Signalchip)		Prof. Rohini Hallikar
71	Ammati Vinaykumar	1RV17EC012	ZS Assosciates	Segmentation and call planning exercise for Oncology therapeutic area	Prof. S Praveen

72	Nafisa Ali	1RV17EC078	ZS ASSOCIATES	Developing a UI based on classification of theauptic areas based on Streamlit Based Application	Prof. S Praveen
73	Vijayalaxmi Nuchchi	1RV17EC179	SAP Labs	Development of mediation and charging tools for CPEA Consumption model	Prof. S Praveen
74	Mahesh Chandru C	1RV17EC070	Cognizant	Customization of ITSM module using Service-Now platform	Prof. Rajith B. K
	Pramath Bharadwaj S	1RV17EC106			
	Rahul J	1RV17EC114			
	Rahul Ratnu Chavan	1RV17EC117			
75	Nekkanti Visaal	1RV17EC088	TESSRAC	Heart disease detection using machine learning	Prof. Rajith B. K
76	Snehal Rajesh Lalage	1RV17EC157	Qualcomm	SysMonApp	Dr. Mahesh A
77	SAHIL VIDAY SINGH	1RV17EC188	Cardinal Health	Mobile App test Automation	Dr. Mahesh A
78	Rhutu Kallur	1RV17EC123	Whatfix		Prof. Sujatha D Badiger
79	Chayank S	1RV17EC032	Phone Pe		
80	Suhas T M	1RV17EC168	HPE	CI/CD devops	Prof. Sowmya Nag K
81	Sandesh Krishna Shetty	1RV18EC423	Analog Devices	Validation of Wireless Battery Management System (wBMS)	Prof. Sowmya Nag K
82	Mayuka C	1RV17EC074	HPE	Automation Testing on HPE OneView	Dr. Geetharani P
83	Rohit Veeradhi	1RV17EC178	HPE	Automation in Order Processing	Dr. Geetharani P
84	Geethanjali S	1RV18EC405	In-House	A real time distress monitoring system for geriatric people	Dr. Srividya P
	Lavanya S	1RV18EC411			
	Priyanka Vinayaka Bhandari	1RV18EC417			
85	Rakshitha N D	1RV18EC419		Bank locker security system	Dr. Srividya P
	SEEMA A S	1RV18EC426			
	SANDUR ANITHA	1RV18EC424			
86	Chandana	1RV17EC030	Cypress Semiconductors	Performing Logic Equivalence Check and Low Power Check on an ASIC design	Dr. Srividya.P
87	Chetan	1RV17EC033	Analog Devices India Private Limited	Validation of Wireless Battery Management System (wBMS) - Gen 2	Prof. Sujatha Hiremath
88	Shravan M Jakkannavar	1RV17EC145	Texas Instruments	Design and Characterization of Level shifter cell library for hpa9 process	Prof. Sujatha Hiremath
89	Akshay Narayan Pai	1RV17EC010	Amagi Media Labs Pvt. Ltd	Real Time implementation of HDR Deinterlacing	Prof. Sahana B
	Vinay Varma Bhupathiraju	1RV17EC181			
	Karthik	1RV17EC056			
90	Dandolu Chetan Karthikeya Reddy	1RV17EC034	Hewlett Packard Enterprise	PLDM Framework development to simulate PLDM Implementations on PLDM Capable devices	Prof. Sahana B
91	Gautham S	1RV17EC047	Infinite Computer Solution India Limited		Prof. Sahana B
	M Abhijit	1RV17EC065			
92	Soudri Sai Vishnu	1RV17EC197	Cisco Systems	Enhancement of observability in WebEx contact center	Prof. Sahana B
93	Arjun Kankanavadi	1RV18EC402	In-House		Prof. Deepika P
	Rajkumar	1RV18EC418			
	Jafar Sharif	1RV17EC411			
	Jagdeesh Kishore	1RV14EC059			
94	Swaroop	1RV17EC171	Analog Devices India Private Ltd	Safety application with ADI SIMD processor using 3D ToF	Prof. Deepika P
95	Poornima Asuti	1RV17EC100	Signaltron Systems Pvt. Ltd.	Design and testing of Robust 50W RF Transmitter modules for GSM/WCDMA/LTE based Remote Radio Head applications	Prof. Deepika P
96	Peddi Saurabh	1RV17EC099			
97	Vishnu Teja Raju G	1RV17EC182	Qualcomm	Design of BC Dataset of TDPM using CRDL	Dr. Shilpa D R
98	Anirudh Kashyap	1RV17EC014	Texas Instruments	Design for Testability	Dr. Shilpa D R
99	Divyananthan C	1RV17EC043	Qualcomm	Static Timing Analysis for PD Signoff	Dr.Shilpa D R
100	Shreyas Rao	1RV17EC147	Analog Devices India	Verification of Vital Sign Monitoring platform using C++ SDK	Dr. Shilpa D R
101	GOLLAMUDI SAI SRIKAR	1RV17EC048	Cypress Semiconductor	PSoC Full chip verification	Prof. Sowmya KB
102	Kevin Mathew	1RV17EC061	Cypress Semiconductors (An Infineon Technologies Company)		Prof. Sowmya K.B

103	Siddarth Sai Amruth Yetikuri	1RV17EC152	Analog Devices	Implementation of TIE functions in Xtensa processor for performance enhancement of chip	Prof. Sowmya K B
104	CHARU LATKAR	1RV17EC196		Railway Track Monitoring System using Machine Learning	Prof. Ravishankar Holla
	SOUBHIG SHOME	1RV14EC159			
	RIshan Rai	1RV15EC120			
105	PRATEEK	1RV14EC112	In-House	Disease Prediction by Machine Learning	Prof. SUBRAHMANYA KN
	NITIN KUMAR	1RV16EC416			
	BANNAPPA	1RV16EC401			
	SARAVANA V	1RV16EC431			
106	Tharun Sivakumar	1RV17EC173	ABB		Prof. Ravishankar Holla
107	Amrathesh	1RV17EC192	ARM Embedded Technologies Private Ltd.	Architecture Compliance Kit on Arm based servers	Dr. Govinda Raju M
108	Arpita S.K	1RV17EC022	ARM Embedded Technologies Private Ltd.	Design and development of Fixed Virtual Platforms	Dr. Govinda Raju M
109	Maanas M D	1RV17EC067	Mentor Graphics	Development of an automated test framework for Mentor Embedded Linux based products	Dr. Govinda Raju M
	Sahana K S	1RV17EC190			
110	Nagendra Kumar Jamadagni	1RV17EC083	Qualcomm	Reduction in Communication Overhead in Heterogeneous Multicore Systems	Dr. Govinda Raju M
111	Srayan Sankar Chatterjee	1RV17EC163	Rober Bosch Business and Engineering solution	Enhancement and development of FOTA packaging tool for software updation in ECUs	Prof. Subrahmanya K N
112	Vivek Thomas Matthew	1RV17EC185	Qualcomm	Design and Automation of Floorplan for SoC at Subsystem Level	Prof. Subrahmanya K N
113	Mahantesh Magi	1RV17EC068	In-House	Development of printed CNT/Metal Oxide Nanocomposite thinfilm for sensor and device application	Dr Ramavenkateswaran N
	Rahul.M.G	1RV17EC115			
	Sammed Endoli	1RV17EC135			
	Srujan R Rajanalli	1RV17EC165			
114	Niranjan V	1RV18EC415		PLC based Intelligent Storm Drain Cleaning System	Prof. Pratibha K
	Vinaykumar G	1RV18EC435			
	Vinay M	1RV17EC180			
	Vinay B	1RV18EC434			
115	Nishant Agrawal	1RV17EC189		Objective Function Estimation	Dr Ramavenkateswaran N
	Kumar Shashank	1RV17EC063			
	Shashank.R.S	1RV17EC140			
116	Praneeth Reddy M	1RV17EC077	HPE	FrontEnd GUI using react js	Prof. Sujata Priyambada Mishra
117	Mayur Raj Singh Chouhan	1RV17EC075	zs associates		Prof.. Sujata Priyambada Mishra
118	Abhinav Agarwal	1RV17EC002	Bosch	DESIGN OF SUBSYSTEMS IN A 2-WHEELER ELECTRIC VEHICLE	Prof. Pratibha K
	Abhishek H Chachadi	1RV17EC004			
	Akshay Kumar Singh	1RV17EC009			
	Sabit Auti	1RV18EC421			
119	Rithwik Goel	1RV17EC126	PwC	Feature implementation , Testing & Analytics in Property & Casualty Core Insurance Systems	Prof. Pratibha K
	Hardik Devrangadi	1RV17EC050			
	Vishnusai Reddy Tadiparthi	1RV17EC183			
120	Nagaraj N	1RV17EC079	Signalchip Innovations	Schematic and Physical Design of a high-speed, low-power Custom library for RISC-V processors	Dr. Nithin M
121	Nagaraja Sekhar Uppugunduri	1RV17EC080	Texas Instruments	Reliable selection of Hot Swap FETs for high power designs	Dr. Nithin M
122	NIRMALA J P	1RV17EC417	In-House	Retrofitment of electronic system for enhanced safety features	Dr.Usha Rani K
	SACHIN B	1RV15EC122			
	VIDYA D S	1RV17EC433			
123	Aniruddh M	1RV17EC013	Qualcomm	Simulate video dejitter buffer behavior from existing logs collected from network	Dr. Usha Rani.K.R
124	Anjana Mahaveer Daigond	1RV17EC015	Tejas Networks	Induction of 75GHz Channel Spaced Optical Add-Drop MDU in C-band	Dr. Usha Rani.K.R
125	Bille Giriteja	1RV17EC029	Epsilon		Dr. Usha Rani.K.R
126	Karan Bantia R	1RV17EC191	SAP labs	implementation and integration of alternative clauses in enterprise contravt assembly	Prof. Chethana G
127	Vajra R Singh	1RV17EC176	RBEI	Design of DC-DC converter for automotive telematics	Prof. R Sindhu R
128	Purushottam Joshi	1RV17EC111	RBEI	Battery Management system for Electric vehicles	Prof. R Sindhu R

129	Rahul Desingh S	1RV17EC113	Bosch	Automation of sensor testing	Prof. R Sindhu R
130	Sindhu T S	1RV18EC430		Design and Development of Functionalized CNT an rGO based Thin Film Sensor for Mercury Ion Detection	Dr Rajani Katiyar
	Sneha Jain H D	1RV18EC431			
	Vidyashree V	1RV18EC433			
131	Ankur	1RV17EC018	Qualcomm	Improving the performance of Hardware adaptive filter	Dr. Veenadevi
132	SR. Ahrthi	1RV17EC162	Telstra	On prem cloud solution for virtual network functions	Dr. Rajani Katiyar
133	Vishwas V	1RV17EC184	Samsung Semiconductor India Research	Validation of SFR and SRAM testing using UVM RAL model	Dr. Rajani Katiyar
134	Apoorvaditya Singh	1RV17EC021	Infinite computer solutions	Cloud storage auditing with deduplication with strong privacy protection	Prof. Anusha L S
	Dhanyashree R Prasad	1RV17EC039			
	Dileep Kumar B.C	1RV17EC041			
	Samiksha Rana Singh	1RV17EC134			
135	Nidhi Ravi	1RV17EC089	Kuliza Technologies	Providing Digital Solutions in Lending-SME Loan Product	Prof. Anusha L S
136	Nikhil G Mudakavi	1RV18EC414	Publicis Sapient	Inventory Management Website for maintenance of the corporate computer equipment's.	Prof. Anusha L S
137	HK Kiran Kumar	1RV17EC049	Cisco Systems India Pvt Ltd	Deployment of Static analysis tool in CI/CD pipeline and developing a SAN Simulator GUI	Prof. Shwetha Baliga
	K Subrahmanya	1RV17EC055			
	Kavana R	1RV17EC059			
138	N R Pavan Santosh	1RV17EC092	BOSCH Limited	Vehicle Driver Model for Powertrain parameters estimation	Prof. Shwetha Baliga

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UG PROJECT ACADEMIC YEAR 2022-23

Sl No	USN	Name	Project Title
1	1RV19CS098	Navnith Bharadwaj	Fire detection on drone captured images using ensemble learning
	1RV19CS006	Aditya Singh	
	1RV19CS010	Akshay Kumar Nalatawad	
	1RV19CS185	Vijay Raghav	
2	1RV19CS117	Praneeta Immadisetty	Implementation of optimized image processing library using opencl
	1RV19CS084	Manali M Ranade	
3	1RV19CS032	Ayush Dubey	Art generation using arbitrary style transfer
	1RV19CS134	Sagarika M D	
4	1RV19CS115	Prajwal Vijay Kamble	Decentralized crowdfunding using blockchain
	1RV19CS163	Srikantha M L	
	1RV19CS184	Vijay Kumar S	
	1RV19CS187	Vishnu B G Bharadwaja	
5	1RV19CS007	Akansha Banerjee	Hierarchical block chain design for e-voting system
	1RV19CS120	Priyanshu Kumari	
6	1RV19CS075	Koushik B N	Decentralized crowdfunding using blockchain
	1RV19CS090	Mohammed Rafiq BI	
	1RV19CS127	Revanth K	
	1RV18CS147	Shabaaz Ahmed	
7	1RV19CS026	ASHFAQ HUSSAIN SYED	Design and development of neend mattress ecommerce portal with ar/vr features
	1RV19CS024	ARYAN RAJ SINHA	
	1RV19CS034	AYUSH RAJ SINGH	
	1RV19CS036	B MITHRA VARUN	
8	1RV19CS063	Jagruth H	Ai assisted classification of rice diseases and insect pest for crop growth management
	1RV19CS174	Thoyaj Shankar	
	1RV19CS051	G Mahikshith	
	1RV19CS192	Yogesh K N	

9	1RV20CS400	Akshay R M	Emotion based music recommendation system using deep learning
	1RV20CS404	Ganavi G R	
	1RV20CS405	Imran Nazeer Ulla Khan	
	1RV20CS412	Raghu L	
10	1RV19CS089	Mohamed Moin Irfan	Synthetic underwater image data set generation using deep neural networks
	1RV18CS121	Prerana Shekar M S	
	1RV19CS122	Purnodeep Rajankar	
	1RV18CS146	Sathvik Gowda M	
11	1RV18CS176	SUKRIT THAKRAN	A deep relevance matching model for ad-hoc retrieval
	1RV18CS047	CHINMAY MIRANI	
	1RV19CS003	ABHISHEK KUMAR	
	1RV18CS014	AKSHAY H	
12	1RV19CS078	Kumar Prakhar	Crop yield prediction and fertilizer recommendation
13	1RV19CS124	Rachit Dwivedi	Automating and scaling of wireless devices and features using network virtualization
14	1RV19CS070	Keerthan Kumar A	Adaptive anomaly detection system for software defined networks
	1RV19CS091	Mohammed Zaid Sikander	
	1RV19CS101	Nikhil V Hegde	
	1RV19CS109	Omprakash	
15	1RV19CS015	Aman Kumar	Voice based email system for visual impaired using ai
	1RV19CS407	Nethravathi T	
	1RV18CS428	Ranjith Kumar M E	
16	1RV17CS109	Pramod H P	Alzheimer’s disease prediction using convolution neural network
	1RV18CS141	Sachin	
	1RV19CS030	Avyakth M	
	1RV20CS402	Charan Kumar V M	
17	1RV19CS097	NAMYA LG	Cloud native approach to data governance
	1RV19CS100	NIDHI GK	
18	1RV19CS142	Settipalle Sahithi	Emergency tweet categorisation and prioritisation system using bert
	1RV19CS147	Shashwat Sahu	
	1RV19CS180	Vasudev Seth	
19	1RV20CS411	P Kushala	Fish detection and classification using yolov7
	1RV20CS406	Kishor Manahoar Adde	Underwater naval Mines Detection Using Deep

20	1RV20CS408	Mahantesh Kamate	Convolution
	1RV20CS416	Swaraj Sanjay Somanache	Neural network

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Sl No	USN	Name	Project Title
1	1RV19CS001	Abdur Rahaman	Customizable Benefits Management Solution
2	1RV19CS002	Abhay H Kashyap	Device Firmware Update and its application in Voice and Music
3	1RV19CS004	Adarsh Ramakrishna Hegde	Scout open data architecture for work graph
4	1RV19CS005	Adithi Viswanath	Firmware Development on Cloud AI 100 accelerator
5	1RV19CS008	Akshat Bansal	Derive Caregiver efficiency and evaluate Patient Experience
6	1RV19CS009	Akshat Khare	Devops Audit Dashboard
7	1RV19CS011	Akshay Mammen Koshy	Efficient Archival Data Migration to Amazon S3 leveraging automation for streamlined transfer and retrieval
8	1RV19CS012	Akshay Shankar	Monitoring Tools for Primera, Alletra and Distributed Storage Systems
9	1RV19CS013	Akshita Gupta	Route Streaming for Nexus Cloud
10	1RV19CS014	Alle Naga Rishikesh Reddy	Design and development of mobile application to upskill underprivileged children in English domain
11	1RV19CS016	Amish Chopra	Elastic Charging Engine
12	1RV19CS016	Amish Chopra	Elastic Charging Engine, Churn Prediction
13	1RV19CS017	Anish A S	Dynamic Inventory management
14	1RV19CS018	Ankit	Efficient Migration of Omniture and Security Optimisation of Funnel
15	1RV19CS019	Annapoorneswari	Zephyr Porting and Qualification of the Port
16	1RV19CS020	Anupama Shalavadi	DLC feature in commercial automation lighting
17	1RV19CS021	Anvithkumar A Shetty	Converged charging system
18	1RV19CS022	Arthik Bhandary	Customizable Benefits Management Solution
19	1RV19CS023	Aryan Agarwal	Wealth Strategy Analytics Automation

20	1RV19CS025	Aryn Barman	Model Interpretability for Deep Learning Models in Object Detection
21	1RV19CS027	Ashish Ballatigi	Firmware Development on Cloud AI 100 accelarator
22	1RV19CS029	Athreya V Shet	Customizable Benefits Management Solution
23	1RV19CS031	Ayaz Abdulla A A	creating monitoring dashboard for safe streaming jobs
24	1RV19CS035	B Aravind	Users classification and click prediction using Recommendation engine
25	1RV19CS039	Chakit Kalra	Security Operations Center (SOC) Dashboard and Risk Register
26	1RV19CS040	Charan M R	Conversion of Legacy Chef Recipes to Ansible
27	1RV19CS041	Chinmay B S	Development of application to map various network configuration commands
28	1RV19CS042	Darshan J	Design and development of utility for Elasticsearch cluster sizing and resource planning
29	1RV19CS043	Deepankur Gupta	Regulatory reporting for OTC credit data
30	1RV19CS044	Dency Narendra Patel	Developing BMS application and integration with AIMS portal
31	1RV19CS045	Devathi N Nikhil	Vision Based Landing of UAV
32	1RV19CS046	Divyang Mishra	Contact Case and Knowledge Management
33	1RV19CS047	Edupuganti Akhil	Decentralised Identity Orchestration using PingOne DaVinci
34	1RV19CS048	Emil Soloman	Mulitmodal Learning for Emotion Recognition
35	1RV19CS049	G V Karuna Sagar	FADEC control law diagram analysis
36	1RV19CS052	Gaurav Pai B	Customer Self Upgrade And Customer Self Repair - CSX
37	1RV19CS053	Gaurav Yelluru	Design and development of mobile application to upskill underprivileged children in English domain
38	1RV19CS055	Harikiran G	Developing a system for remote view and control of devices placed in ICUs in hospitals.
39	1RV19CS056	Harsh Goyal	Performance tuning and benchmarking of workloads on Intel computing and networking silicon features
40	1RV19CS057	Hima J Kammachi	Efficient Data Migration from a decommissioned Monolith Service to micro service model leveraging Amazon S3 buckets using Spark .
41	1RV19CS058	Himanshu Gupta	Grafana's notification integration with outlook and slack
42	1RV19CS059	Hritesh Kachroo	Full stack development of a portal to manage config keys.

43	1RV19CS060	Hrithik Raina	Catalog Quality Assurance Automation of Data Ingestion
44	1RV19CS061	Isha V P	Suite of graphql microservices for cloud based risk calculation and retrieval
45	1RV19CS062	Jagadeesh Patil	Real time notification services to the clients using Kafka, Message Queues and and Websockets
46	1RV19CS064	Jaikishan Jaikumar	Identification of Personal Identifiable Information labels and integrating the workflow into Azure cloud
47	1RV19CS065	Jeril Saban Joy	Schedule Management in Broadcast
48	1RV19CS066	Jinka Rakesh	Configuration of PVOS switches
49	1RV19CS067	Anirudh Jm	Unified model for speech and speaker recognition
50	1RV19CS068	K N Prasanna	CMIS compliant document management service with support for third party repository
51	1RV19CS069	Karthik Bharadwaj	Cloud based Device Configurator
52	1RV19CS071	Khetan Rishabh Purushotam	crop recognition using satellite images
53	1RV19CS072	Khushi Arora	Green Supply Chain Management - Reduction of Carbon Footprint of Inbound Logistics Based on Supplier Selection
54	1RV19CS073	Konde Sasidhar Reddy	Delta display feature for flow counters
55	1RV19CS074	K Likitha	Predictive Demand Planning - A Cloud native predictive service
56	1RV19CS076	Krithika V	Information Solicitation Engine
57	1RV19CS079	Lovey Vishnani	Advanced Trade and Order Analysis Report for ETF Exchange Manager
58	1RV19CS081	Mahendra	Cyberattack Network Threat Detection & Modelling
59	1RV19CS082	Mahesh Bhaskar Hegde	ETL Infrastructure in Dunzo Data Platform
60	1RV19CS086	Manish Psm	Data driven decision making: market research for effective analysis and strategization
61	1RV19CS087	Mayank Agarwal	Tool for on-demand calculation of account balances
62	1RV19CS088	Mehul Gilotra	Automation of Financial Planning using BOARD in insurance sector
63	1RV19CS092	Mudit Nawalgaria	Automation of Data Ingestion Pipeline
64	1RV19CS093	Muskan Agrawal	Event's Portal
65	1RV19CS094	Mythri Naik	WebUI License Control in Virtual Control-4
66	1RV19CS095	N K Sharath Chandra	Spelling correction and next word prediction in categorizer data

67	1RV19CS096	Naman Arya	Distributed Microservice for Creating Alerts and Notifications
68	1RV19CS099	Neetanshu Tyagi	Nayan - Domain Services
69	1RV19CS102	Nikiram C	Contact case and Knowledge Management
70	1RV19CS103	Nishchal D V	Revamping the UI and UX of Apache Avro website for the Apache open-source community
71	1RV19CS104	Nishil Rajan	Establishment of PACE Portal to Automate the Software Development Cycle
72	1RV19CS105	Niteesh Hegde	Empowering the users with self-service configuration management and instant processing through automated cache updation.
73	1RV19CS106	Nitesh Kumar Tiwari	CloudCat - provisioner : Single platform to handle creation and management of AWS, GC and on Prem cloud instances
74	1RV19CS107	Nitin Kumar Rajesh	Developing Framework for Auotomation of Bigbasket Health Quality Assurance
75	1RV19CS110	P. V. Koundinya	Document cognition - optimisation of information search & retrieval from documents
76	1RV19CS111	Perla Leela Charan	Migration of REST to web client, case study: Smart Licensing
77	1RV19CS112	Phalaksha C G	Dev-ops and full stack development of Lean application in Oracle Primavera Cloud
78	1RV19CS113	Pooja Rajesh	The need for graphical database Neo4j to solve the clustering problem
79	1RV19CS116	Pranav Hariharan	Travel Assistant ChatBot using GPT-4
80	1RV19CS116	Pranav Hariharan	Travel Assistant using GPT-4
81	1RV19CS118	Praneeth	Optimizing Performance in Remote Action Execution: Action Device Watch Dog.
82	1RV19CS119	Priya Nayak	Areapedia AI search engine cloud computing Tool
83	1RV19CS121	Priyanshu Singh	Migration of data from public cloud to private cloud using on premise ERP system
84	1RV19CS123	R Sharath Chandra	Migration of Party Universal Matching Application to Google Cloud Platform
85	1RV19CS124	Rachit Dwivedi	Automating and scaling of wireless devices using network virtualization
86	1RV19CS125	Raghunandan Venugopal	Sales Optimisation Using AI/ML Algorithm

87	1RV19CS126	Ragvi Gupta	Offers Admin Tool
88	1RV19CS129	Rohan Maheshwari	Loans GO Live ! SRE Readiness
89	1RV19CS131	Rohith Nair	Cloud-Optimized Process Management with Dynamic Resource Allocation
90	1RV19CS132	Gokul Raj S	Automation & Scaling of Wireless Deployments by Virtualization
91	1RV19CS133	Saahil Shailendra Mehta	Remote Asset Performance Data Analytics
92	1RV19CS136	Sanga Bhavesh Nivas Royal	UI and API Automation
93	1RV19CS137	Sanjana N	Modernization efforts for Portfolio Accounting System
94	1RV19CS138	Sanskriti Bajpai	Implementing Wireguard Protocol For SRX devices
95	1RV19CS139	Santosh	News feed recommendations for OTT platform(sling tv)
96	1RV19CS140	Sarthak Sharan	Enhancing Loyalty Web Application using Snaplogic
97	1RV19CS141	Satvik Patil	Development of Azure Service Bus connector
98	1RV19CS143	Shadakshari Arutagi	Bus Growth Charter for Omniture and Security Fixes Encryption
99	1RV19CS144	Sharan R Shetty	Development of alert microservice for XIO cloud
100	1RV19CS145	Sharayu B Badiger	Implementation of Error Handling Mechanism and Error Injection for SSD System
101	1RV19CS146	Shashank Pasumarthy	Predictive Analysis of Faults in EV's
102	1RV19CS148	Krishna Shedbalkar	Optimising workloads, Live Workload Benchmarking in a Kubernetes cluster with Grafana
103	1RV19CS150	Shivaneetha G	Design and Development of a Testcase Driver Application for Fidelity Databases
104	1RV19CS151	Shravasti Sarkar	Constraint based outdoor path planning with dynamic obstacle avoidance
105	1RV19CS152	Shravya Dasu	Development of univariate models for commodity price forecasting during procurement
106	1RV19CS153	Shreyas P	Automation of networking configuration and Analysis of Overlay communication
107	1RV19CS154	Shreyashee De	Full Stack Development of an Application for automobile industry
108	1RV19CS155	Shrivatsa Kulkarni	Planning tool performance analysis and improvements
109	1RV19CS156	Shrujan R	Canary Deployments and Management for Pipelined Services

110	1RV19CS157	Shubbhum Yadav	Deep Neural Network for classification of ships from ISAR images
111	1RV19CS158	Sinchana Raj	Real time event streaming for financial enterprise system with Kafka/Amazon MQ
112	1RV19CS159	Sneha A Biradar	Data center system utilization measurement and reservation
113	1RV19CS161	Sourabh Mallappa Kamate	Storage and analysis of network data
114	1RV19CS162	Sourav Kannantha B	Deep packet inspection
115	1RV19CS164	Sudhanshu Garg	Access-Control-List Optimization for ASA
116	1RV19CS165	Sujala Reddy R S	Identity and access management (building micro service applications)
117	1RV19CS166	Sumanth Hegde	Effective Change Management and Alert Notification System
118	1RV19CS167	Sumit Ramesh Kakati	Contact Case and Knowledge Management
119	1RV19CS168	Supriya K N	Notification Service Audit Integration: An Integrated Centralised Service for Notification Client Services
120	1RV19CS169	Suraj K R	Enterprise Data Pipeline for Data Ingestion
121	1RV19CS170	Surya Y	Development of Automated Data Integration Pipeline for API Based Sources
122	1RV19CS171	T J S L Savitri	Quality Assurance of Network Traffic Shaping and Queue Synchronization in a Cluster of Network Devices
123	1RV19CS172	Tanmay Jain	Automation of rate change capturing process in Single Premium Deferred Annuity
124	1RV19CS173	Tanmayananda Mgp	Sequence Discovery using Scout's Process mining module
125	1RV19CS175	Tirumalesh Manjunatha Naik	Application for simulating Oscilloscope and BertScope
126	1RV19CS176	V A Sriram Praveen	Model Interpretability for Deep Learning Models in Object Detection
127	1RV19CS177	Vaibhav Iramani	Integration of whatsapp with app for booking cabs
128	1RV19CS178	Vaibhav Vatsa	Operable K8S level 2 for Kubernet
129	1RV19CS179	Varadraj Patil	Implementation of Exception Logging Framework for DAS, DIS, Coding and Notification services
130	1RV19CS181	Veerabhadra	Fault Injection as a Service
131	1RV19CS182	Venjan V	FADEC control law diagram analysis

132	1RV19CS183	Vihaan Nama	Migration of On- Premises Spark application to cloud using AWS Elastic Kubernetes
133	1RV19CS186	Vinayak Ashok Mikkal	Development of Data Integration Pipelines
134	1RV19CS189	Y.Raghavendra	Firmware development on AI Inference accelerator (Cloud AI 100)
135	1RV19CS190	Yash Manjunath Sannecy	Work and Travel Permit Portal using Angular and Springboot
136	1RV19CS191	Yashas M S	Development of Load Diagram Submission for Distribution Operation Command Center
137	1RV19CS193	Aditya Y Jeppu	Payment and Donation Platform - an STPA and Model Based Security Critical System Analysis
138	1RV19CS194	Divye Sancheti	Migration of Components from MVVM to Virtual DOM Architecture
139	1RV19CS195	Aman Verma	Development of REST APIs and Dockerising the application using Django REST Framework
140	1RV19CS196	Aparna Kini	Decentralised Identity Orchestration using PingOne DaVinci
141	1RV20CS401	Bharath Kumar M	Enabling Alletra4K Platform in Compute Operations Manager and GreenLake Cloud
142	1RV20CS403	Gaganashree D	Migration of DSP Application using Data Analytics
143	1RV20CS403	Gaganashree D	Migration of DSP Application to PAST
144	1RV20CS409	Manjula B	Resource utilization monitoring on Microsoft azure and SSL certificate alerting system
145	1RV20CS414	Spoorti S Javali	A robust runtime environment to run various modern application under one cloud computing server architecture

R.V. College of Engineering, Bengaluru – 59
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Department of Computer Science and Engineering
Course: Major Project Code: 18CS81 – Inhouse Projects

UG PROJECT ACADEMIC YEAR 2021-2022

Sl No	USN	Name	Project Title
1	1RV16CS132	Sanvi Shekar	Development Of Image Super-Resolution Framework
	1RV17CS069	Kakarla Deepthi	
	1RV18CS049	D Rahul	
	1RV18CS051	Dhawan K S	
2	1RV17CS040	Dave Shivangi Devendra	Human-Human Interaction Recognition Using 3D-CNN
	1RV18CS197	Pooja R Sheshagiri	
3	1RV17CS087	Mohammad Salman Alam	Underwater Mine Detection Using Deep Learning
	1RV17CS152	Shreyas Manjunatha	
	1RV17CS149	Shloka Dorepally	
4	1RV17CS208	Himanshu Kalwar	Classification of Satellite Images of Traffic Using Deep learning
	1RV17CS052	Divyanshu Anand	
	1RV18CS432	Shriya Shyam Raikar	
5	1RV17CS402	Amol patil	CNN Based Image Classification For Animal Intrusion Detection System
	1RV18CS403	Chethan N	
	1RV18CS426	Raju S	
	1RV17CS407	Dileep Y	
6	1RV18CS025	Anish Kuila	Face Detection and Gender Identification Using Convolutional Neural Network
	1RV18CS012	Akhilesh Achary	
	1RV17CS034	Chakshul Tyagi	
	1RV18CS188	Vinayakumar Venkatramana Moger	
7	1RV18CS022	Aniqah Ahmed	Acoustic Signal Detection of search-phase echolocation bat calls with Convolutional neural networks
	1RV18CS059	Guransh Kaur Ghai	
	1RV18CS066	Isha B Rameshraj	
8	1RV18CS008	Adarsh Gupta	Load balancing in SDN
	1RV18CS027	Anurag Singh Bhadauria	

8	1RV18CS028	Aravind A	Load balancing in SDN
	1RV18CS041	Bhargavi H S	
9	1RV18CS063	Harshwardhan	Traffic sign Recognition and Detection using CNN [Alerting System]
	1RV18CS079	L V V Raghava Pullaiah	
	1RV18CS110	P Varshitha Preetham	
	1RV19CS414	Sandhya Bhat	
10	1RV18CS074	Kshitij Agarwal	Detection of neurological diseases at an early stage using deep learning
	1RV18CS075	Kumar Ayush Sinha	
	1RV18CS083	Manan Sahu	
	1RV18CS085	Manav Dharora	
11	1RV18CS097	Nakul R S	Detection of Vulnerable GitHub workflows using Machine Learning
	1RV18TE050	Sudarshan B	
	1RV18TE029	Neeraj L	
12	1RV18CS189	Viraj Aurora	Knee Bone Segmentation from MRIs using Deep-Learning based methods
	1RV18CS037	Ayush Srivastava	

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UG PROJECT ACADEMIC YEAR 2021-22

Sl No	USN	Name	Project Title
1	1RV17CS206	PRUTHVI K	ETL and Business Analytics for given raw data
2	1RV18CS001	A S Prajwal Babu	Building an ETL pipeline for Analysing EPG Data
3	1RV18CS002	Aarush Gupta	Container Image Optimisation
4	1RV18CS003	Abhay Jogenipalli	Customer Ticketing Platform: Aruba Service Manager a Service Now application
5	1RV18CS004	Abhay M S	Development of APIs for Delivery/Collection and Automated Dispatch Planning Tool
6	1RV18CS005	Abhishek J	Enhancement in device state and sampling microservice performance
7	1RV18CS006	Abhishek K P	Setting up CI/CD pipeline for Node Js project in Docker using Shell Scripting
8	1RV18CS007	Achinthya Sreedhar	Traffic flow classification on IPv4 / IPv6 destination address on J2 based platforms
9	1RV18CS009	Adithyan Narayanan	Automation of monitoring of active binary versions and protocol message differences
10	1RV18CS010	Aditya K Mishra	Web Based Fuel Dashboard for Efficient Fuel Consumption in Aviation
11	1RV18CS011	Akhil Dua	Kubernetes Migration of Spring Boot Application
12	1RV18CS013	Akshara N Udupa	RPA Bots – Building an automation system from process discovery
13	1RV18CS015	Akshay Kumar	Developing OCI Functions for Safety-One Post-Processing
14	1RV18CS016	Akshay Oppiliappan	Development of Semantic Analysis Tool for the Rust Language
15	1RV18CS017	Aman Singh Baghel	Development of Copper UI Automation Suite
16	1RV18CS018	Amaravathi Shashanth	Weather Services API's Usage Metrics
17	1RV18CS019	Ambu Karthik	Cloud-Based Map for Aviation Services

18	1RV18CS020	Amit S Kotagi	Intelligent Workflow Automation
19	1RV18CS021	Ananya B S	Building a solution blueprint for microservice applications
20	1RV18CS023	Aniruddha S	Digital-Checkout:Customer Centric Vehicle Rental Process
21	1RV18CS024	Anirudh Devpura	Change Data Capture On Relational Databases Using Apache Kafka
22	1RV18CS026	Ansh Singal	Design and Development of the Entanglement layer of QNTSim network simulator
23	1RV18CS029	Arunima Maitra	Court Order Scrutiny Automation Using NLP
24	1RV18CS030	Atreya Bain	Secure Sockets Layer Certificate Management Service
25	1RV18CS031	Avilash M	Microservices authentication to establish an efficient communication through kafka system
26	1RV18CS032	Avulapati Niranjan	Tuning and optimization of deployment pipeline in Jenkins
27	1RV18CS034	Ayush Daga	Development Of An Internal Data Visualization Platform
28	1RV18CS035	Ayush Dwivedi	Realtime Web Application Forensics for Intelligent Target Analysis
29	1RV18CS036	Ayush kumar	Tuning and optimization of deployment pipeline in Jenkins
30	1RV18CS038	B Somu Sashank	Automation Framework Development on Edge Diagnostics
31	1RV18CS039	Bhanu Prakash	Enhancing Transform-Content Feature of Internal Proxy Server
32	1RV18CS040	Bharat Bangari	Development of Business Object reports
33	1RV18CS042	Bhavya Bhagerathi	BAMS clearing firm API
34	1RV18CS043	Bidushi	Perception Model For Autonomous Vehicles
35	1RV18CS044	Birajdar Shiwam	
36	1RV18CS163	Sanjaykumar Shubh Shukla	
37	1RV18CS045	Chaitanya K R	Intelligent Traffic Data Classification And Categorisation Framework
38	1RV18CS046	Chethan S	PC Simulation Framework for DMS
39	1RV18CS048	Chirag Bapat	Fixing DNS issues in proprietary and open-source libraries for network devices
40	1RV18CS050	D S Sharath Shenoy	Decoupling System Dependencies and
41	1RV18CS052	Dhrithi Harish	End-to-End Automated Deployment of Domain Name System and Network Time Protocol Update
42	1RV18CS053	Dinesh Babu S	Building a Monitoring Framework for a Distributed Cloud Application using Prometheus and Chef

43	1RV18CS054	Furqan Abdul Khadar Ramadurg	Dynamic Behaviour Identification of Webpages
44	1RV18CS055	Geeta Shivani	Design a framework to convert text into commands
45	1RV18CS056	Giridhar K Shanbhag	Automated creation of Lab and Jira tickets triggered through Nagios
46	1RV18CS057	Gracious Saxena	Data Completeness and Control by Match Based Reconciliation of HDFS vs OLAP Archive DBs
47	1RV18CS059	Guransh Kaur Ghai	Acoustic Signal Detection of search-phase echolocation bat calls with Convolutional neural networks
48	1RV18CS060	Vibhav Sharma	Managing and Verification of Application Deployment using Appian
49	1RV18CS061	Harish A Jartarghar	Carbravo: Transparent and Smooth Experience of Buying Used Cars Online
50	1RV18CS062	Harish Pukale	QA and Automation for DevProd Applications
51	1RV18CS064	Himanshu Singh	“Productivity Improvement Scheme In Erp System”
52	1RV18CS065	Hrishika Rai	Enhancement of accessibility in Workspace One Content- iOS Application
53	1RV18CS066	Isha B Rameshraj	Acoustic Signal Detection of search-phase echolocation bat calls with Convolutional neural networks
54	1RV18CS067	Ishkabir Kumar	Backend Engineering and Microservice Creation and Deployment
55	1RV18CS068	Karunatharaka B	Minimal multi-tasking Operating System for RISC-V
56	1RV18CS143	Sakshi Kamal	Refactoring And Development Of Hyperlocal Logistics Api
57	1RV18CS070	Kaustubh Shriyans	
58	1RV18CS071	Kirti Nandan	Enabling Transfer of Business Objects From Public Cloud to Private Cloud/on-Premise ERP System
59	1RV18CS072	Krithi D Shetty	IPsec Inline Flow Management interface for unified data path
60	1RV18CS073	Kruthi M N	Automation of logs parser for Windows Performance Analysis
61	1RV18CS076	Kumaraskanda B B	Service Desk Data Analytics
62	1RV18CS077	Kushagra Mishra	Redundant Branch Deletion using Version Control Systems
63	1RV18CS078	Kushagra Sirothia	Data Pipeline Creation and Development Using ETL Tools
64	1RV18CS080	L Venkata Chaitanya Reddy	Standardization of rapid data ingestion (RDI)
65	1RV18CS081	Likhith S Reddy	Invoice Monitoring Dashboard For IoT Control Center

66	1RV18CS082	Mahek Jain	Oil Spill Detection and Containment using Convolutional Neural Network
67	1RV18CS084	Manas Mayank	Security Connector High Availability and Security Hardening
68	1RV18CS086	M. Krishna Saketh	Staging Stack Management for Pull Requests
69	1RV18CS087	Manikhanth Shivanand Katti	Cloud Metering Dashboard
70	1RV18CS088	Manjunath S Nayak	Network Device User Entitlement using System for Cross-Domain Identity Management 2.0
71	1RV18CS089	Manoj Kartik R	Dealer onboarding platform
72	1RV18CS090	Mayur A Bhandare	Building End to End Read to cloud Automation
73	1RV18CS091	Mohammed Amaan	Dynamic Nitro Protocol based Automation Framework for a Web Application Firewall
74	1RV18CS092	Monish S	Enhanced Connector Assembly System using Augmented Reality
75	1RV18CS093	Mridul Mohta	Jenkins Automation & Continuous Integration for ICA Proxy
76	1RV18CS094	N.Kruthik Bhushan	Development of Short Message Peer-to-Peer Analytics Platform
77	1RV18CS095	N Pooja	Go-Test using Cora Sequence and Cora ops Manager
78	1RV18CS096	Nachiket G Kallapur	Automated Data Integration Pipeline for Databases
79	1RV18CS098	Narayan Ravikumar	Query Queueing Based on Load Parameters
80	1RV18CS099	Navya Priya N	Authentication and Authorisation of financial services using spring framework
81	1RV18CS100	Neel Bhandari	E-Commerce Customer Problem Identification and Remediation.
82	1RV18CS101	Nehal Chakravarthy M D	Restructure HPE Serviceguard to improve the product suitability in cloud environment
83	1RV18CS102	Neil Nagaraj Havanur	Encompassing mPulse’s Core with Analytical and Multi-lateral features
84	1RV18CS104	Nidhi K	Device Driver to validate I3C Driver
85	1RV18CS105	Nikitha Srikanth	Clarifying User Intent in Information Retrieval
86	1RV18CS106	Nisarg	Reduced Human-in-the-Loop in Model Based System Validation of Flight Warning System
87	1RV18CS107	Nishchal Jagadeesha	Human Counting In Ultra-Wideband Technology

88	1RV18CS108	S Nishith	Automated Data Integration Pipeline for Application Programming Interfaces using Connector Implementation Language
89	1RV18CS109	P Gunavantha	Test Car Booking Management
90	1RV18CS111	Padmaja B G	eSIM on Device Activation Application
91	1RV18CS112	Pavan K R	Regulatory Compliance Check for Campus Network
92	1RV18CS113	Pavankumar V Badiger	Developing a configurable Whitelabel solution for an E-commerce platform
93	1RV18CS181	Utkarsh Singh	
94	1RV18CS114	Prajwal K	Comprehensive Monitoring, Alerting interface for data pipelines
95	1RV18CS116	Prasanna Bhat	Snowflake Archival Solution
96	1RV18CS117	Prateek Sinha	Development and Industrialization of Engine Line Analytics
97	1RV18CS119	Praveen Erayya Devadiga	Order Workflow Enhancement and Contract Automation
98	1RV18CS120	Prerana K S	Implementing CI/CD Platform to Deploy Applications on Kubernetes
99	1RV18CS122	Priyank Singh	Improving Sub-millisecond data capture in Windows
100	1RV18CS161	Shreyash Gupta	
101	1RV18CS123	Priyanka M B	Create Latest Security Patch for SAPFHIR
102	1RV18CS124	Pulak Pathak	Approval Management System
103	1RV18CS125	R Akash	Building a translation gateway application based on microservice architecture
104	1RV18CS126	R Vijay Chiranjith Reddy	Automation of Wireless LAN controller analytics
105	1RV18CS127	Rahul Laxman	Development of automated web-based employee training application for recruited employees of the organization
106	1RV18CS128	Rajath S Vasisth	Continuous Delivery and Deployment of Container Ready Applications for DevOps and BlockChain
107	1RV18CS129	Rakesha R R	Development of Commercial Data Environment
108	1RV18CS130	Rakshitha A M	Enhance Logging Service To Support Logging Of Objects On Exception
109	1RV18CS131	Ratan Narayan Hegde	Securities Service - Transaction Instruction Manager
110	1RV18CS133	Risha Dassi	Athena Trade and Risk Services
111	1RV18CS134	Rishab Raj P	Development of new features for Apptio Business Intelligence Product using Custom Query Language

112	RV18CS135	Rishabh Chauhan	Transition from legacy system to new UI for Aviation Material Tracking Product
113	1RV18CS136	Rohit Mohan Krishna G V L	Building Customer Identities from heterogeneous sources in retail systems
114	1RV18CS137	Rohit Parashuram Myali	Automating the Deployment and Configuration of ADC
115	1RV18CS138	Rohit Sachin Sadavarte	NADC Rexx Refactoring
116	1RV18CS139	ROUNAK JAIN	Payments System Integration and Administrative Service
117	1RV18CS140	S Nitin Pandit	Natural Language Processing and Reusable Components using PEGA
118	1RV18CS142	Sai Keerthana Arun	Bowl View Application on the GPU and its porting to gen4
119	1RV18CS144	Sami Ur Rehman	Certificate Pinning Identification Using TLS Fingerprinting
120	1RV18CS145	Sanjana Reddy	PDF Generation for Metrics Dashboard
121	1RV18CS148	Shaik Abrar Ul Haq	Application Proxy Development for Sensitive Data Retrieval
122	1RV18CS149	Shailesh Kumar Sharma	Return-API for ARC
123	1RV18CS150	Shaurya Gupta	Automation of Supply Chain and Production Business Process Using Software
124	1RV18CS151	Shivam Shreyansh	Robots
125	1RV18CS152	Shivam Singh	Building Kafka Plugin Support For Generic Notifications In BRM Driver
126	1RV18CS153	Shivanand Adky	Processing Of Incentive Compensation For Pharmaceutial Representatives
127	1RV18CS160	Shreyas S	RDS On Demand Granular Record Retrieval
128	1RV18CS154	Shivani C H	Driving Data Analytics and Visualization for KC
129	1RV18CS156	Shivanshu Singh	Server Patching and Vulnerability Management Automation Portal
130	1RV18CS157	Shivaraj B Karagera	Digital-Checkout: Customer Centric Vehicle Rental Process
131	1RV18CS158	Shreenidhi	Hive ACID replication support for CM/RM backend
132	1RV18CS159	Shreesh Mansotra	Real time Data analytics Platform to support customer facing and Business Analytics
133	1RV18CS162	Shreyas Bhardwaj	Scope Extension of Verify-Config Product and Transition from Legacy System to New UI for Mileage Product
134	1RV18CS164	Shubham Kumatole	Infrastructure as Code

135	1RV18CS165	Shuvam Mitra	Control-M Heterogenous Database Migration (Proof of Concept)
136	1RV18CS166	Siddharth Chauhsn	Implementation of GUI Manager for Novum IQ based Syringe Infusion Pump
137	1RV18CS168	Soumya Saxena	Active Directory Role Recommendation System using Collaborative Filtering
138	1RV18CS169	Soundarya SV	Go-Test using Cora Sequence and Cora ops Manager
139	1RV18CS170	Spoorthi Jayaprakash Malgund	CI-CD Automation of DNS Threat Defense Packages
140	1RV18CS171	Sreedhar S Dhulkhed	Operation and Maintenance of Database-like Data Pipeline
141	1RV18CS172	Srinandan K S	Automate Deployment of OMS components and Set-up Monitoring Dashboard
142	1RV18CS173	Sriram Narayana Cummaragunta	Endoscopic Quality Assessment Using Deep Learning
143	1RV18CS174	Srishti Moorthy	CloudWatch Agent Integration for Cisco Wireless LAN Controller Platforms
144	1RV18CS175	Sujay Hebbar	Performance logs analyzer for SAP Analytics Cloud tenants
145	1RV18CS177	Sumith Kumar S	Development of an API based ELT Pipeline
146	1RV18CS178	Tarun Vijayanand Bagewadi	AI Based Feature Point Extraction and Benchmarking
147	1RV18CS179	Thejas B U	Shadowfax Partner App Development and Maintenance
148	1RV18CS180	Utkarsh Kumar Choubey	Content Management System for Udaan B2B App and Improving Core Buying Experience
149	1RV18CS183	Varsha R Jenni	Global Payments Guardian - Alert Router
150	1RV18CS184	Vecha Rama Surendra	Feature Implementation of Customer Data Comparison
151	1RV18CS185	Vennapusa Venkata Jaswanth Kumar Reddy	Developing a Data Quality and Data Reconciliation Framework
152	1RV18CS186	Vinay R	Design and Development of Provisioning Interface for Broadcast Operations Support System using Angular
153	1RV18CS187	Vinayak	Design and Development of Automated Frequently Asked Questions Generating System
154	1RV18CS190	Virendra Naik	Building Data-pipeline framework for detecting broadband traffic
155	1RV18CS191	Vishal M	Contextual AI Chatbot for Business Platform Assistance
156	1RV18CS192	Yatin Satija	Development of One Stop Workspace to Launch External Utilities

157	1RV18CS193	Shreyas Bharadwaj H S	mPulse’s Server Configuration Automation.
158	1RV18CS194	Akanksh A Manjunath	System Capacity Uplift using Cloud Native and Microservices
159	1RV18CS195	M C Sohan	Function Level Heatmap Generation for UTF Enhancement
160	1RV18CS196	Sathvik C	Development of a framework to support Wireless Analysis stack contingent on Android
161	1RV18CS199	Veerapur Rahul	Deployment of an search engine application
162	1RV18CS434	SURAJ KAMBLE	Optimizing Scrolling Performance & Paginating Users Feed Using Kotlin
163	1RV19CS400	Chaithra S	Design and development of client management system
164	1RV19CS401	Gangadhar G	Integrating Tally with CreditMag Application
165	1RV19CS404	Hema H Godihal	
166	1RV19CS408	Pradeep K	
167	1RV19CS410	Rafeeq Pinjar	
168	1RV19CS402	Harshitha C	Identify the number of misroutes at Horizon Server and Gateway
169	1RV19CS403	Harshitha V	Design And Development of User and Group Application Using Business Process Management [BPM] Technology
170	1RV19CS405	Hobalshetty Kavyashree	Porting Data to the New Enterprise Resource Planning and Data Visualization for Generating Reports.
171	1RV19CS406	M s apoorva	Design and Implementation of Product Alert Service
172	1RV19CS409	Premaa Saai B L	Workflow Development for Test Automation
173	1RV19CS411	Ram kumar m	Android Device Auto Recovery
174	1RV19CS412	Sahithya N D	Event Driven Trade Adapter
175	1RV19CS413	Sameer F	Falcon – Digital Automation Intelligence
176	1RV19CS415	SARAH R NADAF	Customer Experience Management Using Cloud For Customer Sales
177	1RV19CS416	Suresh Shekarappa Hosamani	Digital Authentication for Truck
178	1RV19CS417	Yuktha R	Predictive and Real time analysis to improve manufacturing quality and cost efficiency for Molex industries

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UG PROJECT ACADEMIC YEAR 2021-22

1	1RV17CS082	Mahathi Siddavatam	Recommendation of Right Developer for Bug Detection
	1RV17CS161	Spandana M Patil	
	1RV17CS143	Rahima Tanaz Shaik	
	1RV17CS051	Divya M	
2	1RV17CS047	A Dharma Reddy	Object classification on satellite images using deep learning
	1RV17CS104	P Satya Sriram	
	1RV17CS117	R Shreya	
	1RV18CS429	Riya Naresh	
3	1RV18CS400	Ajay Jadhav	Social network mental disorders detection using online social media data mining
	1RV18CS405	Harshavardhana I	
	1RV18CS408	Karthik Morab	
	1RV18CS419	Niranjana H B	
4	1RV17CS191	R Mahesh	Design & Development of Portable Smart Traffic Light System with AI Enablement
	1RV18CS411	Manikantha S	
	1RV18CS412	Manjunath H	
5	1RV17CS023	Aravind	Road Network Detection Using aerial/satellite images
	1RV17CS100	P Apoorva	
	1RV17CS113	Prathik R M	
	1RV17CS120	Rakesh	
6	1RV17CS054	Goutham G K	Vehicle Detection using Remote Sensing Images
	1RV17CS170	Swapnil Sonkar	
	1RV17CS207	Kaushik Agarwal	
7	1RV17CS084	Md Akbar Khan	Underwater Object Recognition Using Transformable Template Matching Based On Prior Knowledge Using Cnn
	1RV17CS083	Allavali Manish U Ambi	
	1RV17CS025	Arun Rathod	
	1RV17CS185	Vishwanath R K	
8	1RV17CS031	B Sumukha Adiga	Detection and Extraction of Naval Mine Features using CNN Architectures
	1RV17CS035	Chanakya Hosamani	
	1RV17CS142	Satya Sujan C	
	1RV17CS158	Sohan G	

	1RV17CS163	Srinidhi M S	
9	1RV17CS068	K Rakesh Kumar	Detection and Classification of sea mines and depth estimation
	1RV17CS057	H Ramesh	
	1RV17CS144	Shantkumar	
	1RV17CS184	Vishwa Panchal	
10	1RV16CS050	GautamPathak	Human Emotion Analysis using Hybrid CNN Model
	1RV16CS097	P.Bhargav Varma	
	1RV16CS154	Somendra Singh	
	1RV17CS406	DarshanK	
11	1RV18CS406	Harshitha R	Real-Time Human-Human Interaction Recognition Using CNN Model
	1RV18CS409	Kavya S Muttur	
	1RV18CS415	Nandini R	
	1RV18CS407	Jayanth P	
12	1RV18CS427	Ramyashree V	Human Action Recognition using Multimodal CNN
	1RV18CS431	Shalini R	
	1RV17CS174	Tushar Lal	
	1RV17CS188	Aman Verma	
13	1RV17CS015	Akshita L	Diabetic Retinopathy Classification Using Deep Convolutional Neural Network
	1RV17CS059	Harshul Singhal	
	1RV17CS062	Ishita Dwivedi	
14	1RV17CS135	Sajjan Kiran	Subtitle Generation & Video Scene Indexing using Recurrent Neural Networks
	1RV17CS176	Umesh Patil	
	1RV15CS107	Siddarth Shankar	
15	1RV17CS013	Akhilesh U	Machine learning techniques for Quantification of Knee Bone Segmentation and detection of OsteoArthritis severity from MR Images
	1RV17CS030	B Subhash	
	1RV17CS045	Dhananjay N S	
	1RV17CS046	Dhanush B P	
16	1RV15CS403	Arunkumar B N	Design Of Smartbot Application Using Natural Language Progragramming
	1RV14CS085	Monaal Gupta	
	1RV17CS416	Naveen K P	
	1RV15CS403	Tejashwini V B	
17	1RV18CS421	Pavan Kumar Y	Flood detection using remote sensing images

R.V. College of Engineering, Bengaluru – 59
(Autonomous Institution affiliated to VTU, Belagavi)
Department of Computer Science and Engineering
Course: Major Project Code: 16CS81 – Internship

UG PROJECT ACADEMIC YEAR 2020-21

1	1RV17CS134	Sai Venkata Varun Danda	Test Automation For Push To Talk SIP Framework
2	1RV17CS065	Jayesh Kumar Yadav	Testing Tool For Content Delivery Network
3	1RV17CS076	Khushi Talesra	Automation Of User Access Audit And Control
4	1RV18CS425	Rahul Pandurang Pokale	Test Data Automation Framework For Enterprise
5	1RV17CS126	Ruchita R Biradar	Anomalous Traffic Detection System In An Enterprise
6	1RV17CS022	Apoorva	Enhancement Of Athenapractice Application
7	1RV17CS061	Hrithik M R	Migration From Visual Basic 6 (VB6) To Reactjs For Athenapractice
8	1RV17CS095	Nikhit Laxman	AR-VR Assisted Industrial Maintenance
9	1RV17CS139	Sanjay S Hegde	Development Of Parallel Update Channel For FHIR Server
10	1RV17CS036	Chetan B	Automation Of Validation Package For High Performance Computing As A Service
11	1RV17CS097	Nishchal Shetty	Automating File Deployment Onto Hypervisors
12	1RV17CS210	Vedika Agarwal	Automating Regression Test Suite Using CI/CD Pipeline
13	1RV17CS021	Anshul Agrawal	Centralized Based Approach In Wireless Local Area Networks
14	1RV17CS150	Shravan Y R	Automating Data Extraction Report Generation And Dissemination Using Workfusion
15	1RV17CS187	Yash T Jain	Enhanced Switch Security And Simplified Tunnel Deployment
16	1RV16CS055	Haritha Choudhary	Implementation Of Internal Automation Tool - Appsmith
17	1RV17CS002	Aaryaman T P Katoch	GCP Migration Using Terraform
18	1RV17CS169	Susheel S Harsoor	Learning Hub
	1RV17CS181	Veeresh S Koliwad	
19	1RV17CS001	A Suryanarayanan	Health Visualization Of Service Fabric Based Infras Tructure
20	1RV17CS042	Deeksha Shravani	Enhancing A Cloud-Based Learning Management System

21	1RV17CS105	Prableen Singh	Classification And Prediction Of Software And Data Issues In SDLC
22	1RV17CS173	Tejaswini S	Integration Of Custom Logging In Business Applications
23	1RV17CS175	Uday Talwar	Automation Of DOOR Functionalities And Rebuilding Of A702a Protocol
24	1RV18CS424	Priya Darshini R	Invoice Status Portal
25	1RV18CS435	Thanushree S	Fort Systems Google Cloud Platform Migration
26	1RV17CS198	Shubham Jain	Comparative Analysis Of Different Model Interpretability Methods In Machine Learning
27	1RV17CS067	K. Harshith	Administered Blogging Application Using ASP.NET Core MVC
28	1RV17CS070	Kandukuri Vineethkumar Gowd	Development Of Common Platform For Software Procurement Using ASP.Net Core MVC
29	1RV17CS081	L Spoorthi	Processing Of Batch Data Using Data Warehouse And Cloud Technologies
30	1RV18CS420	Pavan Kumar K N	Authorization For Real-Time Events For Ecommerce With Cloud Technology
31	1RV17CS072	Karthik S Rao	Building A Self-Help Support Portal For Microsoft Sales Experience (MSX) Dynamics365
32	1RV17CS157	Sinchana Ravishankar Gaonkar	Price And Position Feeds Inventory And Instrumentation
33	1RV17CS164	Suchit T E	Analytics Tracking Service In Geochina
34	1RV17CS066	K Anirudh	Business Event Notification Service
35	1RV17CS048	Dhruv Behl	Adversarial Robustness Of Image Classification Models Against Patch Attacks
36	1RV17CS075	Keyur Shah	Dynamic Code Coverage
37	1RV17CS004	Abeer Vaishnav	Development Of Application-Based Benchmarking Framework For Quantum Hardware Architectures
38	1RV16CS036	Bhargavi Katti	Detailed Analysis Of Neonatal Jaundice And Its Treatment
39	1RV17CS006	Abijith Trichur Ramachandran	IOT Security For AI Applications
40	1RV17CS134	Sai Venkata Varun Danda	Test Automation For Push To Talk SIP Framework
41	1RV17CS074	Keshav Bhattad	Cloud Based E-Learning Portal In COVID-19 Situation For Rural Schools
42	1RV18CS423	Prashanth Reddy M G	Cloud Storage Auditing With Deduplication And Strong Privacy Protection

43	1RV17CS115	Pruthviraj Deshmukh	Enabling CI/CD Pipelines For Running DDTC On Multiple Builds Parallelly
44	1RV17CS199	SHETTY ROHAN	Central Dashboard For Application Security Management
45	1RV17CS196	Sneh Bhajanka	Implementation Of MAC Randomization In Bring Your Own Device (BYOD) Flow For Android And Ios
46	1RV17CS055	Gowtham H N	Number Masking And Cold Chain Compliance For Last Mile Delivery Platform
47	1RV17CS205	Mangalam Palod	Manual Operations Traceability- Change Data Capture And Data ETL(Extract, Load And Transform)
48	1RV17CS136	Sammed A M	Intelligent Testing Of Storage Device With ML And Multi-Processing - Intellitest
49	1RV17CS058	Harshita S	Support Engineer Status Monitoring Tool
50	1RV17CS129	S Meghna	Casemaster - Automated Tool To Retrieve Cases For Reviewing
51	1RV17CS124	Ritesh M	Automatic Case Assignment Bot For Sres
52	1RV17CS131	Saadhvi Rayasam	Training, Evaluation And Management Platform For Interns
53	1RV17CS019	Annaray Kalashetty	Mig Home App For Increasing Customer Interaction
54	1RV17CS128	S B Rakshith	Auto Reload Of Properties In An Enterprise Application
55	1RV17CS121	Rameshwar Garg	Time Series Analysis & Forecasting Of Network Data
56	1RV17CS138	Sanjana G B	High Resilient Messaging Service Using Apache Kafka
57	1RV17CS055	Gowtham H N	Number Masking And Cold Chain Compliance For Last Mile Delivery Platform
58	1RV17CS098	Nitheesh	Back In Stock Alert System
59	1RV17CS043	Deekshith	Integration Of Mixpanel : A Web And User Analytics Tool
60	1RV17CS094	Nikhil Nayak	E-Commerce Order Delivery Time Prediction
61	1RV17CS141	Sathvik K R	Design And Implementation Of Perfect Order Index
62	1RV18CS416	Nandish B J	Feature Enhancement Of Open-Source Web Conferencing System
63	1RV17CS011	Aishrith P Rao	Big Data Migration And Processing Using Azure Databricks And Selective Feature Deployment Tool
64	1RV17CS039	Dashrathkumar Yadav	A CMS (Content Management System) For Fresh, Food And Fast-Moving Consumer Goods Portal
65	1RV17CS127	Rujula Singh R	Helpdesk Tool For Cloud Contact-Center Lifecycle
66	1RV18CS430	Samrudhi Narayan Santaji	Essential Sales Assistant

67	1RV17CS008	Adithya H	Deploying Adaptive Security Appliance In Firecracker
	1RV17CS192	Sagar P	
68	1RV17CS018	Aneesh Sidharth	Business Process Management Application For General Data Protection Regulation Compliance
69	1RV17CS193	Mohit Singh	Centralized Service For Device Management In Large Networks
70	1RV17CS132	Sahana Srinivasan	Product Alerts Service REST API Microservice For Intrusion Detection Using Machine Learning, Explainable AI And Causal Discovery
71	1RV17CS159	Sourabh S Badhya	Generation And Visualization Of Static Function Call Graphs For Large C Codebases
72	1RV17CS012	Aishwarya G	Risk Management For Cryptocurrency
	1RV17CS032	Balusa Venkata Sai Harika	
73	1RV17CS020	Annette Shajan	Deployment Of Security Service On A Cloud Platform
74	1RV17CS160	Spandana Kottur	Operational Risk Management Dashboard
75	1RV17CS077	Krishna Yash Raj	Video Encoding And Decoding Using Codec2.0
76	1RV17CS102	Pallavi	Link Sharing Application
77	1RV17CS182	Vinuthkumar V G Gouda	Link Sharing Application
78	1RV17CS186	Yash Surange	Framework Migration From Load Runner To Jmeter
79	1RV17CS005	Abhishek R	Feature Enhancement Of Open-Source Web Conferencing System
80	1RV17CS116	Purvi G R	Requirement Of A High Scalable And Performing VSAM Data Store For CICS TX
81	1RV17CS130	S Suraj	Optimal Inventory Allocation Using Decision Optimization
82	1RV17CS197	Sarayu Vyakaranam	Machine Learning For Evaluation Of Vendor-Rating Metric In Government E-Market Place (Gem)
83	1RV17CS073	Karthikeya H S	Email Spam Quarantine Threshold Alert
84	1RV17CS122	Rishab V Arun	Developing And Fixing Citrix Gateway Sanity Automation Scripts And Validating Gateway Interoperability
85	1RV14CS009	Ajeeta Singh	‘Extracting Enterprise And Domain Contextual Knowledge From Requirement Using Kdd’
86	1RV17CS037	Chetan Tayal	Unsupervised Clustering For Pairs Trading
87	1RV17CS009	Aditya Patil	Development Of Large-Scale User-Client Application For Automobile Networking Sector

88	1RV18CS401	Anita Muddanna Halundi	Nethra Dashboard A Tracking Tool For Release Plan Of Project
89	1RV18CS413	Mohammed Kalander Shihab	Configuration And Integration Development In Insurance Suite Software
90	1RV18CS414	N Nikhil	Cross Platform E-Commerce Application
91	1RV17CS209	Shambavi	Client Application For The Automation Of The Mergers & Acquisitions Process
92	1RV17CS101	P Haridher	Product Based Search Engine Microservice
93	1RV17CS107	Prajwal V Atreyas	Platform Migration: Data Centers To Cloud Architectures
94	1RV17CS147	Shashwati Jha	Front And Back End Functional Automation
95	1RV17CS063	Jainil Viren Parikh	Dashboard And Real-Time Analysis Service For Globalization Tools
96	1RV17CS108	Prajwal Y R	Application Delivery Management (Adm) Service Network Functions
97	1RV17CS194	Yashwanth Y S	Improvement Of Continuous Integration Pipeline For Faster And Stabilized Builds
98	1RV17CS014	Akshar Prasad	Intelligent Mapping Of Alerts To The Right Responders
99	1RV17CS056	H A Gautham	Enhance Web API Task In Intersight Orchestrator Task Library To Allow Multiple HTTP Authentication Schemes
100	1RV17CS092	Nayana Bannur	Covid-19 Epidemiological Forecasting System
101	1RV17CS103	Deeksha	Time Series Forecasting Of Stock Markets Using Improved LSTM
102	1RV17CS114	Prerana Shenoy S P	Enhancement Of Observability In Contact Center
103	1RV17CS112	Pratheeksha P	Demystifying Resource And Memory Constraints In DSP Multiprocessing
104	**1RV17CS168**	Surya Dheeshjith	Episimmer – An Epidemic Simulation Tool For Decision Support In Communities
105	1RV17CS024	ARPIT KUMAR	Feature Design Of Maintainable Web Application Using React
106	1RV17CS125	Rohit Raj	Framework For Web Based UI Automation
107	1RV17CS148	Shaswat	Indoor Positioning Using BLE Beacons
108	1RV17CS200	Shreya Sahay	Asynchronous Data Stream Processing For Item Ingestion Pipeline In Supply Chain
109	**1RV17CS137**	SANGANBASAVA	Automation In Testing For Network Security

110	1RV17CS155	Shyam A	Automation, Optimization And Migration Of Finops Applications.
111	1RV17CS162	Sparsh G Sarode	Implement Scalable Solution To Detect Conflicting Files In Spark Jobs
112	1RV17CS178	Vaibhav V Athani	Automation For Automatic Access Node Selection During Full Restores For Vmware Virtual Machines
113	1RV17CS165	Suhas S Prasad	Reconciliation Analysis And Justification
114	1RV17CS171	Swathi N R	Ibm Power Servers System Dump Automation Development
115	1RV17CS145	Sharankumar	Building Of End-To-End Test Automation Framework
116	**1RV17CS099**	Nivit Nair	Multi Echelon Inventory Optimization (MEIO) For A Brewing Company
117	1RV17CS204	Pradyumna Chakrapa	Feature Implementation And Testing In Insurance Suite Systems
118	1RV17CS183	Vishak S Bhradwaj	Crawler Management Console
119	1RV17CS154	Shreyas S Kasetty	Automation Framework For Validation Of Optical Modules In Optical Line System
120	1RV17CS189	Faizan Mushtaq	Weblog+ Administered Blogging Application Using ASP.NET Core MVC
121	1RV17CS080	Kushi Kiran	Sales Order Management Using Tableau
122	**1RV17CS090**	Mridul Sadhu	Feature Enhancement Of Open-Source Web Conferencing System
123	**1RV18CS417**	Naziya Akhthar M	Control Tower For Omni Channel
124	**1RV17CS017**	Amisha	Implementation Of Regression Detection Framework
125	**1RV17CS110**	Pranav B M	Volatility Dashboard For Illiquid Assets
126	1RV17CS010	Aditya Raj	ETL Software Migration And Statement Generation
127	1RV17CS151	Shreesha Bhat	Automation Of Corporate Actions On Indices
128	**1RV16CS152**	Sirsha Chatterjee	Partner Integration Platform
129	**1RV17CS071**	Karthik KS	Clustering And Analysis Of Network Logs For Root Cause Analysis (RCA)
130	**1RV17CS153**	Shreyas Nopany	Instrumentation Of Core Matrices For Enhancement Of Platform Adoption
131	**1RV17CS091**	Nadia Tarannum J	Automobile Insights Platform
132	**1RV17CS033**	Chaitanya M R	Surround View Camera System For ADAS

133	1RV17CS089	Monica B	Analyze And Profile Memory Usage Of Split-Rendering Solution In Virtual Reality
134	1RV17CS203	Prerana M Donthi	Safety Subsystem Software Design Of An Automotive Advanced Driver Assistance System
135	1RV17CS166	Suman	Continuous Integrated Test Framework
136	1RV17CS180	Varun Komperla	Improving A Cloud-Based Learning Management System
137	1RV18CS404	Dhara Rajesh Rachh	Leveraging Rhapsody To Automate Cloud Infrastructure Testing
138	1RV17CS050	Dipali Sahay	Epsilon Loyalty – Marketers Ui Application
139	1RV17CS111	Prathamesh Subhash Mali	Data Transfer For CJ Affiliate
140	1RV17CS026	Ashwitha	An Application For PT Sales System
141	1RV17CS028	Ayush Agarwal	Building A Integrated Data Platform
142	1RV17CS038	Chittoor Ravimanya Susrith	Data Anomaly Detection And Reporting
143	1RV17CS195	Devireddy Venkata Manideep	Enterprise E-Sim Management Platform
144	1RV17CS133	Sai Swarna Dowley Rajendran	Stream Processing Engine
145	1RV17CS096	Nikita Kathare	Cloud-Based HR Management System Using Microservices
146	1RV17CS119	Raikar Siddharth Harish	Vehicle Component And Side Prediction
147	1RV17CS202	Srijith	Release Sequence Generator
	1RV17CS201	O Vinati Reddy	

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DEPARTMENT OF TELECOMMUNICATION ENGINEERING
M.Tech inDigital Communication Engineering Project 2019-20

SI. No	Name of the Student	USN	Guide	External Guide	Project Carried at	Title of Work
1.	Bhagyashree A J	1RV18LDC01	Dr. Bhagya R	---	In-house Project carried out at TCE, RVCE, Bangalore	Performance Analysis of Channel Estimation Techniques for High Speed Railways Networks
2.	Aishwarya R	1RV18LDC02	Dr. K.Sreelakshmi	---	In-house Project carried out at TCE, RVCE, Bangalore	EYE BLINK DETECTION TO VOICE COMMUNICATION USING MACHINE LEARNING
3.	Ashwini	1RV18LDC03	K Viswavardhan Reddy	---	In-house Project carried out at TCE, RVCE, Bangalore	Predicting the User Behavior Analysis based on browsing history using Machine Learning Algorithms
4.	Astha Sharma	1RV18LDC04	P Nagaraju	Vishal Narayanan	Intel Technology Pvt Ltd Bengaluru-560103	An Algorithm for Remote Access Tool for the Intel Reference Validation Platforms
5.	Bhavana Ganga R	1RV18LDC05	Dr. Nagamani K	---	In-house Project carried out at TCE, RVCE, Bangalore	Implementation of Intelligent Traffic Management System using Internet of Things
6.	Bindu G Reddy	1RV18LDC06	Dr. G Sadashivappa	Dr. Shanmugam Gunassekaran	Goodix Technology Private Limited	Design and Implementation of Automated Method for Acoustic Performance Analysis of Micro Speaker

7.	CHANDRAKALA J	1RV18LDC07	Shanthi P	Mr. Pavan C	Veoneer India Pvt Ltd	Design and Simulation of Broadband Antenna Array at 78.5GHz for Automotive Radar Applications
8.	Diwakar M	1RV18LDC08	Ranjani G	Dr. Sumesh M A	LEOS-ISRO	FPGA Based Interface Electronics for THz Radiation Detection
9.	Hudha Nargis	1RV18LDC09	Ranjani G	---	In-house Project carried out at TCE, RVCE, Bangalore	Development of Classifier Algorithms for MR Image Analysis
10	Jyoti G	1RV18LDC10	Ranjani G	Karthik, R&D Head,	Ampere Vehicles Pvt.Ltd	Implementation of Driver Efficiency Parameters for Real Time EV Monitoring Using Machine Learning
11	Lakshmi Patil	1RV18LDC11	Dr.K Saraswathi	---	In-house Project carried out at TCE, RVCE, Bangalore	Crop Yield Prediction On The Basis Of Soil Composition Using Machine Learning Algorithms
12	Mahesh karajol	1RV18LDC12	N.N.Nagendra	Ramu Muthangi Project manager	Smart Health Global, Bengaluru ,	Detection of Veins in Subcutaneous Layer using Near - Infrared Light
13	Math Siddalingayya	1RV18LDC13	P Nagaraju	---	In-house Project carried out at TCE, RVCE, Bangalore	Auto suggestion of protocols and adoptive selection of protocols in MRI system
14	Megana S	1RV18LDC14	Dr. B Roja reddy	---	In-house Project carried out at TCE, RVCE, Bangalore	Reduction of Ping Pong Effect in Cognitive Radio Network

15	Mohammad Azharuddin Inamdar	1RV18LDC15	Dr. H V Kumaraswamy	---	In-house Project carried out at TCE, RVCE, Bangalore	Development of PUEA detection method in cognitive radio environment
16	Nagalakshmi Pranitha S	1RV18LDC16	Dr, K Nagamani	---	In-house Project carried out at TCE, RVCE, Bangalore	Implementation of Resource Allocation Algorithm for Cognitive Radio Systems
17	Nagavaishnavi K	1RV18LDC17	Dr. G Sadashivappa	Mr. Subramanya M. S	Nokia - IN	Design and Implementation of Automated Test Verification System for SBTS Software
18	Niveditha V K	1RV18LDC18	Dr.K Saraswathi	---	In-house Project carried out at TCE, RVCE, Bangalore	Design and Simulation of Fog Networks for IOT Application
19	Pateel Shireesha	1RV18LDC19	Mahalakshmi M.N	---	In-house Project carried out at TCE, RVCE, Bangalore	Implementation of Iterative Interference Cancellation in FBMC-QAM System
20	Pooja dayananda K	1RV18LDC20	Dr. B Roja reddy	---	In-house Project carried out at TCE, RVCE, Bangalore	Implementation and Analysis of Uplink Detection Methods for MIMO Systems
21	Raksha K	1RV18LDC21	K Vishwavardhan Reddy	Mr. Malay Si Principal Tester	Nokia solutions & Network	Developing a test Framework for Performance Management of call session control function
22	Ramya Keerthi M R	1RV18LDC22	T P Mithun	---	In-house Project carried out at TCE, RVCE,	An Efficient edge detection Approach to provide better edge connectivity for image analysis

					Bangalore	
23	Rashmi Sadalagi	1RV18LDC23	Nagendra N.N.	---	In-house Project carried out at TCE, RVCE, Bangalore	Free space dielectric measurements using software defined radio
24	Ruben J Franklin	1RV18LDC24	Mohana	Sriram Lakshmina rayana Technical Manager	AMETEK	Design and Implementation of Real time Embedded System for Ultra Precision Machine
25	Sharada N S	1RV18LDC25	Dr B Roja Reddy	---	In-house Project carried out at TCE, RVCE, Bangalore	Design and optimization of polyphase waveform for cognitive radar using artificial Bee Colony Algorithm
26	Sharath S	1RV18LDC26	Dr. Premananda B S	Ramu muthangi	Smart Health Gobal	Development of self assisted voice module in Visually Impaired
27	Shreevalli S	1RV18LDC27	Dr. Premananda B S	---	In-house Project carried out at TCE, RVCE, Bangalore	Estimation Of Reverberation Time By Performing Acousting Echo Cancellation Considering Near-End And Far-End Speech Signals
28	Shrivibhu	1RV18LDC28	Dr. Saraswathi K	---	In-house Project carried out at TCE, RVCE, Bangalore	Design and Development of Device Driver for Storage Controller
29	Sudhan A T	1RV18LDC29	G Ranjani	Mr. Paramesh G.	Nokia solutions & Network	Automation of SSI test cases of Abis and A interface in GSM using Robot framework

30	Tejaswini G Babajiyavar	1RV18LDC30	Dr Bhagya R	Mr. Amritash Kumar	Nokia solutions & Network	Implementation and Analysis of Dynamic spectrum sharing for different RAT's
31	Tejaswini G P	1RV18LDC31	Dr. K Sreelakshmi	---	In-house Project carried out at TCE, RVCE, Bangalore	Brain tumor detection using Deep neural network
32	Usha N	1RV18LDC32	K Vishwavardhan Reddy	---	In-house Project carried out at TCE, RVCE, Bangalore	Dynamic Spectrum Sensing in Cognitive Radio Networks using Machine Learning model
33	Usha V	1RV18LDC33	Dr H V Kumaraswamy	Mr. Anoop P A	Microchip Technology India Pvt. Ltd	Development of UEFI driver compatibility for AHCI controllers
34	Vaibhavi	1RV18LDC34	K Vishwavardhan Reddy	---	In-house Project carried out at TCE, RVCE, Bangalore	Stock market prediction using machine learning techniques
35	Varshitha S	1RV18LDC35	TP Mithun	Anitha Renu Alex Hardware Design Engineer	Intel Technology Pvt. Ltd,	Generic Debug platform for intel’s vision portfolio
36	Vidyashree Dabbagol	1RV18LDC36	Dr. Saraswathi K	Suresh S D Scientist ‘F’	LRDE, DRDO	Design and simulation of target classification based on radar detection

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M.TechRF and Microwave Engineering Project Report List 2019-20

SI. No.	Name of the Student	USN	Guide	External Guide	Project Carried at	Title of Work
1.	Ankita Khandre	1RV18LRF01	Dr. B. Roja Reddy	--	In-house Project carried out at TCE, RVCE, Bangalore	Design and Analysis of 2X2 MIMO Antenna for WLAN Applications
2.	Debasish Dash	1RV18LRF02	Dr. H. V. Kumaraswamy	--	In-house Project carried out at TCE, RVCE, Bangalore	Design of 30 GHz wide band LNA for 5G Cellular Communication using CMOS Technology
3.	Divya A T	1RV18LRF03	Dr K Sreelakshmi	--	In-house Project carried out at TCE, RVCE, Bangalore	Design and simulation of balanced mixers for 5G application
4.	K Radhakrishna	1RV18LRF04	Dr K Sreelakshmi	--	In-house Project carried out at TCE, RVCE, Bangalore	Design of Microstrip Patch Array Antenna for Mobile Satellite Communication.
5.	Misba Fathima	1RV18LRF05	Dr K Sreelakshmi	Mrs Sandhya Reddy	HAL Bangalore	Design and Analysis of Dual circular polarized Array Antenna for X band satellite Applications

6.	Mrunal A Marihal	1RV18LRF06	Dr K Sreelakshmi	--	In-house Project carried out at TCE, RVCE, Bangalore	Design And Analysis of GaN HEMT Based Low Noise Amplifier for UWB Applications
7.	Prakruthi M	1RV18LRF07	N.N.Nagendra	Pratik Mewada	ICON	Analysis of RF transceiver architecture for ultra wide band stepped continuous wave RADAR using VSS
8.	Prathiksha Ramesh	1RV18LRF08	Dr.Shanthi P	--	In-house Project carried out at TCE, RVCE, Bangalore	Design and Fabrication of Planar Antenna for Microwave and Millimeter Wave Applications
9.	Pratiksha R Matlawar	1RV18LRF09	Shambulinga M	Amit Shah	HAL Bangalore	Design and development of S-Band Power Amplifier Module for Satcom Manpack Terminal
10.	Priyanka P N	1RV18LRF10	Shambulinga M	--	In-house Project carried out at TCE, RVCE, Bangalore	Design and simulation of 8W GaN HEMT Power Amplifier for Telemetry Application

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Field Projects

A Project Report
On
"EXTENSIVE SURVEY PROJECT"

At Melukote
(Mandya Dist.)

Submitted in partial fulfillment of the academic requirement in respect of

Project Work

2018-2019

Under the guidance of

Faculty of Civil Engineering Department

R.V. College of Engineering

Project Associates:

BALJIT SINGH KARNAVAT	1RV15CV018
JASTI HARSHA VARDHAN	1RV15CV035
POORNIMA N	1RV15CV057
RANJITH R N	1RV15CV073
SHYAM RAMJI	1RV15CV099
VINAY KUMAR IG	1RV15CV118
ADISHWAR SINGH	1RV12CV072
PANKAJ KIRAN	1RV16CV414

R.V. COLLEGE OF ENGINEERING, BENGALURU-560059

(Autonomous Institution Affiliated to VTU, Belagavi)

DEPARTMENT OF CIVIL ENGINEERING

CERTIFICATE

Certified that the project work entitled "**Extensive Survey Project**" is a bonafide work, carried out by, **JASTI HARSHA VARDHAN (1RV15CV035)** of VII semester in civil engineering during the year 2018-19. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report. The project has been certified as it satisfies the academic requirement in respect of project work.

VALUED

Guide:

Associate Prof: Dr.Vinod A R

Camp officer:

Assistant Prof: Anand Kumar B.G

Assistant Prof: Sunil S

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CONTENTS

1. INTRODUCTION

This extensive survey project is conducted to acquire practical knowledge and applications of theory, and overcome the difficulties that could arise in field during surveying. We also learn the use of different survey instruments and to develop team spirit at work. It also helps develop confidence in handling of survey project. We conducted survey for a new tank project, Highway project, water supply scheme and sewerage project. This survey was conducted at Melukote, located in Mandya District.

1.1 Objects of Extensive Survey Camp:

In order to acquire sound knowledge of both theory and practical necessities and also better appreciate the difficulties that could arise during surveying,

The object of this survey project is as follows:-

1. To impart training in the use of survey instruments and to acquire a comprehensive idea of the project.
2. To train the students under difficult and realistic conditions of surveying work.
3. To develop team spirit in the multi-faceted project work.
4. To instill confidence in the management of survey projects.

1.2 Technical aspects of a project:

The design and construction of any project such as dam, road alignment, water supply system etc requires a thorough investigation of the site as regards to its stability and feasibility. The preliminary investigation starts from the reconnaissance work, study of topo sheets, proposal of alternate sites etc.

The second stage work of investigation includes the survey work at the site in order to collect the data necessary for the design of project elements, preparation of drawings, estimates etc. The office work is confined to the designs, drawings and estimates of the project.

1.3 Historical background of the place:

Melukote in Pandavapura taluk of Mandya District, is one of the sacred places in Karnataka. The place is also known as Thirunarayanapuram.

Melukote is famous for Cheluva Narayana Swamy Temple, with a collection of crowns and jewels which are brought to the temple for annual celebrations. Many more shrines and ponds are located in the town.

2.STUDY OF TOPO SHEET

Toposheet gives the topographical features of the locality like alignment of a railway line, roadway, streams and its distributaries, and permanent structures located in that locality. This map helps in selecting the site for a new tank and also gives a clear picture of transportation facility for men and materials to the proposed site. We also learn about the approximate catchment area of site. This map has to be studied before conducting reconnaissance survey.

2.1 Calculation of yield at site.

The catchment areaof proposed New Tank, determined from the topo sheet is **6.2 Km^2.**

The rainfall of a bad year is always taken as 2/3 of mean amount of rainfall.

Average annual rainfall for Melukote area from Meteorological department data is **70 cm.**

Bad year rainfall is (2/3) of 70cm = 46.7cm

Runoff coefficient is usually assumed as 15 % to 20%

Assuming as 20%

Annual Yield= $\frac{20}{100}$ x46.7cm = 9.34 cm

Yield from catchment $(6.2X10^6)$ x $\frac{9.34}{100}$cum/year = **$0.579 X 10^6$ cum/year.**

3. INTRODUCTION FOR IRRIGATION

Irrigation may be defined as the process of artificially supplying water to soil for raising crops. India is basically an agricultural country and its economy depends to a great extent on the agricultural output. Water is evidently the most vital element in agriculture. Water is normally supplied to the plants by nature through rains.

However, total rainfall in a particular area may either be insufficient or ill timed. In order to get the maximum yield, it is essential to supply the optimum quantity of water and to maintain correct timing of watering. This is possible only through a systematic irrigation system, which includes collecting water during the times of excess rainfall and releasing it to the crop as and when required. The need for irrigation can be summarized in the following four points:

Less rainfall:

When the total rainfall is less than that needed for the crop, artificial supply of water is necessary. In such a case, irrigation system could be developed at the place where more water is available and then, the water can be conveyed to the area where there is deficiency.

Non-uniform rainfall:

The rainfall in a particular area may not be uniform throughout the crop period. During the early periods of the crop, there might be rain, but no water may be available at the end, with the result, that either the yield may become less, or the crop may wither. But the accumulated or stored

water during the excess rainfall period may be supplied to the crop during the period when there is less or no rainfall, but there is a need for watering.

Commercial crop with additional water requirement:

The rainfall in a particular area may be just sufficient to raise the usual crops, but more water may be needed for raising commercial or cash crops, in addition to increasing the annual output by adopting multiple cropping patterns distributed throughout the year.

Controlled water supply:

By constructing a proper distribution system, the yield of crop may be increased. Application of water to the soil by modern methods of irrigation serves the following purpose:

- It adds water to the soil to supply moisture essential for the plant growth.
- It washes out all diluted salts in the soil.
- It reduces the hazard of soil piping.

3.1 BASIC PRINCIPLES OF IRRIGATION

Duty: Duty represents the irrigating capacity of a unit of water. It is the relation between the area of a crop irrigated and the quantity of irrigation water required during the entire period of growth of that crop.

For example, if 5 cumecs of water supply is required for a crop sown in an area of 6200 hectares, the duty of irrigation water will be 6200/5 = 1240 hectares/cumec, and the discharge of 5 cumecs will be required throughout the base period.

Delta: Delta is the total depth of water required by a crop during the entire period from the day of sowing to harvesting.

For example, if a crop requires about 12 watering at an interval of 10 days and a water depth of 10 cm in every watering then the delta for that crop will be 12x10 = 120 cm = 1.2 m. If the area under that crop is A hectares, the total quantity will be 1.2 x A = 1.2A hectare-meters in a period of 120 days.

Crop period: Crop period is the time, in days, that a crop takes from the instant of itssowing to its harvesting.

Base period: Base period for a crop refers to the whole period of cultivation from the time of first watering for sowing the crop, to the last watering before harvesting.

The duty of water is reckoned in the following four ways:

- By the number of hectares that 1 cumec of water can irrigate during the base period, i.e., 1700 hectares per cumecs in the above example.
- By total depth of water, i.e., 1.20 meters.
- By number of hectares that can be irrigated by a million cubic meter of stored water. This system is also used for tank irrigation.

- By the number of hectare meters expended per hectare irrigated. This is also used in tank irrigation.

Relation between duty (D), delta (D) and base period (B) in metric system

Let there be a crop of base period 'B' days. Let one cumec of water be applied to this crop on the field for B days.

Now, the volume of water applied to this crop during B days (V)

$V = 1x\ (Bx60x60x24)m^3$

$= 86,400\ B$ (cubic meter)

By definition of duty (D), one cubic meter supplied for B days irrigates D hectares of land.

Therefore this quantity of water (V) irrigates D hectares of land or $D*10^4$ square meters of area.

Total depth of water applied on this land

= Volume/Area

$= \frac{86400 \times B}{10000}$ meters

$= \frac{8.64 \times B}{D}$ meters

By definition, this total depth of water is called delta (D).

Therefore

$D = \frac{8.64 \times B}{D}$ meters

Or

$D = \frac{864 \times B}{D}$ cm.

Where, D is in cm or m, B in days, and D is duty in hectares/cumec.

Cultivable command area: The gross commanded area also contains unfertile barren land, alkaline soil, local ponds, villages and other areas of habitation. These areas are known as uncultivable areas. The remaining area on which crops can be grown satisfactorily is known as cultivable commanded area. The cultivable command area can be further classified as cultivable cultivated area and cultivable uncultivated area.

Gross command area: An area is usually divided into a number of watersheds and drainage valleys. The canal usually runs on the watershed and water can flow from it, on both sides, due to gravitational action only up-to drainage boundaries. Thus in a particular area lying under the canal system, the irrigation can be done only up-to the drainage boundaries, which can be commanded or irrigated by a canal system.

Consumptive use: Consumptive use of water by a crop is the depth of water consumed by evaporation & transpiration during the crop growth, including water consumed by the accompanying weed growth.

4. INTRODUCTION TONEW TANK PROJECT

4.1. INVESTIGATION FOR A NEW TANK PROJECT

The design and construction of any dam whether earthen, masonry or concrete has to be preceded by a thorough investigation to select the most suitable and economical site. The thoroughness of the investigation depends upon the size of the project.

4.2. PRELIMINARY INVESTIGATION

Before taking up a detailed survey of the project, it is essential to carry out considerable reconnaissance work. The toposheet study of the probable project area gives possible sites in that area and the catchment area of the site.

The reconnaissance survey was carried out by us the day before we started the actual survey. During this survey, we decided the site for the construction of bund, weir & canal alignment. Using chain or tape, rough data regarding the level and the length of the dam was collected.

The preliminary investigation should include:

1. A rough levelling work to give the topography of the site.
2. A study of the rocky out crop and a little boring, to note the nature of the foundation.
3. Availability of construction materials such as earth and good quarry etc.
4. Nature and extent of land, roads, bridges, etc. that would be submerged by the construction of the dam.
5. Benefitsofthe dam to the people.
6. Collection of hydrological data like rainfall, flood discharge etc.
7. Facility for discharging the flood water.

Keeping the above points in view, a thorough study was done, based on which the final choice of the site was made.

4.3. FACTORS CONSIDERED FOR SELECTION OF SITE FOR EARTHEN DAM.

The following topographical and geological features affect the selection of site for earthen dam.

1. The water storage should be largest for the minimum possible height and length; the site should be located in a narrow valley.
2. Good impervious strata [foundation] should be available at moderate depth.
3. Satisfactory and suitable basin should be available.
4. Material for construction should be available locally.
5. There should be suitable site available for waste weir location.
6. Value of the property and land likely to be submerged by the proposed dam should be sufficiently low in comparison with the benefit expected out of the project.

7. Dam should be accessible in all seasons.
8. Overall cost of construction and maintenance is to be taken into consideration.

After the selection of site, the final and precise investigation is carried out. In the present survey work it was assumed that a choice of site was made and the type of dam to be earthen damwith this assumption the detailed survey was carried out, which included

A. Longitudinal section and cross-section along the center line of the bund.
B. Block levelling at the waste weir site.
C. Water spread contours.

4.4. FLY LEVELLING

It is one method to determine the Reduced Level (RL) of a required point. This levelling work is carried from the nearby Permanent Bench Mark (PBM), for example from a railway station or other permanent structure. In this project we established a Temporary Bench Mark (T.B.M) near the bund.

The field work is carried out as follows:

1. Set the levels near the PBM and carry out temporary adjustment.
2. Keep staff on PBM and take readings and enter it as Back Sight (BS) in the field book.
3. Take intermediate points towards the direction of required pointtill it is reached.
4. If the staff is invisible, shift the level and note down the last reading as Fore Sight (FS). After shifting the level, do the necessary temporary adjustment, take the readings of that point and note it down as back sight.
5. Continue this procedure until the required point is reached.
6. The RL of the point is determine by using these formulae:
   1. PC= PBM +BS
   2. RL = PC-IS or PC-FS

4.5 LONGITUDINAL SECTIONS & CROSS SECTIONS ALONG THE PROPOSED CENTRE LINE OF THE TANK BUND:

Object: -

- To obtain the Profile of the valley along the assumed centre line of the bund.
- To estimate the quantity of earthwork for the proposed construction of the bund.

To estimate the quantity of earthwork, the following points should be considered:

TOP WIDTH: Top width of earth dam should be sufficient to keep the seepage line well within the body of dam. It should be able to withstand earthquake and wave action. For small dams, top width is generally governed by minimum road way requirements. Top width of earth dam can be selected as per the following recommendations.

1. $T = 0.2 \times Z+3$ for very low dams (<15 m)
2. $T = 0.55 \times (\sqrt{Z}) + 0.2 \times Z$ for height less than 30m

3. $T = 1.65 \times (\sqrt{(Z + 1.5)}$ for height greater than 30m

where Z is the max. height of dam in metre. We have found **Z=29.850m**

$T = 0.55 \times (\sqrt{29.850}) + 0.2 \times 29.850 = 8.96 = 9$**mts**

FREE BOARD:-

Free board of an earth dam is the height provided above Maximum Water Level (MWL)/Full Reservoir Level (FRL)uptothe Top Bund Level (TBL) in order to prevent over topping of water due to wave action.

"Minimum free board" is defined as vertical distance between max reservoir level and top of dam. The vertical distance between full reservoir level and top of dam is called**"Normal free board".**

The Minimum height of free board for wave action is $\mathbf{1.5h_w}$ where h_w = max. height of wave.

The wave height (h_w) in metre can be calculated according to

1. Molitor's Formula

$$\mathbf{h_w(metre) = 0.032 \times \sqrt{(V \times F)} + 0.763 - 0.271 \times \sqrt{\sqrt{F}}}$$

Where F is fetch in km and F<32 Km

Fetchis defined as the longest unobstructed distance for wind to blow from one edge of reservoir up to the dam on u/s side of the dam. (Fetch can be measured from capacity contour sheet); V is wind velocity in km/hr.

(The max wind velocity in the area is 60 kmph according to meteorological data)

1. Molitor's formula

$$\mathbf{h_w\,(metre) = 0.032 \times \sqrt{(V \times F)} + 0.763 - 0.271 \times \sqrt{\sqrt{F}}}$$

F = 1.4km

V = 60kmph

h_w= 0.763m

$\mathbf{(h_w)max} = 1.5 \times 0.763$

$= \mathbf{1.15\ m}$

4.6. CLASSIFICATION OF EARTHEN DAMS

Earth dams are classified as follows:

1. **Homogenous earth dam**: A purely homogeneous earth dam is composed of single kind of material{Exclusive of the slope protection}. Figure 1 shows a typical cross-section of a purely homogeneous type earth dam.

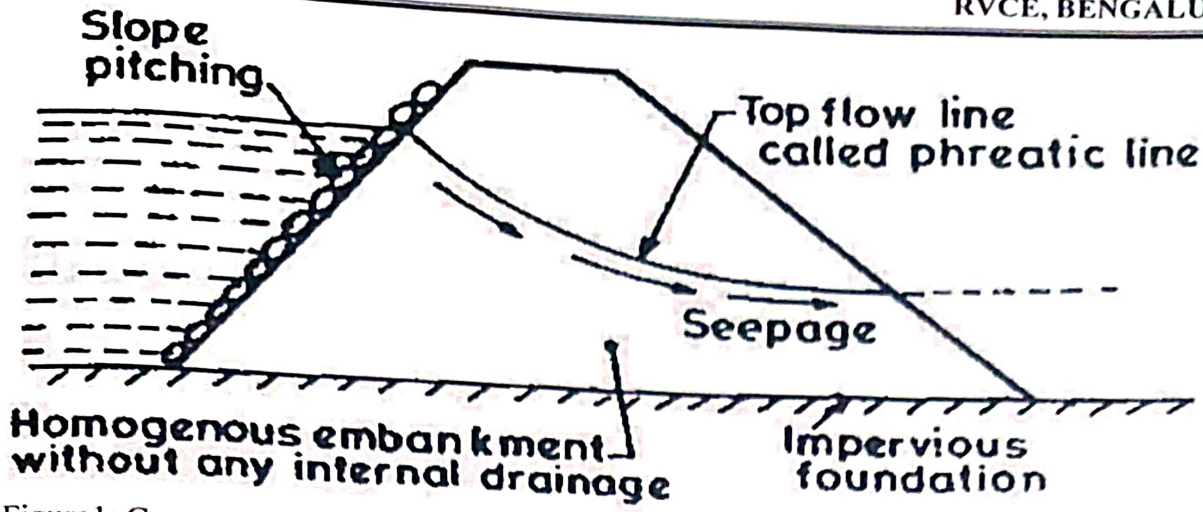

Figure1: Cross-section of a purely homogenous type earthen dam

2. **Zoned embankment type earth dam:** It is the one in which the dam is made up of more than one material. The most common type of a rolled earth dam section is that in which a central impervious core is flanked by zones of material which are considerably more pervious. Figure 2 shows a typical cross-section of a Zoned Embankment type earth dam.

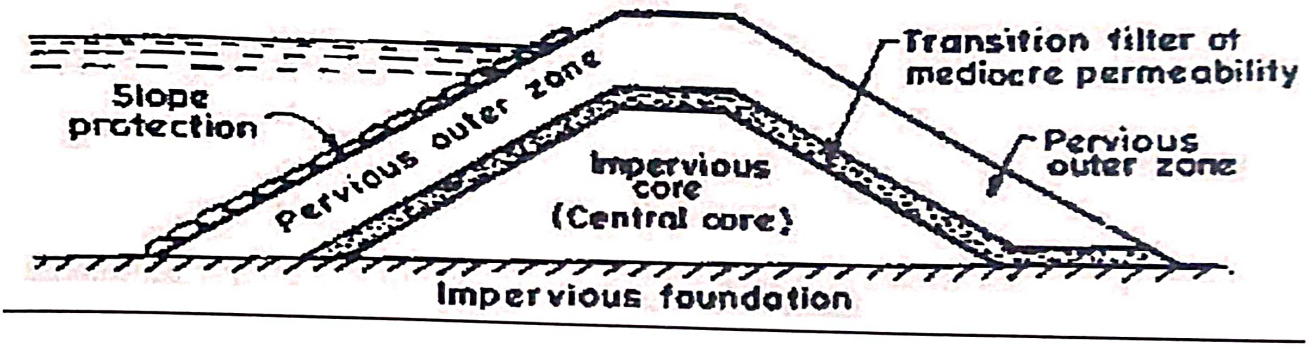

Figure 2: Cross-section of a zoned embankment type dam

3. **Diaphragm Embankment type:** This is a modification over the homogeneous embankment type, in which the bulk of the embankment is constructed of pervious material and a thin diaphragm of impermeable material is provided to check the seepage. The diaphragm may be of impervious soils, cement concrete, bituminous concrete, or any other material, and may be placed either at the center of the section as a central vertical core, or at the upstream face as a blanket. Figure 3 below shows a typical cross-section of a Diaphragm Embankment type earth dam.

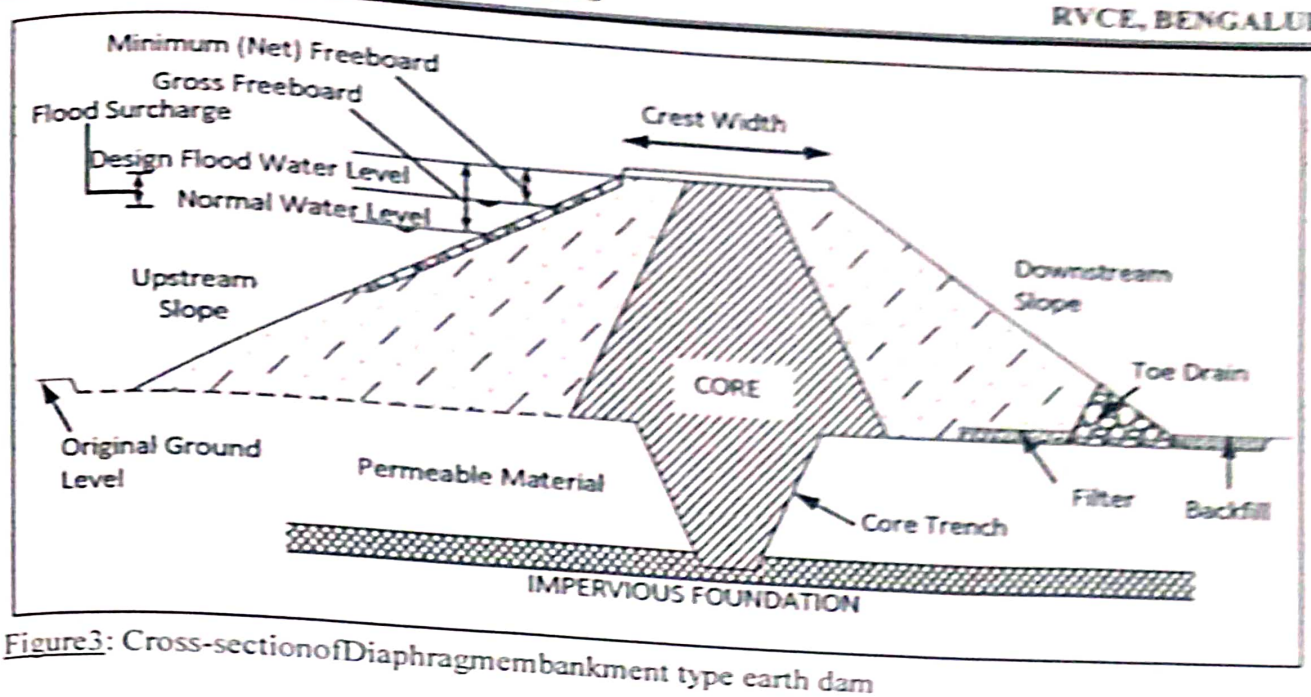

Figure3: Cross-sectionofDiaphragmembankment type earth dam

Table 01: RECOMMENDED SLOPES FOR SMALL HOMOGENEOUS EARTHFILL DAMS ON STABLE FOUNDATION:

Case	Type	Purpose	Soil Classification	Upstream slope	Downstream slope
1)	Homogeneous or Modified Homogeneous	Detention or Storage	a) GW GP SW SP b) GC GM SC c) SM d) CL ML CH MH	Previous 2.5:1 3:1 3.5:1	Not suitable 2:1 2.5:1 2.5:1
2)	Modified Homogeneous	Storage	a) GW GP SW SP b) GC GM SC c) SM d) CL ML CH MH	Previous 3:1 3.5:1 4:1	Not suitable 2:1 2.5:1 2.5:1

Table 02: RECOMMENDED SLOPES FOR SMALL ZONED EARTHFILL DAMS ON STABLE FOUNDTION:

Case	Type	Purpose	Shell Material Classification	CoreMaterials Classification	U/S slope	D/S slope
A	Zoned with "Minimum"	Any	Not critical, rock-fill; GW,GP,SW,SP	Not critical GC, GM, SC, SM, CL, ML, CH, MH	2:1	2:1
B	Zoned with "Maximum" Core 1	Detention OR Storage	Not critical, rock-fill: GW,GP,SW,SP	GC,GM, SC,SM, CL,ML, CH,MH	2:1 2.25:1 2.5:1 3:1	2:1 2.25:1 2.5:1 1:1
C	Zoned with "Maximum" Core1	Storage	Not critical, rock-fill, GW,GP, SW,SP	GC,GM SC,SM CL,ML CH,MH	2.5:1 2.5:1 3.0:1 3.5:1	2:1 2.25:1 2.5:1 3.0:1

Note: CL and IH soils are not recommended for major portions of the cores of earth fill dams. Though any one of the tables can be used for preliminary selection of the bund section the current practice has been in favour of Strange's table.

Core (Hearting): Core or Hearting is a clay type material provided mainly to prevent seepage through the body of the dam. The different types of clay silt for construction of core is provided in Table 01 and Table 02.

Rip Rap or U/S Revetmentisa layer of coarse material placed on the embankment to prevent erosion of soil.

Rip Rap is of two types:

1. Dumped
2. Placed (also known as "Pitching"

The minimum weight of each rock for rip rap is calculated by using Iribarren – Hudson formula.

$$W = \frac{K'\gamma S\mu^3 h^3}{(\mu Cos\beta - Sin\beta)^3 (S-1)^3}$$

W= Minimum weight of Rock to be placed on rip rap in kN.

K'= A coefficient = 0.02

γ = Specific weight of water =9.81 kN/m^3

S= Specific gravity of rip rap material (2.20 to 2.45)

μ = Coefficient of friction of rip rap material (1 to 1.1)

h= effective wave height in meters, calculated using Sverdup –Munk formula

$h = 0.0045 \times F^{0.423} \times U^{1.154}$

F= fetch in km, U =wind velocity in kilometer per hour

β= Angle of U/S slope with the horizontal.

Rip Rap is placed in layers. The innermost layer is the "cushion" which acts as filter to prevent washing off of the soil in the shell zone. It also prevents sinking of the coarse rock into the softened surface of the shell.

Table 03:DIMENSION OF RIPRAP AS A FUNCTION OF WAVE HEIGHT

Max. Wave height	Minimum rip rap Thickness	Min thickness of cushion	
		Fine	**Thickness**
0 to 1.5	300mm	150mm	150mm
1.5 to 3.0	150mm	150mm	150mm
> 3.0m	600mm	150mm	150mm

Cut Off wall

When river bed is having thick stratum of sand, an impermeable structure is constructed within the stratum to reduce seepage through the foundation.

There are two types of cut off wall:

If the bottom of the cut off wall permeates into the impermeable layer then itis called positive cut off wall. This type has the advantage of reducing seepage loss, but the disadvantage of increasing neutral stress due to water, thus decreasing the factor of safety of slope-stability on U/S side.

1) If the bottom of cut off wall does not permeate into loose stratum completely, cut off is called "Partial cut off wall"

The Minimum bottom width of cut off wall is 4m, side of at least 1:1 or flatter slope may be provided in case of overburden. ½:1 or ¼:1 may be provided in soft rock and hard rock respectively. It also prevents seepage, erosion, and mass, instability, boiling and piping.

Internal drainage system:

The drainage system consists of two components.

a) Protective filter which is in contact with core.

b) The conduits, which collect & dispose off seepage water.

Table 4: Minimum thickness of protective filter is provided as follows

Filter Material	Thickness for given head (M)		
	0 to 22m	22 to 46m	46 to 92m
Fine sand	150mm	300mm	450 mm
Coarse sand	200 mm	450 mm	650 mm
Gravel	300mm	600 mm	750mm

Rock toe/ toe drain

The toe drain is placed at D/s side toe of each dam. In small dams only drains are provided. In large dams embankment will be saturated below the phreatic line. And tow drain acts as a disposal zone of the drainage water. Its height varies from 5% of dam height (above tail water level), with external drainage system, to as much on 20% in small dams with no internal drains. The Rock toe designed like protective filter except for the gravel zone. The top width of rock toe will have the dimension same as of berm.

5.WATER SPREAD CONTOUR:

This survey is necessary to draw the capacity contours by the help of witch the storage levels of the tank are fixed. This can be carried out by the following methods.

1. One set of levels is taken along the course of the river on the up stream and another set at right angle to it at the widest region and counters are interpolated.
2. The FTL counter is traced directly and cross section at suitable intervals are taken across this until F T L on the other side is reached. The lowest point of main valley is met and the contours' are interpolated.
3. The entire water spread is covered by block leveling and any number of contours is interpolated.

Of the above three methods the third method is most accurate but it is tedious. Any of the above methods may be adopted depending upon the degree of the accuracy required and the size of the project.

Calculation of the storage capacity of reservoir:

Areas of successive contours are measured using planimeter or by constructing squares.

CONTOUR	AREA ENCLOSED (Km^2)
920	0.00718
930	0.083
940	0.229
950	0.44

If A1, A2, A3 … An, are the areas of successive contours, h being the contour interval, then by Prismoidal rule. The storage capacity can be calculated. Using Prismoidal rule

7 CHANNEL ALIGNMENT

A canal is defined as artificial channel constructed on the ground to carry water from a river or another canal or reservoir to the fields. Usually, canals have a trapezoidal cross section.

Classification of canals

Canals can be classified as in the following ways:

1. **based on nature of source of supply**
   a) **Permanent:** a permanent canal has a continuous source of water supply. Such canals are also called as perennial canals.
   b) **Inundation canal:** an inundation canals draws its supplies from a river only during the high stages of the river. Such canals do not have any head works for diversion of river water to the canal, but are provided with a canal head regulator.
2. **Based on their function**
   a) **Irrigation:** an irrigation canal carries water from its source to agriculture fields.
   b) **Navigation:** canals used for transport of goods are known as navigation canals.
   c) **Power:** power canals are used to carry water for generation of hydroelectricity.
   d) **Feeder canal:** a feeder canal feeds two or more canals.

   A canal can serve more than one function.
3. **Classification based on financial output**
   a) **Productive canal:** the canals which yield net revenue to the nation after full development of irrigation in the area are called productive canal.
   b) **Protective canal:** protective canal is a short relief work for protecting a particular area from famine.
4. **According to size and capacities the canals are classified as:**
   a) **Main canal:** the main canal takes its supplies directly from the river through the head regulator or from reservoir. Its main function is to supply water to the branch canal and sometimes
   b) **Branch canal:** for supply water to large area, the main canal is bifurcated into two or three canals. Each one is called branch canal and particular area under its command. Usually the branch canal also does not supply water directly to the field. In branch canal the discharge varies from 5 to 10 cumec.
   c) **Distributaries:** it takes water from branch canal and distributes same to the field directly. Depending upon the capacity distributaries may be classified as major and minor distributaries.

   Major distributaries: carry 0.25 to 5 m^3/s of discharge. These distributaries take their supplies generally from the branch canal and sometimes from the main canal. The distributaries feed either watercourses through outlets or minor distributaries.

Minor distributaries: are small canals which carry a discharge less than 0.25 m^3/s and feed the water courses for irrigation. They generally take their supplies from major distributaries or branch canals and rarely from the main canals.

d) **Field channel or water courses:** these are small channels maintained by the farmers. The water is supplied through outlet provided in the distributor. The length of the water course is limited to 3km.

5. **Classification based on canal alignment: depending upon the topography, canals may be aligned as**

a)Contour canal

b) Water shed canals

c) Side slope canal

a) Contour canal

A channel aligned nearly parallel to the contours of the country is called as a contour canal. The contour canal can irrigate only one side. As the ground level on other side is quite high, it intercepts drainage sometimes, hence it requires cross drainage works which is a costlier process.

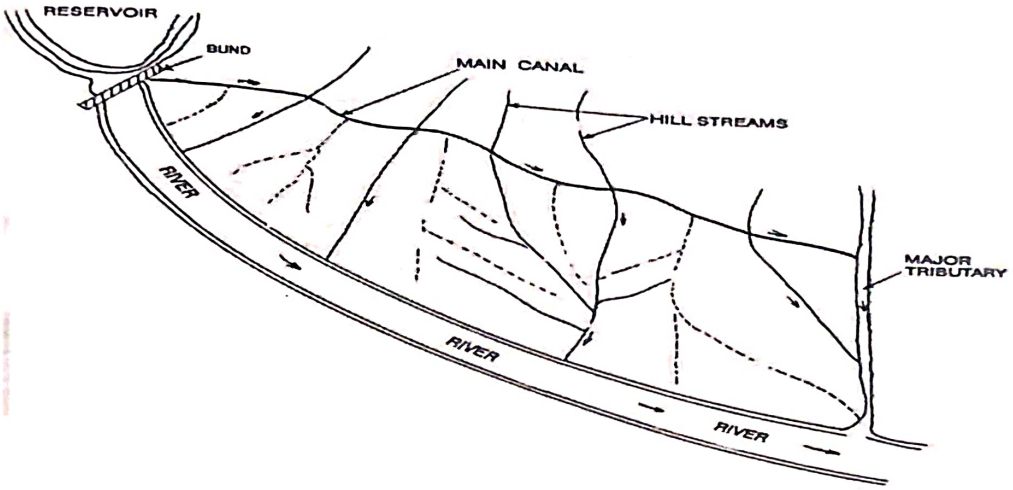

Figure 05: Alignment of contour canal

b) Water shed canal or ridge canal

A ridge canal is aligned along water shed and runs for most of its length in a water shed. When a channel is on water shed, it can command areas on both sides and so large area can be brought under cultivation and also no drainage can intercept water shed and hence the necessity of constructing cross drainage work is avoided.

c)Side slope canal: This canal is roughly almost right angles to the contour . It is either in ridge nor in the valley. this canal will not cross the natural drainage. Hence no cross drainage works are necessary here also. But the slope of side slope canals is very steep. This canal can irrigate only on one side.

distributaries, a service road on only one side9usually, left bank) is provided. These are also called as inspection road. The width of the service roads for main canal varies from 4 to 6m. he width of the road for the branch canal varies from 3 to 4m.

Dowla: the raised portion of the bank is called dowla. It is provided by side of inspection road .they are provided as measure of safety for automobile to drive on the service road. The stop width is generally 0.5m and the height above the road level is 0.5m. the side slope is similar to the side slope of the bank.

Borrow pit: when the earth work excavated is not sufficient for earthwork in filling, then extra earth is borrowed or taken from the pits. These pits are dugged in the adjoining lands and are called borrow pits.

Spoil bank: these are the additional banks constructed with surplus excavated soil which is not required for construction of the bank.

Balancing depth: a canal section will be economical when the excavated earth becomes equal to the earth work in filling. It is possible only when the canal is partially cutting and filling. It also eliminates the need for the spoil banks and borrow pits. Therefore for a given cross section of a canal there can be only one depth t which earth works in excavation is equal to the earth work in filling. The depth is called the balancing depth.

Canal bank: in case of partly cutting, the banks are constructed on sides of the canal to water. The height of the banks depend on the fully supply level of the canal and hydraulic gradients.

In case of fully cutting, the banks are constructed on both sides of the canal to provide with inspectional road. The height of the bank will be low and the top width will be maximum just to provide the road way.

In case of fully embankment, the canal and both the canal banks are constructed above the ground level. The height of the bank will be high and its section will be large due to hydraulic gradient.

Hydraulic gradient: when the water is retained by the canal bank due to the resistance through line which may pass through country side of the bank. This sloping line is known as the hydraulic gradient or saturation gradient. The soil below this line is saturated, but the soil above that line. The hydraulic gradient depends on the permeability of the soil.

Counter berm:when the water is retained by canal bank the hydraulic gradient line passes through the body of the bank. For stability of the bank, this gradient should not intersect the counter side of the bank. It should pass through the base and a medium cover. This projection is known as counter beam. The width of the berm depends on the site condition.

Land width: the total land width required for the construction of a canal depends on the nature of the site condition, such as fully in cutting or fully in banking or partly cutting partly in banking. The total land width=top width of the canal+ twice the berm width+ twice the bottom width banks + A margin of one meter from the heel of the bank on both sides.

Canal lining The impervious layer which protects the beds and sides of the canal is called lining.

Objects of lining

Following are the objects of lining

1. To minimize the seepage losses in canal.
2. To increase the discharge in canal section by increasing the velocity.
3. To prevent erosion of bed and sides due to high velocity.
4. To reduce maintenance of canal
5. To prevent water logging
6. To increase the command areas by decreasing water losses.
7. To protect the canal from the damage by flood due to erosion and scouring of banks.
8. To control the growth of weeds.

Advantages of canal lining:

1. The lining of canal prevents seepage losses and thus more area can be irrigated by the water so saved.
2. The lining provides a smooth surface and hence the velocity of flow in the lined canal increases.
3. The increased velocity minimizes the losses due to evaporation.
4. Lining of canal prevents or reduced the growth of weeds.
5. Canal lining prevents water to come in contact with harmful salts during transit.
6. Water logging of the surrounding area is reduced due to canal lining.
7. Since the velocity of water increased silting is reduced.
8. A lined channel provides safety against breaches. Because of relatively asmooth surface of lining, a lined channel requires a flatter slope. This results in an increase in the command area.
9. It provides the stable selection of the canal.

Disadvantages of canal lining:

1. Initial cost is more.
2. It is very difficult to repair damaged lining.
3. It takes more time to complete the project.

Calculation of Ground level for starting channel alignment

Sluice level	:	927.750m
Full supply depth of water	:	0.280 m (According to Channel design)
Free board	:	0.470 m (Assumed)
Ground level	:	928.500m

Calculation of actual gross command area:

The area enclosed between center line of bund, the mother valley and the final alignment is defined as gross command area. This area can be calculated by using planimeter or by constructing squares method.

Design of Channel Section:

Determination of Irrigable area:

The yield of catchment has been found to be 0.579×10^6 cum

Assuming 10% for evaporation loss and 15 % of conveyance loss i.e., 25% as total loss in reservoir storage capacity.

Volume of water available for irrigation is = $0.75 \times 0.579 \times 10^6$ cum

$= 0.434 \times 10^6$ cum

Assuming average duty of 286 Hectares per million cum for mixed crop pattern.

Area that can be irrigated: $\frac{0.434 \times 10^6 \times 286}{10^6}$ hectares

= 124.412 Hectares.

It is assumed that the reservoir gets filled once annually.

Design of channel section using Lacey's silt theory

Taking average duty for mixed crop pattern as 3000 hectares/cumec.

Discharge $Q = \frac{\text{Area}}{3000} = \frac{124.412}{3000} = \mathbf{0.0415\ m^3 / sec}$

Side slope =1:1

Lacey silt factor = 1.0 (for standard silt)

Velocity in channel $= V=(\frac{Q \times f^2}{140})^{\frac{1}{6}}$

$= (\frac{0.0415 \times 1^2}{140})^{\frac{1}{6}} = \mathbf{0.258 m/s}$

Area of flow $A = \frac{Q}{V} = \frac{0.0415}{0.258} = 0.16\ m^2$

A = (B+Zh) h = (B+h) h = 0.16 (Z: a Horizontal Component of side slope)

Assuming bed width of 30cm

We get **depth of flow** h = **0.28 m**

Longitudinal slope of channel $S= \left[\frac{f^{5/3}}{3340Q^{1/6}}\right] = 1/1965$

Hence assumed **slope of (1/2000) is correct.**

PARTICULARS AND SALIENT FEATURES OF THE NTP

1.	**Place of the project**	Melukote, Pandavapura taluk Mandya district.
2.	**Distance from Bangalore**	133 km.
3.	**Nature of Project**	New Tank Project
4.	**Type of Bund**	Earthen Bund.
5.	**Bund**	
	• Length of Bund • Deepest Streambed • TBL • MWL • FTL • Max height of Bund	288.80m 920.150m. 950m. 948.850m. 947.000m. 29.850m.
6.	**Length of Weir**	60m
7.	**Capacity contour**	$4.12 \times 10^6 m^3$
8.	**Canal** • Length of the Canal • Bed Width • F.S.D. • Free Board	 345 m 0.300 m. 0.280 m. 0.470 m.

Table05:PARTICULARS AND SALIENT FEATURES OF THE NTP

Requirements:

The basic requirements of an ideal alignment between two terminalstations are that is should be:

- Short
- Easy
- Safe
- Economical

8.2 Need for Roadway Planning:

In the present era, planning is considered as a pre-requisite before attempting any development program.This is particularly true for any engineering work, as planning is the basic need for highway development.

Particularly planning is of great importance when funds available are limited in contrast to the amount required which would be very high. This is actually the most important problem that has to be addressed by the developing countries like India as funds have to be utilized in the best possible and economic way.

8.3 The objects of Roadway planning are as follows:

- To plan a road network for efficient and safe traffic operation, but at a minimum cost.
- The cost of the construction, maintenance and renewal of pavement layers and the vehicle operation costs must be given due considerations.
- To arrive at a road system and lengths of different categories of roads, which could provide maximum utility and can be constructed within the available resources during the plan period under consideration.

- To fix up date wise priorities for development of each road link based on utility as the main criterion for phasing the road development program.
- To plan future requirements and improvements of road in view of anticipated developments.
- To work out financing system.

5.4 Factors controlling alignment:

For an alignment to be shortest, it should be straight between the terminal stations. This is always not possible due to various practical difficulties such as intermediate obstructions and topography. The shortest route may have very steep gradients and hence not suitable for vehicle operation. Similarly, there may be construction and maintenance problems along a route, which may otherwise be short and easy. Roads are often deviated from the shortest route in order to cater for intermediate places of importance of obligatory points.

A road which is economical in the initial construction cost need not necessarily be the most economical in maintenance or in vehicle operation cost. It may also happen that shortest and easiest route for vehicle operation may work out to be costliest of the different alternatives from construction view point. Thus it may be seen that an alignment can seldom fulfill all the requirements simultaneously hence, a judicial choice is made considering all the factors

The various factors controlling the alignment of the roadway are:

- Obligatory points
- Traffic
- Geometric design
- Economics
- Other constructions

In hilly areas, additional care has to be taken for setting up the alignment and the factors governing are as follows:

- Stability
- Drainage
- Geometric standards of hill roads
- Resisting length

STEPS INVOLVED IN A NEW PROJECT REPORT

- Map Study
- Reconnaissance Survey
- Preliminary Survey
- Location of Final Alignment
- Detailed Survey
- Materials Survey
- Design

- Earth Work
- Pavement Construction

The following points may be kept in mind while aligning any type of road:

1. Cutting and embankment must be balanced.
2. Curves of larger radius should be used in no case; the radius of curves should be less than 16m.
3. A flat gradient as far as possible should be used, only when unavoidable conditions, the ruling gradient has to be given.
4. Super elevation has to be given for all the curves.
5. Transition curves should be provided between curve and a straight alignment.
6. Vertical curve should be provided whenever the gradient changes.
7. The alignment should be most economical with minimum drainage crossing, so it should follow the ridge.

Table 06: GRADIENTS FOR ROADS IN DIFFERENT TERRAINS

Terrain	Ruling Gradient	Limiting Gradient	Exceptional gradient
Plain or Rolling	1/30	1/20	1/15
Mountainous & steep terrain with elevation more than 3000m above MSL	1/20	1/16.7	1/14.3
Step terrain up to 3000m Height above MSL	1/16.7	1/14.3	1/12.5

Table 07: WIDTH OF ROADWAY FOR VARIOUS CLASSES OF ROADS

Sl No.	Road classification	Roadways width in meters	
		Plain & Rolling Terrain	Mountainous & Steep terrain
1	National & State Highway		
	a) Single lane	12.00	6.25
	b) Two lane	12.00	8.60
2	Major District Roads		
	a) Single lane	9.00	4.75
	b) Two lanes	9.00	--
3	Other District Roads		
	a) Single lane	7.50	4.75
	b) Two lanes	9.00	--
	c) Village Roads	7.50	4.00

Table 08: DESIGN SPEEDS

Road Classification	Plain		Rolling		Mountain		Steep	
	Ruling	Minimum	Ruling	Minimum	Ruling	Minimum	Ruling	Minimum
NH&SH	100	80	80	65	50	40	40	30
MDR	80	65	65	50	40	30	30	20
ODR	65	50	50	40	30	25	25	20
VR	50	40	40	35	25	20	25	20

Table 09: MINIMUM RADII OF ROADS

Classification of Road	Plain		Rolling		Mountain				Steep			
					Area Not affected by snow		Snow bound area		Area Not affected by snow		Snow bound area	
	Ruling	Absolute	Ruling	Absolute	Ruling	Absolute	Ruling	Absolute	Ruling	Absolute	Ruling	Absolute
NH&SH	360	230	230	155	80	50	90	60	50	30	60	33
MDR	230	155	155	90	50	30	60	33	30	14	33	15
ODR	155	90	90	60	30	20	33	23	20	14	23	15
VR	90	60	60	45	20	14	23	15	20	14	23	15

9 DESIGN OF ROADWAY ELEMENTS

9.1.DESIGN OF HORIZONTAL CURVE

Designing of horizontal curve at 180m, 700m, 1020m:

$e+f=\frac{v^2}{127R}$;

where

e is the maximum super elevation that can be provided which is taken as 0.07,

f is the maximum value of lateral friction which is equal to 0.15,

v is the design speed taken as 40 kmph for other village roads,

R is the minimum radius of curve to be provided.

$0.07+0.15=\frac{40^2}{127R}$

R=57.26m

For the horizontal curve encountered provide 58m radius.

Average annual daily traffic = AADT = $134 + \frac{1.2 \cdot 1 \cdot 134 \cdot 182}{365} = 215$ vehicles

From traffic survey, No. of HCV = 12

No. of LCV = 66

Initial traffic volume in terms of no of commercial vehicles per day	Rolling / plain terrain	Hilly terrain
0-150	1.5	0.5
150-1500	3.5	1.5
More than 1500	4.5	2.5

Indicative VDF values (IRC: 37-2001)

CSA = cumulative equivalent standard axles = $N \times 365 \left\{\frac{(1+r)^n-1}{r}\right\} \times L$

CSA= $117 \times 365 \left\{\frac{(1+0.69)^{10}-1}{0.69}\right\} \times 1$ =11700528.67=11.7msa

N = total number of CV x VDF = 78 x 1.5 = 117

r = annual growth rate = 7.5 % (assumed as per SP 72)

L = lane distribution factor = 1 for single lane

Therefore, CSA = (117 x 365) (14.14) x 1 = 8546982.3=8.55msa

As per IRC guidelines , we get

Total pavement thickness-581mm thick

BC = 36 mm

DBM = 60 mm

Granular base = 250 mm

Granular sub base = 235 mm

The following pavement distresses were observed on the stretch that was surveyed:

Distress	Nos.	Quantity
Pothole	35	190m^2
Rutting	6	50mm
Ravelling	28	350.50m^2
Patching	15	75.2m^2
Fatigue cracking	5	6mm

Suitable measures should be undertaken to eliminate these distresses. Some of the measures are: excavating the distressed area and repaving it; laying a fresh wearing course or a patch thick enough to fill the distress; ensuring adequate drainage so as to avoid stagnation of water on the road

INTEGRATED ENVIRONMENTAL ENGINEERING PROJECT FOR MELUKOTE

1. **Water Supply project:**
   a) New source project
   (b) Augmentation scheme.
   c) Water treatment system
   d) Pumping system
   e) Distribution system.
2. **Sewerage project:**
   a) Sewerage system
   b) Sewage Treatment facility.

10. WATER SUPPLY PROJECT FOR MELUKOTE.

Data:

a) Geological
b) Hydrological
c) Sanitary conditions
d) Topography showing elevations of various points, density of population in various zones. This map helps in positioning intake works, treatment plant and type of system to be adopted for conveyance and distribution of water.
e) Legal data of lands
f) Public opinion.

Water supply

1. **Population Forecast :**

	Population in no.	increment	% increase
P_{1991}	3156	-	-
P_{2001}	3235	79	2.5%
P_{2011}	3315	80	2.4%

Increment (i)= $(0.025 \times 0.024)^{1/2}$

$= 0.0244$

Population forecast for 2031,

P_{2031} =?

$F = P(1 + i)^n P_{2031}$

$P_{2031} = 3315(1 + 0.0244)^2$

(2) Sedimentation tank:

(it should be designed for twice the avg. daily demand)

Water demand = 2 X 472500 = 945000 l/day

= 0.011 m^3/sec

Equating horizontal and vertical time of flowing particles.

According to design consideration, the velocity of flow ranges from 15cm/min to 90cm/min

Assuming V= 15 cm/min

= 0.15/60 = 2.5x10^{-3}m/s

$A=\frac{Q}{V}=\frac{0.011}{2.5*10^{-3}}=4.40m^2$

Providing 3 tanks (one tank as stand by)

Assuming D=2B

$B=\sqrt{\left(\frac{7.5}{2}\right)}$ =1.936 ≈ 2m, D = 4m

c/s area of tank = 2m x 4m

Assuming detention period as 5 hours (as the range is 4 to 8 hours)

Volume = 0.01875 x 5 x 3600 = 337.5m^3

Length $L=\frac{337.5}{2\times4\times3}$ = 15m

(3) Slow Sand Filter:

Water tight shallow tank of 2.5m depth

Sand-90cm

Gravel-60cm (4 layers of 15cm)

Rate of filtration= 2250-3400 L/m^2/day

Assuming rate of filtration = 3000 L/m^2/day (as the range is 100 to 200 l/hr/m^2)

P = 3500

Maximum demand = 2 X 472500 = 945000 l/day

= 0.011 m^3/sec

Area of filter required = $\frac{Q_{design}}{ROF}$

$=\frac{0.011\times1000\times24\times3600}{3000}$

= 316.8 m^2

Lets provide 3 filter unit = 105.6 m^2

Assume L=2B

$2B^2$=105.6

B = 7.25 m

L = 14.5 m

H = 3 m (as range is 2.5 to 3.5 m)

Free board = 0.3 m

Filter head = 0.9 m

Sand layer of effective size 0.3 mm = 0.9 m

(range of sand layer should be 90 to 110 cm depth placed over a gravel support & 0.2 mm ∠D10 of sand < 0.4mm)

Gravel layer of 0.6 m thick which contains 3 layers of 0.2 m each , top layer has got a gravel size of 4mm , middle layer is of 20mm & bottom layer of 50mm , gap of under drainage is equal to 0.3 m.

Providing size of one unit as (7.25 x 14.5)m , then provide 3 such units of slow sand filter.

(4) **Disinfection:**

P= 3500

Q=0.011 m^3/s =945000 L/day

Assuming bleaching powder containing 30% of active chlorine & chlorine dosage as 0.3ppm or 0.3mg/l.

Quantity of chlorine required $= \frac{0.3 * 945000}{10^6}$

$= 0.2835$ kg/day

Quantity of bleaching powder required,

$= \frac{0.2835 * 100}{30} = 0.945$ kg/day

Quantity of bleaching powder required per year

$= 0.945 \times 365$

$= 344.925$ kg/year

3. **Overhead Tank:**

$Q_{design} = 0.01875 m^3/s$

$Q_{avg} = 6.25 \times 10^{-3} m^3/s$

Capacity of tank = $(1/3) \times 6.25 \times 10^{-3} = 2.07 \times 10^{-3} m^3/s$

$= 178848$ l/day

Assuming 200000 liters volume tank.

$= 200 m^3$ volume

Providing circular tank

$\frac{\pi d^2}{4} \times D = 200$

$d^2 \times D = 254.64$

Assume D = 4m

d=8m

4. **Economical Diameter of Pipe**

$$\frac{A}{P} = \frac{\pi d^2}{4\pi d}$$

$$R = \frac{d}{4}$$

Take S = 1 in 7

Manning's Formula

$$V = \frac{1}{n} R^{\frac{2}{3}} S^{\frac{1}{2}}$$

Assuming concrete pipe n = 0.011

$$V = \frac{1}{0.011} \left(\frac{d}{4}\right)^{\frac{2}{3}} \left(\frac{1}{7}\right)^{\frac{1}{2}}$$

$$V = 12.025\, d^{\frac{2}{3}}$$

$$Q = V \times A = 12.025 d^{\frac{2}{3}} \times \frac{\pi d^2}{4} = 9.445 d^{\frac{8}{3}}$$

$$d = \left(\frac{0.152}{9.445}\right)^{\frac{3}{8}}$$

d=0.213m

Provide **d=21 cm** as economical diameter of pipe.

5. **Pump with valves:**

Brake horse power BHP,

$$BHP = \frac{wQH}{75\eta_c}$$

$w = 1000 kg/m^3$

Q = discharge

η_c = efficiency of pump x efficiency of motor

H: head

H = Highest level – Lowest level

= 1036.106– 951.520 = 84.586m

$$V = \frac{Q}{A} = \frac{0.011 \times 4}{\pi \times 0.21^2} = 0.318 m/sec$$

Loss due to friction,

$$H_f = \frac{4fln^2}{2gd} = \frac{4 \times 0.01 \times 750 \times 0.318^2}{2 \times 9.81 \times 0.21}$$

$H_f = 0.736$ m

Height of overhead tank = 8m

H = 84.586 + 0.736 + 8 = 93.322m

... to sudden change in elevation, bends, joints)

Assume D = 4m

d=8m

4. **Economical Diameter of Pipe**

$\frac{A}{P} = \frac{\pi d^2}{4\pi d}$

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Take S = 1 in 7

Manning's Formula

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Assuming concrete pipe n = 0.011

$V = \frac{1}{0.011} (\frac{d}{4})^{\frac{2}{3}} (\frac{1}{7})^{\frac{1}{2}}$

$V = 12.025\, d^{\frac{2}{3}}$

$Q = V \times A = 12.025 d^{\frac{2}{3}} \times \frac{\pi d^2}{4} = 9.445 d^{\frac{8}{3}}$

$d = (\frac{0.152}{9.445})^{\frac{3}{8}}$

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H = Highest level – Lowest level

= 1036.106– 951.520 = 84.586m

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Loss due to friction,

$H_f = \frac{4flv^2}{2gd} = \frac{4 \cdot 0.01 \cdot 750 \cdot 0.318^2}{2 \cdot 9.81 \cdot 0.21}$

$H_f = 0.736$ m

Height of overhead tank = 8m

H = 84.586 + 0.736 + 8 = 93.322m

minor losses (due to sudden change in elevation, bends, joints)

Quantity of sewage to be treated for day= $3500 \times 115 = 402500 = 402.5 m^3$

BOD content per day = $402.5 \times 300/1000 = 120.75$ kg

Assuming the organic loading in the pond as 300kg/hectare/day

Surface area required = $\frac{120.75}{300}$ hectare

= $(0.4025 \times 10^4) m^2 = 4025 m^2$

Assuming the length of the tank (L) or twice its width (B)

L x B = 4025

Assuming L = 2B

$B^2 = 4025/2 = 2012.5$

B=44.86m Say 50m

L=2B =2x50=100m

Then, let the effective depth of the tank be 1m with total depth of 2m including free board

Capacity provided = $(100 \times 50 \times 1) = 5000 m^3$

Now, capacity = Sewage flow per day x Detention time in days

Therefore Detention time in days = $\frac{Capacity}{sewage\ flow\ per\ day} = \frac{5000}{402.5}$ =12.42 say 13 days

Adopt an Oxidation pond of dimensions 100m x 50m x 2m and a detention period of 13 days

12. ABBREVIATIONS:

P.B.M	:	Permanent Bench Mark
T.B.M	:	Temporary Bench Mark
R.L	:	Reduced Level
P.C	:	Plane of Collimation
B.S	:	Back sight
I.S	:	Intermediate Sight
F.S	:	Fore sight
T.B.L	:	Tank bund level
M.W.L	:	Maximum water level
F.T.L	:	Full Tank Level
F.S.L	:	Full Supply Level

Report On

"EXTENSIVE SURVEY PROJECT"

At

Melukote

Mandya District, Karnataka

Submitted in partial fulfillment of academic requirement in respect of Project Work

2019-2020

Under the guidance of

Faculty of Civil Engineering Department

R.V. College of Engineering

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DEPARTMENT OF CIVIL ENGINEERING

CERTIFICATE

Certified that the project work entitled "Extensive Survey Project-16CV74" is a bonafide work, carried out VINAYAK M (1RV17CV428) of seventh semester in civil engineering during the year 2019-2020. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report. The project has been certified as it satisfies the academic requirement in respect of project work.

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28/11/19

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2. Dr. Asha K 30/11/19

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ABSTRACT

The present project is an effort to analyze the existing ground profile and geometric elements of the terrain and to plan, analyze and propose irrigation, highway, integrated environmental engineering projects using GIS and remote sensing at Melukote.

Melukote is a famous pilgrimage place located in Pandavapura taluk of Mandya district and is situated amidst extensive tracts of agricultural lands. This seemed to be a good terrain for analyzing and proposing the plan of New Tank which may help to improve the living conditions.

Providing a New Tank would result in many tangible benefits. This would help the people of Melukote with unhindered supply of water in future years. Providing a new and better alignment would also result in many benefits. The present and future requirements of water can be handled by careful alignmen of canal thus serving many irrigation fields in and around Melukote. Providing a proper road alignment will help the people for better connectivity and the ris of accidents can be reduced. By providing proper water supply and sanitar system, the well being of the people can be improved.

CONTENTS

1. INTRODUCTION

This extensive survey project is conducted to acquire practical knowledge and applications of theory, and overcome the difficulties that could arise in field during surveying. We also learn the use of different survey instruments and to develop team spirit at work. It also helps develop confidence in handling of survey project. We conducted survey for a new tank project, Highway project, water supply scheme and sewerage project. This survey was conducted at Melukote, located in Mandya District, Karnataka.

1.1 OBJECTS OF EXTENSIVE SURVEY CAMP

In order to acquire sound knowledge of both theory and practical necessities and also better appreciate the difficulties that could arise during surveying.

The object of this survey project is as follows:

1. To impart training in the use of survey instruments and to acquire a comprehensive idea of the project.
2. To train the students under difficult and realistic conditions of surveying work.
3. To develop team spirit in the multi-faceted project work.
4. To instill confidence in the management of survey projects.

1.2 TECHNICAL ASPECTS OF A PROJECT

The design and construction of any project such as dam, road alignment, water supply system, etc. requires a thorough investigation of the site as regards to its stability and feasibility. The preliminary investigation starts from the reconnaissance work, study of topo sheets, proposal of alternate sites etc.

The second stage work of investigation includes the survey work at the site in order to collect the data necessary for the design of project elements, preparation of drawings, estimates etc. The office work is confined to the designs, drawings and estimates of the project.

1.3 HISTORICAL BACKGROUND OF THE PLACE

Melukote in Pandavapurataluk of Mandya district, Karnataka, in southern India, is one of the sacred places in Karnataka. The place is also known as Thirunarayanapuram. It is built on rocky hills, known as Yadugiri, Yaadavagiri and Yadushailadeepa, overlooking the Cauvery valley. Melukote is about 51 km (32 miles) from Mysuru and 133 km (83 mi) from Bengaluru.

Melukote is the location of the Cheluvanarayana Swamy Temple, with a collection of crowns and jewels which are brought to the temple for the annual celebration. On the top of the hill is the temple of Yoganarasimha. Many more shrines and ponds are located in the town. Melukote is home to the Academy of Sanskrit Research, which has collected thousands of manuscripts.

Yield from catchment $= \frac{6.31 \times 10^6 \times 78.}{100}$ cum/year

$= 0.4964 \times 10^6$ cum/year

3. INTRODUCTION FOR IRRIGATION

Irrigation may be defined as the process of artificially supplying water to soil for raising crops. India is basically an agricultural country and its economy depends to a great extent on the agricultural output. Water is evidently the most vital element in agriculture. Water is normally supplied to the plants by nature through rains.

However, total rainfall in a particular area may either be insufficient or ill timed. In order to get the maximum yield, it is essential to supply the optimum quantity of water and to maintain correct timing of watering. This is possible only through a systematic irrigation system which includes collecting water during the times of excess rainfall and releasing it to the crop as and when required.

The need for irrigation can be summarized in the following four points:

a) Less rainfall:

When the total rainfall is less than that needed for the crop, artificial supply of water is necessary. In such a case, irrigation system could be developed at the place where more water is available and then, the water can be conveyed to the area where there is deficiency.

b) Non-uniform rainfall:

The rainfall in a particular area may not be uniform throughout the crop period. During the early periods of the crop, there might be rain, but no water may be available at the end, with the result, that either the yield may become less, or the crop may wither. But the accumulated or stored water during the excess rainfall period may be supplied to the crop during the period when there is less or no rainfall, but there is a need for watering.

c) Commercial crop with additional water-requirement:

The rainfall in a particular area may be just sufficient to raise the usual crops, but more water may be needed for raising commercial or cash crops, in addition to increasing the annual output by adopting multiple cropping patterns distributed throughout the year.

d) Controlled water supply:

By constructing a proper distribution system, the yield of crop may be increased. Application of water to the soil by modern methods of irrigation serves the following purpose:

- It adds water to the soil to supply moisture essential for the plant growth.

$V = 1 \times (B \times 60 \times 60 \times 24)\ m^3$

$= 86{,}400\ B$ (cubic meter)

By definition of duty (D), one cubic meter supplied for B days irrigates D hectares of land.

Therefore, this quantity of water (V) irrigates D hectares of land or $D \times 10^4$ square meters of area.

$$\text{Total depth of water applied on this land} = \frac{\text{Volume}}{\text{Area}}$$

$$= \frac{86400 \times B}{10000 \times D}$$

$$= \frac{8.64B}{D} \text{ meters}$$

By definition, this total depth of water is called delta (D).

Therefore

$$D = \frac{8.64B}{D} \text{meters} \qquad \text{Or} \qquad D = \frac{864B}{D} \text{cm}$$

Where, D is in cm or m, B in days, and D is duty in hectares/cumec.

Cultivable command area:

The gross commanded area also contains unfertile barren land, alkaline soil, local ponds, villages and other areas of habitation. These areas are known as uncultivable areas. The remaining area on which crops can be grown satisfactorily is known as cultivable commanded area. The cultivable command area can be further classified as cultivable cultivated area and cultivable uncultivated area.

Gross commend area:

An area is usually divided into a number of watersheds and drainage valleys. The canal usually runs on the watershed and water can flow from it, on both sides, due to gravitational action only up-to drainage boundaries. Thus, in a particular area lying under the canal system, the irrigation can be done only up-to the drainage boundaries, which can be commanded or irrigated by a canal system.

Consumptive use:

Consumptive use of water by a crop is the depth of water consumed by evaporation & transpiration during the crop growth, including water consumed by the accompanying weed growth.

Keeping the above points in view, a thorough study was done, based on which the final choice of the site was made.

4.3 FACTORS CONSIDERED FOR SELECTION OF SITE FOR EARTHEN DAM

The following topographical and geological features affect the selection of site for earthen dam.

1. The water storage should be largest for the minimum possible height and length; the site should be located in a narrow valley.
2. Good impervious strata [foundation] should be available at moderate depth.
3. Satisfactory and suitable basin should be available.
4. Material for construction should be available locally.
5. There should be suitable site available for waste weir location.
6. Value of the property and land likely to be submerged by the proposed dam should be sufficiently low in comparison with the benefit expected out of the project.
7. Dam should be accessible in all seasons.
8. Overall cost of construction and maintenance is to be taken into consideration.

After the selection of site, the final and precise investigation is carried out. In the present survey work it was assumed that a choice of site was made and the type of dam to be earthen dam-with this assumption the detailed survey was carried out, which included

A. Longitudinal and cross-sections along the proposed center line of the bund.
B. Block levelling at the waste weir site.
C. Capacity contours.
D. Channel alignment.

4.4 FLY LEVELLING

It is one method to determine the Reduced Level (RL) of a required point. This levelling work is carried from the nearby Permanent Bench Mark (PBM), for example from a railway station or other permanent structure. In this project we established a Temporary Bench Mark (T.B.M.) near the bund.

The field work is carried out as follows:

1. Set the levels near the PBM and carry out temporary adjustment.
2. Keep staff on PBM and take readings and enter it as Back Sight (BS) in the field book.
3. Take intermediate points towards the direction of required point till it is reached.

FREE BOARD

Free board of an earth dam is the height provided above Maximum Water Level (MWL)/Full Reservoir Level (FRL) upto the Top Bund Level (TBL) in order to prevent over topping of water due to wave action.

"Minimum free board" is defined as vertical distance between max reservoir level and top of dam. The vertical distance between full reservoir level and top of dam is called "Normal free board".

The Minimum height of free board for wave action is $\mathbf{1.5h_w}$ where $\mathbf{h_w}$ = max. height of wave.

The wave height ($\mathbf{h_w}$) in metre can be calculated according to

1. Molitor's Formula

$$\mathbf{h_w = 0.032\ x\sqrt{(V \times F)} + 0.763 - 0.271\ x\ \sqrt{F}} \quad \text{..... m}$$

Where F is fetch in km and F < 32 Kms

Fetch is defined as the longest unobstructed distance for wind to blow from one edge of reservoir up to the dam on u/s side of the dam. (Fetch can be measured from capacity contour sheet); V is wind velocity in km/hr.

(The max wind velocity in the area is 60 kmph according to meteorological data)

Now,

$$\mathbf{h_w = 0.032\ x\ \sqrt{(V \times F)} + 0.763 - 0.271\ x\ \sqrt{F}}$$

We have,

F = 1.310km

V = 60kmph

$\mathbf{h_w}$= 0.757m

$(\mathbf{h_w})_{max}$ = 1.5 x 0.757

= **1.13 m ~ 1.5m**

Actual free board = 1.5 h_w+additional safety provision = 1.5 + 0.5 = 2m

4.6 CLASSIFICATION OF EARTHEN DAMS

Earth dams are classified as follows:

1. **Homogenous earth dam:** A purely homogeneous earth dam is composed of single kind of material (Exclusive of the slope protection}. Fig. 1 shows a typical cross-section of a purely homogeneous.

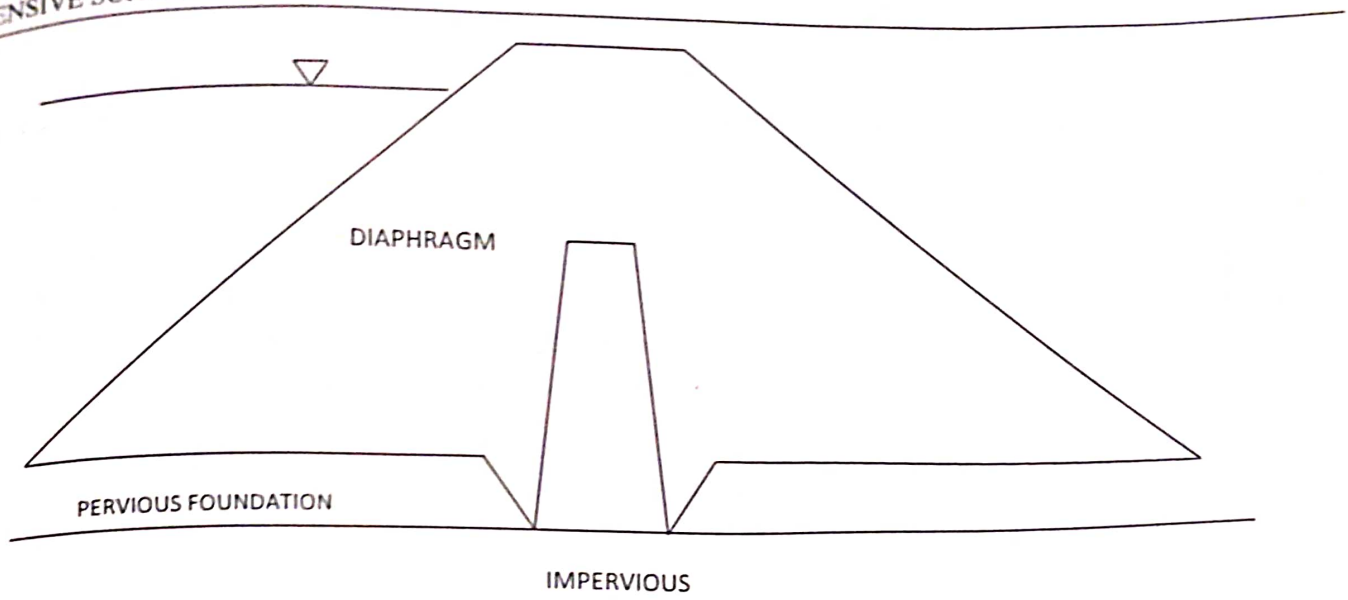


Fig. 3: Cross-section of Diaphragm embankment type earth dam

Table 1: RECOMMENDED SLOPES FOR SMALL HOMOGENEOUS EARTHFILL DAMS ON STABLE FOUNDATION

Case	Type	Purpose	Soil Classification	Upstream slope	Downstream slope
1)	Homogeneous or Modified Homogeneous	Detention or Storage	a) GW GP SW SP b) GC GM SC c) SM d) CL ML CH MH	Previous 2.5:1 3:1 3.5:1	Not suitable 2:1 2.5:1 2.5:1
2)	Modified Homogeneous	Storage	a) GW GP SW SP b) GC GM SC c) SM d) CL ML CH MH	Previous 3:1 3.5:1 4:1	Not suitable 2:1 2.5:1 2.5:1

VALUED

$$W = \frac{K' \gamma S \mu^3 h^3}{(\mu Cos\beta - Sin\beta)^3 (S-1)^3}$$

Where, W = Minimum weight of Rock to be placed on rip rap in kN.
K' = A coefficient = 0.02
γ = Specific weight of water = 9.81 kN/m^3
S = Specific gravity of rip rap material (2.20 to 2.45)
μ = Coefficient of friction of rip rap material (1 to 1.1)
h = effective wave height in meters, calculated using Sverdup –Munk formula
$h = 0.0045 \times F^{0.423} \times U^{1.154}$
F = fetch in km, U = wind velocity in kilometer per hour
β = Angle of U/S slope with the horizontal.

Rip Rap is placed in layers. The innermost layer is the "cushion" which acts as filter to prevent washing off of the soil in the shell zone. It also prevents sinking of the coarse rock into the softened surface of the shell.

Table 3: DIMENSION OF RIPRAP AS A FUNCTION OF WAVE HEIGHT

Max. Wave height	Minimum rip rap Thickness	Min thickness of cushion	
		Fine	**Thickness**
0 to 1.5	300mm	150mm	150mm
1.5 to 3.0	150mm	150mm	150mm
> 3.0m	600mm	150mm	150mm

For height of bund above tail water level

=937-925.5

=11.5m

VALUED

Height of toe drain =.05x11.5=.575m assume to be 0.6m

Cut Off wall

When river bed is having thick stratum of sand, an impermeable structure is constructed within the stratum to reduce seepage through the foundation.

There are two types of cut off wall:

1) If the bottom of the cut off wall permeates into the impermeable layer then it is called positive cut off wall. This type has the advantage of reducing seepage loss, but the disadvantage of increasing neutral stress due to water, thus decreasing the factor of safety of slope-stability on U/S side.

Of the above three methods the third method is most accurate but it is tedious. Any of the above methods may be adopted depending upon the degree of the accuracy required and the size of the project.

Calculation of the storage capacity of reservoir:

Areas of successive contours are measured using planimeter or by constructing squares.

CONTOUR	AREA ENCLOSED (Km^2)
920	0.0123
924.75	0.0825
930	0.2083
935	0.3619

If A1, A2, A3 … An, are the areas of successive contours, H being the contour interval, then by Prismoidal rule. The storage capacity can be calculated.

Using Prismoidal rule

$$V=\frac{H}{3}[(A_1+An)+4(A_2+A_4+A_6+.....)+2(A_3+A_5+A_7+.....)] \text{ cubic meter.}$$

Where, A = in sq.km

$$V=\frac{5}{3}[(0.3619+0.0123)+2(0.2083)+4(0.0825)]$$

$$= \mathbf{1.89 \times 10^6 \ m^3}$$

6. BLOCK LEVELS AT THE WASTE WEIR SITE

WASTE-WEIR

Similarly, as in case of all dam reservoir projects, tanks are provided with arrangements for spilling away the excess water that may enter in to the tank, to avoid over–topping of the tank bund. These escape arrangements may be in the form of a *surplus escape weir or waste weir,* provided in the body or at one end of the tank bund. The weir is a masonry weir with its top level equal to the *Full tank level* (F.T.P). When the tank is full up to its FTL and extra water comes in and discharges over the waste weir. The capacity of the weir is so designed that the water level in the tanks does not exceed the *maximum water level* (M.W.L). The top of the bund will be kept at a level so as to provide suitable freeboard this M.W.L.

A detailed survey at the waste weir site is necessary to design the body wall of waste weir, the approach and draft channel and other protective works and to arrive at the cost of their work. In choosing the site for waste weir the following points must be borne in mind:-

3. **Classification based on financial output**

a) **Productive canal:** the canals which yield net revenue to the nation after full development of irrigation in the area are called productive canal.

b) **Protective canal:** protective canal is a short relief work for protecting a particular area from famine.

4. **According to size and capacities the canals are classified as:**

a) **Main canal:** the main canal takes its supplies directly from the river through the head regulator or from reservoir. Its main function is to supply water to the branch canal and sometimes.

b) **Branch canal:** for supply water to large area, the main canal is bifurcated into two or three canals. Each one is called branch canal and particular area under its command. Usually the branch canal also does not supply water directly to the field. In branch canal the discharge varies from 5 to 10 cumec.

c) **Distributaries:** it takes water from branch canal and distributes same to the field directly. Depending upon the capacity distributaries may be classified as major and minor distributaries.
Major distributaries: carry 0.25 to 5 m^3/s of discharge. These distributaries take their supplies generally from the branch canal and sometimes from the main canal. The distributaries feed either watercourses through outlets or minor distributaries.
Minor distributaries: are small canals which carry a discharge less than 0.25 m^3/s and feed the water courses for irrigation.

d) **Field channel or water courses:** these are small channels maintained by the farmers. The water is supplied through outlet provided in the distributor. The length of the water course is limited to 3km.

5.Classification based on canal alignment: depending upon the topography, canals may be aligned as

a) Contour canal
b) Water shed canals
c) Side slope canal

a) Contour canal

A channel aligned nearly parallel to the contours of the country is called as a contour canal. The contour canal can irrigate only one side. As the ground level on other side is quite high, it intercepts drainage sometimes, hence it requires cross drainage works which is a costlier process.

b) Water shed canal or ridge canal

A ridge canal is aligned along water shed and runs for most of its length in a water shed. When a channel is on water shed, it can command areas on both sides and so large area can be brought under cultivation and also no drainage can intercept water shed and hence the necessity of constructing cross drainage work is avoided.

8. It should be aligned centrally to the commanded area. This will reduces the length of the other canals and ensure better.

7.3 PARTS OF THE CANAL CROSS SECTION

Side slopes: it should be stable. The side slopes depends on the type of the soil. So filling side slopes is (H: V) 1:1 to 2:1 and in cutting 1:1 to 1.5:1 are generally adopted.

Berm: the horizontal distance left at ground level between the top edge of cutting and of the bank.

The berm is provided for the following reasons:

a) to protect bank from erosion
b) to provide a space for widening the canal section in future if necessary.
c) To protect the bank from sliding down towards the canal section
d) The slit deposition on the berm makes an impervious lining.

Free board: is the gap or margin of height or vertical distance between fully supplied level and top of the bank level is called as free board. Free board provides the margin of safety against overlapping of the bank level due to sudden rise in the water surface of a channel on account of improper operations of gates at the head regulator, accidents in operations, wave actions, landslides and inflow during heavy rainfall.

It is provided for the following reasons:

a) to keep a sufficient margin so that the canal water does not overlap the bank in case of heavy rainfall or fluctuation in water.
b) To keep the saturation gradient much below the top of the bank.

Service road: for proper maintainance and inspection of irrigation channels, service roads are provided on both sides of main canals and major branches. In the case of smaller branches and distributaries, a service road on only one side9usually, left bank) is provided. These are also called as inspection road. The width of the service roads for main canal varies from 4 to 6 m. The width of the road for the branch canal varies from 3 to 4 m.

Dowla: the raised portion of the bank is called dowla. It is provided by side of inspection road .they are provided as measure of safety for automobile to drive on the service road. The stop width is generally 0.5 m and the height above the road level is 0.5 m. the side slope is similar to the side slope of the bank.

Borrow pit: when the earth work excavated is not sufficient for earthwork in filling, then extra earth is borrowed or taken from the pits. These pits are dugged in the adjoining lands and are called borrow pits.

Spoil bank: these are the additional banks constructed with surplus excavated soil which is not required for construction of the bank.

Balancing depth: a canal section will be economical when the excavated earth becomes equal to the earth work in filling. It is possible only when the canal is partially cutting and filling. It also

Advantages of canal lining:

1. The lining of canal prevents seepage losses and thus more area can be irrigated by the water so saved.
2. The lining provides a smooth surface and hence the velocity of flow in the linned canal increases.
3. The increased velocity minimizes the losses due to evaporation.
4. Lining of canal prevents or reduced the growth of weeds.
5. Canal lining prevents water to come in contact with harmful salts during transit.
6. Water logging of the surrounding area is reduced due to canal lining.
7. Since the velocity of water increased silting is reduced.
8. A lined channel provides safety against breaches. Because of relatively asmooth surface of lining, a lined channel requires a flatter slope. This results in an increase in the command area.
9. It provides the stable selection of the canal.

Disadvantages of canal lining:

1. Initial cost is more.
2. It is very difficult to repair damaged lining.
3. It takes more time to complete the project.

7.5 CALCULATION OF GROUND LEVEL FOR STARTING CHANNEL ALIGNMENT

Sluice level	:	925.5.5m
Full supply depth of water	:	0.55 m (According to Channel design)
Free board	:	0.2 m (Assumed)
Ground level	:	926.25m

7.6 CALCULATION OF ACTUAL GROSS COMMAND AREA

The area enclosed between center line of bund, the mother valley and the final alignment is defined as gross command area. This area can be calculated by using Planimeter or by constructing squares method.

7.7 DESIGN OF CHANNEL SECTION

Determination of Irrigable area:

The yield of catchment has been found to be 0.49642×10^6 cum

Assuming 10% for evaporation loss and 15 % of conveyance loss i.e., 25% as total loss in reservoir storage capacity.

Volume of water available for irrigation is $= 0.75 \times 0.4964 \times 10^6$ cum

$= 0.3723 \times 10^6$ cum

Assuming average duty of 286 Hectares per million cum for mixed crop pattern.

Table 5: PARTICULARS AND SALIENT FEATURES OF THE NTP

1.	**Place of the project**	Melukote, Pandavapurataluk Mandya district.
2.	**Distance from Bangalore**	133 km.
3.	**Nature of Project**	New Tank Project
4.	**Type of Bund**	Earthen Bund.
5.	**Bund** • Length of Bund • Deepest Streambed • TBL • MWL • FTL • Max height of Bund	 290.0m 99.38m. 937.000m. 935.00m. 934.000m. 31.05m.
6.	**Length of Weir**	35m
7.	**Capacity contour**	1.89 x 10^6 cum
8.	**Canal** • Length of the Canal • Bed Width • F.S.D. • Free Board	 290.00 m 0.400 m. 0.550 m. 0.200 m

9. NEED FOR HIGHWAY PLANNING

In the present era, planning is considered as a pre-requisite before attempting any development program. This is particularly true for any engineering work, as planning is the basic need for highway development.

Particularly planning is of great importance when funds available are limited in contrast to the amount required which would be very high. This is actually the most important problem that has to be addressed by the developing countries like India as funds have to be utilized in the best possible and economic way.

10. THE OBJECTIVES OF HIGHWAY PLANNING

- To plan a road network for efficient and safe traffic operation, but at a minimum cost.
- The cost of the construction, maintenance and renewal of pavement layers and the vehicle operation costs must be given due considerations.
- To arrive at a road system and lengths of different categories of roads, which could provide maximum utility and can be constructed within the available resources during the plan period under consideration.
- To fix up date wise priorities for development of each road link based on utility as the main criterion for phasing the road development program.
- To plan future requirements and improvements of road in view of anticipated developments.
- To work out financing system.

11. FACTORS CONTROLLING ALIGNMENT

For an alignment to be shortest, it should be straight between the terminal stations. This is always not possible due to various practical difficulties such as intermediate obstructions and topography.

The shortest route may have very steep gradients and hence not suitable for vehicle operation. Similarly, there may be construction and maintenance problems along a route, which may otherwise be short and easy. Roads are often deviated from the shortest route in order to cater for intermediate places of importance of obligatory points.

A road which is economical in the initial construction cost need not necessarily be the most economical in maintenance or in vehicle operation cost. It may also happen that shortest and easiest route for vehicle operation may work out to be costliest of the different alternatives from construction view point. Thus it may be seen that an alignment can seldom fulfill all the requirements simultaneously hence, a judicial choice is made considering all the factors

The various factors controlling the alignment of the highway are:

- **Geometric standards of hill roads**

Different sets of geometric standards are followed in hill roads with reference to gradient, curves and speed, they consequentially influence the sight distance, radius of curve and other related features.

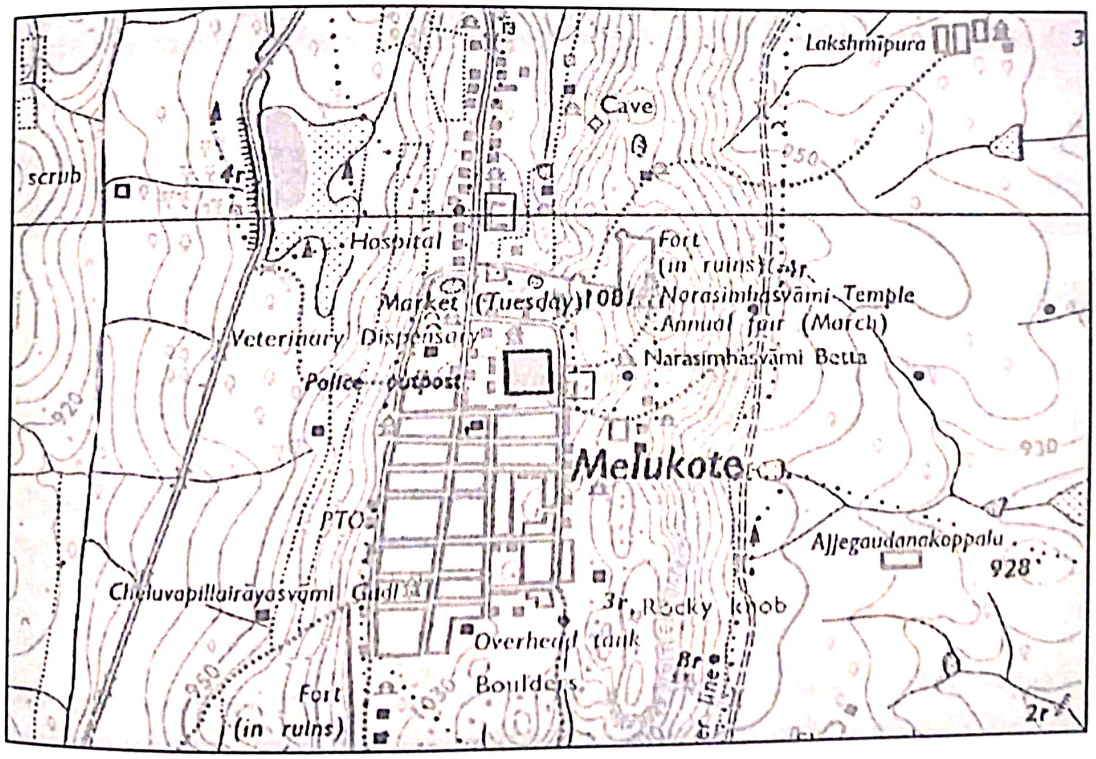
- **Resisting length**

The resisting length of a road may be calculated form the total work to be done to move the loads along the route taking the horizontal length, the actual difference in level between the two stations and the sum of ineffective rise and fall in excess of floating gradient.

12. STEPS INVOLVED IN A NEW PROJECT REPORT

- Map Study
- Reconnaissance Survey
- Preliminary Survey
- Location of Final Alignment
- Detailed Survey
- Materials Survey
- Design
- Earth Work
- Pavement Construction

12.1 MAP STUDY



	5		0	0			3					
VR	90	60	60	45	20	14	23	15	20	14	23	15

RADIUS OF THE CURVE

At chainage 540m,

$$e+f=\frac{v^2}{27R}$$

where,

e is the maximum super elevation that can be provided which is taken as 0.07,

f is the maximum value of lateral friction which is equal to 0.15,

v is the design speed taken as 40 kmph for other district roads,

R is the radius of curve to be provided.

R is the radius of curve was provided $=0.07+0.15=\frac{40\text{^}2}{127R}$

$$R=\frac{40\text{^}2}{127 \times 0.22}$$

$R=57.27$ m $\approx$**58m**

ROAD WIDENING AT CURVE

At chianage 540m

$$W_e=\frac{(n \times l\text{^}2)}{2R}+\frac{V}{9.5\sqrt{R}}$$

n=1 which is the number of lanes

R is the radius of curve provided

V is the design speed taken as 40 kmph for other village roads

l = length of the wheel base of longest vechicle in m (normally 6 or 6.1m is taken)

Existing road width @ horizontal curve =3.75 m

Therefore,

$$We=\frac{(1 \times 6\text{^}2)}{2 \times 58}+\frac{40}{9.5\sqrt{58}}$$

We = **0.86m**

Required road width @horizontal curve = 5.5+0.86 =**6.36m**

Suitable measures should be undertaken to eliminate these distresses. Some of the measures are: excavating the distressed area and repaving it; laying a fresh wearing course or a patch thick enough to fill the distress; ensuring adequate drainage so as to avoid stagnation of water on the road.

AS per MORTH specification:

Distress	Remedies
Pothole	GRT4000, A polymer solution can be used to repair potholes.
Rutting	Pavement with deeper ruts should be leveled and overlayed.
Raveling	Remove the raveled pavement and patch.
Patching	Remove and replace the defective pavement.
Fatigue cracking	Remove the cracked pavement area then dig out and replace the area of poor subgrade and improve the drainage of that area if necessary. Patch over the repaired subgrade.

14. SUGGESTIONS FOR IMPROVEMENT OF THE ROAD:

- **Clearing of drains and construction of the same for discharge of water.**

The drains were filled with mud and weeds, it is necessary to clear the drains so that there won't be any blockage for the flow of water from starting point to 510m. Well constructed and maintained drainage will be provide clean and safe usage of roads from the chainage of 630m to 965m..

- **Providing of road humps on roads and rotary at intersection at chainage of 865m.**

Road humps aren't provided at the necessary points, such as corners or junctions. The area where the survey was done had buildings at the corner of junction, which can block the sight. Hence, road humps need to provided at the these areas for the safety of users.

- **The pedestrian crossing at any point was not given enough attention.**

Side walks had to provided for safety of pedestrians. The roads did not have side walks, hence definite spacing from the roads with enough clearance will be enough for pedestrians to walk. Marks with zebra crossing will help the users to cross the roads safely.

- **Requirement of sign boards, for safe usage of vehicles.**

Enough sign boards are not given at the points, at a distance of 540m there is sharp cut to left, so the sign board at that point can prevent disasters. There is school at the beginning of the chainage point, hence sign there is really important to slow down the vehicle.

15. INTEGRATED ENVIRONMENTAL ENGINEERING PROJECT FOR MELUKOTE

i. WATER SUPPLY PROJECT

a) New source project

b) Augmentation scheme

c) Water treatment system

d) Pumping system

e) Distribution system.

ii. Sewerage project:

a) Sewerage system

b) Sewage Treatment facility.

15.1 WATER SUPPLY PROJECT FOR MELUKOTE.

DATA:

a) Geological

b) Hydrological

c) Sanitary conditions

d) Topography showing elevations of various points, density of population in various zones. This map helps in positioning intake works, treatment plant and type of system to be adopted for conveyance and distribution of water.

e) Legal data of lands.

f) Public opinion.

16. WATER SUPPLY

(1) Population Forecast:

$P_{2011} = 3315$

Increment = 8%

Population forecast for 2031, P_{2031} =?

$F = P(1+i)^n$

$P_{2031} = P_{2011}(1+i)^n$

$P_{2031} = 3500(1+0.08)^2$

$= 3867$ Nos. ≈ 3900 Nos.

Quantity of water required considering leakage and evaporation losses as 25%,

$Q = (3900 \times 135) \times 1.25 = 0.658$ MLD

Assuming N = 0.011 ; M = d/4 ; s = 1 in 80 (Assuming)

$$V = \frac{1}{0.011}\left(\frac{d}{4}\right)^{2/3}\left(\frac{1}{80}\right)^{1/2}$$

$$= 90.91 \times \left(\frac{d}{4}\right)^{2/3} \times 0.043$$

$$V = 4.04d^{2/3}$$

To find dia,

$$Q(0.0206m/s) = V \times A = 4.04d^{2/3} \times (3.14 \times d^2/4) = 3.171d^{8/3}$$

$$d = [0.0206/3.171]^{3/8}$$

$$d = 0.151 \text{ m}$$

Provide d = 160mm as economical diameter of distribution pipe.

(4) **Water treatment unit:**

(i) **Screenings:**

Max. Depth = 1m

Inclined at 45 degree

Detention period = 0 (continuous flow)

Velocity = 1m/sec

(ii) **Sedimentation tank:**

Design for Max. Daily demand

$Q = 1.8 \times 0.658MLD = 1.2 \text{ MLD} = 0.0138 \text{ m}^3/s$

Let Velocity of flow be 0.15/min (As the range is 0.15 to 0.9m/min)

Let Detention period be 4 hours, t = 240min. (as range is 4 to 8 hours)

Length of Detention tank required = d x 0.15 x 240 = 36m

Capacity of Sedimentation tank = $0.0138 \times 4 \times 60 \times 60 = 198.72 \text{ m}^3$

Area of tank = V/L = $198.72/36 = 5.52\text{m}^2$

Let the dimension of tank be 36m x 2.35m x 3.15m

So, provide 3 sedimentation tank out of which is one for standby.

(iii) **Slow Sand Filter:**

P = 3900

Pumping rate/hr,	43875ltrs.
Water requirement/hr	21937.5ltrs.

Period in hours	Demand in Units of Average hourly demand	Cumulative demand	Discharge from Pump	Cumulative Discharge	MBT	Cumulative Discharge per hour	Excess of Demand	Excess of supply
1	0.15	0.15	-	0	0.033	0.033		-
2	0.15	0.30	-	0	0.033	0.066		-
3	0.15	0.45	-	0	0.033	0.099		-
4	0.20	0.65	-	0	0.044	0.143		-
5	0.25	0.90	-	0	0.055	0.198		-
6	0.40	1.30	0.638	0.438	0.088	0.286		
7	0.80	2.10	0.438	0.876	0.176	0.462	0.152	
8	1.20	3.30	0.438	1.314	0.263	0.725	0.589	
9	1.80	5.10	0.438	1.758	0.395	1.120	**0.632**	
10	2.20	7.30	0.438	2.19	0.483	1.600	0.587	
11	2.20	9.50	0.438	2.63	0.483	2.086	0.544	
12	1.50	11.0	-	2.63	0.329	2.415	0.215	
13	1.00	12.0	-	2.63	0.219	2.630	0	
14	0.80	12.8	-	2.63	0	2.810		-
15	0.60	13.4	0.438	3.1		2.942	0.152	
16	1.10	14.5	0.438	3.54		3.183	0.357	
17	1.50	16.0	0.438	3.88		3.512	0.368	
18	1.80	17.8	0.438	4.32		3.907	0.413	
19	1.80	19.6	0.438	4.76		4.302	0.458	
20	1.60	21.2	0.438	5.19		4.653	0.537	
21	1.40	22.6	-	5.19		4.960	0.230	
22	0.80	23.4	-	5.19		5.136	0.050	

Manning's Formula: $V = \frac{1}{N} m^{2/3} i^{1/2}$ $\quad m = d/4$

From water supply scheme, we know that,

Total avg. flow of water = 658 m^3/day

Assuming 85% of water supply is coming out as waste water,

Max sewage flow = 0.85 x 658

= **560** m^3/day

1. **Outfall Sewers:**

Maximum quantity of sewage that is flowing = 2.7 x 560 m^3/day = 0.0175 m^3/s

Assuming velocity = 1m/s (for full running conditions)

Q = A x V

0.0175 = A x 1

A = 0.0175m^2

Providing Circular sewer, so for the above area dia of sewer would be 0.15m, this value obtained is for domestic sewage on considering 75% full running conditions and excluding storm water quantity. Upon considering this we may take the **diameter of outfall sewer as 40cm.**

2. **Main Sewer**: As five mains are connected to outfall sewer,

Discharge coming from main sewer, $Q_{max}/2$ = 0.0175/2= 0.0087 m^3/s and assuming v as 1m/s.

Q = A x V ; A = 0.0087 : So, **d = 10.50 cm.**

This value obtained is for domestic sewer on considering 75% full running conditions and excluding storm water quantity. Upon considering this we may take the **diameter of main sewer as 20cm.**

3. **Branch Sewer**: As minimum of three branch sewers are connected to one main sewer.

Discharge coming from main sewer, $Q_{max}/3$ = 0.0035/3= 0.0012 m^3/s and assuming v as 1m/s.

Q = A x V ; A = 0.0012^2 : So, **d = 3.91 cm.**

This value obtained is for domestic sewer on considering 75% full running conditions and excluding storm water quantity. Upon considering this we may take the **diameter of branch sewer as 10cm.**

Since the velocity of flow developed in a sewer of a particular material depends only upon the hydraulic depth of the sewer and the slope on which the sewer line has been laid, hence for different

18.Solid waste management

Current waste generation = 570 tones/year

Estimated increase in waste generation in a year = 8%

Proposed year of land fill = 20 years

Waste generation after n years = $W(1+x)^n = 570(1+0.08)^{20} = 2656.74$ tones/year

Total waste generated in T years = $\frac{(570+2656.74)}{2} \times 365 \times 20 = 12 \times 10^6$ tones

Total waste in volume = $12 \times 10^6/1 = 12 \times 10^6 m^3$., where 1 tones/cum is the density of waste.

On accounting for 10% cover

Volume of land fill = 13.2×10^6 m^3

Let the height of the land fill site be 20m

Area of the land fill site = 660000 m^2. On increasing 10% of this area for accommodating equipment's etc. We have, A = 726000 m^2.

Let L = 3B

Therefore, dimensions of the land fill site is 1500 x 500 x 20 i.e., 75 hectares.

ABBREVIATIONS:

PBM	:	Permanent Bench Mark
TBM	:	Temporary Bench Mark
RL	:	Reduced Level
PC	:	Plane of Collimation
BS	:	Back sight
IS	:	Intermediate Sight
FS	:	Fore sight
TBL	:	Tank bund level
MWL	:	Maximum water level
FTL	:	Full Tank Level
FSL	:	Full Supply Level

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Criterian_1.3.3

Sample Major Projects

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Feature Enhancement and Qualification of TotemSC and PathfinderSC

A Major Project Report
16EC81

Submitted by,

Nischith T R **1RV17EC093**

Under the guidance of

Prof. Namita Palecha
Assistant Professor
Dept. of ECE
RV College of Engineering

John Alwyn
Principal Product Specialist
SCBU
Ansys

In partial fulfillment of the requirements for the degree of

Bachelor of Engineering in

Electronics and Communication Engineering

2020-2021

RV College of Engineering®, Bengaluru

(Autonomous institution affiliated to VTU, Belagavi)

Department of Electronics and Communication Engineering

CERTIFICATE

Certified that the major project (16EC81)work titled ***Feature Enhancement and Qualification of TotemSC and PathfinderSC*** is carried out by **Nischith T R** (**1RV17EC093**) who is bonafide student of RV College of Engineering, Bengaluru, in partial fulfillment of the requirements for the degree of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the Visvesvaraya Technological University, Belagavi during the year 2020-2021. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the major project report deposited in the departmental library. The major project report has been approved as it satisfies the academic requirements in respect of major project work prescribed by the institution for the said degree.

Signature of Guide	Signature of Head of the Department	Signature of Principal
Prof. Namita Palecha	Dr. K S Geetha	Dr. K. N. Subramanya

PRINCIPAL
RV COLLEGE OF ENGINEERING
BENGALURU - 560 059

External Viva

Name of Examiners	Signature with Date
1. SHILPA D R	
2. Online Exam	

DECLARATION

I, **Nischith T R** students of eighth semester B.E., Department of Electronics and Communication Engineering, RV College of Engineering, Bengaluru, hereby declare that the major project titled '**Feature Enhancement and Qualification of TotemSC and PathfinderSC**' has been carried out by me and submitted in partial fulfilment for the award of degree of **Bachelor of Engineering** in **Electronics and Communication Engineering** during the year 2020-2021.

Further I declare that the content of the dissertation has not been submitted previously by anybody for the award of any degree or diploma to any other university.

I also declare that any Intellectual Property Rights generated out of this project carried out at RVCE will be the property of RV College of Engineering, Bengaluru and we will be one of the authors of the same.

Place: Bengaluru

Date: 10/07/2021

Name	Signature
1. Nischith T R(1RV17EC093)	Nisch

August 25, 2020

Nischith T R

RV College of Engineering

Subject: Offer letter

Dear Nischith,

This refers to our discussions and interviews you have had with us. We are happy to extend you an offer to join our company as an Intern in our Product Specialist Team in Bengaluru.

Your internship will begin on January 5, 2021 and your last working day will be July 5, 2021. During the internship, you will be paid stipend of INR 35,000/- per month (10% TDS will be deducted from this).

This offer will be valid subject to all the facts set forth in your application are true. Please give us your acceptance by signing the duplicate copy of this letter and confirm your date of joining.

For Ansys Software Pvt. Ltd.

DocuSigned by:
Sanjay Asane
22538108871B4D4...

Sanjay Asane
Country Human Resources Manager

I have read and understand the offer of employment and accept it.

DocuSigned by:
Nischith T R
C4ED4B9007814FA...

Nischith T R

ACKNOWLEDGEMENT

I am indebted to my guide, **Prof. Namita Palecha**, Assistant Professor, RV College of Engineering . for the wholehearted support, suggestions and invaluable advice throughout my project work and also helped in the preparation of this thesis.

I also express our gratitude to my panel members **Dr. ShylaShree N**, Associate Professor and **Prof. Namita Palecha**, Assistant Professor, Department of Electronics and Communication Engineering for their valuable comments and suggestions during the phase evaluations.

My sincere thanks to the project coordinators **Prof. Subrahmanya K N**, **Dr Nithin M** and **Dr Veena Devi** for their timely instructions and support in coordinating the project.

My gratitude to **Prof. Narashimaraja P** for the organized latex template which made report writing easy and interesting.

My sincere thanks to **Dr. K S Geetha**, Professor and Head, Department of Electronics and Communication Engineering, RVCE for the support and encouragement.

I express sincere gratitude to our beloved Principal, **Dr. K. N. Subramanya** for the appreciation towards this project work.

I thank all the teaching staff and technical staff of Electronics and Communication Engineering department, RVCE for their help.

Lastly, I take this opportunity to thank my family members and friends who provided all the backup support throughout the project work.

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Server Emulator and Virtualizer for Next-Generation Rack Servers

A Major Project Report (18EC81)

Submitted by,

Chinmay N **1RV18EC035**

Under the guidance of

Dr.Sujata D. Badiger
Assistant Professor
Dept. of ECE
RV College of Engineering

Deepak K
Software Engineer
CSPG UCS
Cisco

In partial fulfillment of the requirements for the degree of

Bachelor of Engineering in

Electronics and Communication Engineering

2021-22

RV College of Engineering®, Bengaluru

(Autonomous institution affiliated to VTU, Belagavi)

Department of Electronics and Communication Engineering

CERTIFICATE

Certified that the major project (18EC81) work titled ***Server Emulator and Virtualizer for Next-Generation Rack Servers*** is carried out by **Chinmay N (1RV18EC035)** who is bonafide student of RV College of Engineering, Bengaluru, in partial fulfillment of the requirements for the degree of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the Visvesvaraya Technological University, Belagavi during the year 2021-22. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the major project report deposited in the departmental library. The major project report has been approved as it satisfies the academic requirements in respect of major project work prescribed by the institution for the said degree.

Signature of Guide	Signature of Head of the Department	Signature of Principal
26/7/22	26/7/22	
Dr.Sujata D. Badiger	Dr. Ravish Aradhya H. V.	Dr. K. N. Subramanya
	Professor & Head Dept. of Electronics & Communication Engg. RV College of Engineering Bengaluru-560 059.	VICE PRINCIPAL RV College of Engineering Mysore Road, Bengaluru-560 059

External Viva

Name of Examiners	Signature with Date
1. Dr. Gowda Raju M	05/08
2. Dr. K. R Sudhindra	5/8

Cisco Systems (India) Private Limited
SEZ, Cessna Business Park,
Sarjapur Marathalli Outer Ring Road
Bengaluru - 560 103, India
CIN: U31909KA1995PTC019505
Tel : 91-80-4426 0000
Fax : 91-80-4426 4040

01 July 2022

To Whom It May Concern:

Dear Sir/Madam,

Internship Completion Letter

This is to confirm that Chinmay Niranjan, was an Intern with Cisco Systems from 02 February 2022 until 01 July 2022.

Chinmay Niranjan, held the position of COLLEGE INTERN.TECH UNDERGRAD.

During the internship, Chinmay worked on the project under the guidance of Venkata Ramanamurthy Saripalli.

If you have any questions, please contact People Support on 000 800 040 2244 (India) or +1 408 906 1477 (Outside India).

Yours Sincerely,

Rashmi Naik
People Shared Services Specialist
Authorized Signatory
Cisco Systems (India) Private Limited

DECLARATION

I, **Chinmay N** student of eighth semester B.E., Department of Electronics and Communication Engineering, RV College of Engineering, Bengaluru, hereby declare that the major project titled '**Server Emulator and Virtualizer for Next-Generation Rack Servers**' has been carried out by me and submitted in partial fulfilment for the award of degree of **Bachelor of Engineering** in **Electronics and Communication Engineering** during the year 2021-22.

Further I declare that the content of the dissertation has not been submitted previously by anybody for the award of any degree or diploma to any other university.

I also declare that any Intellectual Property Rights generated out of this project carried out at RVCE will be the property of RV College of Engineering, Bengaluru and we will be one of the authors of the same.

Place: Bengaluru

Date:

Name	Signature
1. Chinmay N(1RV18EC035)	

ACKNOWLEDGEMENT

I am indebted to my guide, **Dr.Sujata D. Badiger**, Assistant Professor, RV College of Engineering . and **Deepak K**, Software Engineer, Cisco for their wholehearted support, suggestions and invaluable advice throughout my project work and also helped in the preparation of this thesis.

I also express my gratitude to my panel members **Dr.Sujata D. Badiger**, Assistant Professor and **Dr. M Uttara Kumari**, Professor, Department of Electronics and Communication Engineering for their valuable comments and suggestions during the phase evaluations.

My sincere thanks to the project coordinators **Dr Nithin M**, **Dr Veena Devi** and **Prof. Sindhu Rajendran** timely instructions and support in coordinating the proj My gratitude to **Prof. Narashimaraja P** for the organized latex template which made report writing easy and interesting.

My sincere thanks to **Dr. Ravish Aradhya H. V.**, Professor and Head, Department of Electronics and Communication Engineering, RVCE for the support and encouragement.

I express sincere gratitude to our beloved Principal, **Dr. K. N. Subramanya** and Vice Principal, **Dr. Geetha.K.S** for the appreciation towards this project work.

I thank all the teaching staff and technical staff of Electronics and Communication Engineering department, RVCE for their help.

Lastly, I take this opportunity to thank my family members and friends who provided all the backup support throughout the project work.

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CERTIFICATE

Certified that the major project work titled ***'Enterprise Datawarehouse Reporting in MicroStrategy'*** is carried out by **Krupa Sindhu S (1RV16CS074)** in partial fulfilment for the award of degree of **Bachelor of Engineering in Computer Science and Engineering** of the Visvesvaraya Technological University, Belagavi during the year 2019-2020. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the major project report deposited in the departmental library. The major project report has been approved as it satisfies the academic requirements in respect of major project work prescribed by the institution for the said degree.

14/7/2020

Signature of Guide	Signature of Head of the Department	Signature of Principal
Dr.Azra Nasreen	Dr. Ramakanth Kumar P	Dr.K.N.Subramanya

External Viva

Name of Examiners	Signature with Date
1 Dr. NAGARAJA. G.S.	G.S. NR 11/09/2020
2	

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And NBA, New Delhi

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Enterprise Datawarehouse Reporting in MicroStrategy

PROJECT REPORT

Submitted by

Krupa Sindhu S **1RV16CS074**

Under the guidance of

Dr. Azra Nasreen
Assistant Professor
Dept of CSE
RV College of Engineering

Shivakumar D
Manager
Mast Global

In partial fulfilment for the award of degree
of
Bachelor of Engineering
in
Computer Science and Engineering
2019-2020

Individual certificate/Letter of Engagement as Intern from the Company

Sun 05-Jul-20 4:23 PM

Gowda, Shivakumar

Internship Letter - Krupa Sindhu Srinivas

To Shetty, Lakshmi

Cc Srinivas, Krupa Sindhu

Retention Policy LBI - Mail - 365 Days (1 year) Expires 05-Jul-21

You replied to this message on 05-Jul-20 6:32 PM.

Hi ,

Please find the below Internship program details for Krupa.

Name: Krupa Sindhu Srinivas
Internship start date: 8th January, 2020
Internship End date: 7th July, 2020
Organization Name: Mast Global Business Services India (Lbrands)
Team name: Business Intelligence, Data Services
Project name: Enterprise Data warehouse Reporting in MicroStrategy

Krupa is quick learner and effective during her Internship Program. She hone up technical skills quickly and successfully completed and contributed to her Internship Program.

Krupa: Thanks and Best of luck for your future endeavors.

Regards!
Shiva

Thanks & Regards,
Shivakumar D | Manager, BI | Mast Global Business Services India| Manyata Embassy Business Park, SEZ, H2, Mountain Ash, 5th Floor | Bangalore - 560045 , India |
Desk: 66747172 | Mobile: +91 9538433453 | Email - sgowda@mast.com |

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DECLARATION

I, **Krupa Sindhu S**, student of eighth semester B.E., Department of Computer Science and Engineering, RV College of Engineering, Bengaluru-59, bearing **USN: 1RV16CS074** hereby declare that the major project titled **'Enterprise Datawarehouse Reporting in MicroStrategy'** has been carried out by me and submitted in partial fulfilment for the award of degree of **Bachelor of Engineering** in **Computer Science and Engineering** during the year 2019-20.

Further I declare that the content of the dissertation has not been submitted previously by anybody for the award of any degree or diploma to any other university.

Place: Bengaluru

Date:

Name **Signature**

Krupa Sindhu S (1RV16CS074)

ACKNOWLEDGEMENT

I am indebted to my guide**, Dr. Azra Nasreen, Assistant Professor, Dept of CSE** for her wholehearted support, suggestions and invaluable advice throughout our project work and also helped in the preparation of this thesis. I would also like to extend my gratitude to **Mr. Shivakumar D, Manager, Mast Global** for his guidance in the mechanics of the project.

I express my gratitude to my panel members **Dr. Krishnappa H K, Associate Professor, Dr. Soumya A, Associate Professor,** Department of Computer Science and Engineering for their valuable comments and suggestions.

My sincere thanks to **Dr. Ramakanth Kumar P.**, Professor and Head, Department of Computer Science and Engineering, RVCE for his support and encouragement.

I express sincere gratitude to my beloved Principal, **Dr. K. N. Subramanya** for his appreciation towards this project work.

I thank all the **teaching staff and technical staff** of Computer Science and Engineering department, RVCE for their help.

Lastly, I take this opportunity to thank my **family** members and **friends** who provided all the backup support throughout the project work.

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Feature Design of Maintainable Web application Using React js

PROJECT REPORT

Submitted by

ARPIT KUMAR **1RV17CS024**

Under the guidance of

Prof. Sneha M
Assistant Professor
Dept of CSE
RV College of Engineering

Sravan Kumar
Tech Lead (HUB)
MiQ Digital

In partial fulfilment for the award of degree
of
Bachelor of Engineering
in
Programme Name
2020-2021

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CERTIFICATE

Certified that the major project work titled ***'Feature Design of Maintainable Web application Using React js'*** is carried out by **Arpit Kumar (1RV17CS024)** in partial fulfilment for the award of degree of **Bachelor of Engineering in Computer Science and Engineering** of the Visvesvaraya Technological University, Belagavi during the year 2019-2020. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the major project report deposited in the departmental library. The major project report has been approved as it satisfies the academic requirements in respect of major project work prescribed by the institution for the said degree.

16/7/21

Signature of Guide	Signature of Head of the Department	Signature of Principal
Prof. Sneha M	Dr. Ramakanth Kumar P	Dr.K.N. Subramanya

External Viva

	Name of Examiners	Signature with Date
1	Dr B Sathish Babu	23/7/21
2	Dr shilpa chandhari	

Individual certificate/Letter of Engagement as Intern from the Company Should be Attached (Applicable only for Internship Students)

MiQ Digital India Pvt. Ltd.
5th & 6th floor SKAV 909,
9/1 Lavelle road,
Bengaluru-560001

23rd June 2021
Bangalore

TO WHOSOEVER IT MAY CONCERN

This is to certify that Mr. Arpit Kumar is pursuing his internship with MiQ Digital India Pvt. Ltd. from 4th Jan 2020.

Sincerely,
For MiQ Digital India Pvt. Ltd.

Ramya Parashar
Chief Operating Officer

ACKNOWLEDGEMENT

I am indebted to my guide**, Prof Sneha M,** Assistant Professor**, Dept of CSE** for her wholehearted support, suggestions and invaluable advice throughout the project work and also helped in the preparation of this thesis. I would also like to extend my gratitude to **Sravan Kumar, Tech Lead, MiQ Digital** for his guidance in the mechanics of the project.

I also express my gratitude to the panel member **Dr. Krishnappa H K**, Assistant Professor**,** Department of Computer Science and Engineering for their valuable comments and suggestions.

My sincere thanks to **Dr. Ramakant Kumar P.**, Professor and Head, Department of Computer Science and Engineering, RVCE for his support and encouragement.

I express sincere gratitude to our beloved Principal, **Dr. K. N. Subramanya** for his appreciation towards this project work.

I thank all the **teaching staff and technical staff** of Computer Science and Engineering department, RVCE for their help.

Lastly, I take this opportunity to thank my **family** members and **friends** who provided all the backup support throughout the project work.

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Monitoring Tools integrating with ODIN for Alletra, Primera and Distributed Storage Systems

PROJECT REPORT

Submitted by

Akshay Shankar **1RV19CS012**

Under the guidance of

Dr. Prapulla S. B.
Assistant Professor
Dept of CSE
RV College of Engineering

Pradeep Dixit
Senior Storage Manager
Hewlett Packard Enterprise

In partial fulfilment for the award of the degree
of
Bachelor of Engineering
in
Computer Science Engineering
2022-2023

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CERTIFICATE

Certified that the major project work titled **'Monitoring Tools integrating with ODIN for Alletra, Primera and Distributed Storage Systems'** is carried out by **Akshay Shankar (1RV19CS012)** in partial fulfilment for the award of the degree of **Bachelor of Engineering in Computer Science and Engineering** of the Visvesvaraya Technological University, Belagavi during the year 2022-2023. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the major project report deposited in the departmental library. The major project report has been approved as it satisfies the academic requirements in respect of major project work prescribed by the institution for the said degree.

Signature of Guide	Signature of Head of the Department	Signature of Principal
Prapulla S. B.	Dr. Ramakanth Kumar P	Dr.K.N.Subramanya

External Viva

	Name of Examiners	Signature with Date
1	Dr. Kaavya	
2	Dr. Shobha G	7/6

Hewlett Packard Enterprise

Hewlett Packard India Software Operation Pvt. Ltd.
Survey. No.192, Whitefield Road
Mahadevapura Post
Bengaluru - 560 048
www.hpe.com/in
CIN: U72200KA1988PTC009435

Registered Office:
Survey No. 192 Whitefield Road
Mahadevpura Post
Bengaluru - 560 048
Karnataka, India

June 3, 2023

TO WHOM SO EVER IT MAY CONCERN

Employment Certificate

This is to confirm that the individual mentioned below is an active employee of Hewlett Packard Enterprise.

Employment Information

Legal Name	Akshay Shankar
Employee ID	[redacted]
Legal Entity	Hewlett Packard India Software Operation Pvt. Ltd.
Job Title	College Intern
Hire Date	January 24, 2023
FULL / Part Time	Full time

This letter is being issued on the request of the employee.

Sincerely,

Bhaskar Gopal
Manager Human Resources

ACKNOWLEDGEMENT

I am indebted to my guide**, Dr. Prapulla S. B.,** Assistant Professor**, Dept of CSE** for her wholehearted support, suggestions and invaluable advice throughout my project work and helped in the preparation of this thesis. I would also like to extend my gratitude to **Pradeep Dixit, Senior Storage Manager, Hewlett Packard Enterprise** for his guidance in the mechanics of the project.

I also express my gratitude to my panel members **Dr. Soumya A**, Associate Professor, and **Dr. Sandhya S**, Assistant Professor**,** Department of Computer Science and Engineering for their valuable comments and suggestions.

My sincere thanks to **Dr Ramakanth Kumar P.**, Professor and Head, Department of Computer Science and Engineering, RVCE for his support and encouragement.

I express sincere gratitude to our beloved Principal, **Dr. K. N. Subramanya** for his appreciation towards this project work.

I thank all the **teaching and technical staff** of the Computer Science and Engineering department, RVCE for their help.

Lastly, I take this opportunity to thank my **family** members and **friends** who provided all the backup support throughout the project work.

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Major Project: Phase-II Report
On
DESIGN AND DEVELOPMENT OF FRAMEWORK FOR SYSTEM VALIDATION USING ARTIFACTS

18 MCN 41

Submitted by

Ganapatsa Kalburgi
USN: 1RV19SCN06

Under the Guidance
of

Dr. SHARVANI G. S.
Associate Professor
Department of CSE
RV College of Engineering®
Bengaluru - 560059

Ms. PUNEETHA MUKHERJEE
Project Manager
Infineon India Pvt Ltd
Bengaluru – 560001

Submitted in partial fulfillment for the award of degree
of
MASTER OF TECHNOLOGY
in
COMPUTER NETWORK ENGINEERING

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

2020-2021

RV COLLEGE OF ENGINEERING®,

(Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Bengaluru– 560059

CERTIFICATE

Certified that the project work titled **"Design And Development Of Framework For System Validation Using Artifacts"** carried out by **Ganapatsa Kalburgi, USN: 1RV19SCN06**, a bonafide student, submitted in partial fulfilment for the award of **Master of Technology** in **Computer Network Engineering** of **RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi,** during the year **2020-21.** It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

Dr. Sharvani G. S.	**Dr. Ramakanth Kumar P**	**Dr. K. N. Subramanya**
Associate Professor	Head of Department	Principal
Department of CSE,	Department of CSE,	RVCE,
RVCE, Bengaluru –59	RVCE, Bengaluru–59	Bengaluru–59

PRINCIPAL
RV COLLEGE OF ENGINEERING
BENGALURU - 560 059

Name of the Examiners	**Signature with Date**
1._____	_____
2._____	_____

RV COLLEGE OF ENGINEERING®,

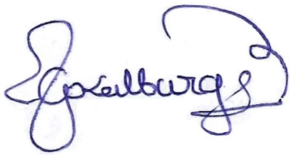
(Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Bengaluru– 560059

DECLARATION

I, **Ganapatsa Kalburgi**, student of fourth semester M.Tech in **Computer Network Engineering**, **Department of Computer Science and Engineering,** RV College of Engineering®, Bengaluru, declare that the Major Project titled **"Design and Development of Framework for System Validation Using Artifacts",** has been carried out by me. It has been submitted in partial fulfilment for the award of degree in **Master of Technology** in **Computer Network Engineering** of RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2020-21**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.



Date of Submission: **Signature of the Student**

Student Name: Ganapatsa Kalburgi

USN: 1RV19SCN06

Department of Computer Science and Engineering

RV College of Engineering®,

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IFIN HR- 2021
23 June 2021

CERTIFICATE

To Whom It May Concern

Formal Data:

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Evaluation of work:

Ganapatsa is working as a Student Trainee with us from 03 Aug 2020 to 30 Jun 2021 and working on project **"Automated Test Case Generation From Requirements/Use case/User Stories using NLP"**

Ganapatsa is an avid and independent learner, has good analytical & application skills and has shown exemplary performance during the internship period.

We wish Ganapatsa a long fruitful career and success in future endeavors.

For Infineon Technologies India Pvt. Ltd.

Vijay Manjeshwar
Sr. Director -IFIN HR

Shyam Kommajosyula
Sr. Director - IFIN ATV MC

ACKNOWLEDGEMENT

I am indebted to **Rashtreeya Sikshana Samithi Trust**, Bengaluru for providing me with all the facilities needed for the successful completion of Major Project Phase-II work at **Rashtreeya Vidyalaya College of Engineering (RVCE)** during the tenure of my Course.

I would like to thank **Dr. K N Subramanya, Principal,** for giving me an opportunity to be a part of RVCE and for his timely help and encouragement during the tenure of the Major Project Phase-II work.

I am greatly thankful to **Dr. Ramakanth Kumar P., Professor and Head, Dept. of CSE** for his motivation and constant support during my tenure of my Major Project Phase-II work.

I take this opportunity to convey my sincere gratitude to my internal guide and panel member Dr**. Sharvani G. S., Associate Professor**, Dept. of CSE, and external guide **Puneetha Mukherjee, Project Manager, Infineon India Pvt Ltd** for their advice, support and valuable suggestions help me to accomplish the Major Project Phase-II work in time.

Special thanks to **Dr. Nagaraja G.S., Professor & Associate Dean** and panel member**, Prof. Sandhya S.,** Department of Computer Science & Engineering for their valuable comments, constructive inputs and feedback during the Phase-I and Phase-II oral presentations.

I extend my thanks to all who have directly or indirectly extended their constant support for successful completion of my Major Project Phase-II work.

Ganapatsa Kalburgi
1RV19SCN06

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RV COLLEGE OF ENGINEERING®

(Autonomous Institution Affiliated to VTU, Belagavi)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Bengaluru– 560059

2018-19

A Dissertation Report on

"HLR Framework Development for Continuous Integration"

Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY
in
COMPUTER NETWORK ENGINEERING
by

Chaitra N Korlahalli
USN: 1RV17SCN04

Under the guidance

of

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Mr. Prasad Vasa
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Rashtreeya Sikshana Samithi Trust

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Bengaluru– 560059

CERTIFICATE

Certified that the project work entitled **"HLR Framework development for Continuous Integration"** carried out by **Ms. Chaitra N Korlahalli,** USN: **1RV17SCN04**, a bonafide student of **RV College of Engineering, Bengaluru** in partial fulfillment for the award of **Master of Technology** in **Computer Network Engineering** of **RV College of Engineering, Bengaluru affiliated to Visvesvaraya Technological University, Belagavi** during the year 2018-19. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

Prof. Sandhya S Assistant Professor, Department of CSE, R.V.C.E., Bengaluru –59	13/6/19 **Dr. Ramakanth Kumar P.** Prof & Head of Department, Department of CSE, R.V.C.E., Bengaluru–59	**Dr. K. N. Subramanya** Principal, R.V.C.E., Bengaluru–59 Principal RV College of Engineering Mysuru Road Bengaluru - 560 059

Name of the Examiners **Signature with Date**

1

2

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Bengaluru– 560059

DECLARATION

I, Chaitra N Korlahalli, student of fourth semester M.Tech, in the Department of Computer Science and Engineering, RV College of Engineering, Bengaluru declare that the project entitled **"HLR Framework development for Continuous Integration"** has been carried out by me and submitted in partial fulfillment of the course requirements for the award of degree in **Master of Technology** in **Computer Network Engineering** of RV College of Engineering, Bengaluru affiliated to Visvesvaraya Technological University, Belagavi during the academic year **2018-19**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

Date of Submission: 13/06/2019

Signature of the Student

Student Name : Chaitra N Korlahalli
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U72900DL2006PTC155149

This is to certify that **Chaitra Korlahalli N (NOKIA ID: 62175553)** of RV College of Engineering, pursuing M. Tech in "Computer Network Engineering" programme of 2018-19 batch affiliated to Visveswaraya Technological University (VTU), Belagavi has been employed with Nokia Solutions and Networks India Private Ltd., as 'Student Trainee' from 18th July 2018.

The employee has worked on the project titled **'HLR Framework development for Continuous Integration'**, under Nokia Software Core Engineering Registers (NSW CE REG) department.

Authorized Signatory
Prasad Vasa P V B B
R&D Line Manager

ACKNOWLEDGEMENT

Any achievement, be it scholastic or otherwise does not depend solely on the individual efforts but on the guidance, encouragement and cooperation of intellectuals, elders and friends. A number of personalities, in their own capacities have helped me in carrying out this project work. I would like to take this opportunity to thank them all.

First and foremost I would like to express my sincere gratitude to my guide **Prof. Sandhya S,** Assistant professor, Department of CSE, R.V.C.E, Bengaluru, for her able guidance, regular source of encouragement and assistance throughout this project

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I extend my cordial regards and thanks to my principal **Dr. K. N. Subramanya** for his valuable support.

I would also like to thank my manager **Mr. Prasad Vasa** and mentor **Mr. Vishwanathan** who guided me and helped me in completion of this project with all their support.

I thank my parents, and all the faculty members of Department of Computer Science & Engineering for their constant support and encouragement.

Last, but not the least, I would like to thank my peers and friends who provided me with valuable suggestions to improve my project.

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Major Project: Phase-II Report

on

MODELLING, DEVELOPEMNT AND VALIDATION OF CONTACTLESS INTERFACE FOR NFC READER IC

18MPE41

Submitted by

SHRUTHA K V

USN: 1RV20EPE15

Under the Guidance

of

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Vinay Singh P & Rajesh Sugasi
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Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY
in
POWER ELECTRONICS

2021-22

RV COLLEGE OF ENGINEERING®

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(Autonomous Institution Affiliated to Visvesvaraya Technological University, Belagavi)

CERTIFICATE

Certified that the project work titled "**Modelling, Development and Validation of Contactless Interface for NFC Reader C**" carried out by Shrutha K V, USN: 1RV20EPE15, a bonafide student of RV College of Engineering, Bengaluru in partial fulfilment for the award of Master of Technology in Power Electronics of RV College of Engineering, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the year 2021-22. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

12/7/22

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PRINCIPAL
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Name of the Examiners | **Signature with Date**

1._____ _____

2._____ _____

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Bengaluru– 560059

DECLARATION

I, **Shrutha K V**, student of fourth semester M.Tech in **Power Electronics**, **Department of Electrical and Electronics Engineering,** RV College of Engineering, Bengaluru declare that the project titled **"Modelling, Development and Validation of Contactless Interface for NFC Reader IC"**, has been carried out by me. It has been submitted in partial fulfilment of the course requirements for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

12/07/2022
Date of Submission:

Shrutha K.V
Signature of the Student

Student Name: Shrutha K V

USN: 1RV20EPE15

Department of Electrical and Electronics Engineering

RV College of Engineering®,

Bengaluru-560059

Date : 28 June, 2022

To Whomsoever It May Concern

Ongoing Internship Certificate

This is to certify that **Ms. Shrutha K V, ID - NXF79310**, is undergoing an internship at **NXP India Pvt. Ltd., Bangalore**. She started the internship on **27 September, 2021** on the project titled: **Modelling, Development and Validation of Contactless Interface for NFC Reader IC under the guidance of Mr. Vinay Singh P and Mr. Rajesh Sugasi.**

Under the company's Intellectual Proprietary rights clause any disclosure of scripts or software programs written during the Internship tenure which are subjected to be used under project are strictly private and confidential and cannot be disclosed to any person outside the company.

For NXP INDIA Pvt Ltd

Manish Subodh
HR Manager

ACKNOWLEDGEMENT

Any achievement, be it scholastic or otherwise does not depend solely on the individual efforts but on the guidance, encouragement and cooperation of intellectuals, elders and friends. A number of personalities, in their own capacities have helped me in carrying out this project titled, "**Modelling, Development and Validation of Contactless Interface for NFC Reader IC**". I would like to take this opportunity to thank them all.

Firstly, I deeply express sincere gratitude to my guide **Dr. S G Srivani**, Professor, Head of the department and Associate Dean, P.G. studies, Department of Electrical and Electronics Engineering, for her patience, valuable guidance, suggestions, advice and assistance throughout this project. She has been a constant and regular source of encouragement to me during this period.

I would like to express my thanks to **Dr. Rudranna Nandihalli**, Professor and Head of the department (Retired), Department of Electrical and Electronics Engineering, RVCE, Bengaluru, for his motivation and constant support throughout this project.

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I would like to thank all the faculty members and non-teaching staff of the Department of Electrical and Electronics Engineering, RVCE for their constant support.

I am indebted to my parents for their constant support and encouragement throughout my life. I thank all my friends provided me with valuable suggestions to improve the project.

Shrutha K V

Power Electronics

Department of Electrical and Electronics Engineering

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ABSTRACT

Near Field Communication (NFC) is a short-range wireless networking technology that facilitates making transactions, contactless payments, exchanging digital content, and connecting electronic devices with a single tap. NFC is compatible with the millions of contactless cards and readers that have already been installed around the world. NFC transmits data using radio waves in the same way as Bluetooth and Wi-Fi do. RFID (Radio-frequency identification) technology concepts that rely on electromagnetic induction to convey data are also used in the NFC area. NFC operates at a frequency of 13.56 megahertz, with data transmission rates of 106, 212, 424 or 848 kilobits per second. NFC permits two way interactivity between electronic gadgets with additional security and intelligibility. Transmission protocol initialization and anticollision sequence have notable value in the Contactless Interface. There are various types of NFC tags progressed for numerous applications. To communicate, signalling protocol has to exits. The signalling protocol provides two devices to communicate and exchange information. There are three signalling modes in NFC referred as Type-A, Type-B and Type-F.

The project work aimed to develop Contactless Interface module for the NFC Reader IC to achieve compatibility with NFC Type-A and Type-B Cards. To resolve multiple card selection, anticollision technique was implemented along with the activation sequence using C language. Entire Contactless Interface module was validated utilizing Cadence Software using tcl scripts to simulate the behaviour of a Type-A and Type-B card. Buck-Boost converter was designed and simulated with the defined parameters to provide required voltage to the contactless integrated module depending on the placement of card on the NFC Reader IC using PSIM software.

The NFC system was designed and developed to operate in contactless interface mode. A test framework was deployed to validate the entire Contactless interface module and NFC Type-A & Type-B using 13 test cases and all the test cases were passed with successful exchange of data. Anticollision technique was incorporated to select one card at a time if multiple card approaches NFC Reader IC. The Buck-Boost converter provided an output of 1.5V to the Contactless Interface module with the supplied input of 5V when the Card was on the utmost proximity to NFC reader IC.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Shrutha K V, Dr S G Srivani "NFC Type A Technology", Journal of Emerging Technologies and Innovative Research, Volume 9 Issue 6 , June-2022 |

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GLOSSARY

NFC	Near Field Communication
PCD	Proximity Coupling Device
PICC	Proximity Card or object
REQA	REQuest command, Type A
REQB	REQuest command, Type B
WUPA	Wake-UP command, Type A
WUPB	Wake-UP command, Type B

CHAPTER 1

INTRODUCTION

A combination of contactless identification and connecting technologies gave rise to NFC, a modern, short-range wireless technology. It was jointly created by Sony and NXP Semiconductors (previously Philips). Between two NFC-enabled devices, such as mobile phones, or between an NFC-enabled mobile phone and a compatible RFID (Radiofrequency identification) chip card or reader that is bear, NFC is designed to allow the exchange of various types of information, such as phone numbers, MP3 files, pictures, or digital authorizations. NFC is intended to be used as a key to access services and content, including cashless payment and access control. The foundation of NFC is inductive coupling. NFC uses magnetic induction between two loop antennas that are placed in close proximity to one another. NFC transmits data at a rate of 106 kbit/s to 848 kbit/s across a distance of around 11 cm and operates at a frequency of 13.56 MHz. In NFC, there must be at least one target device. The initiator works carefully to produce an RF field that will power the passive target, also known as a tag[1]-[6].

NFC is backward compatible with Sony FeliCa card standards as well as the Smart Card infrastructure based on ISO/IEC 14443 standard for proximity contactless smart cards. A new protocol for information exchange between two NFC devices arose and was defined in the ECMA-340 and ISO/IEC 18092 standards. NFC is extensively used across the globe for minuscule range communication with the application of low data rate. There are numerous modes, NFC compliant devices communicates[7]-[9]. There are various types of NFC tags progressed for numerous applications as shown in the figure1.1. To communicate signalling protocol has to exits. The signalling protocol provides two devices to communicate and exchange information. There are three signalling modes in NFC referred as Type-A, Type-B and Type-F[10]-[12].

The Reader to be compatible with all the types of card, one has to follow ISO/IEC 14443 standards. The Buck-Boost converter is a dc to dc converter that provides higher voltage than input and also the lesser voltage than input based on the duty cycle. Therefore, the required voltage to the reader IC of contactless interface module, Buck-Boost Converter can provide seamlessly[13]-[15].

The project work attempted to produce NFC Reader IC compatible to ISO/IEC 14443 standards with adopting anticollision sequence to avoid multiple cards activation at a time. Contactless Interface module of the reader is reconcilable for NFC Type-A and Type -B. Buck-Boost converter is incorporated to provide required voltage as per the placement of card near the NFC Reader IC.

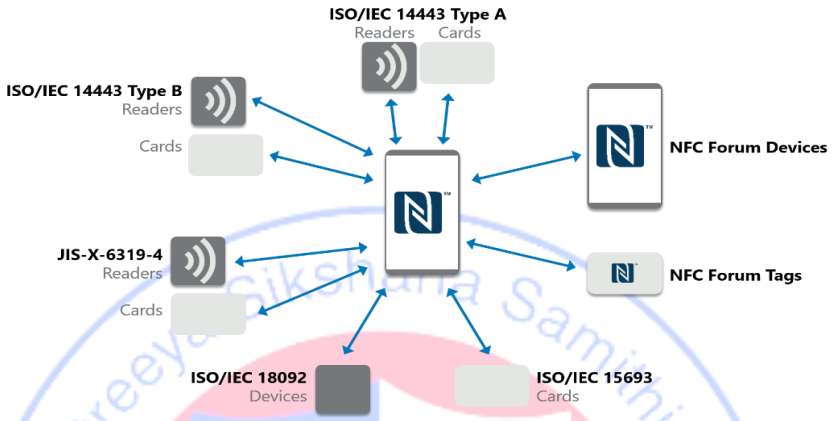

Figure 1.1: NFC Technology

1.1 Literature survey

The NFC technology is widely employed across many industries, including the Internet of Things, mobile devices, financial applications, and identity identification. Numerous scholars have conducted extensive research on subject and have produced numerous academic papers and journal articles on security in NFC applications.

The benefits of employing NFC read/write mode include low protocol overhead and support for various data types. The use of NFC read or write mode, that was initially intended for unidirectional data transfer from an active reader to a passive tag, has been taken advantage of by the authors. They have made an effort to implement bi-directional half-duplex communication between two NFC-enabled active devices[1]. But one major obstacle is dealing with the reader collision issue and performing transactions quickly and securely. In order to construct a secure multi-factor authentication system that leverages bi-directional communication for mutually authenticating two NFC devices, the methodology presented in this paper is suggested. Two-factor authentication is necessary for the proposed system. Kerberos and fingerprints are both used for it. It was noted that it took almost a second to get an authentication ticket from Kerberos. The success of the paper could be seen in the 600 ms it takes to unlock the NFC-

enabled phone. The challenge was to implement bi-directional communication between two active NFC devices and to do so quickly and with minimal energy consumption. One NFC smartphone can exchange data with one NFC tag using the reader/writer mode. Two mobile devices having NFC capabilities can share data with one another in peer-to-peer mode. A mobile phone can communicate with an NFC reader by acting as a smart card in card emulation mode.

The various ISO standards that NFC complies with and NFC operation modes are discussed. They demonstrate that NFC is susceptible to security breaches that could expose sensitive information about users. The adoption of NFC technology and its uses by organizations may suffer as a result. A scientific approach to improve security is also suggested along with a list of various assaults. Data insertion, data alteration, and MITM attacks are attacks that compromise integrity[3]. Eavesdropping and replay attacks are relevant to secrecy in the NFC area. The study demonstrates that although communication in the centimeter range may seem more secure, it is actually quite prone to security breaches since technologies like NFC call for little to no additional verification.The field of identification cards, bus cards, access control, e-wallets, and other smart card applications has seen the most advancements in contactless technology recently. The financial IC card is the application of technology that is just starting to gain traction. Numerous high power consumption modules, such as the CPU, Java coprocessor, EEPROM, and other security algorithm coprocessors, included on the device in this application. The amount of power needed substantially greater than before. The structure's RF interface complies with ISO/IEC 14443-2[4]. Network analysis is used to simulate the system's attributes while treating the antenna and chip as one unit. Network analyzer[5]-[8] measurements were performed using a Reference PICC in accordance with ISO/IEC 10373-6.

Inductive connection between the reader coil and card is the foundation for High Frequency RFID cards' communication. By removing the physical connection between the spiral coil and chip on the card and replacing the chip with a module that comprises a small coil coupled to a chip, several strategies have been used to lower the production cost of the card and improve its durability against mechanical stress. The coil on the module, on the other hand, is too small to retain the same degree of performance as the traditional cards. Two planar coils indicated in [9]–[12] were the major components of the additional circuitry that was added to the card and designated as a booster in order to address the drawback.

To step down the battery supply to the voltage level needed to run various electronic and smart gadgets, dc-dc converters are used. In order to improve energy economy and lower power loss, integrated circuits, including various types of microprocessors, are now made to operate on 3 V or even lower voltage supplies. The supplied voltage is stepped down using a buck converter[13]–[15].

1.2 Motivation

Modern smart devices are increasingly utilizing NFC, a well-known contact-less communication technique. Since it uses relatively little power to operate, it is easily integrated into a variety of devices, including sensors and cellphones. Both magnetic stripe cards and EMV chip-based cards used with the contactless interfaces. The main driving force behind the adoption of contactless technologies is speed, that is particularly alluring for low-value transactions in busy retail settings. The contactless interface is used by issuers and service providers to encourage more card-based transactions and fast earn a return on investment. Retailers can service more customers in a given amount of time by offering quicker transactions. Hence, the project develops anticollision technique in NFC Reader IC for Type A and Type B for hazzle free communication.

1.3 Problem definition

Design, Development and Validation of NFC Reader IC for Type A and B in the RTL using Eclipse IDE. Also design and analyses of Buck-Boost converter in the contactless interface module to provide required voltage depending on the placement of card near the reader.

1.4 Objectives

The objectives of the project is as listed below:

- To design, develop and validate Contactless Interface module for NFC Reader IC utilizing Tortoise SVN, Tortoise Git, Segger JLinks, Eclipse IDE, and Cadence Simvision.
- To realize the activation, anticollision technique, deactivation sequence of the communication protocol for Type-A and Type-B of NFC.
- To design and simulation of Buck-Boost converter to provide required voltage depending on the placement of card near the reader.

1.5 Organization of the report

The complete report presents the review of work and concepts. This is organized in to following four chapters.

Chapter 1: Introduction briefs the introduction of the project, that includes the overview of the project, specific details, literature survey of the project that gives the cons of the project and motivation to take up the project, problem definition, and objectives and scope of the project. It also includes the organisation of the report.

Chapter 2: NFC Technology gives the basic knowledge of NFC system, different modes of NFC, underlying concepts of Contactless Interface mainly NFC Type A and Type B and Buck-Boost Converter theory.

Chapter 3: Methodology and Block diagram presents the methodology used in the execution of the Contactless interface module in the Reader IC using Buck-Boost Converter. It also consists of block diagram, that gives the step-by-step process in the implementation same.

Chapter 4: Specifications and Design involves design values of Buck-Boost Converter and also various tools, languages used to bring up the project.

Chapter 5:Implementation and Simulation provides the Contactless Interface module code flow and simulation details of Buck-Boost Converter.

Chapter 6: Results and Discussion discusses about the simulation result of NFC Type-A and Type-B transmission with NFC Reader IC and also the simulation results of the Buck-Boost Converter.

Chapter 7: Conclusion & Future Scope includes the overall conclusion drawn from the project and the future works that can be carried out.

1.6 Summary

This chapter briefs the introduction of the project, that includes the overview of the project, specific details, literature survey of the project that gives the cons of the project and motivation to take up the project, problem definition, and objectives and scope of the project. It also includes the organisation of the report.

CHAPTER 2

CONTACTLESS INTERFACE

This chapter describes the theory and underlying concepts of Contactless Interface, with the help of NFC technology.

2.1 NFC

NFC is based on inductive-coupling. NFC tasks using magnetic induction between two loop antennas found within each other's near field. NFC operates at 13.56 MHz and provides a data transmission rate of 106 kbit/s - 848 kbit/s within a distance of approximately 11 cm. NFC has two modes of operation mainly[3],

- Active mode: In Active mode of communication, both devices with NFC chip generates an electromagnetic field and exchange data.
- Passive mode: In Passive mode of communication, there is only one active device and the other uses that filed to exchange information

An overview of NFC domain is as shown in figure 2.1

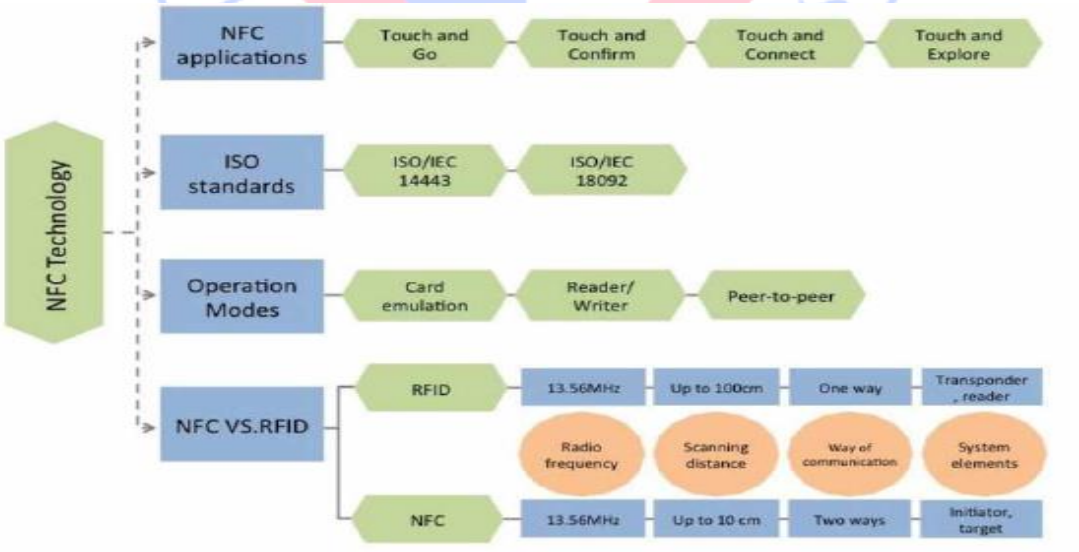

Figure 2.1: NFC Technology

ISO ensures that product or services are safe. Two important ISO certifications of NFC certifications ISO/IEC 18092 and ISO/IEC 14443. The first one defines communication modes for Near Field Communication Interface and Protocol. And second one is for identification of cards or objects for international interchange.

2.2 NFC operation modes

There are three operating modes, reader/writer, peer-to-peer, and card emulation.

2.2.1 Reader/Writer Mode

The NFC gadget serves as a reader for NFC tags, which includes RFID tags and contactless smart cards. By using the collision evasion mechanism, it quickly locates a tag that is nearby. Using read/write mode actions, an application running on an NFC device can read data from and write to the identified tag[2]. In the reader/writer mode, an NFC-enabled mobile phone communicates with an NFC tag with the goal of either reading or writing data to those tags. It distinguishes between two modes: writer mode and reader mode. As seen in figure 2.2, it internally distinguishes between two modes that is, reader mode and writer mode.

Reader/Writer Mode Applications:

i) Poster clever Advertising materials or posters containing NFC tags are referred to as "smart posters"[2]. These tags could include several forms of information, such a URL address, a couponing service, an SMS service, etc. The reader/writer mode is most frequently used for smart posters[2].

ii) Remote marketing

iii) Online shopping

iv) Mobile social such as social networking, location based services and inverter.

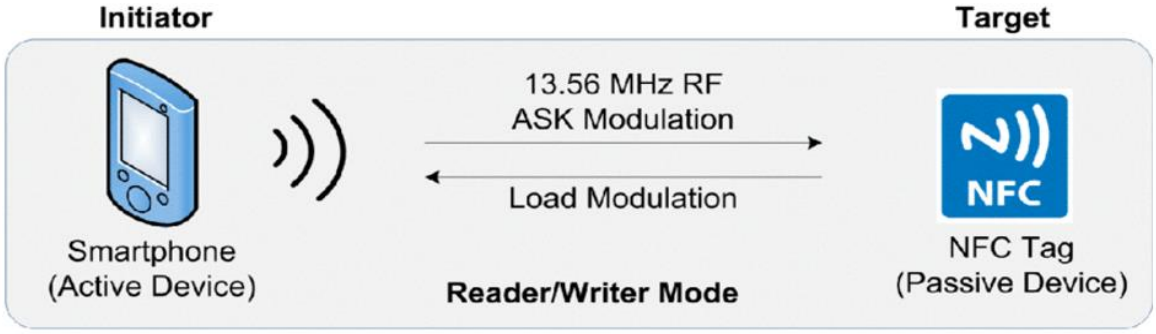

Figure 2.2: Reader/Writer Mode

2.2.2 Peer To Peer Mode

Peer-to-peer mode allows two NFC-enabled mobile devices to share data of any kind, including text messages. There are two standardized solutions for peer-to-peer: LLCP and NFCIP-1. The initiator target paradigm, in which the initiator and the target devices are described before the communication starts, is surpassed by NFCIP-1. However, the devices used for LLCP communication are the same. After the initial handshake, the application executing in the application layer makes the decision[2]. Both devices must be in active mode through peer-to-peer connectivity in order to power the integrated mobile phones, as indicated in figure 2.3. Data are dispatched over a bidirectional half duplex channel, where one device will transmitting, another will listen and it starts transmit data back once the first finishes.

Peer To Peer Mode Applications:

i) Data Exchange A mobile device may securely store sensitive data, and peer-to-peer mode is used to exchange it with other authorised users[3]. Users will feel comfortable using NFC technology to share sensitive information because the transmission takes place over a small distance. Additional security measures must be offered as well as higher levels of security needs are established[3].

ii) Transfer of Funds On NFC mobile devices, two users can transfer money between wallets. Gifts, discounts, and tickets can all be used as exchangeable items[3].

iii) Social Networking: Peer-to-peer mode has produced fewer apps than other operating modes up to this point. Peer-to-peer mode is typically used for file transfers, networking, and device pairing. The mode might be used, for example, to pair Bluetooth devices, trade business cards, or meet new people online. Peer-to-peer mode makes it simple for two devices to exchange data. Secure data exchange between two NFC-compatible devices is possible thanks to the ease of data transfer. Data may be transferred between NFC devices in a matter of centimetres, making the exchange of sensitive information a potential future use for this technology[3]. NFC phones gain quality functionality from the peer-to-peer mode. When brought into close proximity in this mode, two NFC phones can exchange data. By moving NFC-capable phones close to one another, for instance, two business partners can exchange virtual business cards. NFC connections are frequently used to configure Bluetooth pairing or Wi-Fi configuration, that is a

connection handoff to other common technologies. The device may use Bluetooth or Wi-Fi connections after a successful setup[3].

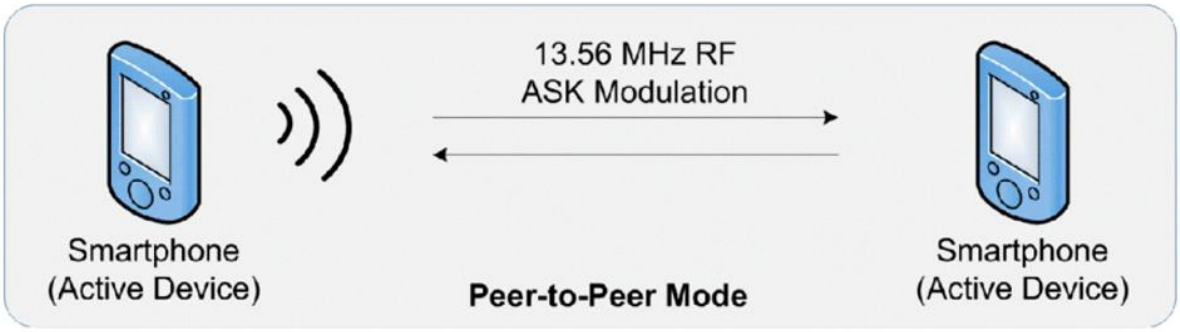

Figure 2.3: Peer-to-Peer Mode

2.2.3 Card Emulation Mode

Card emulation mode provides the opportunity for an NFC enabled mobile device to function as a contactless smart card as shown in the figure 2.4. The card emulation mode allows a mobile device with NFC to function as a contactless smart card. Numerous contactless smart card apps can be stored inside a smart card via mobile devices. Credit cards, loyalty cards, debit cards, transportation cards, and access cards are the best examples. The requirement to carry the cards is eliminated by card emulation mode. One might assume in the near future people may carry NFC-enabled phones to do daily tasks rather than to increase mobility. All tickets, credit cards, and other items could be integrated on mobile devices. There will therefore be plenty options in the future to incorporate commonplace items into NFC-enabled phones[3].

Card Emulation Mode Applications:

i) Payment NFC payment applications come in a variety of forms. The use of credit and debit cards, that is activated by NFC readers, is without a doubt the most significant payment application. There are additional ways to use NFC for payment, including storing and using gift cards and vouchers.

ii) At payment locations, loyalty points is earned. These points can then be redeemed for gifts or free shopping. Additionally, NFC readers utilising this operating mode can utilise coupons that have been downloaded using smart posters in reader/writer mode.

iii) There are numerous ways to implement use cases for ticketing. Users can save many ticket kinds, including those that have been downloaded using smart posters or another manner in the past, including theatre, bus, and aircraft tickets. Through card emulation

mode, these tickets can then be utilised at turnstiles or validation points. You can also save and utilise prepaid or monthly tickets cards.

iv) Users can keep access control objects in mobile devices thanks to access control use cases. Electronic keys for automobiles, buildings, safes, and hotel rooms are a few examples of these situations. An intriguing use case for OTA technology is hotel check-in, that enables the room key to be obtained before arriving at hotel and checking room. Therefore, in this situation, there is no necessity to linger at the reception after arriving.

v) Services for Identity Storing identity based particulars on mobile devices and allowing authorised personnel access to it is another intriguing application for this approach.

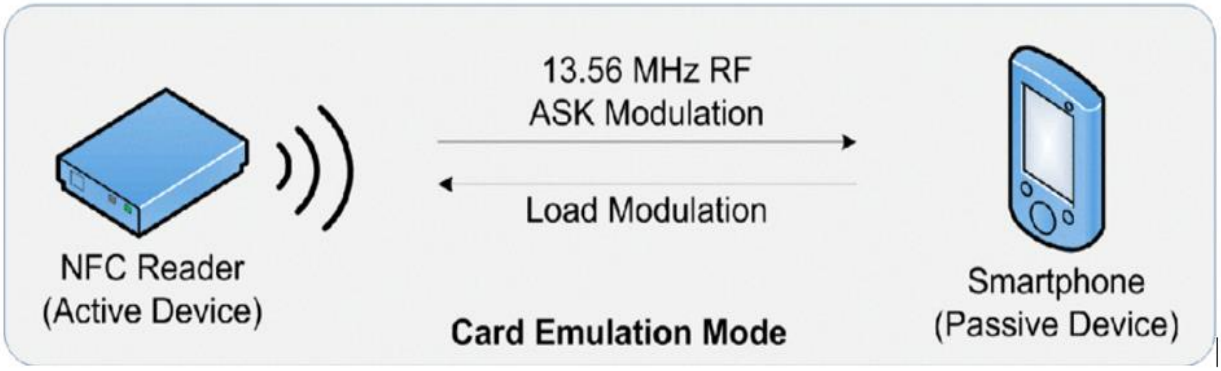

Figure 2.4: Card Emulation Mode

2.3 Working of NFC

NFC uses a frequency of 13.56MHz, it is contactless communication technology designed for data exchange between the devices by a simple tap. Passive mode NFC communication is used. Mainly three tasks are involved in establishing NFC communication.

- The necessary power required for communication is provided by the RF field of NFC reader, the tag/ card gets energized by inductive coupling.
- By modulating the RF field, reader can send information to tag/card.
- The reader receives information from tag/card by sensing load modulation of filed generated by tag/card

2.4 Contactless Interface

The phrase "contactless technology" is frequently used to refer to a group of technologies that were first created to aid with object identification. Access control, inventory management, data interchange, contactless point-of-sale payments, and toll collecting are just a few of the new uses that this technology has found.

2.4.1 NFC Type – A

NFC communication technology uses different coding for signalling and load modulation. Communication protocol used is compliant to the ISO/IEC 14443 Type A standard. Establishment of communication between reader and card involves the following steps.

- NFC uses the modulation principle of ASK 100% of the RF field.
- The subcarrier is modulated using OOK

2.4.1.1 Polling Cycle

- The reader sends frequent request commands, to detect the tag/card present in the operating field. The request command is REQA or WUPA
- The reader polls the card for every 5ms.
- The card present in the unmodulated RF field, accept request within 5ms. Then sends response to the reader.
- The card responds with ATQA (Answer to request Type A) command.

2.4.1.2 Type-A card states

The figure 2.5 specifies all possible state transitions.

Following are the states;

- Power off state:

  Card present in this state when it is not powered by the reader.

- Idle state:

  In this state, card is powered and listens for commands and on REQA and WUPA command enters next state

- Ready state:

  Once card enters this state bit frame anti-collision applied and cascade levels are handled to get UID of the card/tag. Then selects the card with SEL command there by enters active state.

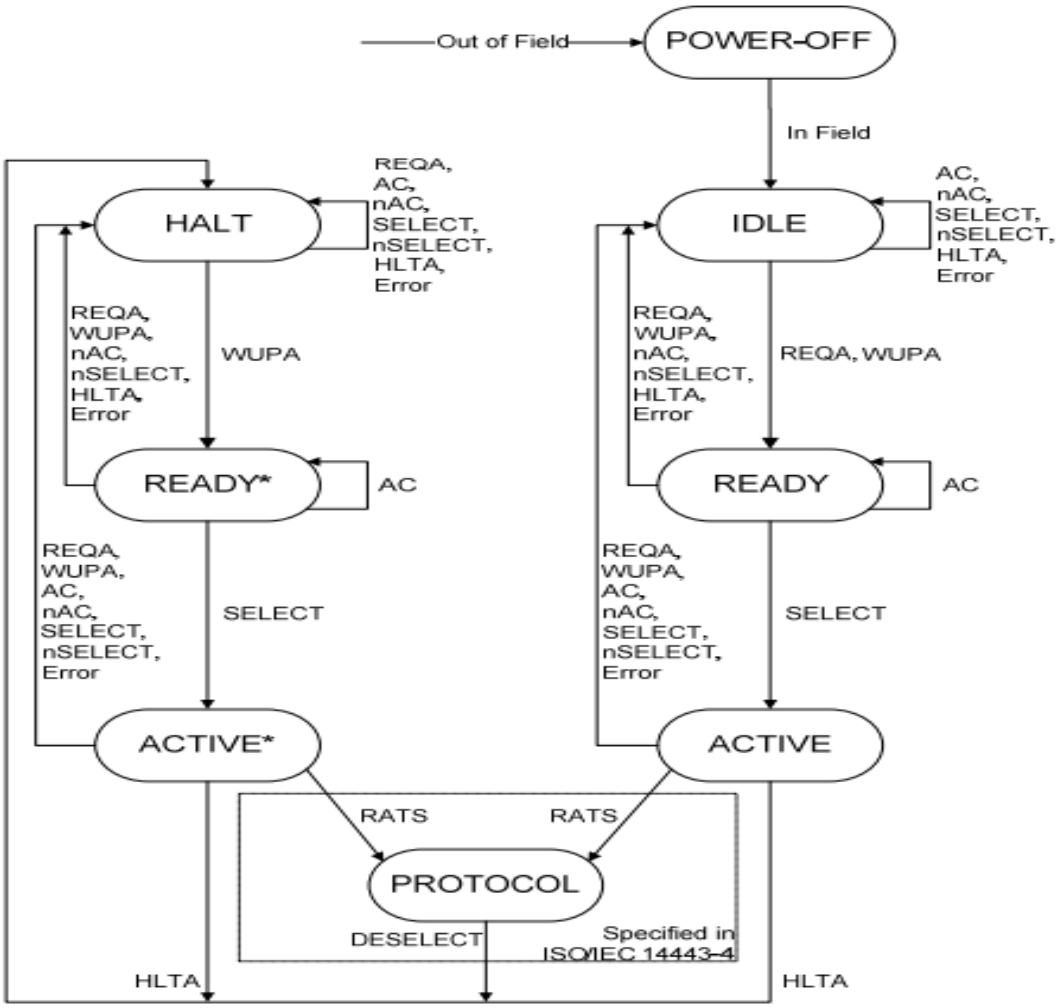

Figure 2.5: PICC Type A State Diagram

- Active state:

  The card compliant to ISO-IEC 14443-4 accepts the protocol activation commands, otherwise continues with non ISO-IEC 14443-4.

- Halt state:

  Cards enter the state on receiving HALT command. In this state card responds only to WUPA commands.

- READY* state:

  Similar to the READY state is the READY* state. The distinctions are shown in Figure 2.5 The anti-collision bit frame approach is used. Level cascades are managed inside a known UID.

- ACTIVE* state:

  The ACTIVE state and the ACTIVE* state are similar. The distinctions are listed in Figure 2.5. If the PICC complies to ISO/IEC 14443-4, it is prepared to take the RATS protocol activation command, which is defined in ISO/IEC 14443-4; otherwise, it may continue with a protocol that is not compliant with ISO/IEC 14443-4.

- PROTOCOL state:

  The PICC behaves in accordance with ISO/IEC 14443-4 in the PROTOCOL state.

The following symbols apply for the above state diagram:

AC	→ ANTICOLLISION command
nAC	→ ANTICOLLISION command
SELECT	→ SELECT command (matched UID)
nSELECT	→ SELECT command (not matched UID)
RATS	→ RATS command
DESELECT	→ DESELECT command
Error	→ transmission error detected or unexpected frame

2.4.1.3 Reader Mode: Multiple Card Resolution & Single Card Activation

Multiple card resolution also called as anti-collision resolution. The reader is designed to identify collision when at least two cards simultaneously transmits bit patterns that is shown in the figure 2.6.

Anti-collision loop consists following commands

- Select code command SEL that is of 1 byte, specifies cascade level.
- Number of valid bits that is of 1byte
- UID CLn of 0 to 40 bits according to value of number of valid bits.

Algorithm to anti-collision:

Step: 1

Reader allots select command SEL with code selected for anti-collision cascade level

Step: 2

Reader allots number of valid bits with value 20, this enables all cards present RF field which respond with a UID CLn.

Step: 3

Reader transmits the anti-collision command (NVB+ SEL).

Step: 4

Cards present in RF field responds with a complete UID CLn.

Step: 5

In case multiple card responds, a collision between cards occurs, if not directly goes to step 6 to 10

Step: 6

Reader identify the position first of collision.

Step: 7

Updating number of valid bits as NVB=20+coll

Step: 8

Reader transmits anti-collision command as SEL+NVB+CID CLn

Step: 9

Card that has part of UID CLn equal to valid bits which are transmitted by reader, transmit UID remaining bits.

Step: 10

In case further collision arises step6 to 9 is repeated and maximum number of loops as specified by ISO 14443 is 32.

Step: 11

If no further collision, reader allots NVB=70 that defines after collision selected cards complete UID is transmitted by reader.

Step: 12

Reader transmits SEL+NVB+UID CLn+CRCA

Step: 13

Card whose UID CLn matches responds with SAK (Select to acknowledge)

After selection of the card, reader activates the card by applying protocol setting.

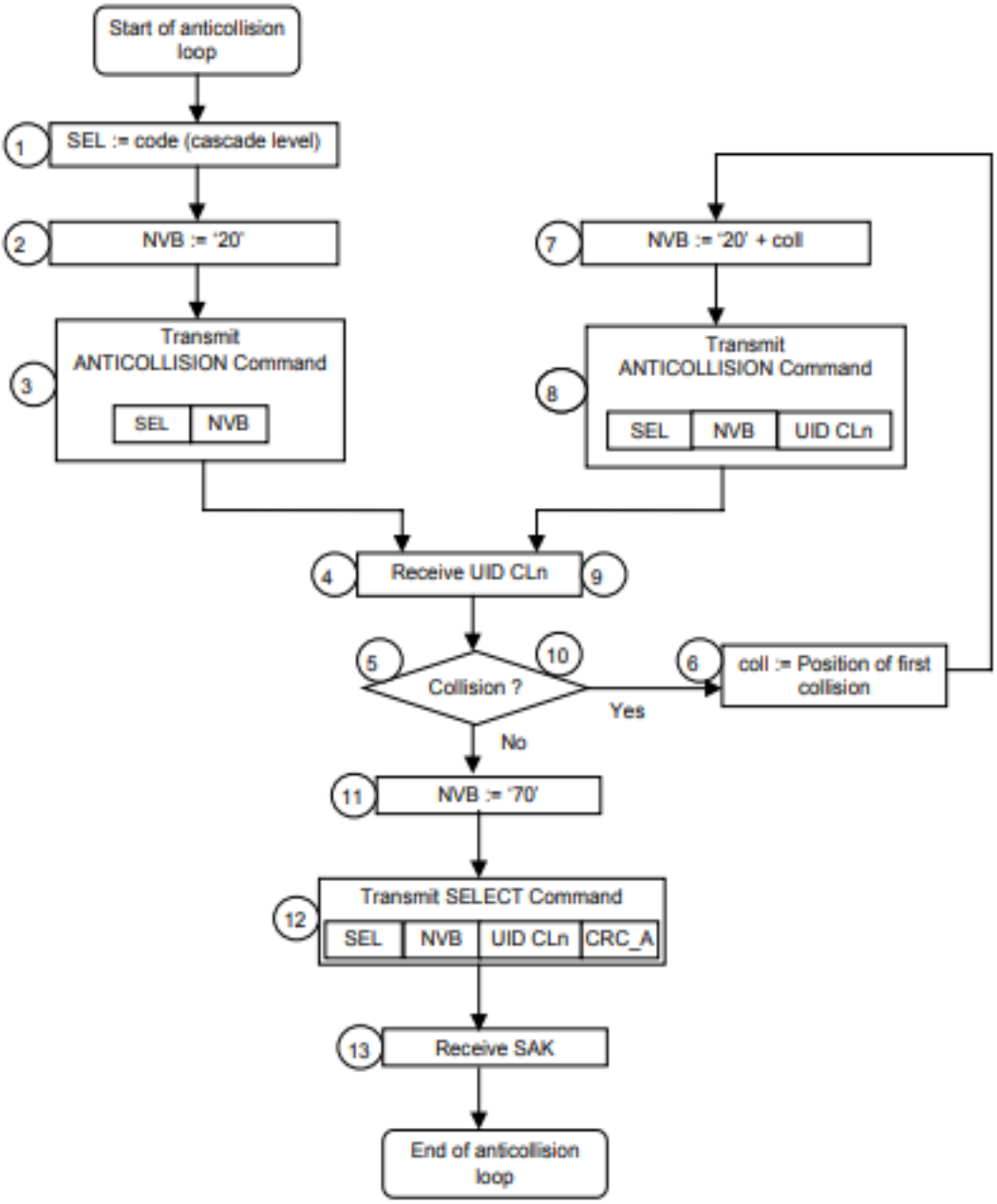

Figure 2.6: Anti-collision algorithm

2.4.2 NFC Type – B

NFC-B and RFID Type B communication are equivalent. Type B uses Manchester encoding as opposed to Miller encoding. Amplitude modulation is set at 10%, that means that the difference from 90% for low to 100% for high equals 10%.

2.4.2.1 Type-B card states

The figure 2.7 specifies all possible state transitions.

1. POWER OFF state:

The PICC is not powered by PCD operating field when it is in the POWER-OFF state.

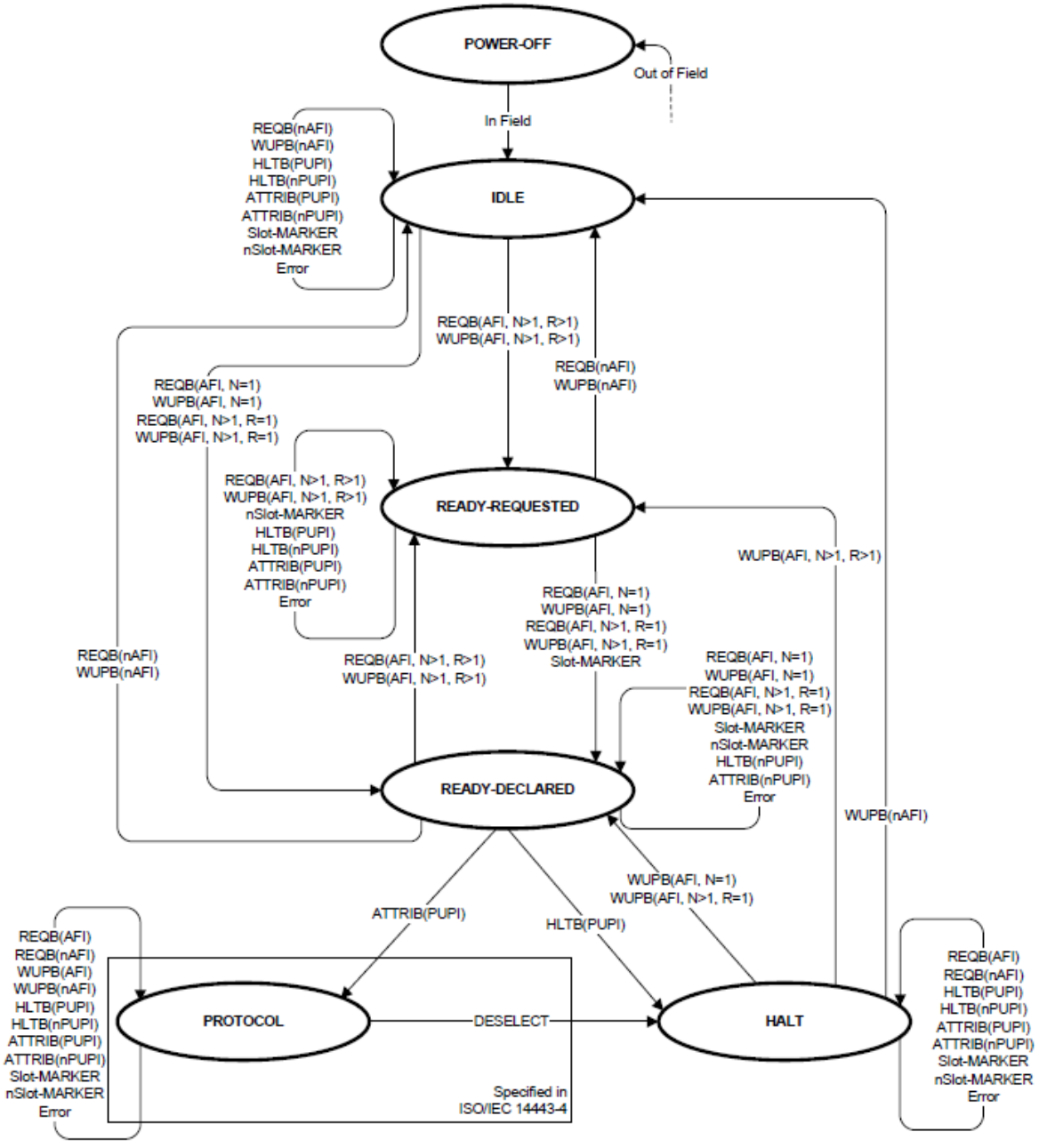

Figure 2.7: PICC Type B state diagram

AFI	→	matched AFI
nAFI	→	unmatched AFI
Slot-MARKER	→	Slot-MARKER command with matched slot number
nSlot-MARKER	→	Slot-MARKER command with unmatched slot number
HLTB(PUPI)	→	HLTB command with matched PUPI
HLTB(nPUPI)	→	HLTB command with unmatched PUPI
ATTRIB(PUPI)	→	ATTRIB command with matched PUPI
ATTRIB(nPUPI)	→	ATTRIB command with unmatched PUPI
Error	→	transmission error detected or unexpected frame

2. IDLE state:

The PICC is powered while in the IDLE state. It is able to distinguish REQB and WUPB commands while listening for frames.

3. READY REQUESTED sub-state:

The PICC powered up and in the READY-REQUESTED sub-state after receiving a valid WUPB or REQB command with the control parameter N. As stated in 7.6, the PICC possesses a random number R that is utilised to regulate its subsequent of operation. It listens for frames and must understand the commands REQB, WUPB, and Slot-MARKER.

4. READY DECLARED sub-state:

The PICC powered up and has transmitted its ATQB in response to last legitimate REQB/Slot-MARKER/WUPB instruction received while it is in the READY-DECLARED sub-state. It listens for frames and must understand the instructions REQB/WUPB, ATTRIB, and HLTB.

5. PROTOCOL state

The PICC powered up and has responded to the command ATTRIB in the PROTOCOL state. The PICC must operate in accordance with ISO/IEC 14443-4 if the 14443-4 protocol was chosen for it using the ATTRIB command; otherwise, it may proceed with a different protocol.

6. HALT state

The PICC is powered during the HALT state. It is able to detect WUPB commands and listen for frames.

2.5 Buck-Boost Converter

A DC to DC converter, the buck boost converter is depicted in figure 2.8. The DC to DC converter's output voltage is either less than or greater than the input voltage. The duty cycle affects the magnitude's output voltage. Because of the comparable step up and step down transformer, these converters are also referred to as step up and step down transformers. Step-up/step-down processes are used to increase or decrease the input voltages by a certain amount. The input power and output power are equivalent when employing the low conversion energy.

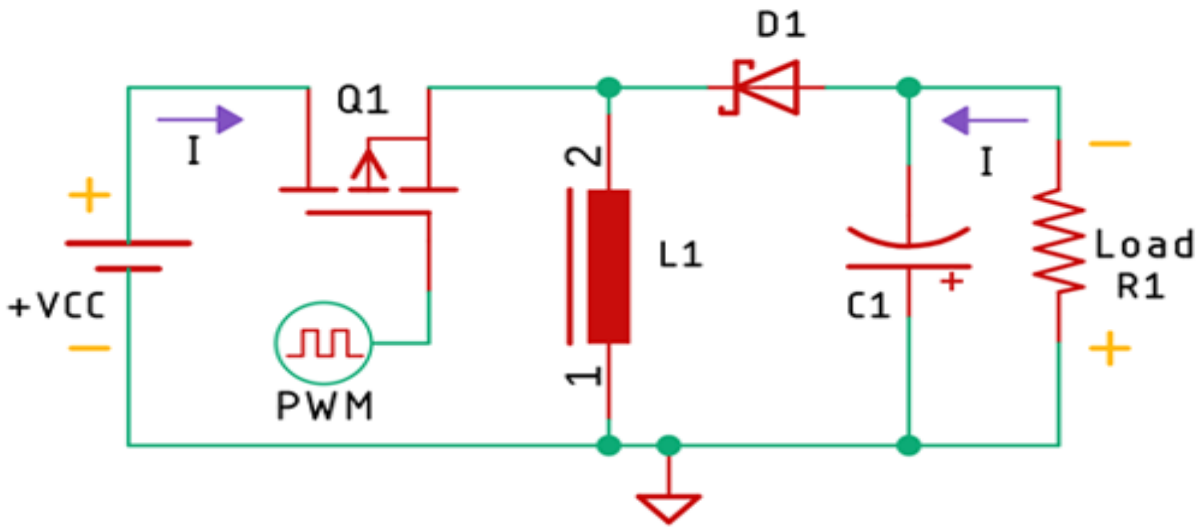

Figure 2.8: Buck-Boost Converter Circuit

The magnitude of the output voltage may be greater or less than that of the input voltage. The fly back circuit is equivalent to the buck boost converter, that substitutes a single inductor for the transformer. The buck boost converter has two different types of converters: the buck converter and the boost converter. These converters have an output voltage range that is greater than the input voltage[13].

2.6 Summary

This chapter gives the basic knowledge of NFC system, different modes of NFC, underlying concepts of Contactless Interface mainly NFC Type A and Type B and Buck-Boost Converter theory.

CHAPTER 3

METHODOLOGY AND BLOCK DIAGRAM

This chapter describes the methodology and block diagram in detail for contactless interface using NFC Reader IC.

3.1 Methodology

NFC Reader IC will make use of roughly 5V to 7V to power up. In particular CLIF module will make use of 1.5V to 5.7V. When card is placed at the nearest possible, CLIF module will use 1.5V and at the maximum distance 5.7V is being used. To get the desired Voltage requirement Buck-Boost converter is incorporated. A brief methodology is shown in the figure 3.1

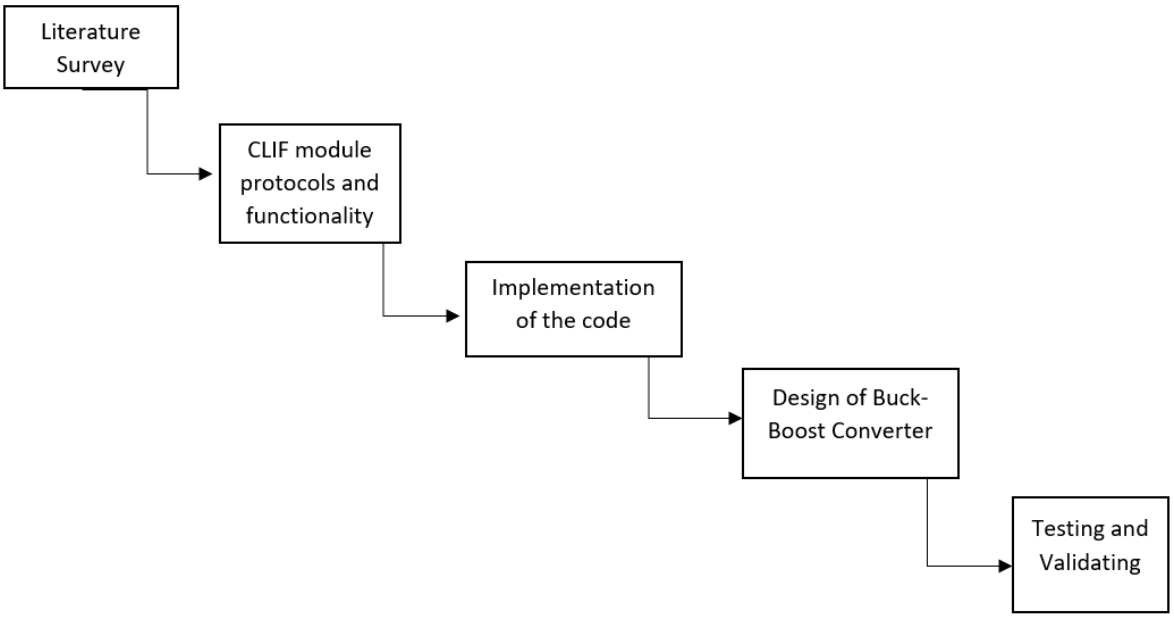

Figure 3.1: Methodology

To ensure that the NFC Type-A and Type-B Contactless Interface unit working properly without any flaws, it is necessary to validate the functionality with the help of Varieties of test scenarios. The test cases are developed on Eclipse IDE platform. The functionality of the CLIF NFC unit is substantiated by the Resister Transfer Level simulation tool provided by Cadence.

Following are the steps of CLIF module validating:

- Open the Eclipse IDE
- Import the project
- Select the appropriate build targets
- Open WinSCP and select particular files
- Trigger the RTL in Cadence

3.2 Block Diagram

NFC works using Polling device and Listening device. Reader/Write mode is used in the project. NFC Reader IC acts as a Polling device and cards acts as a Listening device. Polling device is also called as proximity coupling device and listening device is also called as proximity card or object[7]. Transfer of data packets happens between PCD and PICC that is shown in the figure 3.2.

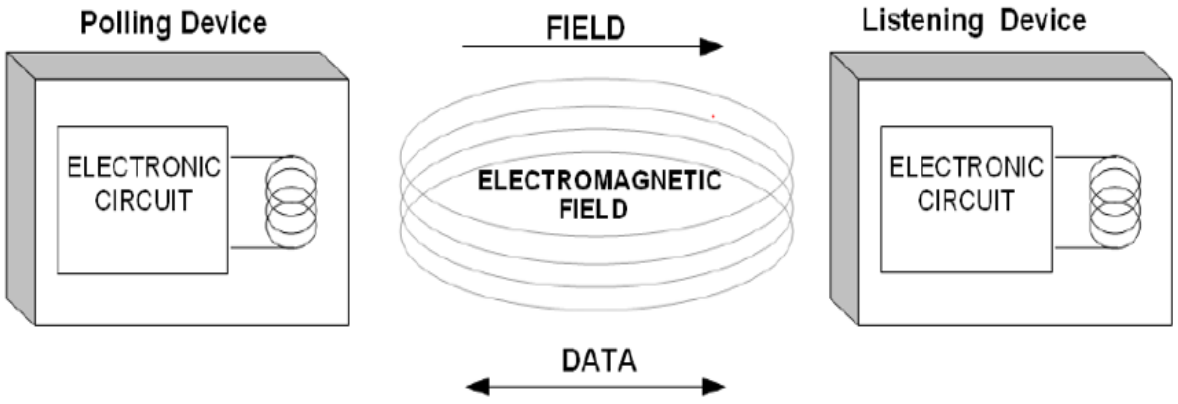

Figure 3.2: NFC Overview

The Dc Input to the NFC Reader IC can vary from 5V to 7V. Based on the input, converter is chosen either to go through step down of voltage or step up of voltage. Contactless Interface module will detail about Transmission protocols and functionality. Overall Block Diagram is shown in the figure 3.3.

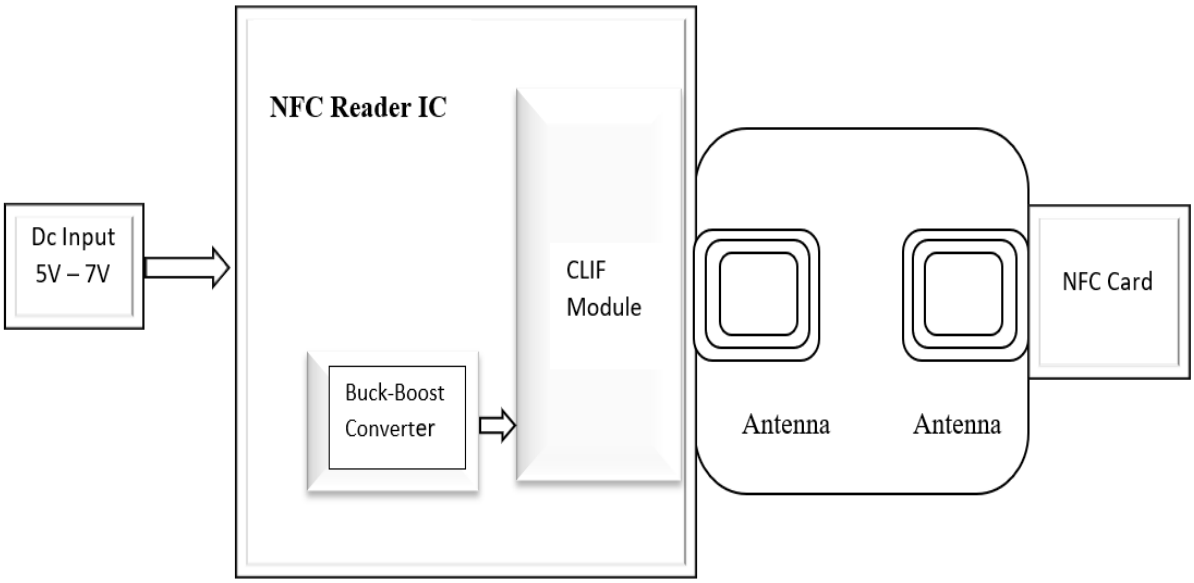

Figure 3.3: Block Diagram

Input DC voltage is provided to the NFC Reader IC. Buck-Boost gives required voltage to the Contactless module based on the Card placement near Reader IC. Card is placed in a proximity distance to the Reader. Internally magnetic Induction takes place between two antennas. Contactless Interface is compatible to the NFC Type-A and Type-B cards with all the transition states and activation sequence and anticollision techniques.

3.3 Summary

This chapter presents the methodology used in the execution of the Contactless interface module in the Reader IC using Buck-Boost Converter. It also consists of block diagram, that gives the step-by-step process in the implementation same.

CHAPTER 4

SPECIFICATIONS AND DESIGN

The chapter deals with the design and various tools that will provide efficient result.

4.1 Design of Buck-Boost Converter

Buck-Boost Converter is designed using the below shown table 4.1

Table 4.1: Specification for Buck-Boost Converter

Sl.no	Parameter	Value
1	Supply Voltage	5V
2	Output Voltage	1.5V
3	Switching Frequency	100KHz
4	Output Current	1.5A

The Duty Cycle is calculated using Equation (4.1)

$$\frac{V_{out}}{V_{in}} = \frac{D}{1-D} \quad \text{.....(4.1)}$$

$$\frac{1.5}{5} = \frac{D}{1-D}$$

$$D = 23\%$$

Determining Inductor value(L) using Equation (4.2)

$$L = \frac{V_S D}{f \Delta i_L} \quad \text{.....(4.2)}$$

$$= 3.45\text{uH}$$

Determining Capacitor value(C) using Equation (4.3)

$$C = \frac{V_o D}{f \Delta V_o R} \quad \text{.....(4.3)}$$

$$= 34.5uF$$

Calculating Resistor value(R) using Equation (4.4)

$$R = \frac{V_o}{I_o} \quad \text{.....(4.4)}$$

$$= 1ohms$$

4.2 Tools Required

Following are the tools required to build the contactless Interface module and to validate.

4.2.1 Tortoise SVN

As shown in figure 4.1, TortoiseSVN is a Subversion client that is implemented as a Microsoft Windows shell extension to assist programmers in managing various versions of the source code for programmes. Under the terms of the GNU General Public License, it is free software.

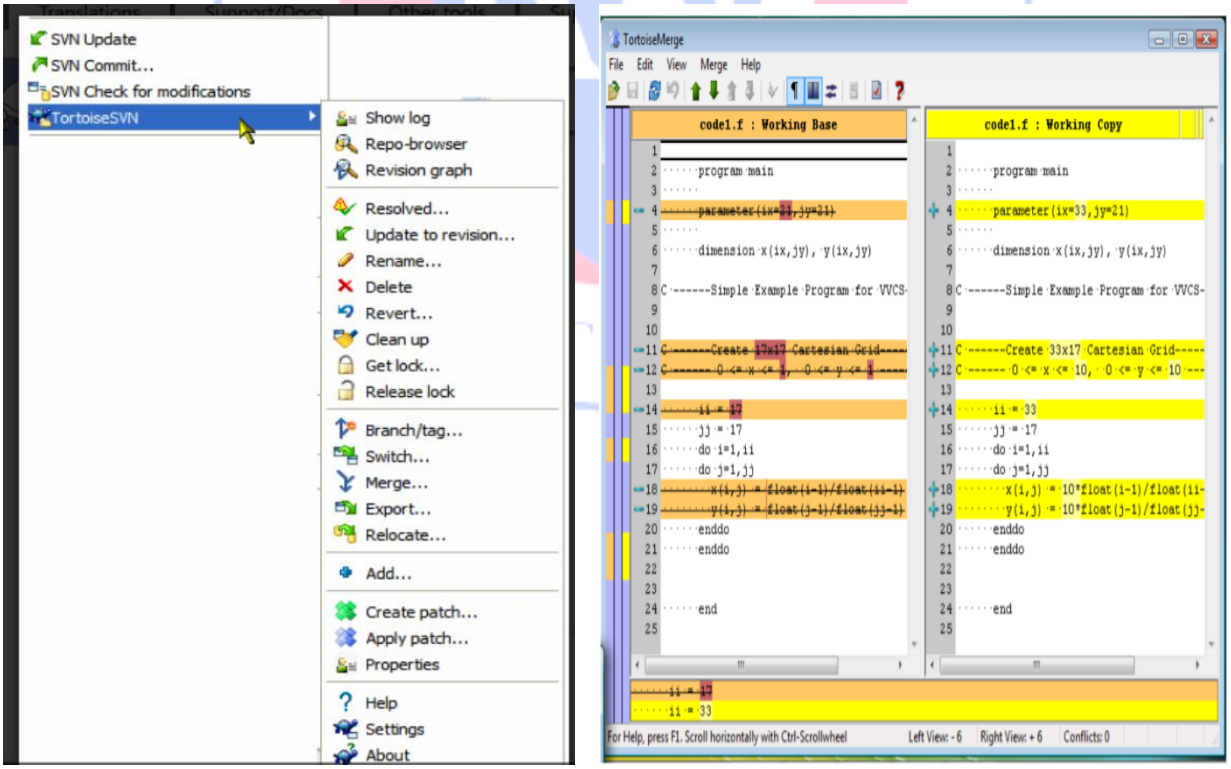

Figure 4.1: Tortoise SVN

4.2.2 Tortoise Git

Based on TortoiseSVN, TortoiseGit is a Windows Shell interface for Git. It is open source and may be completely built with the free software depicted in figure 4.2. TortoiseGit offers help through routine operations including committing, presenting logs, diffing two versions, establishing branches and tags, and writing patches.

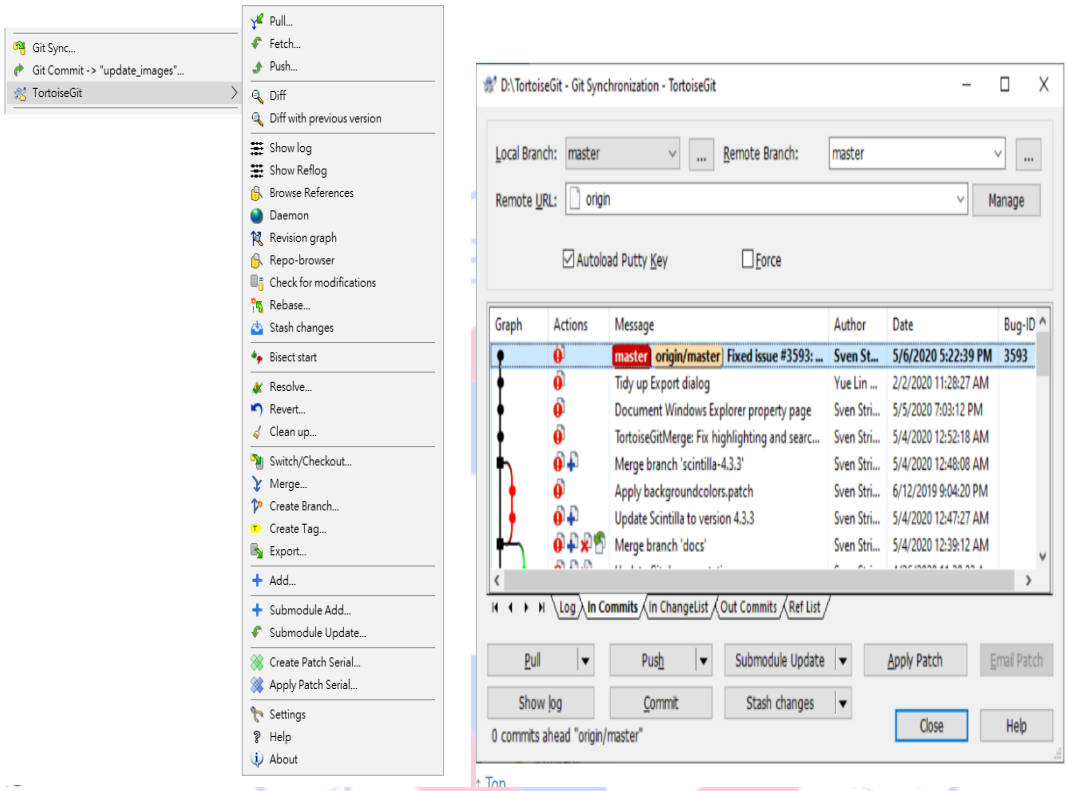

Figure 4.2: Tortoise Git

4.2.3 Eclipse IDE:

As seen in figure 4.3, the C/C++ Development Toolkit (CDT) is a group of Eclipse-based tools that enables users to develop, edit, explore, build, and debug projects that use the C and/or C++ programming languages. The CDT provides the frameworks that enable such tools to be integrated in a consistent manner, but it does not come with the compilers and debuggers required to translate C/C++ code into executable programmes and to debug such programmes. This enables you to combine and match such products based on the demands of your project.

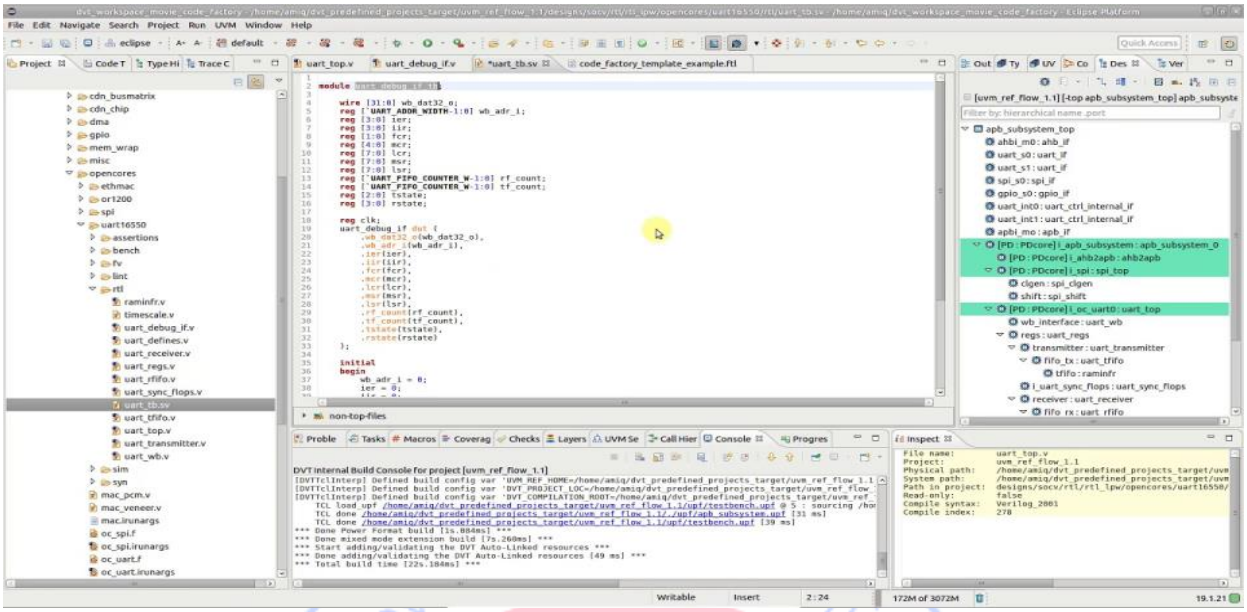

Figure 4.3: Eclipse IDE

4.2.4 Cadence Simvision

The most popular technique for confirming the accuracy of digital IC designs is RTL (Register Transfer Level) simulation. RTL simulation is very time-consuming when modelling a big IC design with complex internal characteristics (such as CPU cores running embedded software), as seen in figure 4.4.

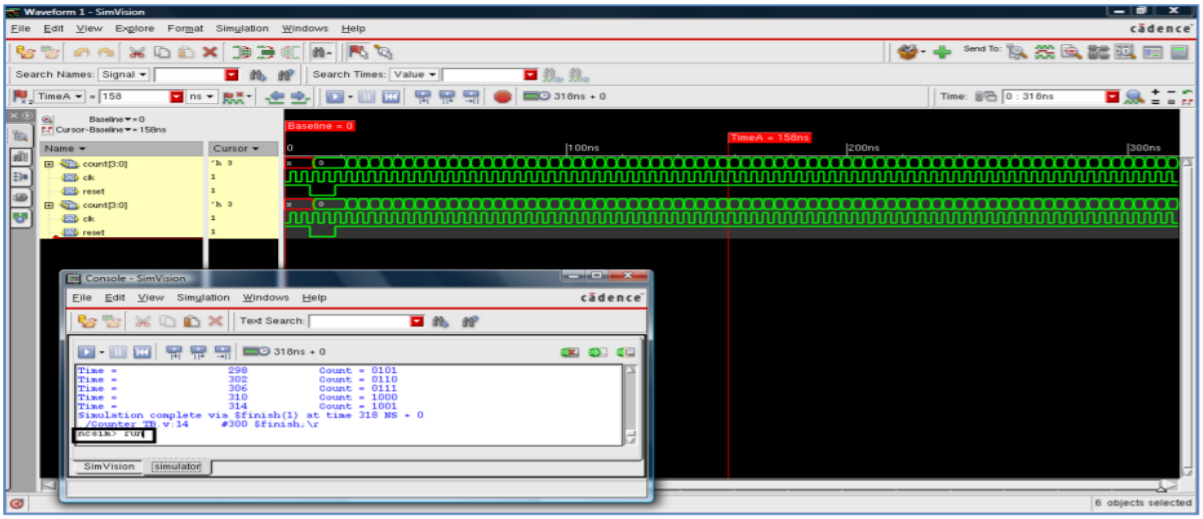

Figure 4.4: Cadence

4.3 Summary

This chapter involves design values of Buck-Boost Converter and also various tools, languages used to bring up the project.

CHAPTER 5

IMPLEMENTATION AND SIMULATION ANALYSIS

As discussed before Reader side is called as PCD and Card side is called as PICC. NFC Reader source code is implemented in the Eclipse IDE and built the required binaries. Card is being virtual here and tcl scripts acts as a Card. Communication of NFC Reader and Card is seen using Cadence Platform through RTL. Overview is shown in the figure 5.1

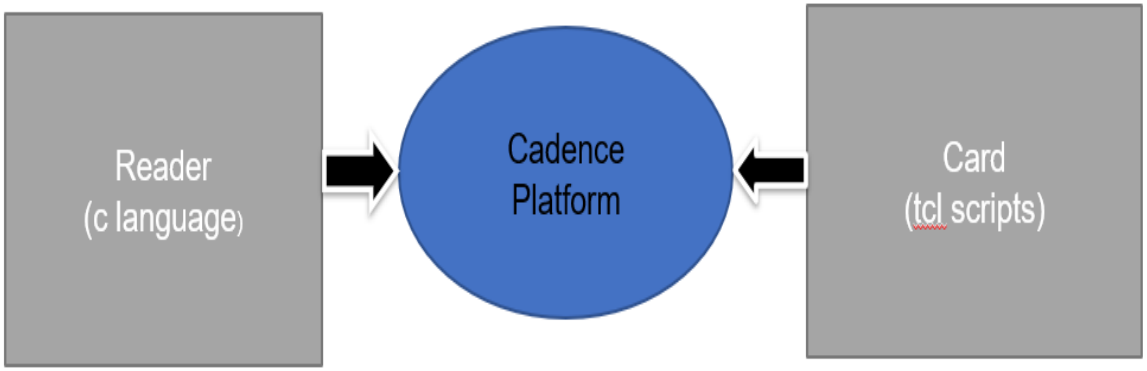

Figure 5.1: Transceiver language

5.1 Implementation

Code of NFC Reader is written in C language. In the Eclipse IDE platform, we have a flexibility in building particular module using appropriate build target. Therefore, once after the IC boots up, it does all the dependencies initialization followed by loading RF related parameter as shown in the figure 5.2. Later it checks for the card type and does all activation sequence and anticollision detection. Once both acknowledge each other data packets transfer takes place. Once the exchange of data packets done RF filed will go Off. Card responded through tcl scripts.

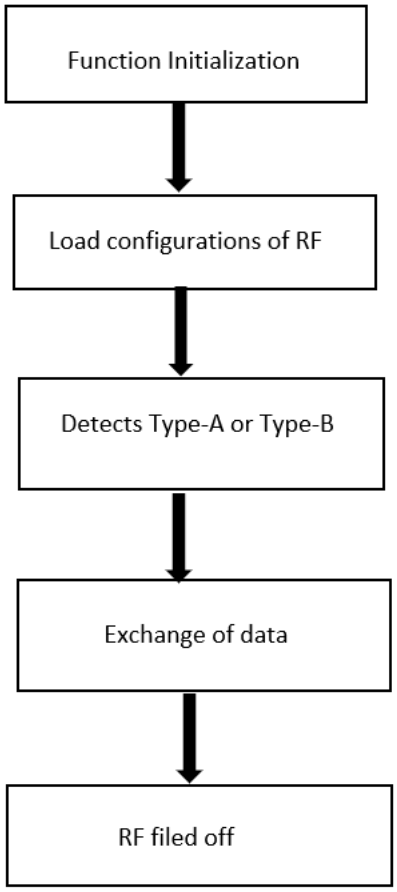

Figure 5.2: Flow Chart

Following are the steps of CLIF module validating:

- Open the Eclipse IDE
- Import the project
- Select the appropriate build targets
- Open WinSCP and select particular files
- Trigger the RTL in Cadence

5.2 Simulation of Buck-Boost Converter

Buck-Boost Converter is simulated in the PSIM software by defined parameters is shown in the figure 5.3. Inductor and Capacitor being storing elements. When the switch is closed Inductor stores the charge as long as the switch is closed. When switch opens it discharges to the load. For example if the duty cycle is 30%, duration of switch being closed is less than switch

being open, the charge stored in the inductor is less, therefore it results in stepping down the voltage. Similarly, if the duty cycle is 70%, duration of switch being closed is more than the switch being open, the charge stored in the inductor is more this time, therefor it results in stepping up the voltage.

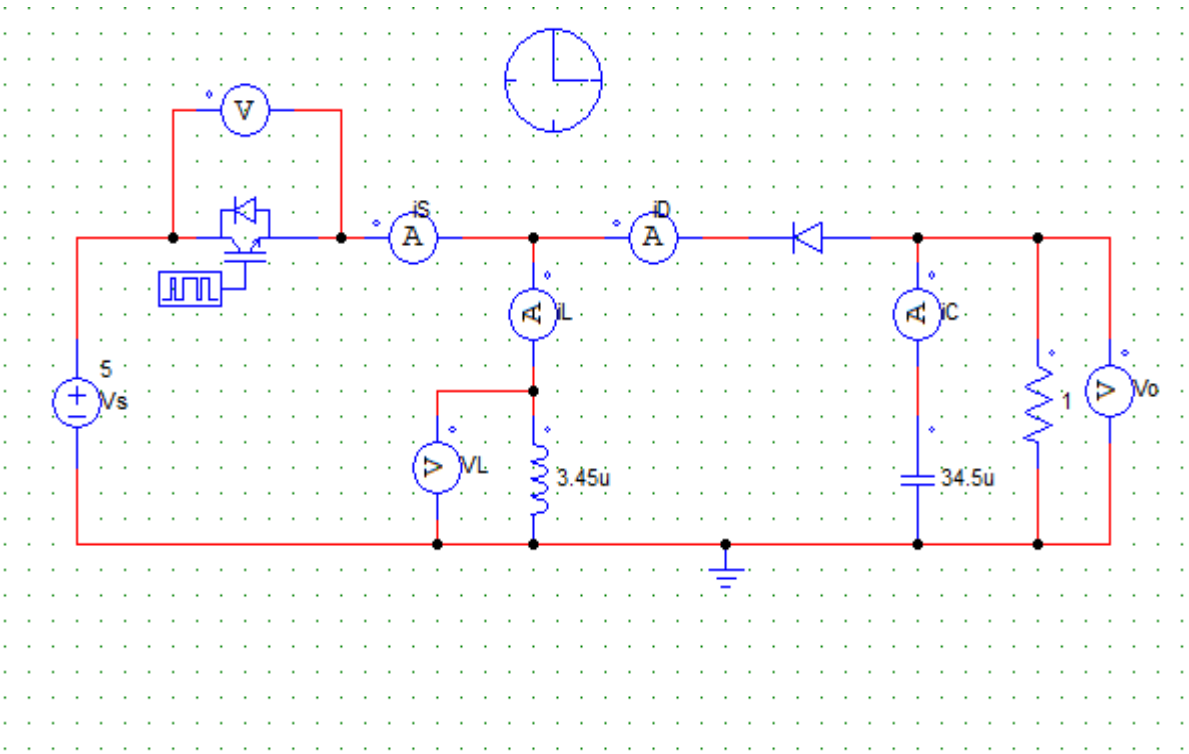

Figure 5.3: Buck-Boost converter simulation circuit

5.3 Summary

This Chapter provides the Contactless Interface module code flow and simulation details of Buck-Boost Converter.

CHAPTER 6

RESULTS AND DISCUSSIONS

This chapter briefly discusses about the simulation of Contactless Interface module between the NFC Reader IC and Type-A, Type-B cards. Also discusses the simulation results obtained in the PSIM software for Buck-Boost Converter.

6.1 NFC RF ON

NFC Reader IC once after the Boot up loads the application configurations. Here since the application is dependent on Radio Frequency, NFC Reader IC loads the RF configuration to start the communication within the proximity of cards. RF turns on after interrupt request toggles and RF will be kept continuously on until the exchange of data. RF will get turned off if the system goes to low power mode or any.

Figure 6.1: RF ON

6.2 NFC Type-A

NFC Type A Card and NFC Reader is compliant to ISO/IEC 14443 and has used Miller encoding. Command response between the NFC Reader IC and Type-A card is shown in the figure 6.2 and multiple data packets transfer is shown in figure 6.3

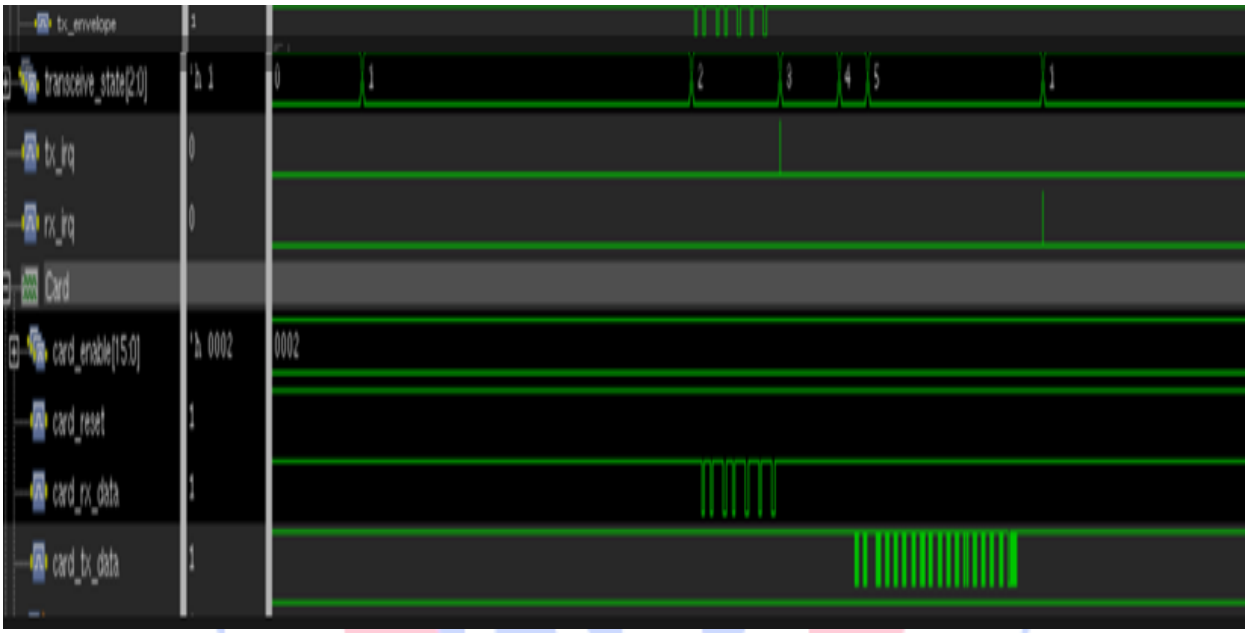

Figure 6.2: Type A single data packet

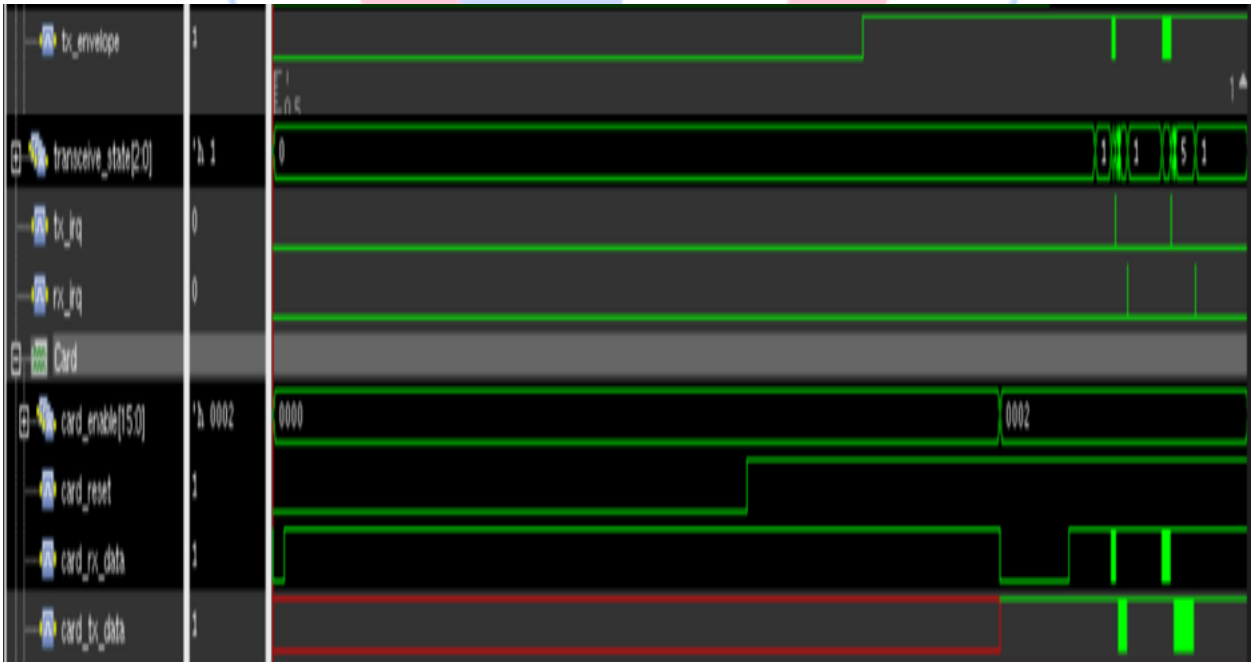

Figure 6.3: Type A multiple data packets

6.3 NFC Type-B

NFC Type B Card and NFC Reader is compliant to ISO/IEC 14443 and has used Manchester encoding. Command response between the NFC Reader IC and Type-B card is shown in the figure 6.4 and multiple data packets transfer is shown in figure 6.5

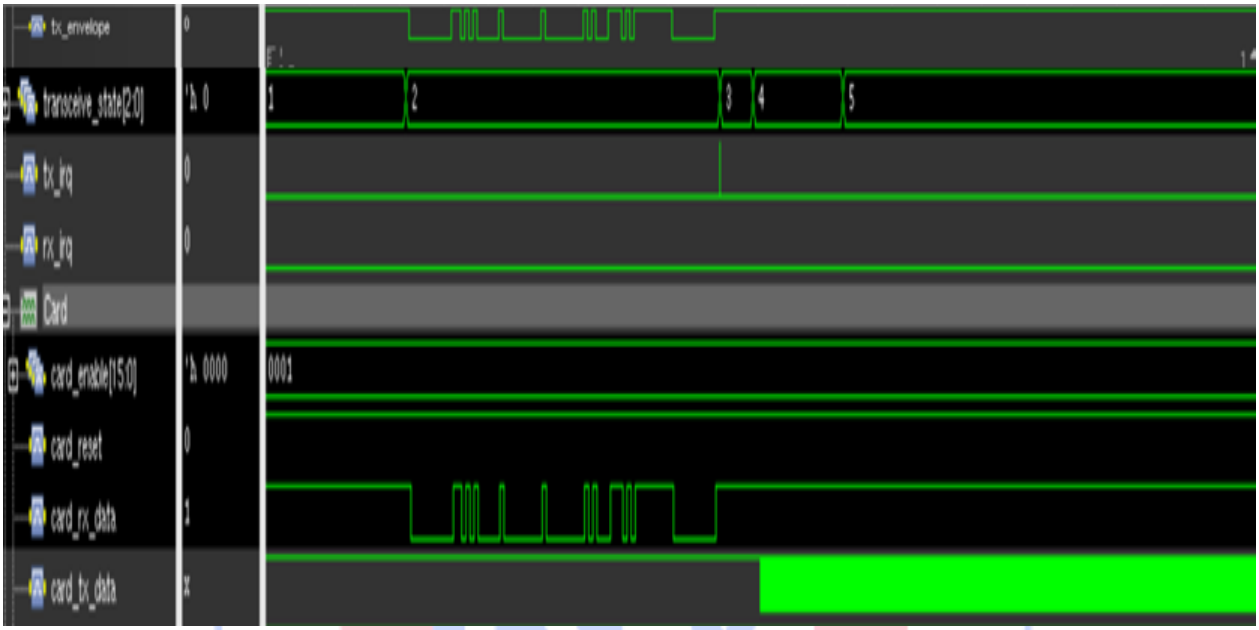

Figure 6.4: Type B single data packet

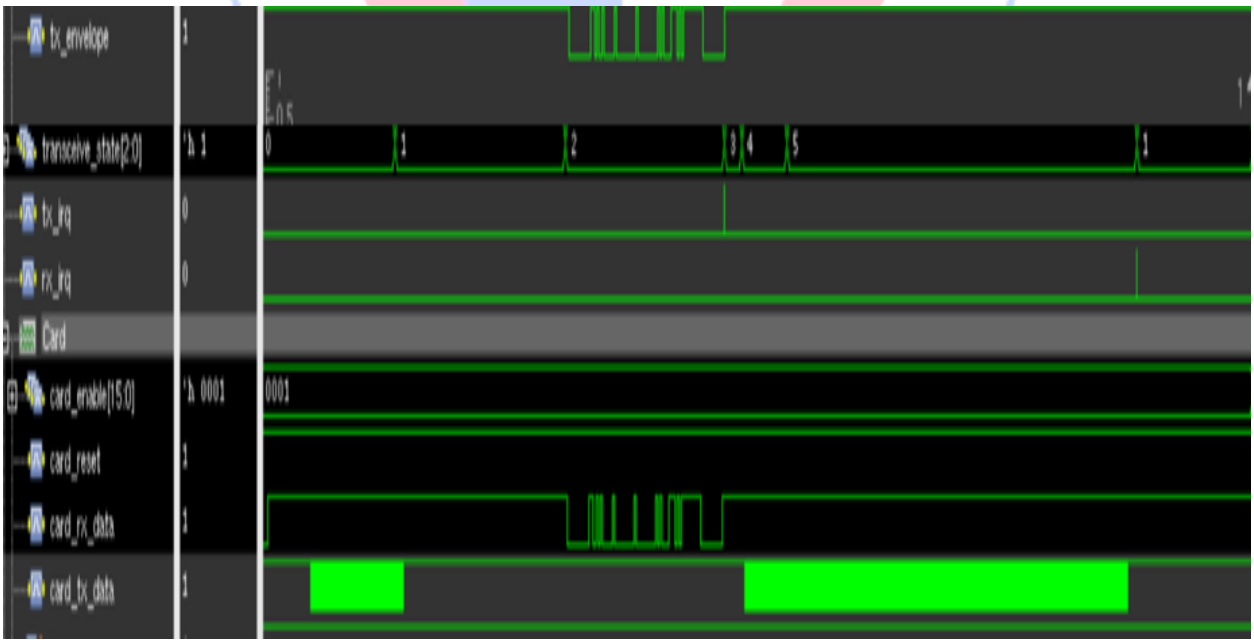

Figure 6.5: Type B multiple data packets

6.4 Buck-Boost Converter simulation result

The simulation circuit is discussed in Chapter 5, and the results are included in the following section.

The output voltage, inductor current, capacitor current, voltage across the switch, diode current are shown in the figure 6.6. Inductor helps in storing the charge during the switch is closed. The stored charge is discharged to the capacitor by making use of free wheeling diode to result in high voltage than given input voltage. Voltage across the switch reflects the switch being turned on and off time.

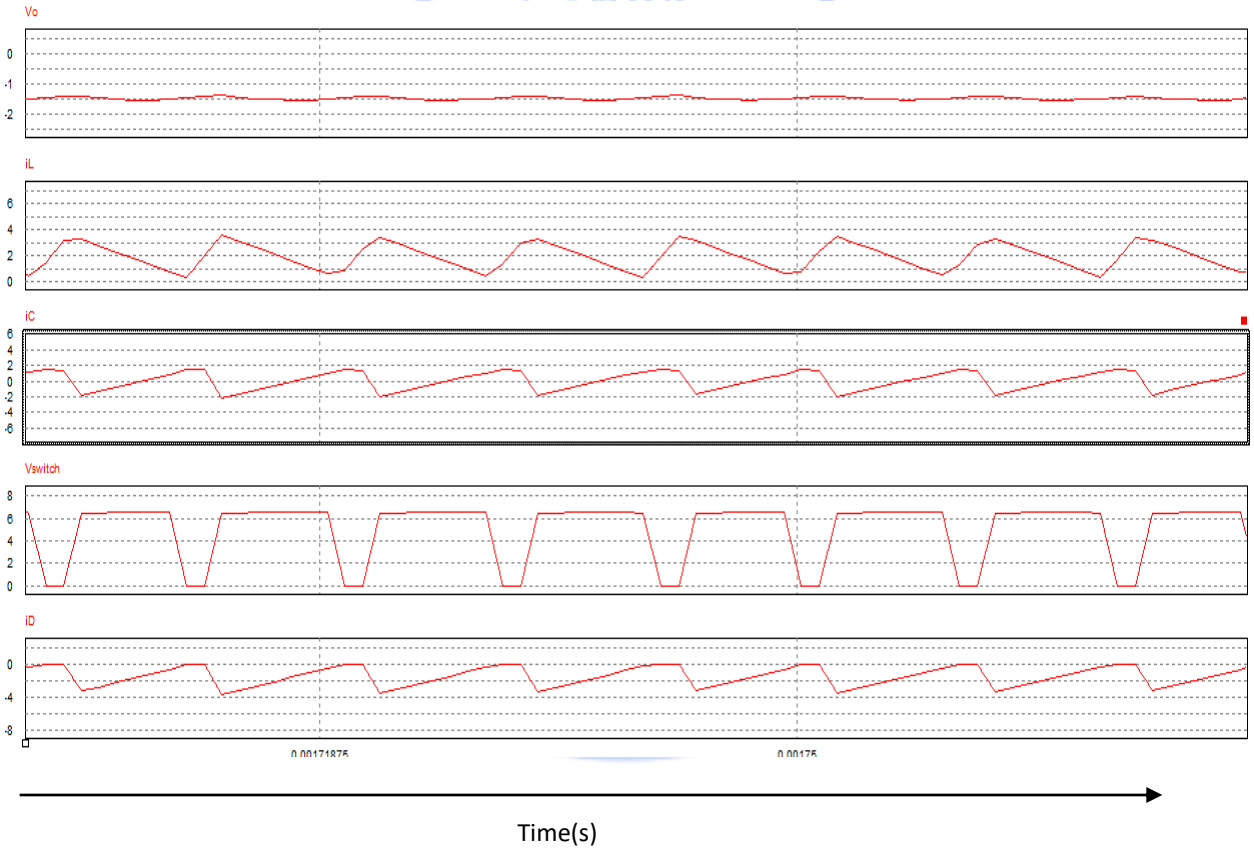

Figure 6.6: Vo, iL,iC,Vswitch,iD vs time

For the input of 5V, contactless interface module was expecting the output voltage of 1.5V since the card was placed right above the reader. The output voltage absorbed across the load is almost same as expected that is shown in the figure 6.7. Voltage required by the reader for the exchange of data when the card is just above the reader is very minimal.

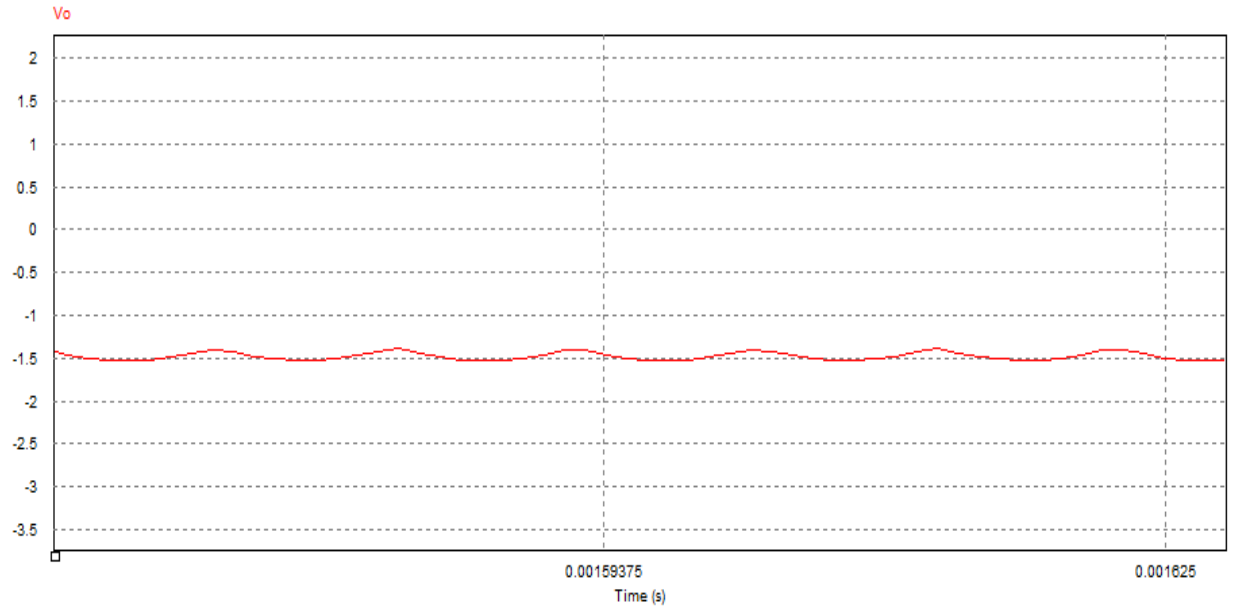

Figure 6.7: Output Voltage waveform

The current drawn by the reader to produce the active field is around 1.5A during the card is placed at the minimum distance to the reader. NFC Reader IC being active device, the card makes use of the filed produced by the reader to power up and transmits the data. The output current is almost equal to the 1.5A that is shown in the figure 6.8.

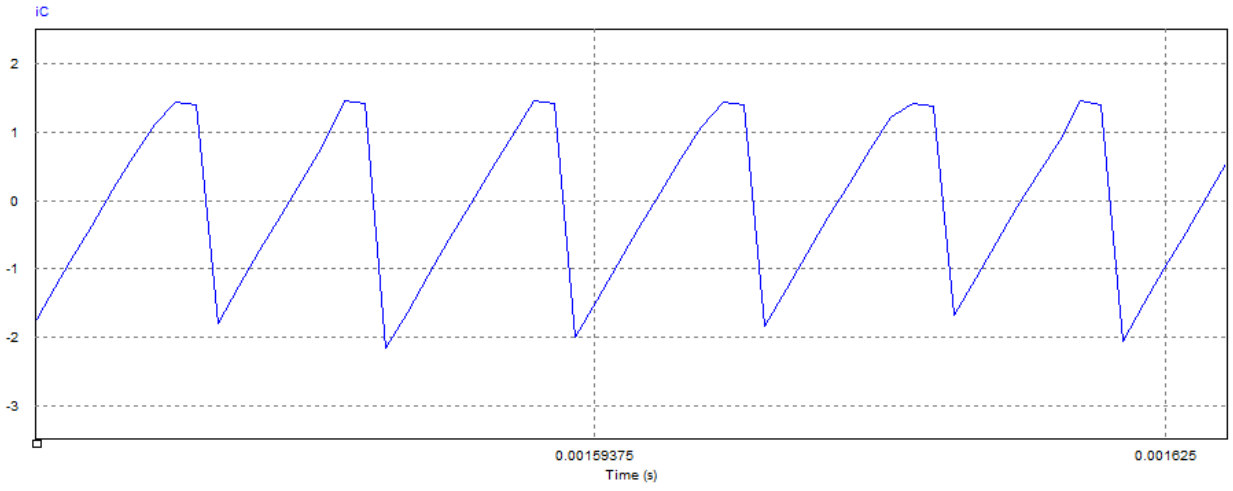

Figure 6.8: Output Current waveform

6.5 Summary

This chapter discusses about the simulation result of NFC Type-A and Type-B transmission with NFC Reader IC and also the simulation results of the Buck-Boost Converter.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

NFC is short-range wireless connectivity technology that has evolved from a combination of existing contactless identification and interconnection technologies, that works within a distance of 4cm approximately. NFC market is expected to grow from 18 billion USD (2020) to 34.9 billion USD by 2025. The main use cases of NFC are in mobile commerce and usage of wearable technology.

Applications in reader/writer mode can improve the user's mobility and reduce physical effort. Therefore, here in the project will detail about the Transmission protocols for the reader/write mode. NFC enables users to perform intuitive, safe, contactless transactions, access digital content and connect electronic devices simply by touching or bringing devices into close proximity.

7.1 Conclusion

- The development of an NFC system to operate in contactless interface was carried out using Eclipse IDE. Anticollision technique and selection procedure was incorporated in the source code of NFC Reader IC. A test framework to validate the functionality of the NFC Type-A and Type-B was developed in the Cadence platform.

- NFC Reader IC will make use of supply either 5V or 7V. Contactless Interface module requires supply from 1.5V to 5.7V depending the placement of card near reader. Therefore, Buck-Boost Converter was used to get that flexible supply. The simulation was carried out using PSIM software, expected output voltage was 1.5V and obtained output voltage was 1.4V

7.2 Future Scope

NFC Type A and B would allow all the users to make payments straightforwardly by tapping mobile phones with reader like debit card or credit card transactions. It can also be used in Numerous banks, mobile operators and companies.

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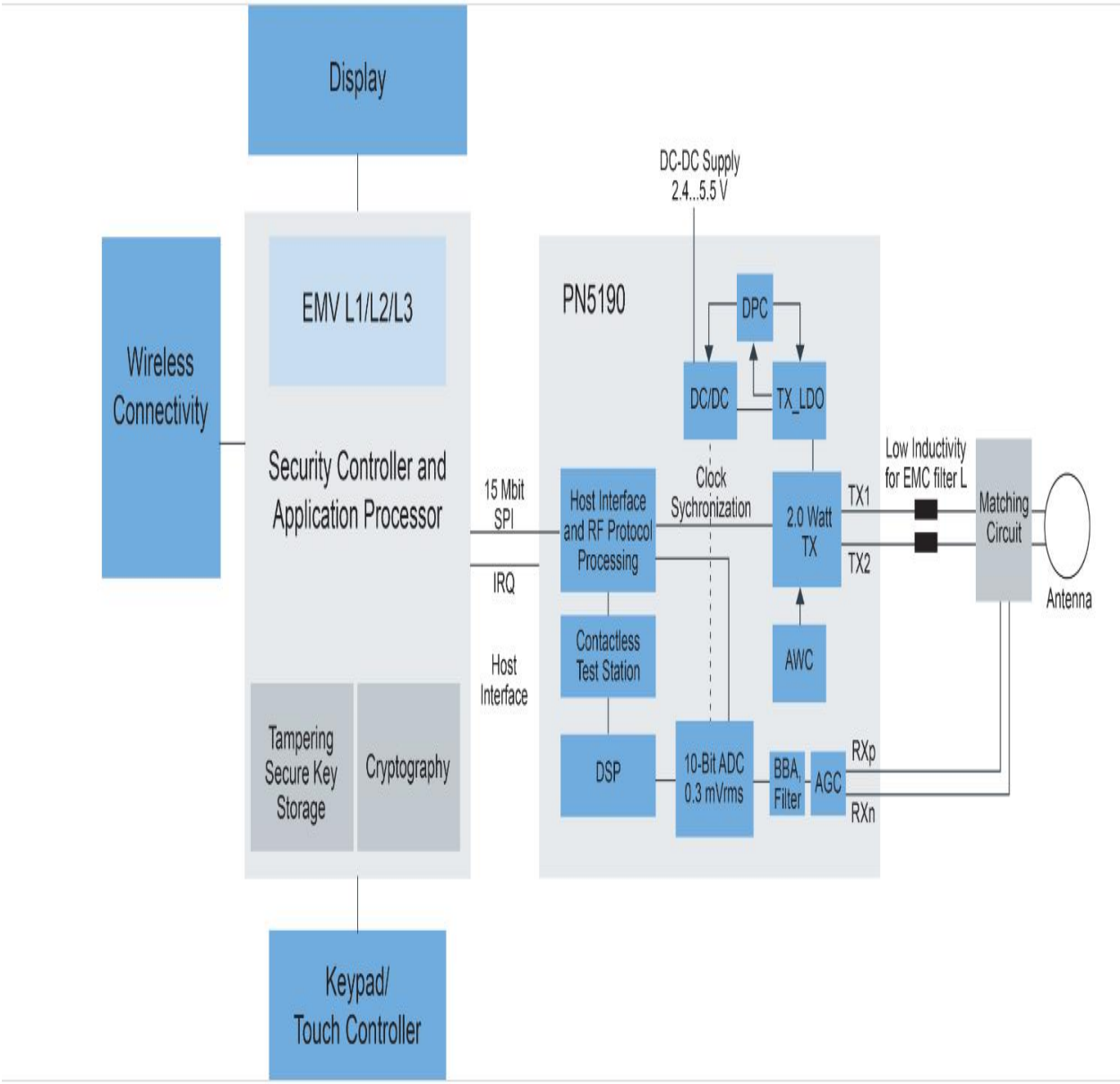
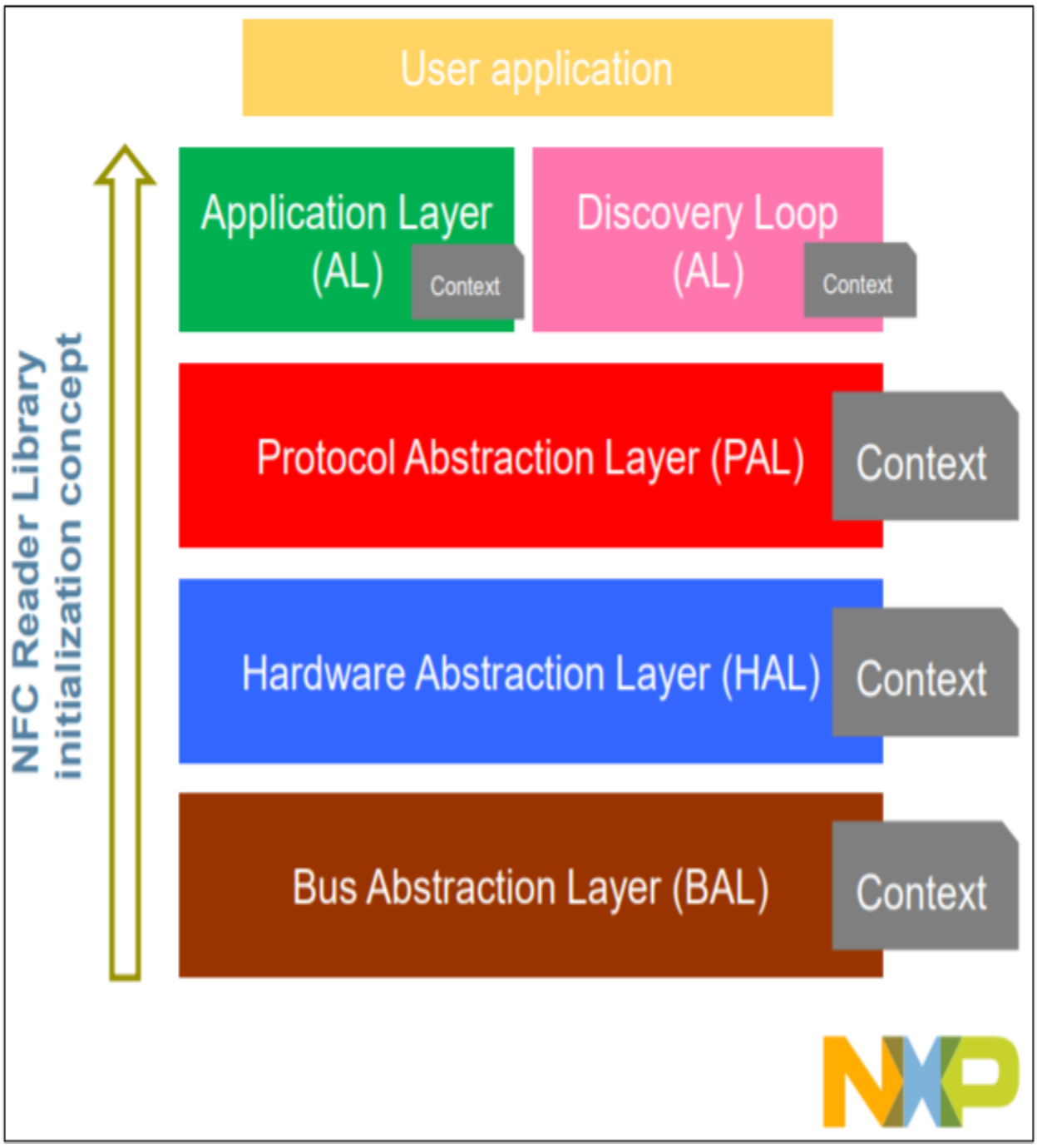
APPENDIX A

PN5190 System Block Diagram



Initialization of Reader Library



Modelling, Development and Validation of Contactless Interface for NFC Reader IC
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NXP Semiconductors
OBJECTIVE
Project Methodology
Methodology
NFC Technology
Buck-Boost Converter
Analysis of operation in CLIF module
Select Sequence
Anticollision Technique
Results and Discussion
RF ON
NFC Type-A
NFC Type-B
Output Current Waveform
Output voltage waveform
Conclusion
Future Scope
Buck Boost Converter would create flexible environment to the NFC technology.
Acknowledgement
Guide Information- Dr. S. G Srivani, Professor and Associate PG Dean, Dept of EEE, RVCE, e-mail- srivanisg@rvce.edu.in

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NFC Type-A Technology

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Abstract : Near Field Communication (NFC) is a minuscule wireless networking technology that ease making transactions, contact free payments, switching digital content, and connecting in a single tap to electronic devices. World has millions of contactless cards and readers, NFC is compatible with those all. NFC transmits data employing radio waves in the analogously as Bluetooth. NFC will make use of RFID (Radio-frequency identification) technology postulation that depend on electromagnetic induction to transport data. NFC operates at a frequency of 13.56 megahertz, with data transmission rates of 106, 212, or 424 kilobits per second. NFC Type A uses Miller encoding. NFC permits two way interactivity between electronic gadgets with additional security and intelligibility. Transmission protocol initialization and anticollision sequence have notable value in the Contactless Interface. The main motivation to take advantage of contactless solutions is the speed, which is on the whole appealing for low-value transactions in retail environments.

IndexTerms **– NFC, Anticollision.**

I. INTRODUCTION

NFC is a present day, minuscule wireless connectivity technology that grew from a combination of contactless identification and interconnection technologies. Sony and NXP Semiconductors (formerly Philips) jointly developed it. NFC is delineate to permit the exchange of various types of information, such as telephone numbers, MP3 files, pictures or digital authorizations between two NFC enabled devices like mobile phones, or between an NFC enabled mobile phone and compatible RFID (Radiofrequency identification) chip card or reader that are bear respectively. NFC is deliberated to be used as an access key to contents and services alike cashless payment and access control. NFC is grounded on inductive-coupling. NFC employs magnetic induction betwixt two loop antennas placed within each other's near field. NFC operates at 13.56 MHz and provides a data transmission rate of 106 kbit/s - 848 kbit/s within a distance of approximately 11 cm. NFC uses initiator and at the minimum one target device; the initiator diligently generates RF field that will power a passive target also called as a tag[1].

NFC is backward compatible with the Smart Card infrastructure based on ISO/IEC 14443 standard for proximity contactless smart cards as well as with the Sony FeliCa card standards. For the interchange of information betwixt two NFC devices, a new protocol evolved and defined in the ECMA-340 and ISO/IEC 18092 standards. NFC is extensively used across the globe for minuscule range communication with the application of low data rate. There are numerous modes, NFC compliant devices communicates. There are various types of NFC tags progressed for numerous applications as shown in the figure1.1. To communicate signaling protocol has to exits. The signaling protocol provides two devices to communicate and exchange information. There are three signaling modes in NFC referred as Type-A, Type-B and Type-F[3].

II. NFC - TECHNOLOGY

NFC is based on inductive-coupling. NFC tasks using magnetic induction between two loop antennas finded within each other's near field. NFC operates at 13.56 MHz and provides a data transmission rate of 106 kbit/s - 848 kbit/s within a distance of approximately 11 cm. NFC has two modes of operation mainly,

- Active mode: In Active mode of communication, both devices with NFC chip generates an electromagnetic field and exchange data.
- Passive mode: In Passive mode of communication, there is only one active device and the other uses that filed to exchange information.

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In addition to mode of operation, there are three communication modes in NFC:

1. Reader/Writer mode: The NFC device performs as a reader for NFC tags, that is to say contactless smart cards and RFID tags. It discovers out a tag right away in close proximity by making use of the collision evasion mechanism. An application on an NFC device can read data and write to the detected tag using the read/write mode operations[2]. The reader/writer mode is regarding the communication of an NFC enabled mobile phone with an NFC tag for the intention of either reading or writing data to those tags. It inter defines two different modes: reader mode and writer mode.

2. Peer to Peer mode: Peer-to-peer mode authorizes two NFC enabled mobile devices to exchange information like a text message, or any other kind of data. Peer to Peer has two standardized options; NFCIP-1 and LLCP. NFCIP-1 takes upper hand of the initiator target paradigm where initiator and the target devices are described prior to begin the communication. But, In LLCP communication the devices are identical. The decision are made by the application which is running in the application layer is after the initial handshake[2]. To power the embedded mobile phones, both devices should be in active mode through the communication in peer-to-peer mode. Datas are dispatched over a bidirectional half duplex channel, where one device will transmitting, the other one will listen and it starts to transmit data once the first finishes.

3. Card Emulation mode: Card emulation mode supplies the chance for NFC enabled mobile device to operate as a contactless smart card. Mobile devices can store various contactless smart card applications inside the smart card. The supreme examples are credit card, loyalty card, debit card, transport cards and access cards. Card emulation mode removes the need of carrying the cards. One can anticipate that in the near future people might carry NFC enabled phones not to gain mobility but to carry out daily functions. All credit cards, tickets, keys and so on will be possibly embedded on mobile phones. Therefore, there will be enough opportunities to integrate everyday objects into NFC enabled phones in the future.

III. NFC Type A

NFC communication technology uses distinct coding for signaling and load modulation. Communication protocol used is compliant to the ISO/IEC 14443 Type A standard. Configuration between Proximity Coupling Device(PCD) and Proximity Card or Object(PICC) is shown in the figure 1.

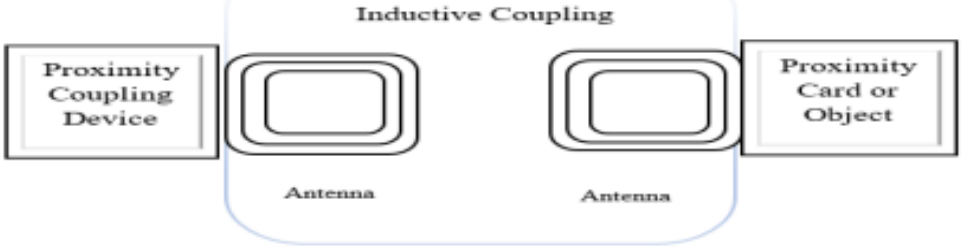

Fig.1 Proximity coupling device and proximity card or object configuration

Following are the Initial dialogue for proximity cards:

- activation of the PICC by the RF of the PCD
- the PICC will wait for a command from the PCD
- command transmission by the PCD
- command transmission by the PICC

The PCD will produce a high frequency magnetic field. This field inductively couples with PICC to transfer power and it is modulated to communication. The frequency of the RF will be 13.56 MHz ±7 kHz. The PCD modulates the amplitude of magnetic field with the modulation pulses to transmit data from the PCD to the PICC. PICC loads magnetic field with a modulated subcarrier signal in order to transmit data from the PICC to the PCD. NFC uses 100% ASK modulation principle to the RF field. Carrier frequency of 13.56MHz. Communication between PCD and PICC can be accomplished with four different bit rates. Bit rates of fc / 64, fc / 32 and fc / 16 are optional and might be independently reinforced by PCD and PICC in each direction communication[4].

PCD frame:

- start of PCD communication
- information
- error detection by the PCD
- end of communication of PCD

PICC frame:

- start of PICC communication
- information
- error detection by the PICC

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- end of communication of PICC

There should be minimum frame delay between PCD to PICC and PICC to PCD

The figure 2 specifies all possible state transitions.

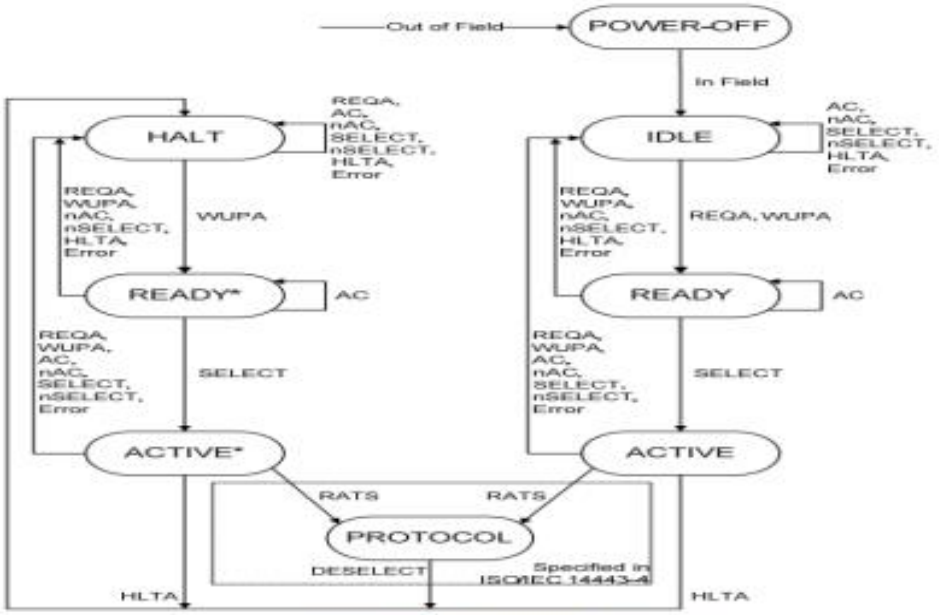

Fig.2 PICC State Diagram

The following symbols apply for the above state diagram:

AC	→ANTICOLLISION command (matched UID)
nAC	→ANTICOLLISION command (not matched UID)
SELECT	→SELECT command (matched UID)
nSELECT	→SELECT command (not matched UID)
RATS	→ RATS command
DESELECT	→DESELECT command
Error	→transmission error detected or unexpected frame

Following are the states;

1. POWER-OFF state:
   In the POWER-OFF state, the PICC is unpowered by operating field of PCD.

2. IDLE state:
   In the IDLE state, PICC is powered. PICC will listen to commands and it will recognize WUPA and REQA commands.

3. READY state:
   In the READY state, the bit frame of anticollision method is applied. Cascade levels are controlled inside READY state to get the entire UID.

4. ACTIVE state:
   If the PICC complies with ISO/IEC 14443-4 then the PICC should be get ready to accept the protocol activation command that is RATS which is specified in ISO/IEC 14443-4, otherwise it may continue with non ISO/IEC 14443-4 protocol.

5. HALT state:
   In the HALT state, PICC should respond only to WUPA command. The PICC set into the READY* state after it received a correct WUPA command and ATQA transmitted.

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6. READY* state:
The READY* is alike to the READY state. The differences are specified in Figure 2. The bit frame of anticollision method is applied. Cascade levels are handled inside to known UID.

7. ACTIVE* state:
The ACTIVE* is alike to the ACTIVE state. The differences are specified in Figure 2. If the PICC complies with ISO/IEC 14443-4 then the PICC should be ready to accept the protocol activation command that is RATS which is specified in ISO/IEC 14443-4, otherwise it may continue with non ISO/IEC 14443-4 protocol.

8. PROTOCOL state:
In the PROTOCOL state the PICC behaves according to the ISO/IEC 14443-4.

IV. ANTICOLLISION ALGORITHM

The following algorithm shall apply to the anticollision loop as shown in the figure 3:

Step 1:
The PCD should assign SEL to the code for the chosen anticollision level.

Step 2:
The PCD should assign NVB to the value of '20'. '20' defines that the PCD will transmit no devision of UID CL*n*. Therefore, this command forces PICCs in the region to respond with entire UID CL*n*.

Step 3:
The PCD should transmit SEL and NVB.

Step 4:
All PICCs in the region should respond with their entire UID CL*n*.

Step 5:
A collision will occur, if more than one PICC responds. Steps 6 to 10 should be skipped, if no collision.

Step 6:
The PCD should recognize the first collision position.

Step 7:
The PCD should assign NVB with a valid bits of UID CL*n*. The valid bits should be part of the UID CL*n* which was received before a collision followed by a (0)b or (1)b. A implementation adds (1)b.

Step 8:
The PCD should transmit NVB and SEL, followed by valid bits.

Step 9:
Only PICCs part of UID CL*n* is equal to the valid bits transmitted by the PCD. It should transmit their UID CL*n* remaining bits.

Step 10:
If additional collisions occur, steps 6 to 9 should be repeated. 32 is the maximum number of loops.

Step 11:
If no collision occurs further, the PCD should assign '70' to the NVB. This value tells that the PCD will transmit the entire UID CL*n*.

Step 12:
The PCD should transmit NVB and SEL, followed by UID CL*n* 40 bits followed by CRC_A.

Step 13:
The PICCs which UID CL*n* matches the 40 bits should respond with their SAK.

No need of performing the anticollision loop if the UID of a PICC is complete and known by the PCD[5].

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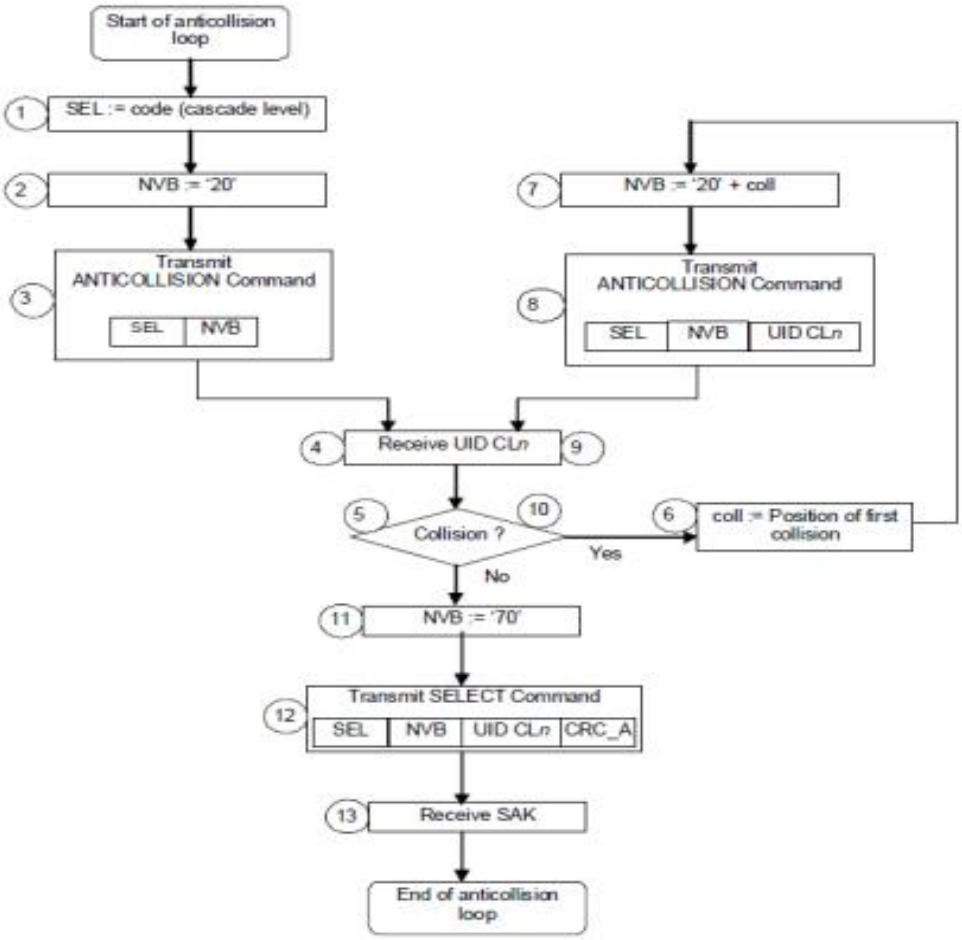

Fig.3 Anticollision loop

V. CONCLUSION

NFC would permit all the users to make payments straightforwardly by tapping their mobile phones with reader like debit card or credit card transactions. Numerous banks, mobile operators and companies are implementing NFC technology. NFC compliant to the ISO/IEC 14443 Type A standard results in NFC Type A and it undergoes anticollision to avoid uncertainty during multiple cards.

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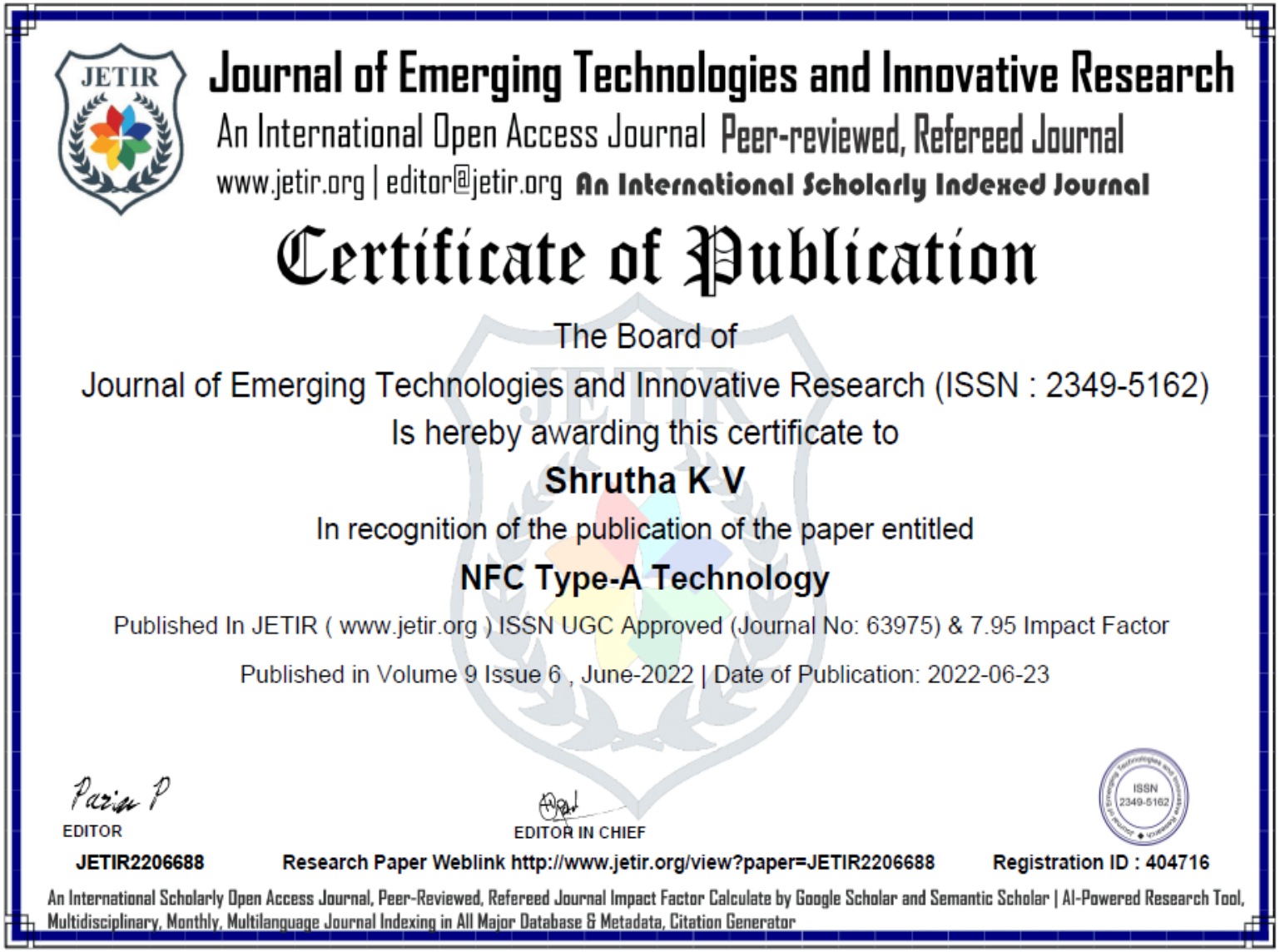

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Major Project: Phase-II Report

on

DESIGN AND IMPLEMENTATION OF TECHNIQUE FOR SUPPRESSION OF TORQUE RIPPLE IN SRM DRIVE

18MPE41

Submitted by

SHAMBHAVI K N

USN: 1RV20EPE13

Under the Guidance of

Dr. V Chayapathy
Associate Professor,
Electrical & Electronics Engg. Dept.
RV College of Engineering
Bengaluru – 560059

Dr. Narasimha M V
Chief of Advance Engineering
2W and 3W
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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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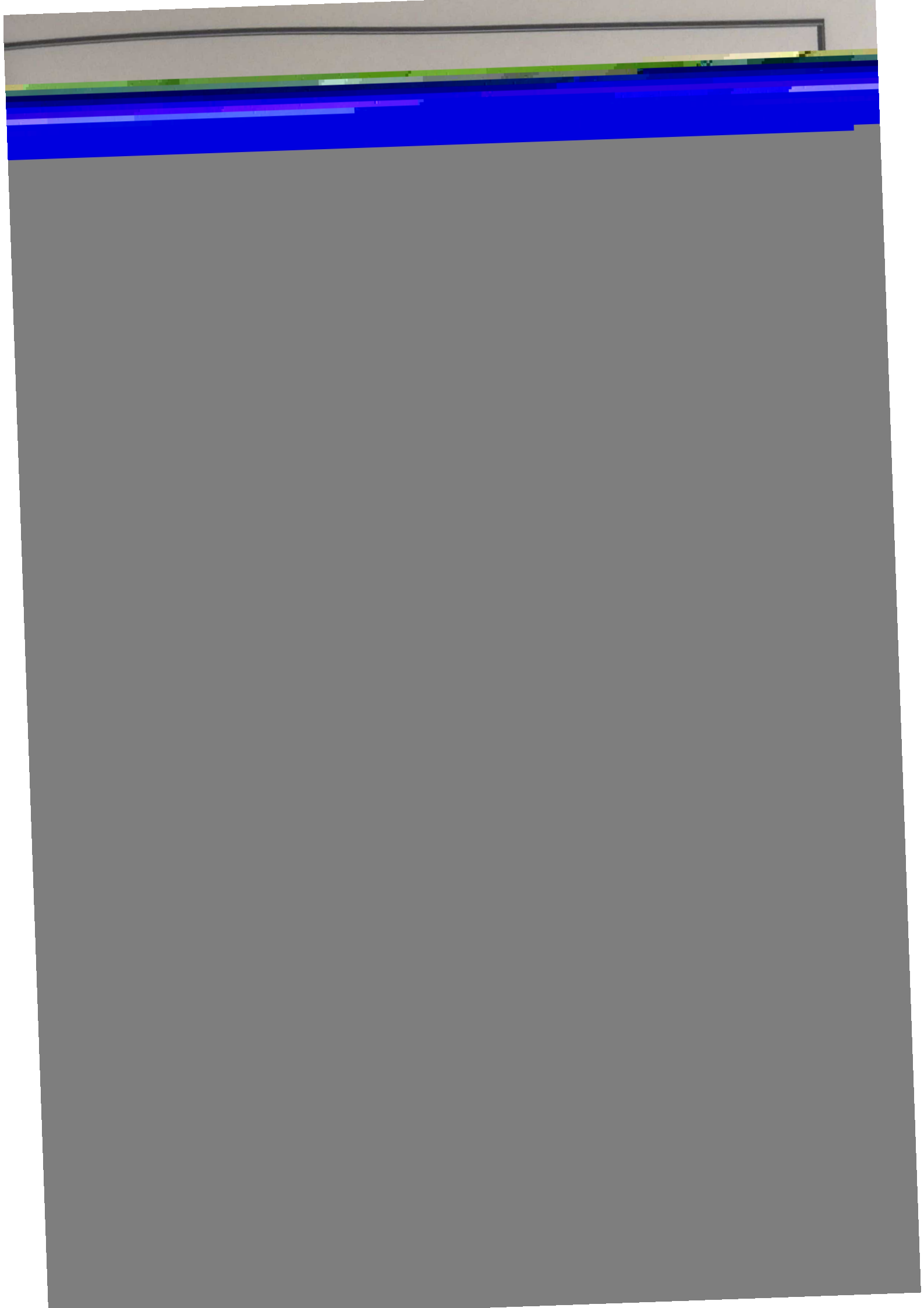

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DECLARATION

I, **Shambhavi K N**, student of fourth semester M.Tech in **Power Electronics**, **Department of Electrical and Electronics Engineering,** RV College of Engineering, Bengaluru declare that the project titled **"Design and Implementation of Technique for Suppression of Torque Ripple in SRM Drive"**, has been carried out by me. It has been submitted in partial fulfilment of the course requirements for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

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During the tenure of the internship at Ampere, her conduct, character, and interest to learn were found good.

We wish her all the best in her future endeavors.

Thanks & regards,

Vithal Acharya
Head – Human Resources
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Any achievement, be it scholastic or otherwise does not depend solely on the individual efforts but on the guidance, encouragement and cooperation of intellectuals, elders, and friends. A number of personalities, in their own capacities have helped me in carrying out this project titled, "**Design and Implementation of Technique for Suppression of Torque Ripple in SRM Drive**". I would like to take this opportunity to thank them all.

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I would like to thank my **parents** and **friends** for their constant moral support.

Shambhavi K N

Power Electronics

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ABSTRACT

Over the past decade, Switched Reluctance Motors (SRMs) have drawn a lot of interest for both residential and industrial applications. However, because of their projecting motor stator and rotor poles, they have an intrinsic torque ripple. To address this shortcoming, various control approaches have recently been presented, which are divided into two broad categories: direct and indirect methods. Indirect methods require larger memory space when compared with direct methods because of which they are undesirable. Among the various converter configurations, Asymmetric Half Bridge Converters are efficient and reliable. However, the drawback of these converters is that they fail to provide multilevel operation. Therefore, a novel asymmetric half bridge converter with the inclusion of a DC link to facilitate multilevel operation to reduce torque ripple in SRM drive is proposed.

The project work aimed at the design and development of asymmetric half bridge converter based on Direct Instantaneous Torque Control. The proposed converter includes a novel DC link enabling multilevel operation. The torque hysteresis controller magnetizes and demagnetizes the stator phases based on the error signals from the speed control unit and torque estimation unit. Typical bridge converter is used for the phases, however, when the required torque is greater than or lesser than reference torque, the capacitive voltage of the DC link is applied for smooth magnetization and demagnetization of successive and previous phases respectively. Multi voltage operation is possible thereby reducing the torque ripple.

The asymmetric half bridge converter based on DC link was designed to reduce torque ripple in SRM drive. Proposed converter was simulated using MATLAB/SIMULINK tool and a hardware prototype was realized for open loop operation. The torque ripple obtained with proposed converter is 5.931% which is less when compared to the torque ripple obtained using conventional converter, that is, 28% for the same speed. The proposed converter inherently improves the power factor as it distributes the current causing its amplitude to decrease. The future scope of the project is to optimize the converter in terms of size and cost. The hardware is to be implemented for closed loop operation for better analysis.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Shambhavi K N, Dr. V Chayapathy "Power Converter Configurations for Switched Reluctance Motors: A Review", International Research Journal of Engineering and Technology, Volume 9 Issue 6, June-2022

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GLOSSARY

DC	Direct current
DITC	Direct Instantaneous Torque Control
DTC	Direct Torque Control
SRM	Switched Reluctance Motor
TSF	Torque Sharing Function

Chapter 1

INTRODUCTION

The fundamental electronic systems used to run electrical equipment like Switched Reluctance Motors (SRMs) are power electronic drives. The drives of the SRMs are utilized to provide the correct electrical outputs for the machine windings combined with an appropriate control approach. As a result, the drive has a significant impact on an SRM's performance. Short-circuit risks across the dc source are be reduced by driving the SRM using an asymmetric bridge. The SRM's strong torque ripple, low torque/power density, and low power factor are its principal drawbacks [1]-[5].

When the needs of traction applications are taken into account, torque ripple reduction is one of the most crucial and difficult SRM design features. Structural design and sophisticated SRM control techniques are two solutions for reducing torque ripples. In order to further lessen the torque ripples of the SRMs, multi-stack and multi-layer constructions are created. To reduce the torque ripples, several converter topologies and control strategies are being explored [6]-[9].

Reluctance motors cannot be powered by an AC or DC source directly, in contrast to induction or D.C. motors. There is some level of power and control electronics. The electrical commutator controls phase currents to provide continuous motion is the power converter. In order to provide proper switching signals for the converter to match the expectations set on the drive by the user, the control circuit continuously checks the current and position feedback. The main goal of the circuit of power converter is to provide the phase winding a way to adjust the current supply by increasing and lowering it. There are several potential power converter circuit topologies for the SRM. The asymmetric half-bridge converter is the most used power converter for switched reluctance drives [10]-[13].

By using torque angle characteristics, an approach to reduce torque ripple is obtained. Theoretical techniques or static tests are used to determine these features. Through correction, deformation, and current optimization, certain techniques attempt to lessen torque ripple. The method is suitable for use at slow speeds. Torque ripple has also been minimized through current correction.

By altering the motor's shape, an effort is made to reduce torque ripple. A four-level converter is used to reduce the reaction time and current peak in SRM alongside simultaneously enhancing

the torque and speed ripple. Reducing losses and the quantity of switches in every converter leg is a practical and effective way to save costs and also increase efficiency. One switch is used for each phase of a novel converter that offers advantages in terms of low cost, high efficiency, and reduced torque ripple [14]-[18].

It is proposed to modify the current controller and lessen torque ripple by using sophisticated approaches and algorithms. The best solution for minimisation of torque ripple in SRM drives is introduced after several proposed methods have been compared.

1.1 Overview

The power converter is basically an electronic circuit that links the motor controller and the motor itself and provides control operations on speed and torque depending on the feedback.

An asymmetric half bridge converter with a cutting-edge DC link is used to power the SRM. The diode bridge rectifier produces pulsating DC. The converter receives its supply from the rectifier output. The torque is used as a feedback signal, providing the torque estimate unit with input. In order to establish the position of the rotor and the subsequent phase that has to be energised, the speed is also used as feedback. The hysteresis controller block receives the error signals from each of these units and uses them to create PWM signals that are sent to the appropriate phase switches to adjust the torque as needed.

1.2 Specific details

The motor considered is a 5.5hp SRM with 8 stator poles and 6 rotor poles. The nominal speed and voltage of the motor are 1500 rpm and 310V respectively. A 310V AC is input to rectifier which converts it into 310V pulsating DC. The is input to the converter. A look up table is referred to determine the subsequent phase to be energised. The inertia of the motor is taken to be 0.008Nms2 and the phase resistance of stator is taken to be 0.7 ohm.

The DC link in the asymmetric half bridge converter consists of diodes, switch, and capacitors, thereby providing multilevel voltage operation. In turn, reduces the torque ripple content in the SRM. The speed control block compares the reference speed and actual speed and sends the error signal to the control block. The torque estimation compares the actual torque and the reference torque and sends the error signal to control block. The controller, using the look up table, determines the next phase to be energised to meet the torque demand. The MATLAB Simulink

software is used to simulate the controller and converter for torque ripple minimisation in SRM drive.

1.3 Literature survey

An innovative active boost power converter was introduced. According to the operational requirements, it modifies the demagnetization voltage of SRMs. The Active Boost Power Converter features a straightforward design and low cost, which makes engineering applications simple. Simulation Results demonstrate that the converter being used complies with the design required. Its use in SRM significantly lowers the ripple in output torque [1].

SRMs for hybrid electric cars, which once used permanent magnet synchronous machines, have recently regained popularity because to the high price of rare-earth elements. Additionally, the SRM has a high fault-tolerance due to its capacity to function even when one or more motor phases are lost. Different electrical control systems are put into practise with the goal of reducing the torque ripples in SRM. Two of these frequently employed strategies were selected and were analysed using simulations. The torque ripples have been shown to be greatly reduced by redesigned Miller converters, which also contribute to a more consistent flux distribution and phase currents in the motor [2]-[3].

A new SRM drive circuit to cut down on torque ripple is proposed. The new circuit is equipped with boost capacitors and a chopper circuit. In order to provide a constant torque, it creates the stator current with a waveform that is as near as feasible to the ideal stator current found by FEM. Under either voltage control or current control, the torque ripple ratio is considerably smaller than that of the SRM operated by the standard circuit [4].

Unfavorable torque ripple is caused by the torque pulsation mechanism and extremely nonlinear magnetic characterization of switched reluctance motors, which also restricts the range of industrial applications. In order to increase the maximum speed of torque ripple-free operation taking converter voltage limitations into account, a modified approach for SRM torque control based on standard torque sharing functions is proposed in [5].

The terminal is magnetized and demagnetized using the proposed driving mechanism. By implementing an online angle control system, SRM is prevented from entering the negative torque area and the average torque and output power are increased [6]. The asymmetric type of

converter is the most appropriate and adaptable Switched Reluctance Motor converter. The converter has the capacity for fault tolerance; continued operation with decreased motor drive power output is also possible in the event of one winding failure. The asymmetric converter type (With MOSFET) is suited for very high-speed operation of SRM drive due to the short rise and fall periods of current, and it also provides little shoot through faults, according to a comparison of other type converter topologies. But because of low conduction losses and high input impedance, IGBT power switches are chosen for medium speed operation at high power [7].

In contrast to the conventional converters, the proposed converter has higher number of switching states that greatly reduce the amount of torque ripple. The simulation and experimental results validate the superiority of the proposed converter based on DITC when compared with the traditional converters [8].

In conjunction with standard drive electronics, a high converter VA rating, and a modified full bridge converter, a six-phase switched reluctance motor creates a torque dense drive with minimal torque ripple [9].

In contrast to normal operating circumstances, the lack of one SRM phase results in a distinct behavior of various machine-related parameters. For the switching angles to maintain the load torque around the same rotor mechanical speed, the reference electromagnetic torque rises. Each healthy phase current exhibits more amplitude, and the electromagnetic torque and harmonic content of the converter supply current also increases. The motor shaft is subjected to increased mechanical strains as a result of an increase in the amplitude of the electromagnetic torque ripple. When the same torque regulation-based control technique is used in both good and unsuitable operating situations, it causes an excessive pick phase current and an unsuitable electromagnetic torque overshoot [10].

The DTC and TSF are thoroughly scrutinized. The DTC technique tries to adjust the torque by speeding or receding the stator flux vector maintaining the stator flux linkage magnitude constant (within hysteresis band). The specific torque of each phase is often controlled by the TSF scheme to follow the reference determined by the TSF profiles [11].

The fundamental issue with the SRM drive system is that during operation, it generates a significant amount of electromagnetic torque ripple and noise. Additionally, when the power switch is turned off, a significant voltage spike is produced on the switch and stator winding end.

The actual findings demonstrate how a competent power converter and driving circuit may decrease switching waste, cut switching times, and enable the optimal operation of power semiconductor devices. As a consequence, the SRM drive system's dependability and efficiency may be improved, and the aforementioned issues are partially resolved [12].

An updated switching strategy is based on the premise that the two switches in each converter leg alternate between performing commutating and chopping operations during each electrical cycle. As a result, the converter's upper and lower transistors reduce the switching losses [13].

The switching of a 12/10-pole SRM from six-phase to three-phase is realized by a mode switching strategy. A mode-changing technique based on a three-phase Asymmetric Half Bridge converter is presented. The parameter relationship between six-phase and three-phase operation modes is examined. The machine is operated separately in six-phase and three-phase modes, along with switching from six-phase mode to three-phase mode, in both simulations and tests [14].

For low-cost and high efficiency, the converter of SRM requires both fewer switch devices and phase independence. A unique N+2 power converter is used to meet the aforementioned requirements. The benefits of split phase and asymmetric half bridge converters are combined in a new converter architecture. Two switches are linked to the midpoint in the foot of the split phase converter to replace midpoint capacitances, and PWM control was used to modify the mid-point voltage. Midpoint switches' current stress is far lower than that of a phase switch, and the voltage stress is equal to that of a DC bus voltage [15].

Switched reluctance machines experience phase overlap during phase commutation leading to electric and electromagnetic mutual coupling. The higher the phase number, the higher the expected influence of the actual coupling. The paper has confirmed previously discussed findings that the coil arrangement and resulting additive or subtractive coupled phase flux have a direct influence on the resulting torque waveform [16]-[19]. Furthermore, a method to include mutual phase coupling in the PWM-based direct instantaneous torque control algorithm is introduced. The control is verified by using a coupled finite element simulation. The results show that the implemented look-up-table-based model in the control is sufficient to incorporate all coupling effects visible in the finite element simulation. Furthermore, a noticeable reduction in the harmonic content of the output torque waveform is observed [20]-[22].

The conventional DTC method produces negative torque more or less, which reduces the torque-ampere ratio of motors. [23] proposes a new DTC method by three improvements. First, the hysteresis-loop control of flux is removed. New selection rule of voltage vectors is established to reduce the torque ripple. Second, the sectors divided in electrical space are reorganized by the actual positions according to the inductance profile. The boundaries between certain sectors are calculated and updated according to real-time working conditions. Finally, the alternative voltage vectors for increasing or decreasing torque are distinguished by whether any phase is excited. Therefore, the output torque tracks the reference accurately, which reduces the torque ripple. Moreover, the negative torque is avoided by the real-time regulation of the turn-off angle, and the torque-ampere ratio is increased accordingly [24]-[26].

A novel DITC with fixed switching frequency is proposed to solve the problem of shaft breaking in the starting and generating system of SRM. The sector of the rotor is reclassified according to the curve of combined torque. According to the rotor sector, polarity of PWM output signal and duty cycle coefficient are determined; so as to acquire the control signal considering both torque deviation and torque characteristics. The simulation results show that the proposed DITC achieves the very good torque ripple suppression effect under the finite switching frequency, and improves the motor operation efficiency [27]-[30]

Many strategies, both indirect and direct, have been put out so far to lessen the torque ripple in SRM motors. By adjusting the phase currents, torque ripple is decreased by using the proper current profiles, and torque is indirectly regulated in indirect methods. These profiles take up lots of space in the microcontroller unit since they are pre-calculated for a certain operating point. Contrarily, with the direct method, torque is directly regulated, and the current control unit is no longer present. The project proposes a converter based on direct torque control method with the inclusion of a novel DC link to provide multilevel voltage operation to reduce the torque ripple content in SRM drives.

1.4 Motivation

The Switched Reluctance motors are extensively taking over conventional motors because of the various advantages including high starting torque, high fault tolerance, self-starting, and cost effectiveness.

The Direct Instantaneous Torque Control method is superior to conventional control methods as it directly considers the instantaneous torque as controllable quantity in feedback block which reduces the torque ripple effectively.

The Asymmetric Bridge Converter has advantages for automotive applications due to its built-in scope for short circuit protection and improved fault tolerance. Performance in each of the three modes viz. magnetising, demagnetising and free-wheeling modes is acceptable. The related disadvantages are outweighed by these advantages.

1.5 Problem statement

To design and implement Direct Instantaneous Torque Control based power converter for reduction in torque ripple of Switched Reluctance Motor. Comparison analysis of torque ripple content in simulation with conventional converter and proposed novel converter to be carried out.

1.6 Project objectives

Design and simulation of power converter based on DITC to reduce torque ripple in SRM drives.

Comparison analysis of torque ripple with the proposed converter and conventional converter.

To implement the hardware prototype of the power converter for torque ripple reduction.

1.7 Organization of thesis

The project report consists of a total of seven chapters. A brief introduction for every phase in developing the work is as listed.

Chapter 1: Consists of a detailed literature survey carried out. It includes the problem definition, objectives of the project, motivation behind carrying out this project.

Chapter 2: Consists of concepts related to the principle of operation of SRM, different power converter topologies, and various control schemes available.

Chapter 3: Consists of the basic block diagram, overall methodology and flowchart of the project.

Chapter 4: Discusses concept of torque ripple in SRM, design of DITC based controller, and design of Asymmetric Half Bridge Converter.

Chapter 5: Consists of simulation models, specifications of hardware components and the hardware implementation of the converter.

Chapter 6: Discusses the simulation results of the closed loop operation of the proposed converter and the results of the open loop hardware implementation.

Chapter 7: Outlines the conclusions drawn from the project and the potential future tasks.

Followed by list of papers and books referred for understanding and analysis of project work.

Chapter 2

SRM AND CONVERTER TOPOLOGIES

In this chapter, the basic concepts of Switched Reluctance Motors, the power converter topologies and DITC method are discussed in detail.

2.1 SRM working principle

The variable reluctance theory is the basis of working of SRM. Power electronics switching circuits are used to produce the rotating magnetic field. The air gap affects the magnetic circuit's reluctance. Therefore, the air gap seen between stator and rotor may be altered to modify the motor's reluctance. The resistance provided to the magnetic flux in the circuit is referred to as the magnetic circuit's reluctance. Fig. 2.1 shows the change in reluctance for varying air gap.

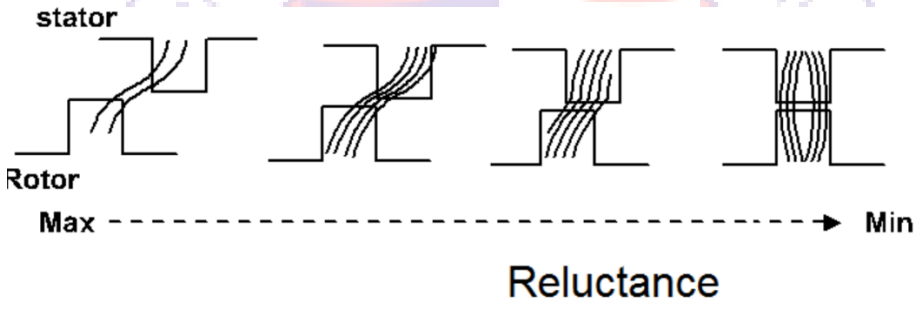


Fig. 2.1 Reluctance vs Air gap

The stator and rotor of SRM both feature projecting poles composed of silicon and soft iron stampings. Hysteresis losses are decreased considerably with the use of silicon stamping. The stator and rotor have corresponding outward and inward extensions. Main field windings are found in the stator, but there are no windings on the rotor. Each stator winding is linked in series with the opposite pole to improve the circuit's effective MMF. These coils are known as Phase Windings. The stator, rotor and the field windings are as shown in the Fig. 2.2.

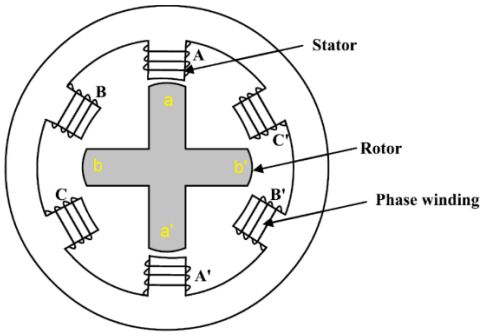


Fig. 2.2 Parts of SRM

Depending on the necessity, the stator and rotor's pole numbers are changed. Traditionally, there are fewer rotor poles than stator poles in a motor. A low angle of rotation for the motor is attained by increasing the number of poles. On the rotor shaft is a position sensor that transmits a signal to the control circuit in order to detect the rotor's position. The control unit sends the motor the input signal to magnetize the succeeding phase winding in the series based on the signal it has received.

SRMs are widely used in many industries owing to the inherent benefits, which include:

• The lack of windings on the rotor eliminates the requirement for slip rings and carbon brushes.

• Economical due to the lack of permanent magnets.

• Because both the stator and the rotor are projected, no external ventilation system is needed.

• The operation of the motor is not significantly impacted by phase loss, and it is self-starting and rather simple to manage.

2.2 Power Converter Topologies for SRM

To achieve the intended operation of the SRM, the use of a suitable power electronic converter and control circuitry is necessary. These components, along with a number of sensors, conditioning circuits, and other devices, make up an electric drive that regulates the SRM currents, which in turn affect torque and speed. Due to the independence of the windings in the machine, it is feasible to control the current independently for each phase according to the rotor position.

Power converters for SRM drives are classified mostly depending on the type of switching employed. There are two categories based on the type of switching: Hard switched converters and Soft switched converters. The sub categories in Hard switched converters include Bridge converters, Magnetic converters, Capacitive converters, and Dissipative converters. Self-

commutating converters like Series Resonant and H Bridge converters are types of Soft switched converters. Bridge converter topologies consist of diodes and switches. They are basically derived from H-Bridge converter topology and stand out owing to the simple structure and controllability. Asymmetric half bridge converter, Shared phase winding converter, Shared switch converter and Full Bridge converter are types of Bridge converters. Asymmetric Bridge Converter is advantageous because of its inherent scope for short circuit protection and greater fault tolerance.

In this type of converter configuration, if there are n motor phases, the converter consists of 2n active switches. The circuit of the same is as shown in Fig. 2.3. When soft switched, the converter provides for operation in 3 different modes: Magnetization, Demagnetization and Free-wheeling mode. When hard switched, it operates in only two, i.e., Magnetization and Demagnetization modes. Maximum versatility due to separate control of the upper and lower switches. The converter operates with the same efficiency irrespective of it being in magnetization or demagnetization mode. Between the two switches, the winding is connected in series. As a result, in the event of a short circuit failure, the inductance of the windings restricts the current surge, giving the protective devices enough time to find and isolate the issue.

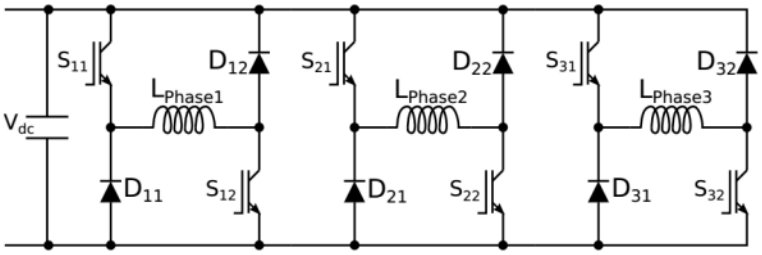


Fig. 2.3 Circuit diagram of Asymmetric Half Bridge Converter

2.3 Direct Instantaneous Torque Control Method

In general, indirect control and direct control are the two subcategories of torque control. Circuit profiling and the Torque Sharing Function are the key factors influencing indirect torque control. The reverse torque model of the motor meets rigid criteria as per the indirect torque control algorithm. The reverse distance model has a complex structure due to the complicated electromagnetic relation and high saturation nonlinearity of SRM, and the number of calculations for pertinent control systems also significantly rise.

Direct Torque control (DTC) and Direct Instantaneous Torque Control are two subtypes of the direct control technique. DTC and DITC are essentially parts of the bang-bang hysteresis control technique, which benefits from a straightforward structure and strong transient performance. An ideal control approach known as DITC uses torque as its optimization goal. The drive circuit of the DITC system uses an asymmetric half bridge (AHB) circuit, and the reference torque is calculated using a look-up table using the feedback values of the current and angular position. The three AHB states in single-phase and commutation-phase are structured to ensure direct control of the instantaneous torque in accordance with the hysteresis scheme. The block diagram of DITC method of torque ripple minimization is shown in Fig. 2.4.

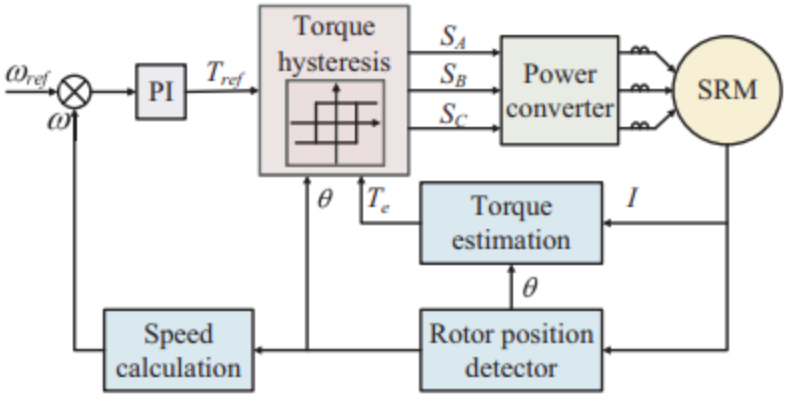


Fig. 2.4 DITC system block diagram

2.4 Summary

This chapter discussed the theory of SRM, its working principle, various converter topologies and particularly, asymmetrical half bridge topology and Direct Instantaneous Torque Control method, with the respective block diagrams.

Chapter 3

METHODOLOGY AND BLOCK DIAGRAM

This chapter discuss about block diagram and methodology for Direct Instantaneous Torque Control based asymmetric half bridge converter for torque ripple reduction in SRM. The chapter covers the basic block diagram, circuit, and different operating modes of the asymmetric half bridge converter.

3.1 Methodology

The Direct Instantaneous Torque Control's fundamental idea is to choose the appropriate voltage vectors using a pre-defined switching table. The choice is made depending on the torque and the stator flux linkage's hysteresis control. The stator voltage determines the flux magnitude. Therefore, the torque is adjusted by changing the angle between the fluxes coming from the stator and rotor. Instantaneous control of torque is possible as the rotation of the stator flux vector with respect to the rotor flux vector is accelerated, decelerated, or kept constant (or stopped) assuming it to remain unchanged during the control action.

The steps involved in the design and development of the proposed power converter based on Direct Instantaneous Torque Control are as shown in the flowchart Fig. 3.2.

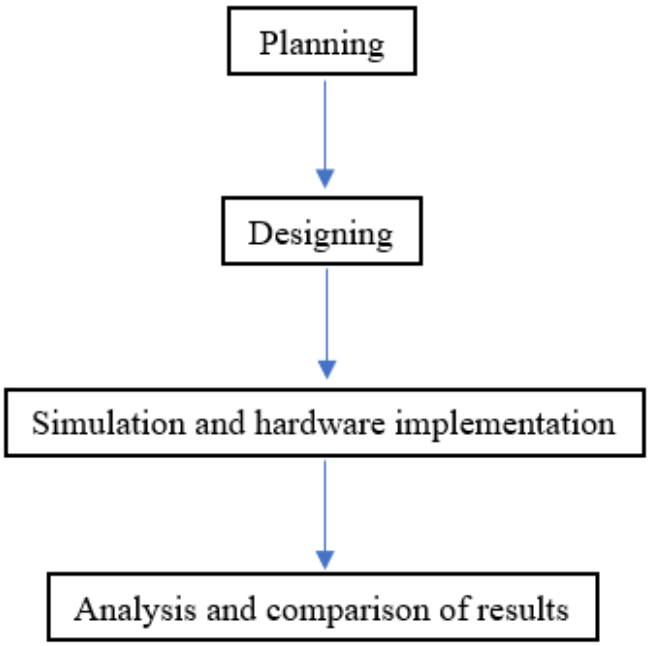


Fig. 3.2 Flowchart of proposed work

- Planning: A detailed literature survey is carried out for selecting required topology of the converter. Various converter configurations and controllers are studied and comparative analysis is carried out. The asymmetrical half bridge converter topology is selected.

- Designing: The SRM is selected based on literature survey. Design of the typical asymmetrical bridge converter along with the novel modification of inclusion of DC link to the conventional circuitry to reduce torque ripple.

- Simulation & Hardware Implementation: Simulation of the SRM with controller based on Direct Instantaneous Torque Control and asymmetric half bridge converter including DC link in MATLAB Simulink. Implementation of the designed power converter using suitable components.

- Analysis and comparison: Analysis and comparison of the simulation result for the torque ripple content for both cases, that is, with conventional converter and proposed novel converter. Analysis of output waveforms of hardware implementation of the proposed converter.

3.2 Block diagram

The Figure 3.1 shows block diagram of Direct Instantaneous Torque Control method. It consists of torque hysteresis controller, torque estimation unit and asymmetric half bridge converter.

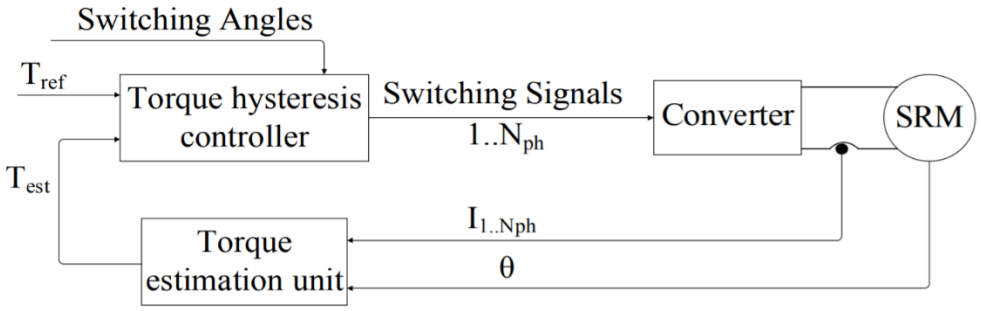


Fig. 3.1 Block diagram of Direct Instantaneous Torque Control

Torque Hysteresis Controller : The hysteresis torque controller receives the error signal after the speed control unit evaluates the motor's actual speed to a reference value. The look up table and phase current determine the actual torque. The switching signals are specified for the converter.

Torque estimation unit: The rotor's location is computed using this error signal, allowing the excited phase to be identified. By comparing the actual torque with the reference torque, the torque estimation unit provides the error signal to the torque hysteresis controller.

Speed control unit: The speed control unit compares the actual speed of the motor to error signal assisting in determining the position of the rotor. The signal is input to torque hysteresis controller unit.

The torque hysteresis controller decides which phase is to be magnetized after receiving input from both blocks.

3.3 Asymmetric half bridge converter

- The circuit diagram of the asymmetrical half bridge converter along with novel DC link circuit is as shown in Fig. 3.3.

- The conventional asymmetric converter construction is implemented to the phases. Both capacitors link to the excited phase when the auxiliary switch is turned on, which increases the phase voltage. This happens when the torque is decreasing or when a phase is being driven. Other times, the phase voltage is supplied by the AC source, which enhances the power factor.

- The auxiliary switch is used to raise phase voltage and enhance power factor. The converter draws current from the source when the torque is not decreasing, and the AC source is able to supply the necessary voltage. Additionally, C1's voltage is automatically managed and does not require any voltage sensors. C1's voltage rises to the peak of the AC source's voltage. D4 does not conduct at that point, causing C1's voltage to once again drop.

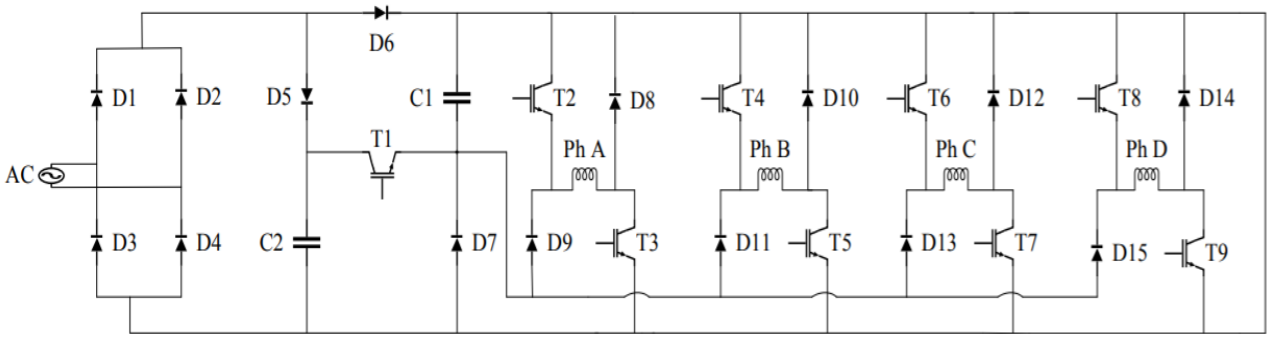
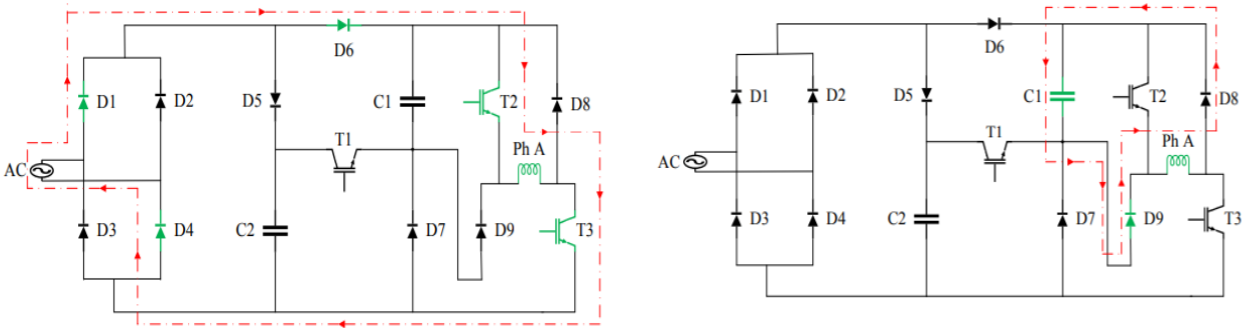


Fig. 3.3 Novel asymmetric half bridge converter with DC link

3.3.1 Operating modes

Due to providing multilevel voltage and controlling the power factor in this converter, there are more operating modes than the conventional converter.

- When the AC voltage source in Fig. 3.4(a) exceeds the voltage of C1, D6 conducts, and the AC source supplies the necessary current.
- In Fig. 3.4(b), both switches for the phase switch off when the phase current reaches its maximum value, and the voltage of C1 is supplied to the phase with negative polarity. In this mode, C1 is charged and D8 and D9 conduct the demagnetized current.
- In Fig. 3.4(c), the torque is decreasing and the voltage of C1 is higher compared to the voltage of the AC source. The motor phase receives voltage from C1, increasing the current and torque. Torque falls inside the hysteresis band.
- The motor is running at high speed in Fig. 3.4(d), and the back-emf prevents the torque from matching the reference. The current does not have enough time to increase because of the rapid speed. This calls for applying a voltage to the phase that is higher than the dc voltage. VC1+VC2 is applied as T1 turns on. The torque is contained within the hysteresis band.
- In Fig. 3.4(e), T2 turns off when the current reaches its reference, allowing the phase winding's stored energy to freewheel on its own. The D8, D9, and T3 conduct in this manner. The phase's applied voltage is zero, causing the current to gradually decrease.



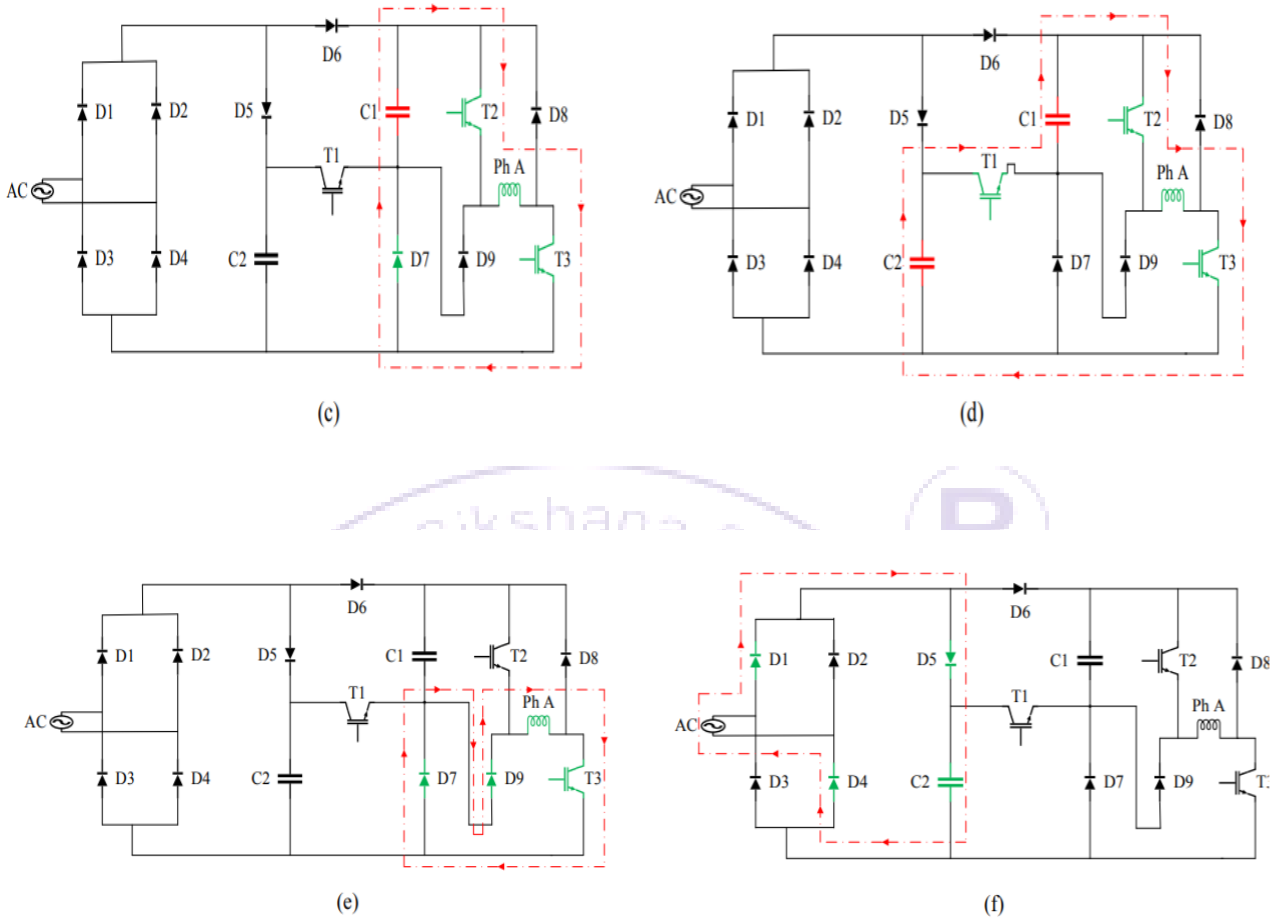


Fig. 3.4 Operating modes of the converter

3.4 Summary

The block diagram, methodology and design of torque ripple reduction of SRM using Direct Instantaneous Torque Control method-based power converter is explained in detail with the block diagram, circuit diagram and operating modes.

Chapter 4

SPECIFICATION AND DESIGN DETAILS

This chapter discusses the specifications of the SRM used. The design details of the asymmetric half bridge converter including novel DC link and design of the controller are also discussed in detail.

4.1 Specifications

The specifications of the SRM selected after extensive literature review are depicted in Table 4.1. The number of rotor poles selected is lesser than the number of stator poles to minimize the torque ripple content.

Table 4.1 Specifications of the motor

Parameters	Specifications
Number of stator poles	8
Number of rotor poles	6
Nominal speed	1500 rpm
Nominal power	5.5 hp
Phase resistance	0.7 ohm
Motor inertia	0.008 NmS^2
Nominal voltage	310V

4.2 DITC design

DITC based torque hysteresis controller limits the torque within specified bands by maintaining the error signal obtained as minimum as possible. The conventional DITC creates a series of hysteresis schemes based on the torque error. The torque error ΔT is obtained from the expression (1).

$$\Delta T = T_{ref} - T_e \quad (1)$$

where,

ΔT - Torque error

T_{ref} - Reference torque

T_e - Electromagnetic torque.

To prevent excessive torque ripple, the switch tube is only employed in the excitation and freewheeling states when the motor is working in single-phase. Fig. 4.1 (a) depicts the hysteresis in the single-phase area, where T_{min} and T_{max} represent the torque error's minimum and maximum values, respectively. The switching states of the overlapping phases do not change simultaneously throughout the commutation. The control priority of the incoming and outgoing phases is carefully taken into consideration in order to maintain the smoothness of commutation. The outgoing phase functions as a demagnetizing phase to lower the torque when $T_e > T_{ref}$. The incoming phase is excited, which creates torque primarily, when the generated torque is inadequate. Fig. 4.1 (b) illustrates the hysteresis in the commutation phase. With both the upper and lower arms of active, a magnetized state (S = 1) is established. Freewheeling condition (S = 0) is the circumstance in which only one of the upper and lower bridge arms conducts. Demagnetization state (S = 1) is the term for when both the upper and lower arms switches are switched off simultaneously. This working of the asymmetric bridge converter is depicted in Fig. 4.2.

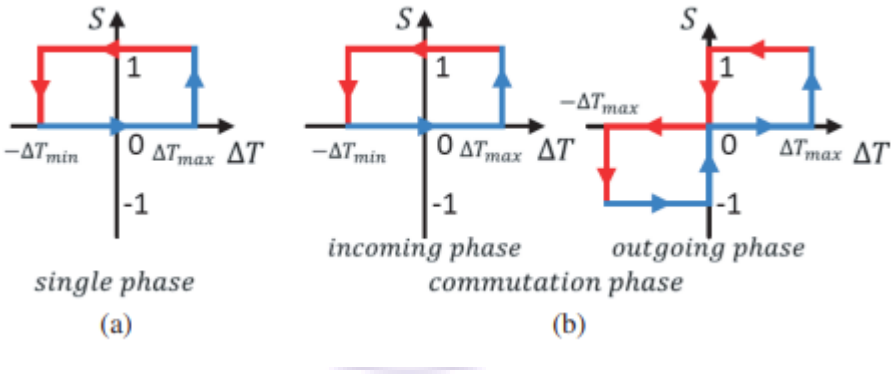


Fig. 4.1 DITC based hysteresis controller

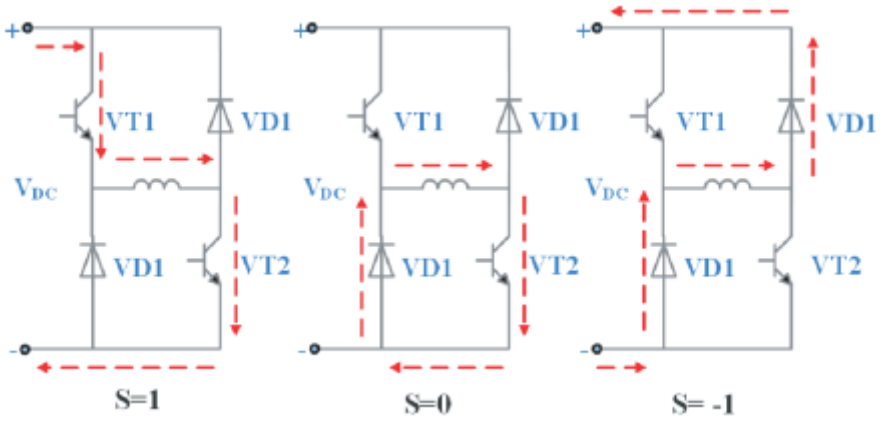


Fig. 4.2 Switching states of asymmetric half bridge circuit

4.3 Torque Ripple in SRM

Although the torque ripple is successfully reduced by the conventional DITC hysteresis technique, the reduction effect is not perfect, and the torque ripple in the commutation zone is still too great. The torque is created by the rotor's propensity to rotate to its minimal reluctance position due to the SRM's doubly salient construction. Phase current and inductance gradient are the only two factors that affect the torque when the magnetic saturation effect is taken into account. The motor's inherent characteristic is the rate at which SRM inductance varies with rotor position, and the steady electromagnetic torque is produced by adjusting the current and inductance slope. The expression for single phase torque is depicted in (2) [23].

$$Tn = \frac{1}{2} i_n^{\,2} \frac{dLn}{d\theta} \qquad (2)$$

Where,

T_n – Torque of n^{th} phase

i_n – Current of n^{th} phase

L_n – Inductance of n^{th} phase

Θ - Position of the rotor

In the real discrete control process, the variation of the current occurs with its serrated wave change in a specific range rather than with the smooth change of the theoretical curve. As a result, torque ripple is caused by the serrated torque waveform.

Also, in the commutation region, the torque is provided by (3) [23].

$$Tcom = \frac{1}{2} i_n^2 \frac{dLn}{d\theta} + \frac{1}{2} (i_{n+1}^2)(\frac{dL_{n+1}}{d\theta}) \quad (3)$$

Where,

$Tcom$ – Torque in commutation region

i_{n+1} – $(n+1)^{th}$ phase current

L_{n+1} - $(n+1)^{th}$ phase inductance

In commutation zone, excitation phase and demagnetization phase are superimposed to produce torque, and the inductance region of the two phases are different. The demagnetization phase falls the excitation phase, dL/dϴ, begins to increase. The two phases' inductance slopes vary and exhibit nonlinear change, respectively. The slope of inductance rises as a result of the torque superposition concept. Formula (3) indicates that the equivalent torque slope dT/dt likewise rises, increasing the torque ripple in the commutation zone.

Under conventional DITC, the torque produced by the SRM's minimum and maximum inductance regions is not properly taken into account. According to the aforementioned evaluation, DITC certainly maintains the torque ripple within the hysteresis range as the SRM is operating in single-phase. The excitation phase and demagnetization phase, however, are in the critical states of minimal and maximum inductances, respectively, after entering the commutation zone. The torque ripple in the commutation zone cannot be successfully suppressed by hysteresis because the torque slope there is substantially larger than it is in the single-phase region.

4.4 Asymmetric Half Bridge Converter

For SRM drives, an asymmetric half-bridge converter offers the greatest degree of control flexibility and fault tolerance. As seen in Fig. 4.3, each phase of this standard converter is made up of two controllable switches and two diodes. The converter applies the same DC-link voltage to the switches and diodes, respectively, for magnetization and demagnetization. With the hard chopping scheme's magnetization and demagnetization modes, phase current may be controlled.

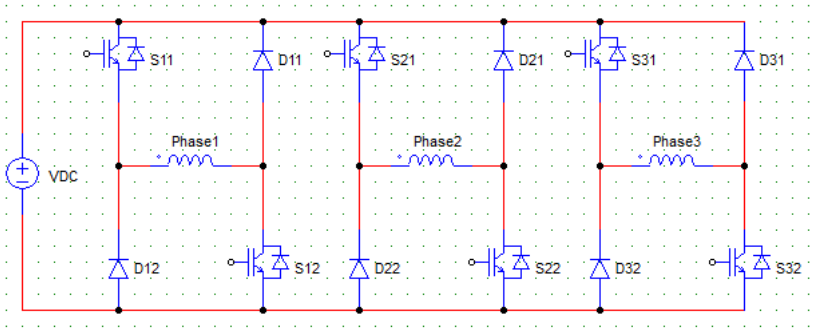


Fig. 4.3 Conventional asymmetric half bridge converter circuit

Considering one of the phases, two modes of operation are possible for hard chopping, namely, magnetization mode and demagnetization mode. The switches S11 and S12 are on and diodes D11 and D12 are non-conducting for magnetization mode. The current in the phases increases. In contrast to this, the switches S11 and S12 are off and the diodes D11 and D12 are conducting for demagnetization mode. In accordance with this, the phase current in this mode decreases.

Magnetizing mode:

In this mode, for one phase, the voltage across the phase is described by (4).

$$V_{ph} = V_{DC} - V_{Sw} \quad (4)$$

Where,

V_{ph} – Voltage across the phase

V_{Sw} – Voltages across the switches S11 and S12

Since, V_{Sw} is negligible,

$V_{ph} = V_{DC}$

The voltage drop across the switches when on is approximated to zero as represented in (5)

$$V_{sw1} = V_{Sw2} = V_{Sw} \sim 0 \quad (5)$$

Where,

V_{Sw1} = Voltage drop across switch S11

V_{Sw2} = Voltage drop across switch S12

Demagnetizing mode:

In this mode, for one phase, the voltage drop across one phase is described by (6).

$$V_{ph} = -V_{DC} - V_{FSw} \quad (6)$$

Where,

V_{FSw} – Forward voltage of the switch approximated to 0

Therefore,

$V_{ph} = -V_{DC}$

The voltage across the switches during chopping is shown in (7).

$V_{sw1} = V_{Sw2} = V_{DC} + V_{FSw}$

The pulse-width modulation (PWM) technique is used to regulate the phase current, and the switching frequency corresponds to the frequency of the chopping switch current during that process. The chosen switching frequency does not change with rotor speed; it is always constant. Only this frequency type is involved in the calculation of power losses of the converter's switching components. A high switching frequency results in high switching loss.

4.5 Summary

The specifications of the motor, torque ripple in SRM, and the design procedures of DITC based torque hysteresis controller and asymmetric half bridge converter were explained.

Chapter 5

SIMULATION ANALYSIS AND HARDWARE APPROACH

This chapter discusses the simulation of the novel Asymmetric Half Bridge Converter with DC link based on DITC torque controller to reduce torque ripple simulated using MATLAB Simulink software. The hardware approach for the project is discussed.

5.1 Simulation analysis

A simulation model is developed for Asymmetric Half Bridge Converter based on DITC for torque ripple reduction in SRM drive using MATLAB Simulink software. The Simulink model of the same is represented in Fig. 5.1.

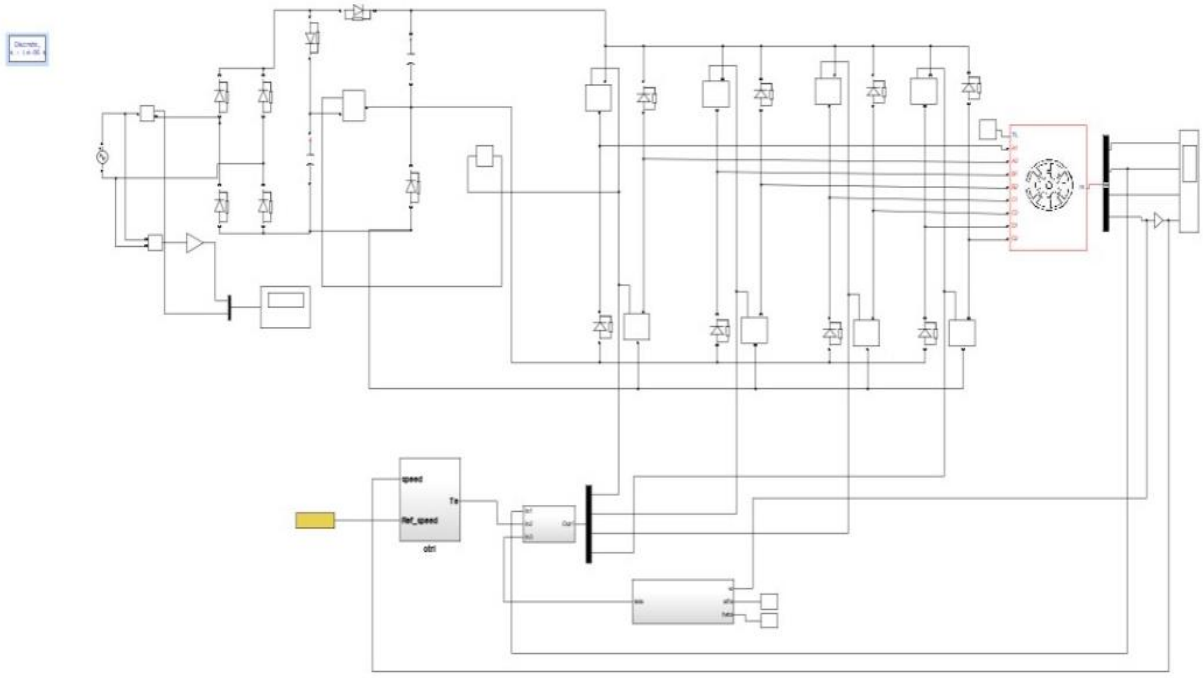


Fig. 5.1 MATLAB Simulink model of Novel Asymmetric Half Bridge Converter

The look-up table's inputs of rotor position and phase currents are used to determine the actual torque, which is compared to the reference torque. The switching signals are specified by the hysteresis controller. The control unit chooses the incoming and outgoing phases based on the rotor position and switching signals. To limit the overall torque, the information obtained from the current states of the incoming and outgoing phases dictates the subsequent states of both phases.

For the torque commutation, the discussed strategy for three consecutive phases is as tabulated in Table 5.1.

Fig. 5.1 Strategy for torque commutation for three consecutive phases

Active Ph N-1	Active Ph N	Active Ph N+1	Ph N-1 State	Ph N State	Ph N+1 State
0	0	0	x	x	x
1	0	0	1|0	x	x
1	1	0	1|0|-1	1|0	x
0	1	0	-1|x	1|0	x
0	1	1	x	1|0|-1	1|0
0	0	1	x	-1|x	1|0

Managing the torque of the excited phase allows the overall torque to be changed when just one of the motor phases is excited. When the measured torque is less than the reference and positive voltage is provided to the phase, the switching state S equals 1. If the measured torque exceeds the reference value, the switching state equals to -1, and the phase receives a negative voltage. The phase is said to be in a freewheeling mode when it is in a zero (0) condition. The overall torque of the motor is regulated by adjusting the torque of the two adjacent phases during the time it is in a two-phase conducting state, also known as phase commutation.

The feedback loop consists of three blocks, namely, speed control unit, torque estimation unit and hysteresis torque controller.

The speed control unit compares the actual speed of the motor with the reference value and the error signal is input to the hysteresis torque controller. The Simulink model of the same is as shown in Fig. 5.2. This error signal is also used to determine the position of the rotor so that the phase to be excited is determined.

The torque estimation unit compares the actual torque and the reference torque and sends the error signal to torque hysteresis controller.

The torque hysteresis controller takes input from both the blocks and determines the next phase to be excited. Based on the signals from speed control unit and torque estimation unit, by referring to the look up table, the switching signals are provided to the switches so that the required phase is excited.

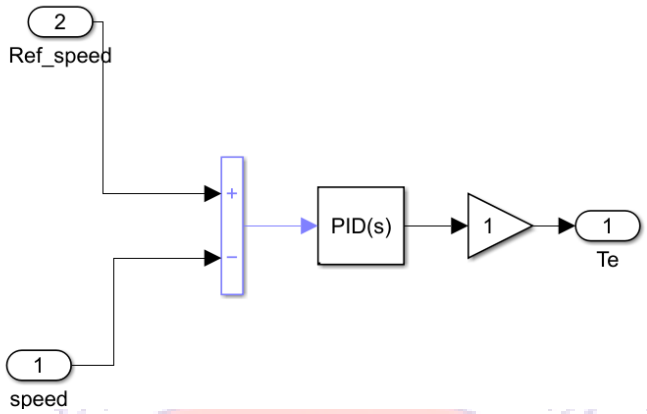


Fig. 5.2 MATLAB Simulink model of speed control unit

5.2 Hardware implementation

The hardware prototype of the novel asymmetric half bridge converter with DC link is implemented for open loop operation. The PIC16F877A microcontroller is used to provide the switching pulses to the switches. MOSFETs are used for switching operation. A MOSFET driver TLP250 is used to amplify the pulses to the required value. The hardware specifications are as depicted.

5.2.1 Microcontroller

- Only 35 one-word commands, making programming simple.
- All instructions are single-cycle, with the exception of programme branches, which are two-cycle instructions.
- Operating speed: 200 ns for an instruction cycle and a clock input of 20 MHz.
- Higher limit of 8K x 14 words of Flash Program Memory, upper limit of 368 x 8 bytes of Data Memory (RAM) and utmost 256 x 8 bytes of EEPROM Data Memory.
- Pin out compatible to other 28-pin or 40/44-pin
- PIC16CXXX and PIC16FXXX family of microcontrollers.

- The microcontroller is as represented in Fig. 5.3.

Fig. 5.3 PIC16F877A microcontroller

5.2.2 Transformer

Two transformers of the rating 230/12V are used to provide power to the microcontroller and the converter circuit. A transformer basically increases or decreases the magnitude of voltage or current at the output keeping the frequency constant. The pictorial representation of the same is in Fig. 5.4.

Fig. 5.4 230/12V Step-down transformer

5.2.3 MOSFET

MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor. MOSFETs are voltage-controlled switches with high input impedance and high thermal stability. A 4N60 MOSFET is used in the proposed implementation which is depicted in Fig. 5.5.

Fig. 5.5 4N60 MOSFET

5.2.4 MOSFET driver

The MOSFET driver TLP250 amplifies the pulses generated by the microcontroller to 12V as required by the converter. It consists of two npn and one pnp transistor in Darlington circuitry for the operation. The same is depicted in Fig. 5.6.

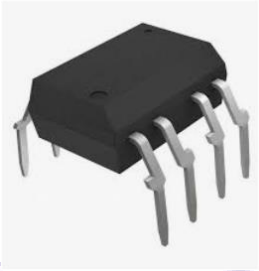


Fig. 5.6 TLP250 MOSFET driver

The complete hardware setup of the proposed converter along with power and control circuitry is represented in Fig. 5.7.

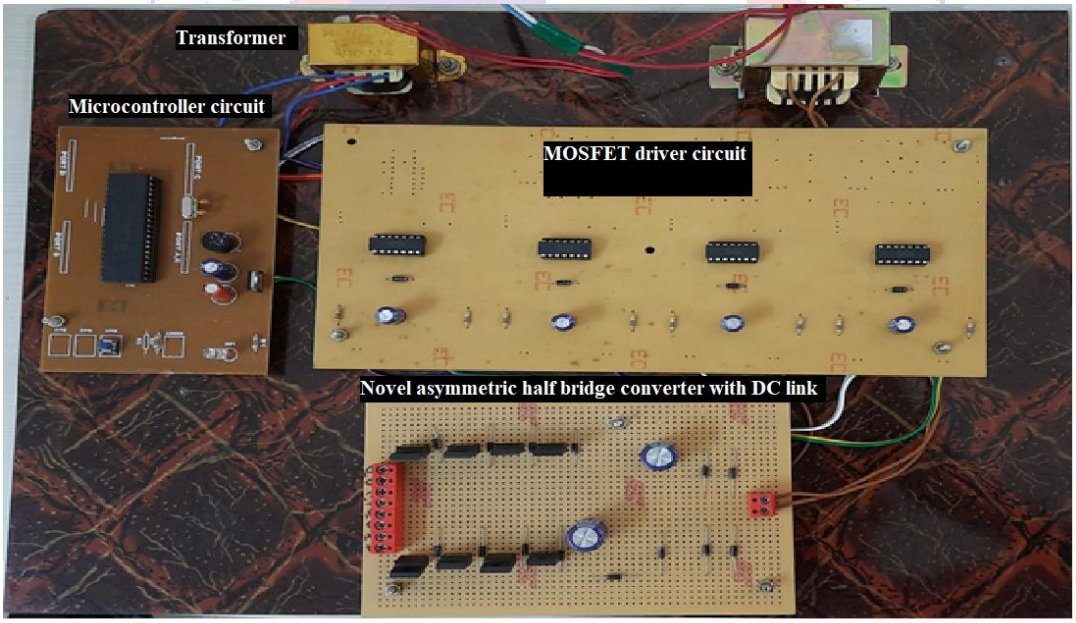


Fig. 5.7 Hardware set up of the proposed novel converter for open loop operation

The hardware is implemented for open loop operation wherein the control circuit provides excitation for each of the eight phases consecutively. The additional DC link facilitates smooth magnetization and demagnetization of phases.

5.2.5 Power circuit for microcontroller

The microcontroller is supplied by a 230/12V transformer. A diode bridge rectifier and

electrolytic capacitor are connected to rectify and filter, respectively. The regulator connected converts the rectified 12V DC to 5V DC. The capacitor filter is connected to fine tune. The oscillator output signal is supplied to the microcontroller. An LED turns on for the time period that the Microcontroller is on. The circuit of the same is depicted in Fig. 5.8.

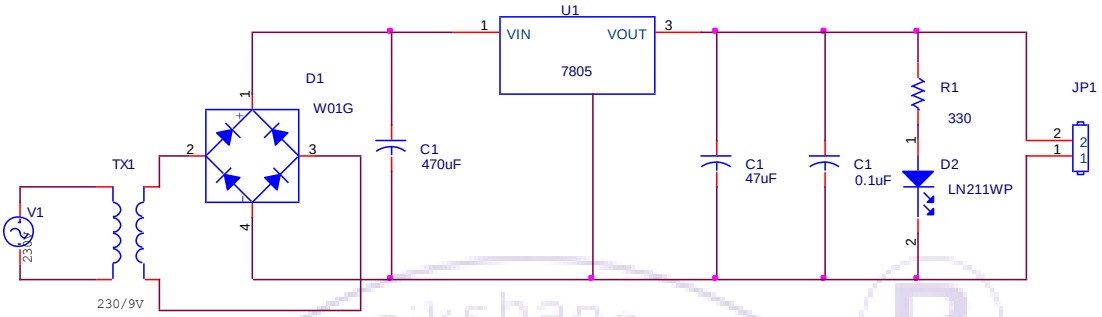


Fig. 5.8 Power circuit for microcontroller

5.3 Summary

The simulation models, specifications of hardware components and the implementation of the converter were discussed in this chapter.

Chapter 6

RESULTS AND DISCUSSIONS

This chapter discusses the simulation results of the closed loop operation of the proposed converter. The results of the open loop hardware implementation are also observed.

6.1 Simulation results

The rectifier circuit consisting of diode bridge rectifier converter 310V AC to 310V pulsating DC. This signal is input to the converter circuit. The output waveform of the rectifier is illustrated in Fig. 6.1.

The rectifier circuit consists of 4 diodes. The output of the same is pulsed DC of the same magnitude, i.e., 310V.

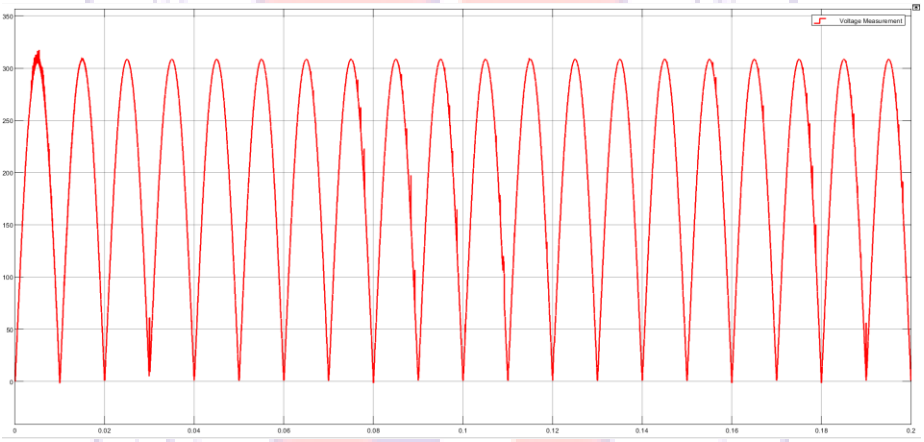


Fig. 6.1 Rectifier output waveform

The motor speed is set at 900rpm. The flux, current, torque and speed waveforms at 900rpm using the proposed converter are shown in Fig. 6.2. The flux obtained is trapezoidal in shape as the current is distributed. The amplitude of the current is also reduced.

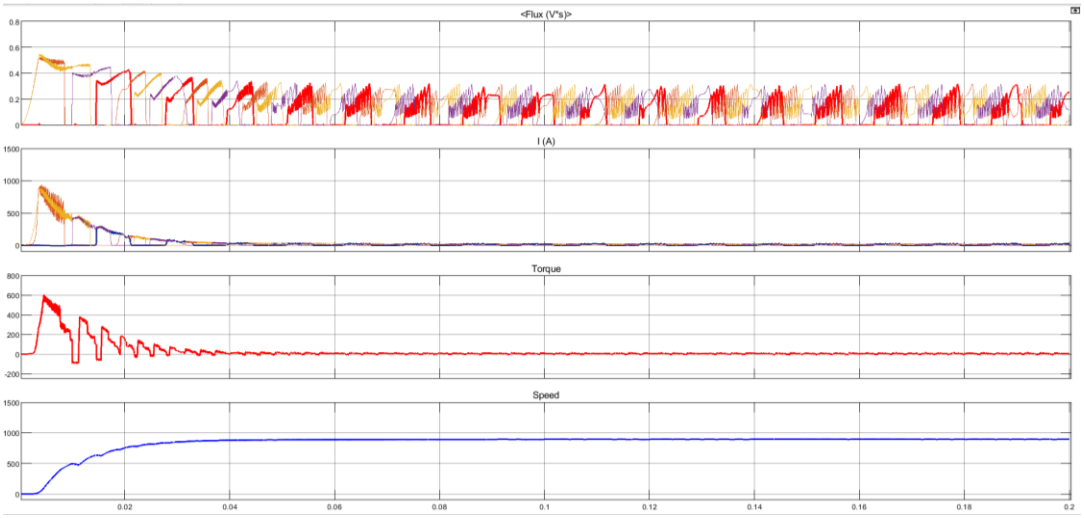


Fig. 6.2 Output waveforms at 900rpm using proposed converter

The flux, current, torque and speed waveforms at 1200rpm using the proposed converter are shown in Fig. 6.3. The flux waveform is trapezoidal in shape. The torque ripple is initially high, reduces gradually.

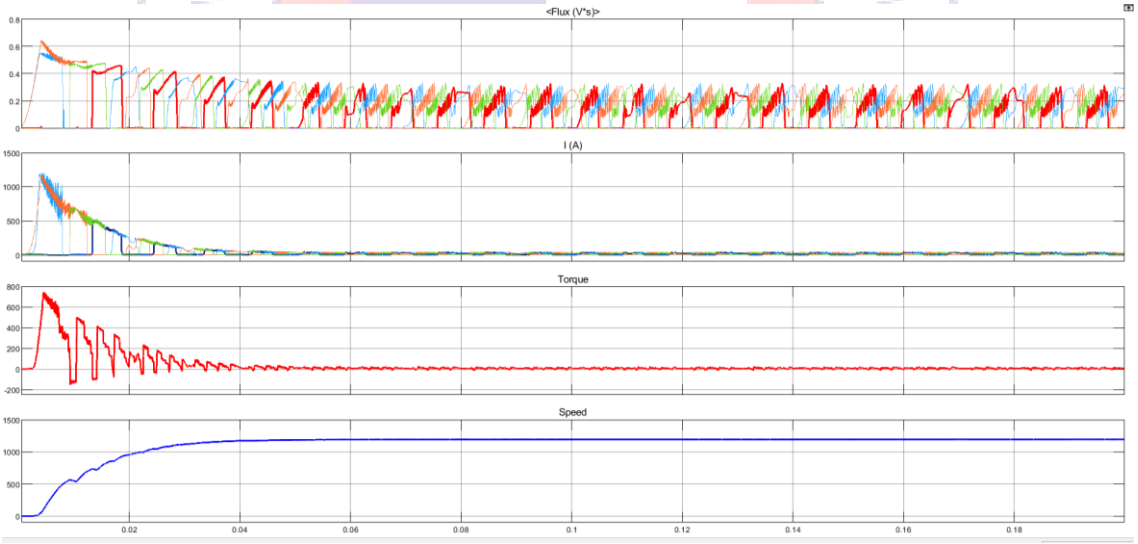


Fig. 6.3 Output waveforms at 1200rpm using proposed converter

The torque waveforms of the proposed converter along with the signal statistics at 900rpm and 1200rpm are shown in Fig. 6.4 (a) and Fig. 6.4 (b) respectively. The waveform represents the torque waveform at steady state. The transient shoot up can be reduced by incorporating changes in the design parameters.

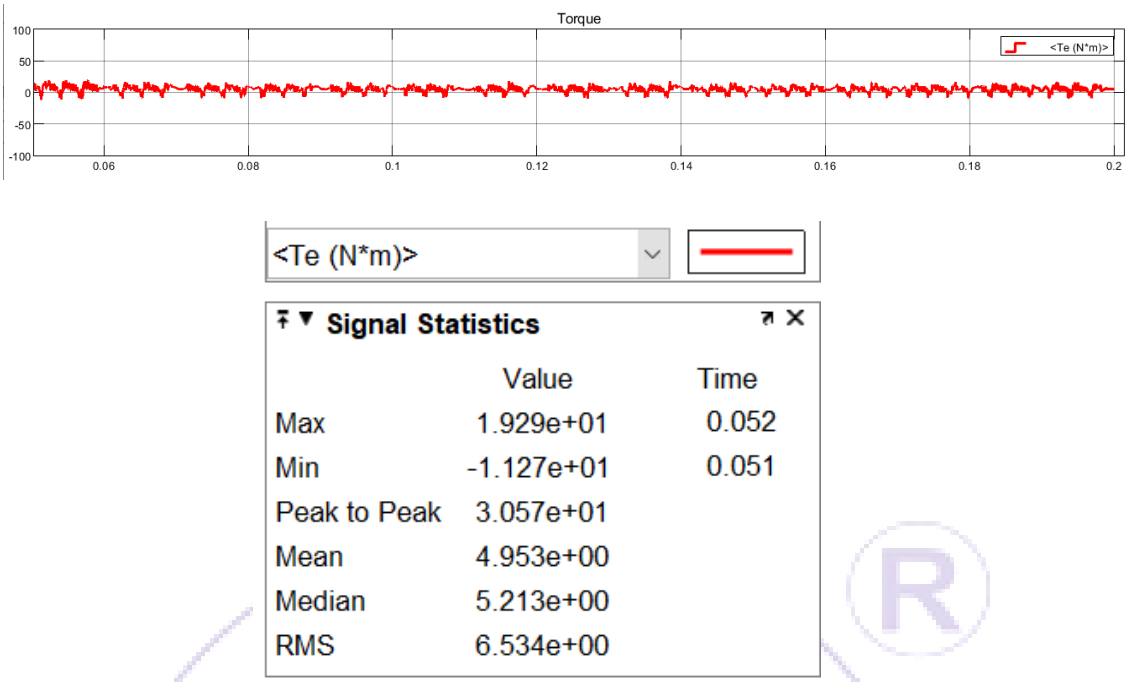


Fig. 6.4 (a) Torque waveform with signal statistics at 900rpm using proposed converter

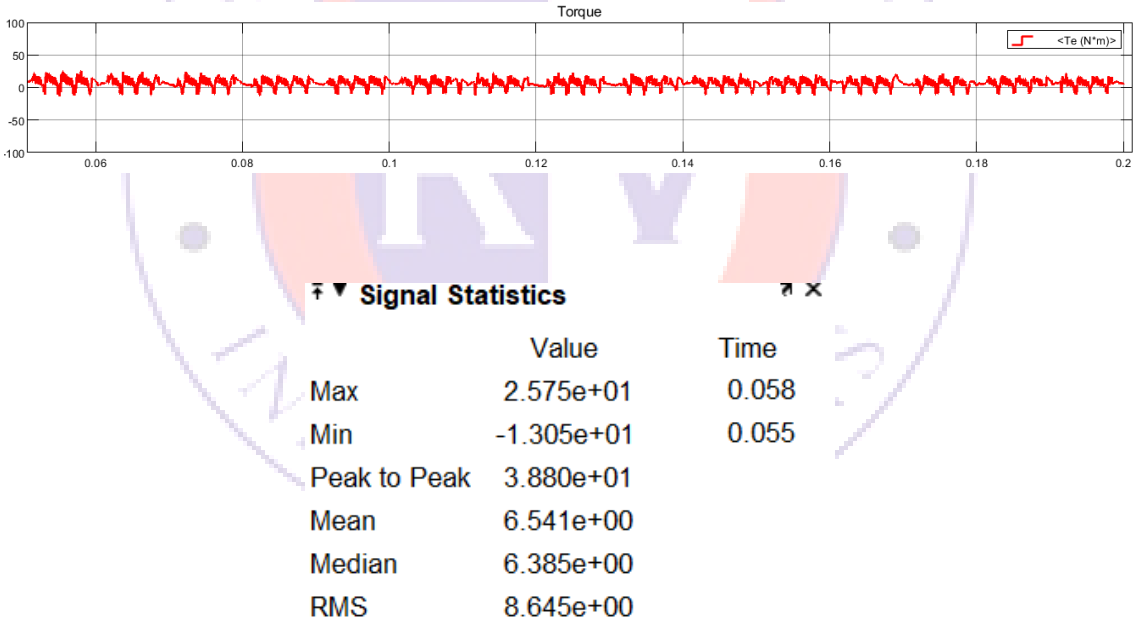


Fig. 6.4 (b) Torque waveform with signal statistics at 1200rpm using proposed converter

A capacitor filter is added in parallel to the rectifier circuit to minimize the ripple content in the supply. The torque ripple is also considerably reduced because of this inclusion. The output waveforms including capacitor in the rectifier circuit is illustrated in Fig. 6.5.

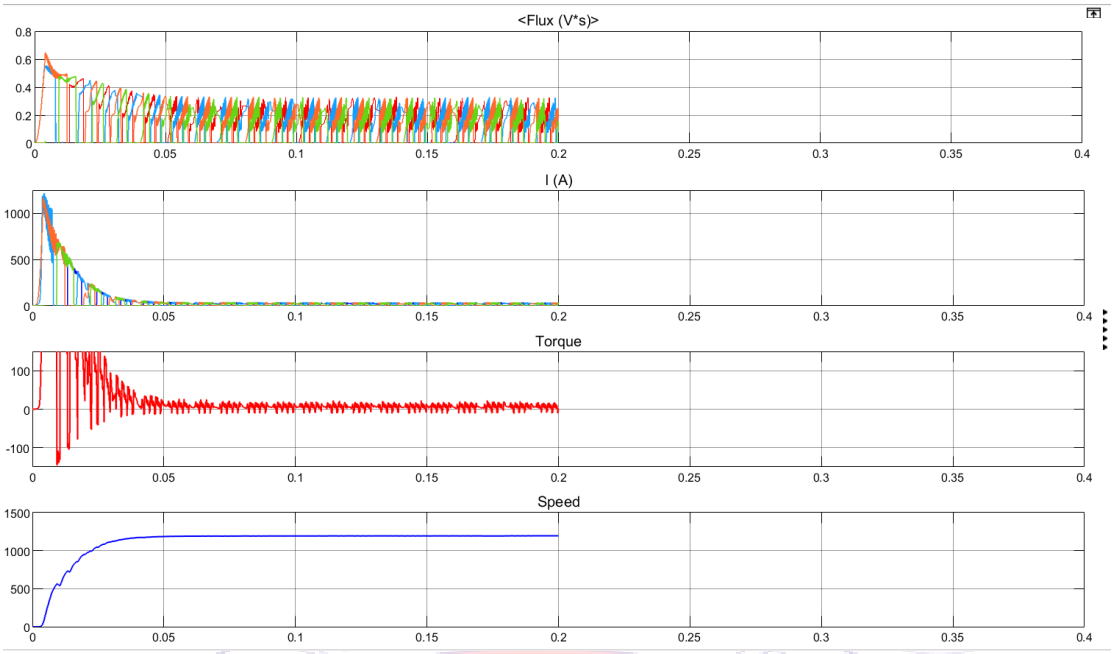


Fig. 6.5 Output waveforms at 1200rpm using proposed converter including filter capacitor

The torque waveform of the proposed converter including filter capacitor along with the signal statistics at 1200 rpm is shown in Fig. 6.6. It can be inferred that the ripple in torque is considerably reduced by including filter capacitor.

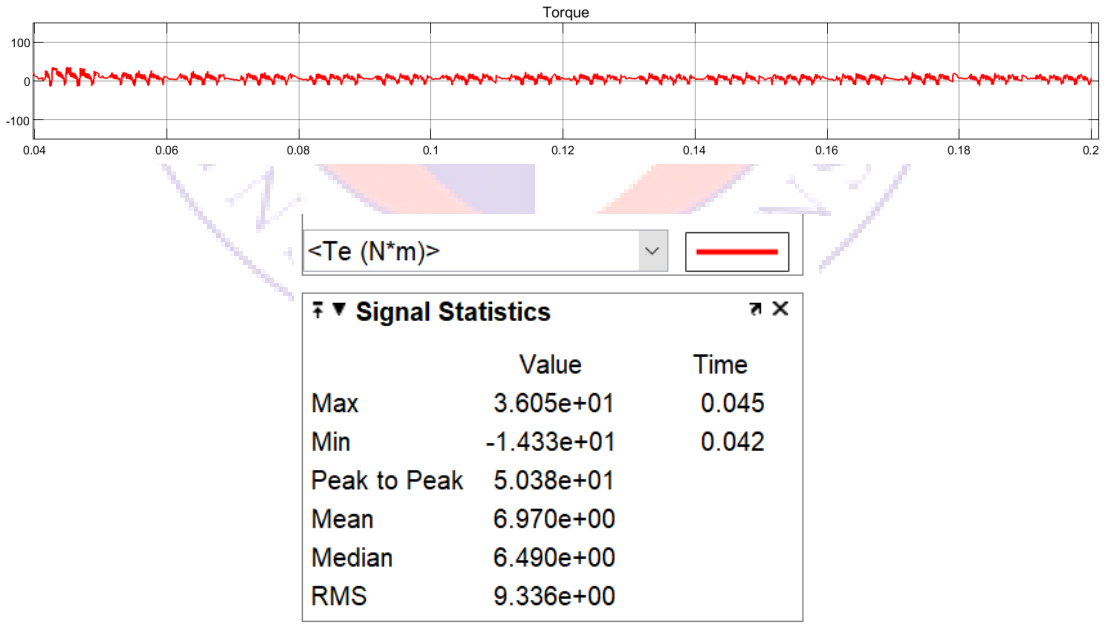


Fig. 6.6 Torque waveform with signal statistics at 1200rpm including filter capacitor

The torque waveform of the conventional converter along with the signal statistics at 1200rpm is shown in Fig. 6.7.

The proposed converter has lesser ripple content when compared to conventional converters.

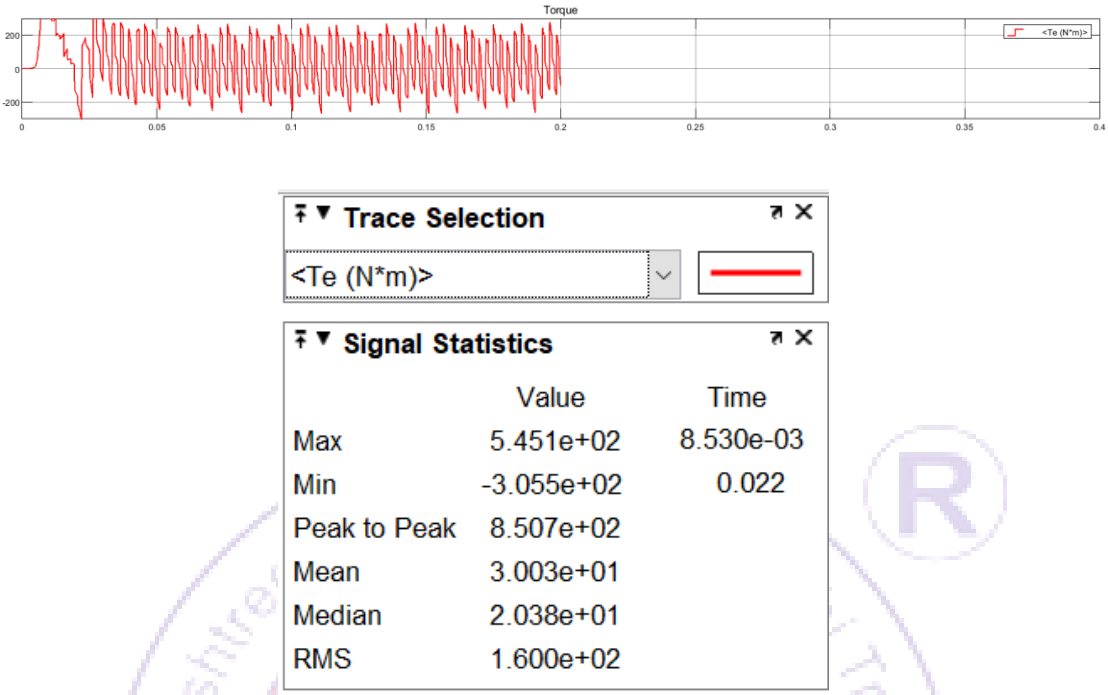


Fig. 6.7 Torque waveform with signal statistics at 1200rpm using conventional converter

The torque hysteresis controller provides the switching signals to the switches in each leg of the converter so as to magnetize the required phase appropriately. The output pulses of the controller to each leg of the converter is illustrated in Fig. 6.8.

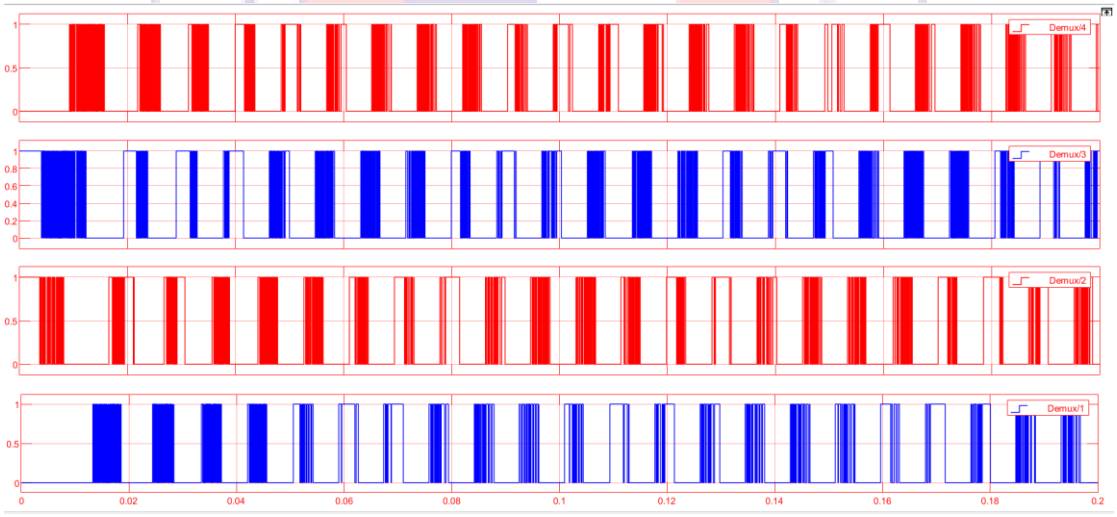


Fig. 6.8 Output pulses of torque hysteresis controller

6.2 Hardware results

The input and output waveforms of the hardware implementation as seen using a DSO are illustrated in Fig. 6.9 and Fig. 6.10 respectively.

Input voltage: 12V, 50Hz

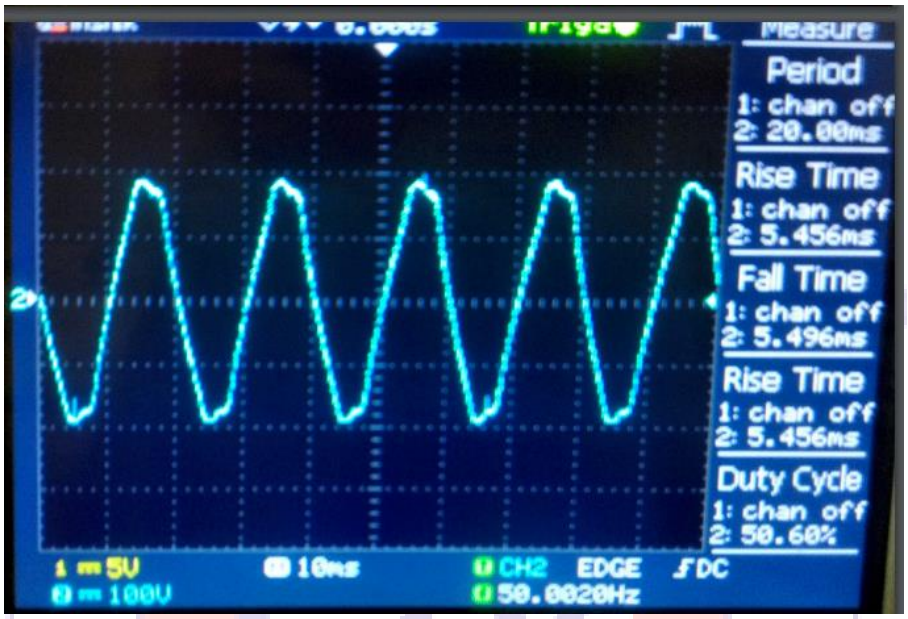


Fig. 6.9 Input voltage to the converter

When one of the phases of the stator are magnetized, the other phases are demagnetized. All phases are sequentially magnetized. In the Fig. 6.7, phase A is magnetized. During the time phase A is demagnetized, the remaining phases, phases B, C and D are magnetized.

Fig. 6.10 Output voltage of the converter

6.3 Numerical results

With conventional asymmetric half bridge converter:

Source	:	310V
Speed	:	1500 rpm
Stator poles	:	8
Rotor poles	:	6

Torque ripple = [(Tmax – Tmin)/Tavg]

Torque ripple at 1200 rpm

Average torque ripple	:	28

With proposed asymmetric half bridge converter:

Source	:	310V
Speed	:	1500 rpm
Stator poles	:	8
Rotor poles	:	6

Torque ripple = [(Tmax – Tmin)/Tavg]

Torque ripple at 900 rpm

Average torque ripple	:	6.169
Torque ripple at 1200 rpm		
Average torque ripple	:	5.931

The input to the hardware is 230V AC stepped down to 12V. the input to the converter is 12V DC. The output voltage observed is 12V for every phase consecutively.

6.3 Summary

The results of the simulation model in MATLAB Simulink were discussed including analysis of the waveforms. The voltage output of the hardware implementation was also analyzed.

Chapter 7

CONCLUSION AND FUTURE SCOPE

The primary control challenge with an SRM is the generation of torque that is ripple free. Presence of torque ripple causes undesired vibration and noise to be produced during the operation of the machine. The degree of torque ripple during operation is determined by the static properties and magnetization patterns of the various phases.

Various control methods are available to reduce the torque ripple in SRMs. Among them, modified control circuits, converter circuits, and modified design of stator and rotor are extensively used. These methods minimize the torque ripple but negatively affect other parameters. Therefore, it becomes extremely necessary to select the appropriate control scheme considering the tradeoff. The proposed project consists of a novel asymmetric half bridge converter based for reduction in torque ripple in SRM drive.

7.1 Conclusion

The conclusions drawn from the simulation and hardware analysis of the project are as stated.

- The simulation of Novel Asymmetric Half Bridge Converter is simulated using MATLAB Simulink software. The simulation results obtained using the proposed converter are compared with the results of the conventional Asymmetric Half Bridge Converter.
- The percentage of torque ripple obtained with proposed converter is 5.931 which is less when compared to the percentage of torque ripple obtained using conventional converter, i.e., 28.
- The proposed converter inherently improves the power factor as it distributes the current causing its amplitude to decrease.
- The hardware prototype of the proposed converter has been implemented for open loop operation. The input and the output are in accordance with theoretical expectations.

7.2 Future scope

The proposed project paves way for research to be conducted in the following aspects.

- Closed loop implementation of the converter must be carried out to better analyze the reduction in torque ripple.

- Research must be carried out to reduce the number of power electronics components required so that the converter is size and cost optimized.

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Appendix A

Datasheets

UTC **UNISONIC TECHNOLOGIES CO., LTD**

4N60 *Power MOSFET*

4 Amps, 600 Volts
N-CHANNEL POWER MOSFET

TO-220

TO-220F

*Pb-free plating product number: 4N60L

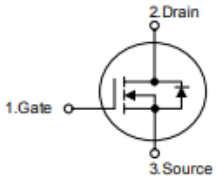
■ DESCRIPTION

The UTC 4N60 is a high voltage MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

■ FEATURES

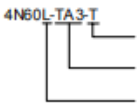
* $R_{DS(ON)}$ = 2.5Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 15 nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 8.0 pF)
* Fast switching capability
* Avalanche energy Specified
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
4N60-TA3-T	4N60L-TA3-T	TO-220	G	D	S	Tube
4N60-TF3-T	4N60L-TF3-T	TO-220F	G	D	S	Tube



(1) T: Tube, R: Tape Reel
(2) TA3: TO-220, TF3: TO-220F
(3) L: Lead Free Plating Blank: Pb/Sn

4N60 *Power MOSFET*

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	600	V
Gate-Source Voltage		V_{GSS}	±30	V
Avalanche Current - (Note 1)		I_{AR}	4.4	A
Continuous Drain Current	T_C = 25°C	I_D	4.0	A
	T_C = 100°C		2.8	A
Pulsed Drain Current, T_P Limited by T_{JMAX} - (Note 1)		I_{DM}	16	A
Avalanche Energy, Single Pulsed (Note 2)		E_{AS}	260	mJ
Avalanche Energy, Repetitive, Limited by T_{JMAX}		E_{AR}	10.6	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Power Dissipation (T_C = 25°C)		P_D	106	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient	θ_{JA}			62.5	°C/W
Junction-to-Case	θ_{JC}			3	°C/W
Case-to-Sink	θ_{CS}		0.5		°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	600			V
Drain-Source Leakage Current		I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V			10	μA
			V_{DS} = 480 V, T_C = 125°C			100	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
	Reverse		V_{GS} = -30 V, V_{DS} = 0 V			-100	nA
Breakdown Voltage Temperature Coefficient		$\triangle BV_{DSS}/\triangle T_J$	I_D = 250 μA, Referenced to 25°C		0.6		V/°C
On Characteristics							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0		4.0	V
Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 2.2 A			2.5	Ω
Forward Transconductance		g_{FS}	V_{DS} = 50 V, I_D = 2.2 A (Note 4)		4.0		S
Dynamic Characteristics							
Input Capacitance		C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz		520	670	pF
Output Capacitance		C_{OSS}			70	90	pF
Reverse Transfer Capacitance		C_{RSS}			8	11	pF
Switching Characteristics							
Turn-On Delay Time		$t_{D(ON)}$	V_{DD} = 300V, I_D = 4.0 A, R_G = 25Ω (Note 4, 5)		13	35	ns
Turn-On Rise Time		t_R			45	100	ns
Turn-Off Delay Time		$t_{D(OFF)}$			25	60	ns
Turn-Off Fall Time		t_F			35	80	ns
Total Gate Charge		Q_G	V_{DS}= 480V, I_D= 4.0A, V_{GS}= 10 V (Note 4, 5)		15	20	nC
Gate-Source Charge		Q_{GS}			3.4		nC
Gate-Drain Charge		Q_{DD}			7.1		nC

■ **ELECTRICAL CHARACTERISTICS(Cont.)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source- Drain Diode Ratings and Characteristics						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 4.4 A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				4.4	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				17.6	A
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 4.4 A,		250		ns
Reverse Recovery Charge	Q_{RR}	dI_F/dt = 100 A/μs (Note 4)		1.5		μC

Notes: 1. Repetitive Rating : Pulse width limited by T_J
2. L = 25mH, I_{AS} = 4.4A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 4.4A, di/dt ≤200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

TOSHIBA TLP250

TOSHIBA Photocoupler GaAlAs Ired & Photo−IC

TLP250

Transistor Inverter
Inverter For Air Conditionor
IGBT Gate Drive
Power MOS FET Gate Drive

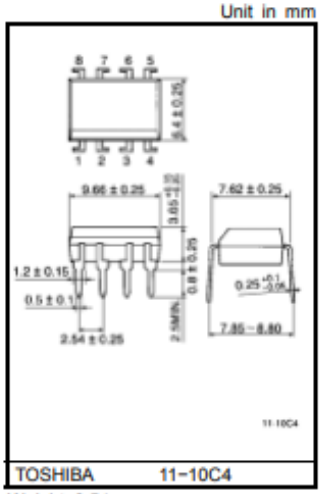
The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
This unit is 8−lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: I_F=5mA(max.)
- Supply current (I_{CC}): 11mA(max.)
- Supply voltage (V_{CC}): 10−35V
- Output current (I_O): ±1.5A (max.)
- Switching time (t_{pLH}/t_{pHL}): 1.5μs(max.)
- Isolation voltage: 2500V_{rms}(min.)
- UL recognized: UL1577, file No.E67349
- Option (D4) type
  VDE approved: DIN VDE0884/06.92,certificate No.76823
  Maximum operating insulation voltage: 630V_{PK}
  Highest permissible over voltage: 4000V_{PK}

(Note) When a VDE0884 approved type is needed, please designate the "option (D4)"

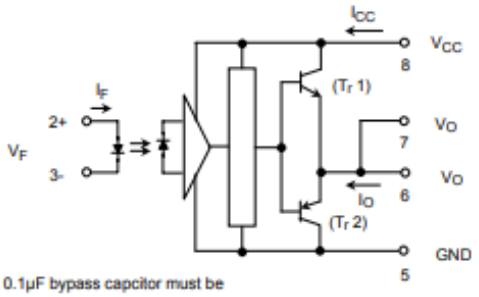
- Creepage distance: 6.4mm(min.)
  Clearance: 6.4mm(min.)

Unit in mm



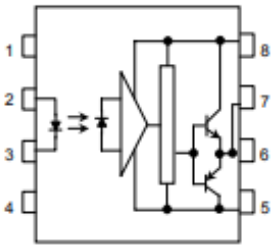
TOSHIBA 11−10C4
Weight: 0.54 g

Schmatic



A 0.1μF bypass capcitor must be connected between pin 8 and 5 (See Note 5).

Pin Configuration (top view)



1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : V_O (Output)
7 : V_O
8 : V_{CC}

Truth Table

		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On

TOSHIBA TLP250

Absolute Maximum Ratings (Ta = 25°C)

	Characteristic		Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 70°C)		$\Delta I_F / \Delta Ta$	−0.36	mA / °C
	Peak transient forward curent	(Note 1)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Junction temperature		Tj	125	°C
Detector	"H"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPH}	−1.5	A
	"L"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPL}	+1.5	A
	Output voltage	(Ta ≤ 70°C)	V_O	35	V
		(Ta = 85°C)		24	
	Supply voltage	(Ta ≤ 70°C)	V_{CC}	35	V
		(Ta = 85°C)		24	
	Output voltage derating (Ta ≥ 70°C)		$\Delta V_O / \Delta Ta$	−0.73	V / °C
	Supply voltage derating (Ta ≥ 70°C)		$\Delta V_{CC} / \Delta Ta$	−0.73	V / °C
	Junction temperature		Tj	125	°C
Operating frequency		(Note 3)	f	25	kHz
Operating temperature range			T_{opr}	−20~85	°C
Storage temperature range			T_{stg}	−55~125	°C
Lead soldering temperature (10 s)		(Note 4)	T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H.≤ 60%)		(Note 5)	BV_S	2500	Vrms

Note 1: Pulse width P_W ≤ 1μs, 300pps

Note 2: Exporenential wavefom

Note 3: Exporenential wavefom, I_{OPH} ≤ −1.0A(≤ 2.5μs), I_{OPL} ≤ +1.0A(≤ 2.5μs)

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considerd a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 6: A ceramic capacitor(0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching proparty. The total lead length between capacitor and coupler should not exceed 1cm.

Recommended Operating Conditions

Characteristic		Symbol	Min.	Typ.	Max.		Unit
Input current, on	(Note 7)	$I_{F(ON)}$	7	8	10		mA
Input voltage, off		$V_{F(OFF)}$	0	—	0.8		V
Supply voltage		V_{CC}	15	—	30	20	V
Peak output current		I_{OPH}/I_{OPL}	—	—	±0.5		A
Operating temperature		T_{opr}	−20	25	70	85	°C

Note 7: Input signal rise time (fall time) < 0.5 μs.

TOSHIBA TLP250

Electrical Characteristics (Ta = –20~70°C, unless otherwise specified)

Characteristic		Symbol	Test Cir-cuit	Test Condition		Min.	Typ.*	Max.	Unit
Input forward voltage		V_F	—	I_F = 10 mA , Ta = 25°C			1.6	1.8	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta Ta$	—	I_F = 10 mA		—	–2.0	—	mV / °C
Input reverse current		I_R	—	V_R = 5V, Ta = 25°C			—	10	μA
Input capacitance		C_T	—	V = 0 , f = 1MHz , Ta = 25°C		—	45	250	pF
Output current	"H" level	I_{OPH}	3	V_{CC} = 30V (*1)	I_F = 10 mA V_{8-6} = 4V	–0.5	–1.5	—	A
	"L" level	I_{OPL}	2		I_F = 0 V_{6-5} = 2.5V	0.5	2	—	
Output voltage	"H" level	V_{OH}	4	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, I_F = 5mA		11	12.8	—	V
	"L" level	V_{OL}	5	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, V_F = 0.8V		—	–14.2	–12.5	
Supply current	"H" level	I_{CCH}	—	V_{CC} = 30V, I_F = 10mA Ta = 25°C		—	7	—	mA
				V_{CC} = 30V, I_F = 10mA		—	—	11	
	"L" level	I_{CCL}	—	V_{CC} = 30V, I_F = 0mA Ta = 25°C		—	7.5	—	
				V_{CC} = 30V, I_F = 0mA		—	—	11	
Threshold input current	"Output L→H"	I_{FLH}	—	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, V_O > 0V		—	1.2	5	mA
Threshold input voltage	"Output H→L"	I_{FHL}	—	V_{CC1} = +15V, V_{EE1} = –15V R_L = 200Ω, V_O < 0V		0.8	—	—	V
Supply voltage		V_{CC}	—			10	—	35	V
Capacitance (input–output)		C_S	—	V_S = 0 , f = 1MHz Ta = 25°C		—	1.0	2.0	pF
Resistance(input–output)		R_S	—	V_S = 500V , Ta = 25°C R.H.≤ 60%		1×10^{12}	10^{14}	—	Ω

* All typical values are at Ta = 25°C (*1): Duration of I_O time ≤ 50μs

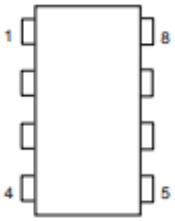
Switching Characteristics (Ta = –20~70°C , unless otherwise specified)

Characteristic		Symbol	Test Cir-cuit	Test Condition	Min.	Typ.*	Max.	Unit
Propagation delay time	L→H	t_{pLH}	6	I_F = 8mA (Note 7) V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω	—	0.15	0.5	μs
	H→L	t_{pHL}			—	0.15	0.5	
Output rise time		t_r			—	—	—	
Output fall time		t_f			—	—	—	
Common mode transient immunity at high level output		C_{MH}	7	V_{CM} = 600V, I_F = 8mA V_{CC} = 30V, Ta = 25°C	−5000	—	—	V / μs
Common mode transient immunity at low level output		C_{ML}	7	V_{CM} = 600V, I_F = 0mA V_{CC} = 30V, Ta = 25°C	5000	—	—	V / μs

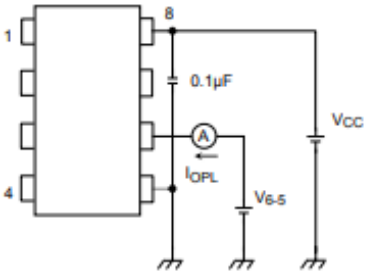
* All typical values are at Ta = 25°C

Note 7: Input signal rise time (fall time) < 0.5 μs.

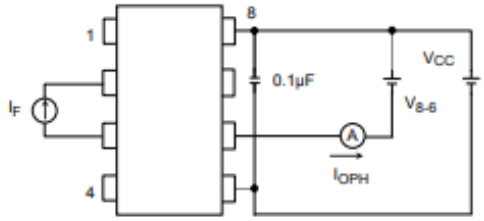
Test Circuit 1 :



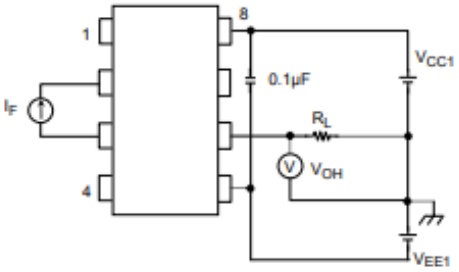
Test Circuit 2 : IOPL



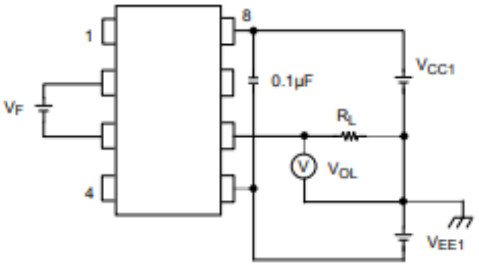
Test Circuit 3 : IOPH



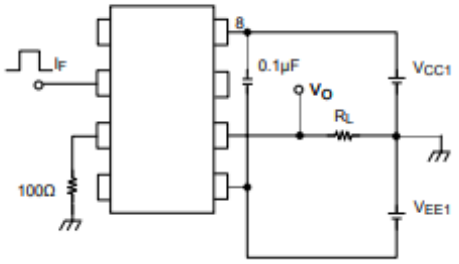
Test Circuit 4 : VOH

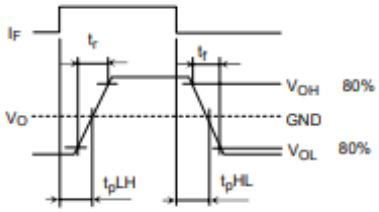


Test Circuit 5 : V_{OL}

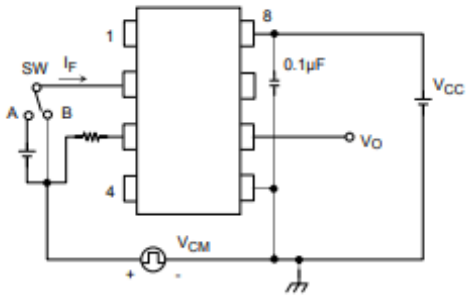


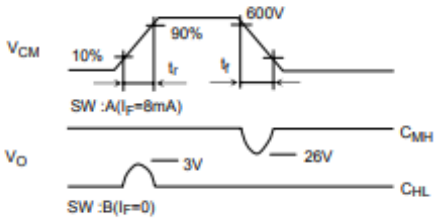
Test Circuit 6: t_{pLH}, t_{pHL}, t_r t_f





Test Circuit 7: C_{MH}, C_{ML}



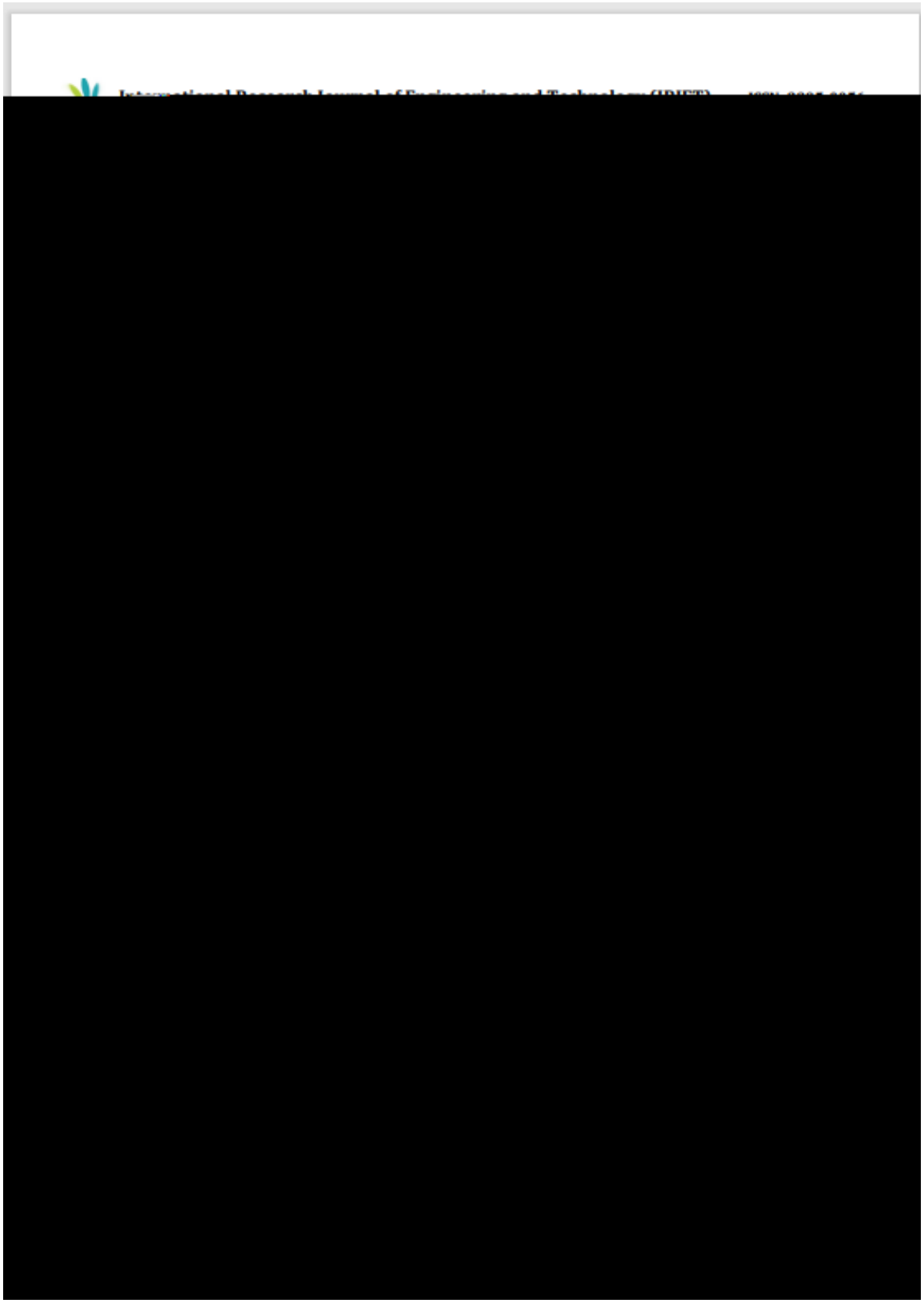


$$C_{ML} = \frac{480\ (V)}{t_{r\ (\mu s)}}$$

$$C_{MH} = \frac{480\ (V)}{t_{f\ (\mu s)}}$$

C_{ML}(C_{MH}) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

Design and Implementation of technique for suppression of torque ripple in SRM drive
Shambhavi K N and 18MPE41
M.Tech in Power Electronics, Department of Electrical Engineering
R.V College of Engineering, Bangalore - 560059, INDIA
Objective
Design and implementation of power converter for reduction in torque ripple of Switched Reluctance Motor and comparision of simulation result of ripple content with and without the proposed converter.
Project Methodology
The basic principle is to select proper voltage vectors using a pre-defined switching table. The torque is thus controlled by varying the relative angle between the stator flux and the rotor flux. Thus, the torque can be almost instantaneous controlled by accelerating, decelerating or stopping the rotation of the stator flux vector relative to the rotor flux vector, which can be assumed to remain unchanged during the control action.
Block diagram
Switching table
Circuit diagram
Working principle :
For the phases, the typical structure of the asymmetric converter is used.
When the torque is reducing or when a phase is being excited, the additional IGBT is activated and both capacitors connect to the excited phase which causes the phase voltage to increase.
In other times the AC source provides the phase voltage, and in this way, the power factor is improved.
When the meter is operating at high-speed operating points and the back-emf voltage is high, the total torque and current will decrease.
When torque is inside its band and the voltage of C1 is less than the voltage of the ac source, the source provides the required voltage and the converter drains current from the source.
If the torque becomes less than a specific amount, C1
Results and Discussions
Rectifier output : 310 V
Torque waveform at 1200rpm using conventional converter
Torque waveform at 900rpm using proposed converter
Signal statistics
At 900rpm
Signal Statistics
Value Time
Max 1.929e+01 0.052
Min -1.127e+01 0.051
Peak to Peak 3.057e+01
Mean 4.953e+00
Median 5.213e+00
RMS 6.534e+00
Torque waveform at 1200rpm using proposed converter
At 1200rpm
Signal Statistics
Value Time
Max 2.575e+01 0.058
Min -1.305e+01 0.055
Peak to Peak 3.880e+01
Mean 6.541e+00
Median 6.385e+00
RMS 8.645e+00
Result
With conventional asymmetric half bridge converter:
Source : 310V
Speed : 1500 rpm
Stator poles : 8
Rotor poles : 6
Torque ripple at 1200 rpm : 28
With proposed asymmetric half bridge converter:
Source : 310V
Speed : 1500 rpm
Stator poles : 8
Rotor poles : 6
Torque ripple at 900 rpm
Average torque ripple % : 4.12
Torque ripple at 1200 rpm
Average torque ripple % : 5.931



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- Phase overlap control must be permitted.
- The energy from demagnetization must be utilized by sending it back to source and/or using it in next phase.
- Sufficient high negative voltage must be generated to demagnetize the off going phase quickly thereby reducing demagnetization time.
- Switching frequency and its losses must be mitigated by operating in freewheeling mode.
- High positive voltage excitation must be given to increase the phase current so that output power is improved.

2. CLASSIFICATION OF POWER CONVERTER TOPOLOGIES

Power converters for SRM drives are classified mostly depending on the type of switching employed. There are two categories based on the type of switching: Hard switched converters and Soft switched converters. The sub types in each of these categories is illustrated in Fig. 2.1.

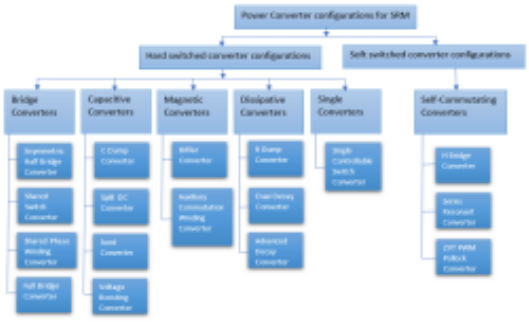

Fig – 2.1: Classification of power converter topologies

3. BRIDGE CONVERTERS

These converter topologies consist of diodes and switches. They are basically derived from H-Bridge converter topology and stand out owing to their simple structure and controllability. The different types of Bridge Converters are explained below with their circuit diagrams, benefits, and drawbacks.

3.1 Asymmetric Half Bridge Converter

In this type of converter configuration, if there are q motor phases, the converter consists of 2q active switches. The circuit of the same is as shown in Fig. 3.1. When soft switched, the converter provides for operation in 3 different modes: Magnetization, Demagnetization and Free-wheeling mode. When hard switched, it operates in only two, i.e., Magnetization and Demagnetization modes.

Advantages:

- Maximum flexibility as the upper and lower switches can be controlled independently.
- The converter has the same efficiency in Magnetisation mode as in case of Demagnetisation mode.
- The winding is in series between the two switches. Thus, in case of a short circuit fault, the inductance of the windings limits the current rise thereby providing sufficient time to the protective devices to locate and isolate the fault.

Disadvantages:

- The number of power electronic devices per phase is high.
- In case of low voltage operations, the total forward voltage drop of the two switches may be significant when compared to the available DC voltage.
- Voltage ripple is very significant due to the magnetisation and demagnetisation of the phase winding which necessitates the use of a large capacitor to filter it out.

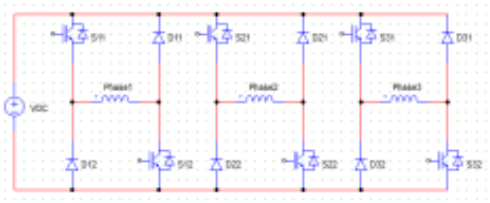

Fig – 3.1: Asymmetric half bridge converter

3.2 Shared Switch Converter

This converter configuration is similar to Asymmetric Half Bridge Converter but differs in the fact that the power electronic devices like the switch and the diode are shared between different phases in Shared Switch Converter unlike Asymmetric Half Bridge Converter. It is also called Miller Converter. The general version makes use of q+1 switches where q is the number of phases. Analogous to Asymmetric Half Bridge Converter, Shared Switch Converter operates in

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3 modes, Magnetization, Demagnetization and Freewheeling mode, when soft switched and in Magnetization and Demagnetization mode when hard switched. Fig. 3.2 represents a general Shared Switch Converter.

Advantages:

- The necessary number of power electronic devices is reduced.
- The number of power supplies required for driver circuits is less.

Disadvantages:

- Very limited freedom of operation and lesser fault tolerance as the operation of all phases depends considerably on the shared switch.
- When reversing the direction of the machine, the reference speed must be maintained at zero until all phase currents are zero and only then negative motion can be achieved.
- Significantly high switching stress on the shared switch.

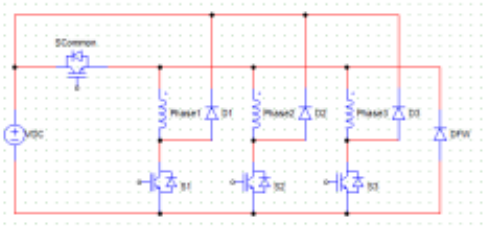

Fig – 3.2: Shared Switch Converter

3.3 Shared Phase Winding Converter

In this converter configuration, a single asymmetric half bridge converter is shared between 2 phases. It uses the same number of switches as the number of phases (q). Thyristors are used to steer current into the desired phase but not for control. This configuration is particularly useful for SRMs with even number of phases. Freewheeling mode can be achieved by making use of diodes. This converter can be operated with both soft switched and hard switched approaches. The circuit representation of the same is shown in Fig. 3.3.

Advantages:

- Independent control of phase current is possible because of freewheeling diode.
- Lesser number of power electronic device and better utilization of each of them.
- Positive, negative and zero output can be obtained from the converter which allows greater current control flexibility.

Disadvantages:

- Very less fault tolerance.
- Even within the same half bridge, current overlap between phase windings is not possible.
- Inclusion of thyristors increases the cost as well as complexity of the circuit.

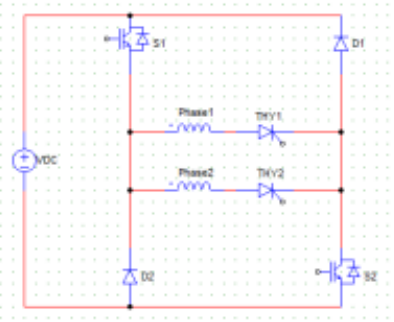

Fig – 3.3: Shared Phase Winding Converter

3.4 Full Bridge Converter

In this converter configuration, 4q switches are used where q is the number of phases, as shown in Fig. 3.4. This converter configuration is similar to half bridge converter except the usage of switches instead of diodes. Not unlike Asymmetric Half Bridge Converter, even this converter operates in 3 modes, Magnetization, Demagnetization and Freewheeling mode, when soft switched and Magnetization and Demagnetization mode when hard switched. The usage of switches reduces conduction and switching losses during Demagnetization and Freewheeling mode.

Advantages:

- This converter configuration provides improved control flexibility when working as motor and generator.
- During Demagnetisation mode and Freewheeling mode, the operational efficiency is sufficiently enhanced.

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Disadvantages:

- As the number of power electronics devices used is more, it suffers from underutilisation of devices.
- The cost of the converter is comparatively high because of the inclusion of more devices and the driving circuits corresponding to them.

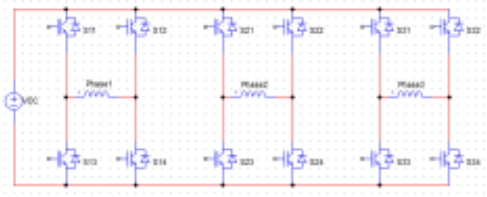

Fig – 3.4: Full Bridge Converter

3. CONCLUSIONS

A comprehensive review of different types of Bridge Converter circuits for SRMs has been discussed. Each of the topologies have their own merits and limitations. The choice of the converter mainly depends on the type of application and requirements. For automotive application, the Asymmetric Bridge Converter is advantageous because of its inherent scope for short circuit protection and greater fault tolerance. The performance in all three modes, namely, magnetization, Demagnetization and Freewheeling, is satisfactory. These benefits make up for the drawbacks associated. These are the reasons owing to which this configuration is widely accepted.

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Major Project: Phase-II Report

on

DESIGN AND IMPLEMENTATION OF BATTERY MANAGEMENT SYSTEM USING PASSIVE CELL BALANCING

18MPE41

Submitted by

YOGALAKSHMI R

USN: 1RV20EPE18

Under the Guidance

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Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY
in
POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

2021-22

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Certified that the project work titled "**Design and Implementation of Battery Management System using Passive Cell Balancing**" carried out by **Yogalakshmi R, USN: 1RV20EPE18**, a bonafide student of **RV College of Engineering, Bengaluru** in partial fulfilment for the award of **Master of Technology in Power Electronics** of **RV College of Engineering, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi**, during the year **2021-22**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

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DECLARATION

I, **Yogalakshmi R,** student of fourth semester M.Tech in **Power Electronics, Department of Electrical and Electronics Engineering,** RV College of Engineering, Bengaluru declare that the project titled **"Design and Implementation of Battery Management System using Passive Cell Balancing"**, has been carried out by me. It has been submitted in partial fulfilment of the course requirements for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

Date of Submission: 18-07-2022

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Signature of the Student

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This certificate is being awarded to Ms. Yogalakshmi R (**USN:** 1RV20EPE18), a student pursuing an M.Tech in Power Electronics from **R.V. College of Engineering** has done her internship with our Research and Development Department, Bangalore from the 1st of September 2021 to the 30th of June 2022.

Her Project Title is "Design and Implementation of Battery Management System using Passive Cell Balancing" and has completed the project under the guidance of Kappala Venkateswarlu, R&D.

During the tenure of the internship at Ampere, her conduct, character, and interest to learn were found good.

We wish her all the best in her future endeavors.

Thanks & regards,

Vithal Acharya
Head – Human Resources
Greaves Electric Mobility Pvt Ltd

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Yogalakshmi R

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ABSTRACT

Growing response for Electric Vehicles (EVs) across the world implies techno-economical efforts targeted to mitigate the challenges related to fossil fuels. Energy storage powering EVs is a very critical component. A battery pack used as energy storage in EVs uses many battery cells connected in series and parallel. These battery cells need close monitoring and management systems during EVs operation. Such systems are called as Battery Management System (BMS) that ensures a safe operating envelope while increasing battery power delivery capabilities and improving battery life. The cell voltage balancing along with the State of Charge (SOC) and State of Health (SOH) monitoring are some of the critical functions of BMS. Therefore, a Passive Cell balancing technique of Li-ion batteries is proposed.

The project work aimed at the design and develop of passive cell balancing circuit with the coulomb counting method of SOC estimation algorithm. The proposed Cell balancing circuit is formed by connecting a rechargeable lithium-ion battery in series. The excess charge is removed from over-charged cell by controlled operation of the power switches like MOSFETs. Switches are operated according to the control algorithm through an Arduino controller. If there is an unbalance between cells, the controller decides which switch should be turned ON, and the resistor gets shunted across that cell. The control algorithm was programmed in the Arduino-nano controller. The Proposed method was simulated using MATLAB/SIMULINK tool and a hardware prototype was realized for 3 cells of Lithium-ion using SOC estimation algorithm coded on Arduino-nano controller.

The passive cell balancing circuit of Li-ion batteries was designed and implemented. Experiments are carried out during the charging and discharging of battery cells. It can be observed that the voltages of the cells before charging where around 3.86V, 3.88V and 3.84V. And after balancing the voltages were approximately 3.87V, 3.87V, and 3.87V and with a SOC of around 87.02% Voltages of the cells before charging were around 3.80V, 3.83V and 3.79V. And after balancing the voltages approximately equal to 3.81V, 3.82V, and 3. 81V and with SOC of around 87%. These results showed that battery cell balancing and SOC estimation will be effectively achieved using Passive cell Balancing method. By developing a rule-based algorithm strategy based on fuzzy logic control the more accurate cell balancing can be achieved.

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GLOSSARY

ADC	Analog to Digital Converter
BMS	Battery Management System
CPU	Central Processing Unit
DSP	Digital Signal Processor
ESS	Energy Storage System
EV	Electric Vehicle
IDE	Integrated Development Environment
SOC	State of Charge
SOH	State of Health

Chapter 1

INTRODUCTION

In the recent years Electric Vehicles (EV's) have gained considerable popularity mainly attractive due to the integration of much intelligent and energy-efficient eco-friendly technology, thereby addressing bigger problems associated with fossil fuels. As EV technology is evolving, many of the components and subsystems of are improving as advanced technologies. Besides that, most difficulties are witnessed in the improving of Energy Storage Sources (ESS) [1]. ESS plays a critical function within the fields of EVs. The frequently used ESS in EV's is a battery pack. Li-ion batteries are more advantages as compared to the opposing rechargeable batteries like Lead-acid, Li-ion, NiCad, Ni-MH, etc. Li-ion batteries gain advantages such as fast charging, high energy density, prolonged existence, low self-discharge rate, comparatively low maintenance, etc [2]. These batteries supply substantial amounts of current for high-energy applications. Li-ion battery cell holds the nominal voltage of 3.7V, maximum voltage of 4.2V and minimum voltage of 2.7V. If the battery cell is overcharged to over 4.2V or discharged to 2.7V, this will result in unstable battery condition and even causes fire hazard [3]-[4].

Hence, the balancing of the battery pack is necessary to maintain the efficiency and safety of BMS. Balancing methods are frequently classified into two types. That is Active cell balancing and Passive cell balancing. The active cell balancing method, the cell consisting of more of charge is moved to the other battery cells with the least amount of charge, to eliminate the variations occurring in the battery pack by the utilization of passive components such as inductors and capacitors. The active balancing method of charge equalization is capable to accomplishing high energy consumption, but the complex circuit design, and high cost [5]-[7]. The Passive cell balancing method, the additional charge is dissipated through a resistor. These resistors are positioned in series to the battery cell [8]-[11]. This method of charge equalization is simple, convenient, adaptable, and cost efficient. The disadvantages of this method include waste of energy and generate inconvenience to thermal management [11]-[15].

A precise SOC estimation of each battery in a battery pack is necessary for the effective functioning BMS. Multiple strategies for the evaluation of SOC and

different cell balancing methods are proposed in the literature. These are grouped into numerous types, including direct methods, Book-keeping methods, model-based methods, etc. An important method of estimation SOC utilizing Coulombs counting is considered. The BMS using passive cell balancing that is based on Arduino-nano controller is selected.

1.1 Specific Details

Battery Management System using Passive Cell Balancing Circuit is to be design for Electric Vehicle Applications. The voltage of the Li-ion battery cell ranges from 2.6V to 4.2V, with a nominal voltage of 3.7V. The bleeding resistor's value is decided by the resistor's allowed average power loss and the desired rate of cell balancing. In this circuit, 10Ω bleeding resistors are connected in series with the battery via a MOSFET switch BS170. The MOSFET is switched using an Optocoupler circuit based on the 4N35. The Arduino-nano controller is employed for the control of switches. The current through the battery pack is measured using ACS712 current sensor and the voltage of a cell is determined by the integral Analog to Digital converter (ADC) of the Arduino-nano controller.

1.2 Literature Survey

The demand for EVs is increasing gradually. Li-ion batteries are widely used as ESS for EVs. The work presents the comparison of constant current charging technique against the constant voltage charging technique. And the observations are made that the constant current charging technique is most suitable for changing of Li-ion battery cells. The simulation is performed using 2 cells using MATLAB. The cells require 3700secs to perform the cell balancing using switching of MOSFET [1].

Battery energy storage plays a vital role in powering EVs. These battery packs can connect either in series or parallel. The battery cell voltage, SOC, and State of Health (SOH) need to be closely monitored and controlled during its operation [2]-[3]. The work illustrates design and implementation of passive cell balancing circuit for Lithium-Iron-Phosphate (LiFePO4) battery pack supported on TMS320F28379D DSP controller. Simulations and hardware prototype were developed, and the results are verified to determine the coulombs counting method of SOC estimation on the passive cell balancing technique [4].

The significance of BMS in passive cell balancing including Li-ion battery pack is presented [5]-[6]. The equivalent circuit battery modelling and the waveforms during charge and discharge of battery cells are illustrated using the equivalent circuit model. The passive balancing using switched resistor method is the focused [7]. The advantages and disadvantages of Active balancing is also discussed to provide the selection of passive balancing technique. MATLAB Simulation is performed for developing of a single cell and four cells of a battery pack [8].

The proposed BMS with passive cell balancing topology incorporated with power resistors is used to remove excess amount of energy from a LiFePO4 battery cell. The experiment was performed on 15 cells connected in series for charging procedures [9]. The results show that the BMS is able to maintain the equal cell voltages corresponding to the reference balancing voltage. As there is a larger difference between the cell with the largest capacity and the smallest capacity, it takes long time to balance. Active cell balancing can compensate for the short-comings of passive cell balancing [10].

Lithium-ion batteries are widely used in large ESS and EVs, as well as other disciplines, because to the superior performance [11]-[13]. The current ratio and SOC level of the individual battery cells in a battery pack have a direct impact on the battery during charging and discharging conditions. The charging and discharging characteristics are examined for passive cell balancing factors [14]. The capacity available in the battery pack reduces as the current in the circuit increases. The balancing capacity ratio equals the balancing current ratio. As a result, increasing the current balancing ratio increases the effect of passive balancing. The capacity gap between single cells is wide, and the balancing effect becomes more precise. The balancing time ratio decreases as the balancing threshold decreases [15].

This report examines the Active cell balancing approach to that of Passive cell balancing approach [16]-[19]. The experimental results demonstrate that whenever the cell has a 10% higher SOC than the other three cells, the energy loss for balancing the circuit is minimized from 2.3 to 0.84 %. The simulation is carried out using MATLAB for Passive cell balancing and Active cell balancing [20]-[23]. It is noticed that with a balancing current of 0.28 reduces the voltage deviation of the greatest capacity of the battery cell in each charge. If the passive cell balancing approach is

applied, the outcome is high power dissipation before the module. In active cell balancing topology, it can reduce power loss to 4 to 4.6W [24].

This document gives a cell balancing algorithm for the BMS, is regarded as one of the fundamental technologies for the Li-ion battery pack in the automobile industry [25]. The outlier detection distance technique designed two parameters voltage and current, to determine unbalanced cell voltages and irregular cell voltages. Unbalanced cells were identified and balanced using a shunt approach with MOSFET switches by the proposed balancing algorithms. The outlier identification equalisation technique can reliably identify abnormal battery cells and boost operating energy and battery pack lifetime after validating the efficiency of the cell balancing procedures using MATLAB simulation [26]-[27].

The estimation of battery SOC is one of the crucial constraints used by the BMS. It is one of the important factors for the functioning of the EVs [28]-[30]. The work presents the comparison of the current based coulomb-counting approach, the voltage dependent modular based approach, and the mixed algorithms that is combination of the two approaches that are SOC estimation algorithms. These models has been created and simulated in MATLAB. It is observed that the Voltage and current data are appropriate under short-circuit and open circuit conditions [31].

The research in the equalization of voltages in the series string of the battery cells in electric vehicles gains more importance in resent trends [32]. The work presents the equalization control through shunt transistor method. As compared to other techniques, this method has the advantages of easy modularization, low cost, and complexity. Speed is increased by avoiding the highly charged cells during EVs charging, that improves efficiency. The simulation research demonstrates that the more the current avoided by the MOSFET switch, the more frequently the battery is charged and discharged. The hardware prototype has been developed. The result shows the current management for the charge equalization process [33].

The Unbalanced cells in a battery pack can result in a variation in cell voltages and a decrease in capacity and lifetime [34]. This study examined the passive cell balancing approach over fixed shunting resistor circuit against switching shunting resistor circuit. And active cell balancing using capacitor, inductor, or transformer. According to the observations, the passive cell balancing approach is simple to adopt

despite the lengthy balancing period. This is also appropriate for low-powered systems. Active cell balancing, on the other hand, requires less balancing time than passive cell balancing. Even though it requires complex control algorithms and a significant cost to assemble the cell balancing circuit [35].

1.3 Motivation

BMS using passive balancing is extensively employed in industries. For low power applications, the control mechanism using passive cell balancing is easy to implement with small size and inexpensive. It is appropriate for Hybrid Electric Vehicles as well as Electric Vehicles. There are numerous ways for estimating SOC, such as open circuit voltage calculation and terminal voltage calculation. However, these approaches require a thorough understanding of the battery's RC properties. On the other hand, SOC calculation through Coulomb Counting does not involve a comprehensive study of battery properties and thus has a basic structure and simple implementation.

1.4 Problem Definition

Design and development of a passive cell balancing circuit considering the various features of the battery pack during different variable working conditions integrated through the efficient controller for 3 cells of Li-ion battery pack, the hardware prototype of the passive cell balancing circuit is to be realized with SOC estimation algorithm.

1.5 Objectives

The main objective of the project is to design and implement Battery Management System using Passive Cell Balancing method through these steps:

- To design a passive cell balancing circuit to protect the Li-ion battery cells from the uneven voltages and SOC.
- To develop a SOC estimation algorithm using Coulomb counting method.
- To simulate proposed the Passive Cell Balancing circuit using MATLAB.
- To develop hardware prototype of Passive Cell Balancing circuit for 3 cells of Li-ion battery cells through the Coulomb counting method of SOC estimation coded on Arduino-nano controller.

1.6 Organization of Thesis

The project report consists of total seven chapters. An introduction to each phase in developing the work is listed as follows.

Chapter- 1: Consists of a literature survey that was carried out to understand the different types of cell balancing methods, the drawbacks and the advantages of passive cell balancing. It includes the problem definition, objectives of the project, motivation behind carrying out this project.

Chapter- 2: This chapter discusses the theory and concepts of different battery cell balancing and SOC estimation techniques.

Chapter-3: This chapter consists of the block diagram, methodology and flow of the proposed work in detail.

Chapter-4: Involves the design of the passive cell balancing circuit and the specifications of the components are described.

Chapter-5: Consists of the simulation analysis of the proposed work, hardware components used for the implementation and the hardware implementation is depicted.

Chapter-6: Discusses about the simulation results obtained during charging and discharging conditions, Passive cell balancing, SOC estimation and the hardware implementation results.

Chapter -7: Includes the overall conclusion drawn from the project and the future works that is carried out.

Followed by References consisting of list of papers referred for understanding and analysing the project work.

Chapter 2

CELL BALANCING AND SOC ESTIMATION METHODS

The fundamentals of Cell balancing techniques and optimize method for automotive application are discussed in this chapter. The Coulomb counting Method of SOC Estimation is also discussed.

2.1 Cell Balancing Methods

Cell balancing is the process of using passive components to balance the voltages of the cells in the battery pack after each charging and discharging cycle. This is performed by either discharging or transferring the charge from one cell to another. This is crucial because any fluctuations in the cell voltages after charging or discharging would cause the pack voltage to fluctuate from the nominal value, providing an inaccurate image of the entire pack's SOC. Additionally, if cell voltages are not evaluated and balanced, a few cells may be overcharged or undercharged, so that is extremely hazardous [6]. Cell balancing methods are classified into two types: passive cell balancing and active cell balancing.

2.1.1 Active Cell Balancing

Active balancing does not dissipate energy with a resistor; rather it stores or transfers the excess amount of energy from one cell to another. Figure 2.1 illustrates the circuit diagram of Active Cell Balancing. This is accomplished using switched capacitors by storing energy in it and transferring the stored energy into a lower voltage cell. Energy is transferred via a transformer in the Flyback technique. The primary side of the transformer is linked to the pack, and each cell is connected to the secondary side separately, it is divided into several sections to give the needed Voltage to the cells. Because transformers do not operate on direct current, switches are used to convert continuous direct current into pulsated direct current. It is then use to activate the transformers [14].

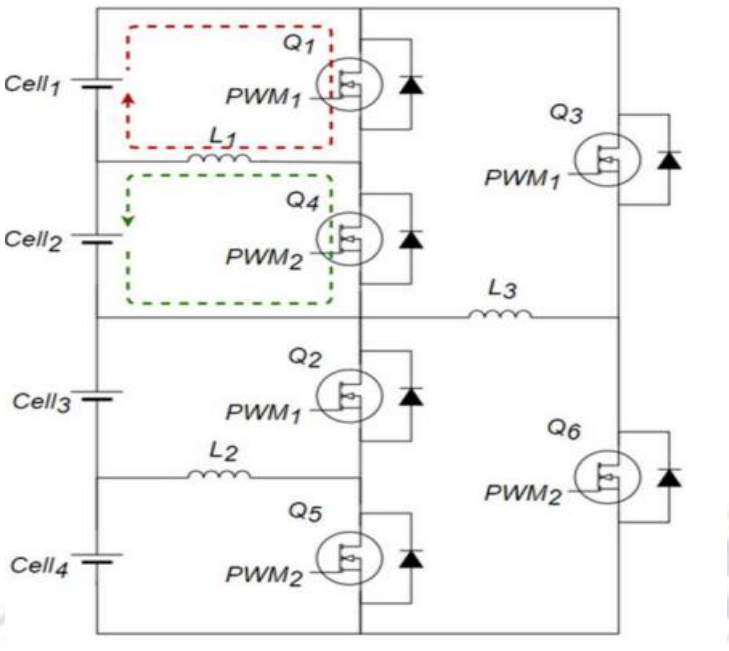

Figure 2.1: Circuit Diagram of Active Cell Balancing [14].

2.1.2 Passive Cell Balancing

In this method, a resistor is used to dissipate the energy of the highest voltage cell in a series-connected battery pack. For the same current, the weakest cell approaches the maximum voltage threshold faster than the rest of the cells in the pack. If the cell voltage go beyond the SOA (safe operational area), the switch is triggered, allowing the cell to discharge through the resistor, also known as the bleeding resistor [14], as shown in Figure 2.2, decreasing the cell voltage and SOC to safe levels. This procedure is continued until all the cells have the equal voltage.

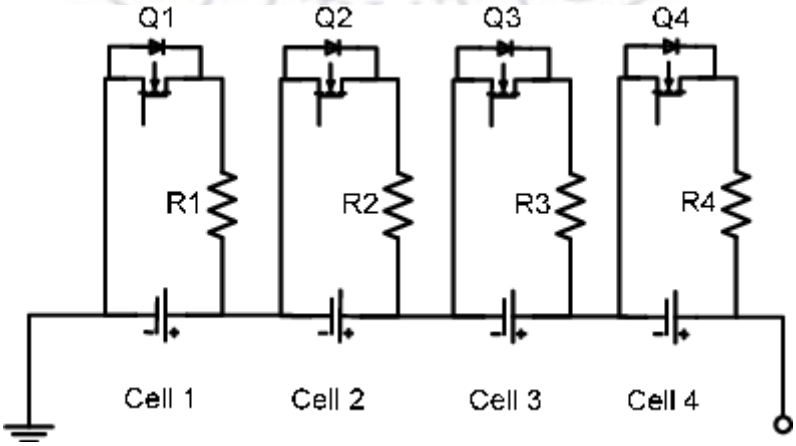

Figure 2.2: Circuit Schematic for Passive Cell Balancing [14].

Although passive balancing has a larger energy loss, it is indeed commonly use in industry due to its consistency and simplicity. The technique of control is also relatively simple and inexpensive. Because of its compact size, it is use for low-power applications, and simple to implement. It is compatible for BEV, PHEVs, HEV and EVs.

2.2 Battery SOC Estimation

State of Charge (SOC) is its current capacity in compared to its maximum capacity of the battery. It is often measured as a percentage ranging from 0% to 100%, representing a battery that is entirely dead to fully charge. To calculate SOC, each cell terminal voltage, current, and temperature are monitored. In most EV battery chemistries, the cell voltage does not always indicate the cell SOC. Therefore, if no current passes through the cell circuit, the cell voltage variations represent the cells SOC. Whenever current passes through the cell circuit, it also indicates the variation in cell resistance [15].

2.2.1 State of Charge Estimating Methods for Battery: The several mathematical SOC estimating approaches are categorized based on methodology. The categorisation of these SOC estimating methods varies across the literature. However, some literature supports categorization as follows:

a) Open Circuit Voltage Method: A lead-acid batteries SOC and Open Circuit Voltage (OCV) have an approximately linear relationship, as shown by:

$$V_{OC}(t) = a1*SOC(t) + a_0 \text{----------[1]}$$

SOC(t) represents the battery SOC at t, a_0 is the terminal voltage of the battery, SOC=0%, and a_1 is derived by knowing the values of a_0 and $V_{oc}(t)$ at SOC = 100% The estimation of the SOC refers to the computation of the OCV according to equation [1.] The SOC is equivalent to the OCV approach based on battery OCV. Such a long disconnection time, however, may be too long for battery use [7].

b) Terminal Voltage Method: The electromotive force (EMF) of the battery is directly proportional to the terminal voltage because the terminal voltage decreases as a result of internal impedances if the battery discharges. Battery EMF approximately follows a linear relationship with OCV, and the voltage at the battery terminal follows a similar relationship. The terminal voltage approach was applied at varied discharge

currents and temperatures. However, because the battery's terminal voltage unexpectedly drops towards the completion of discharge, the predicted error of the terminal voltage method is significant [7].

c) Impedance Method: The magnitudes of the parameters that are shown by impedance measurements can change based on the battery's state of charge. Although impedance characteristics and fluctuations with SOC are not specific to any one type of battery system, it seems required to carry out a variety of impedance studies in order to identify and apply impedance parameters for estimating a battery's SOC [7].

d) Hybrid Methods: The goal of hybrid models is to achieve a globally optimal estimating performance by implementing the benefits of each method. Since the information contained in each individual estimating method is limited, a hybrid method can make the best use of the benefits of multiple estimating by integrating the information from each individual model and optimising the use of the information already available. The literature demonstrates that, as compared to individual methods, hybrid methods typically yield good SOC estimating outcomes. The hybrid approaches incorporate various techniques, including the direct measurement method and the book-keeping estimating method [7].

e) Adaptive System: Resent advancements in artificial intelligence have led to the development of a variety of innovative adaptive methods for SOC estimates. The newly developed techniques include support vector machines, fuzzy neural networks, radial basis function neural networks, fuzzy logic techniques, and Kalman filters. Self-designing adaptive system automatically adapt to changing environments. Adaptive systems are excellent option for SOC estimation because batteries have nonlinear SOC and impacted by various chemical factors [7].

f) Bipolar Neural Network: Bipolar (BP) neural network is the most popular type in artificial neural networks. The BP neural network is applied in SOC estimation due to their good ability of nonlinear mapping, self-organization, and self-learning. As the problem defined, the relationship between the input and target is nonlinear and very complicated in SOC estimation. The artificial neural network based SOC indicator predicts the current SOC using the recent history of voltage, current, and the ambient temperature of a battery. The architecture of the SOC estimating BP neural network is

shown in Figure 2.3. The architecture of BP neural network contains an input layer, an output layer, and a hidden layer. Input layer has 3 neurons for terminal voltage, discharge current, and temperature, hidden layer has neurons, and output layer has only one neuron for SOC [7].

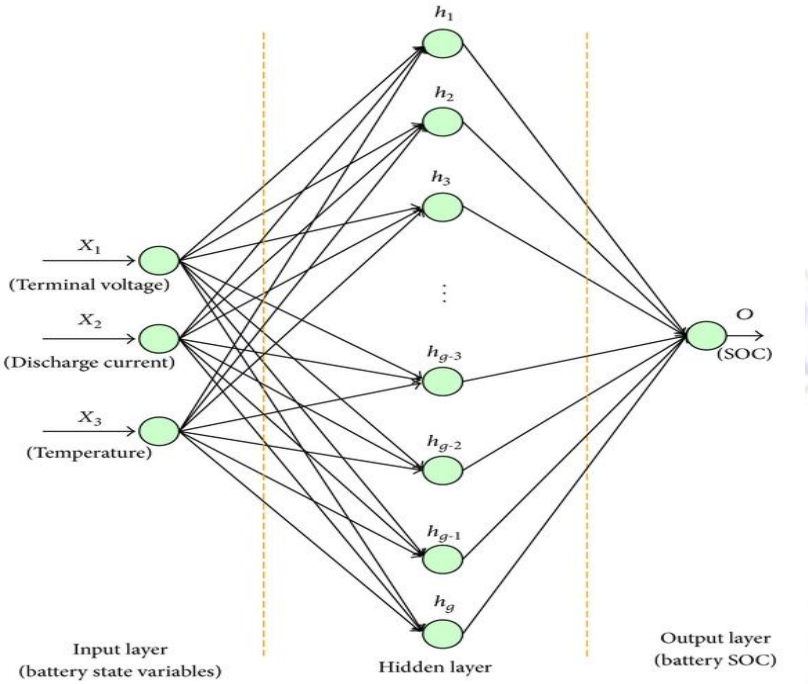

Figure 2.3: The architecture of the SOC estimating BP neural network.

The total input of a neuron in hidden layer is calculated by the following form:

$$net_j = \Sigma x_i v_{ij} + bj \text{----------[2]}$$

Were, net_j is total input of the hidden layer neuron j; x_i is input to the hidden layer neuron j from input layer neuron i; vij is weight between the input layer neuron i and hidden layer neuron j; bj is bias of the hidden layer neuron j.

The activation function applied to neuron in hidden layer is the hyperbolic tangent function which is calculated by the following equation:

$$Hj = f(net_j) = \frac{1-e^{-2netij}}{1+e^{-2netij}} \text{----------[3]}$$

The total input of the neuron in output layer is calculated by

$$net\ o = \Sigma h_i w_i + k \text{----------[4]}$$

were, net o is total input of the output layer neuron ; is input to the output layer neuron from hidden layer neuron ; is weight between the hidden layer neuron and output layer neuron; is bias of the output layer neuron ; is number of neurons in the hidden layer.

The activation function applied to neuron in output layer is the sigmoid function as the following equation:

$$O = f(\text{net } o) = \frac{1}{1+e-net\ o} \text{----------[5]}$$

g) RBF Neural Network: The RBF neural network is a useful estimation methodology for systems with incomplete information. It is used to analyze the relationships between reference sequence and the other comparative ones in a given set. The RBF neural network SOC estimation method uses the input data of the terminal voltage, discharging current, and temperature of battery to estimate the SOC for $LiFePO_4$ battery under different discharging conditions.

h) Fuzzy Logic Method: Fuzzy logic method provides a powerful means of modelling nonlinear and complex systems. A practical method of estimating SOC of battery system has been developed and tested for several systems. The method involves the use of fuzzy logic models to analyze data obtained by impedance spectroscopy and/or Coulomb counting methods. In [26], a fuzzy logic-based SOC estimation method has been developed for lithium-ion batteries for potential use in portable defibrillators. The ac impedance and voltage recovery measurements are used as the input parameters for the fuzzy logic model.

System that can select features in data base to develop fuzzy logic models for both available capacity and SOC estimation, simply by measuring the impedance at three frequencies. In [28], the SOC is estimated by an improved Coulomb metric method, and the time-dependent variation is compensated by using a learning system. The learning system tunes the Coulomb metric method in such a way that the estimation process remains error free from the time-dependent variation. The proposed learning system uses the fuzzy logic models, which is not used for estimation of SOC but performs as a component of learning system.

Various SOC measurement approaches have been presented in the literature, and they are primarily classified as Direct and Indirect methods. One of the direct approaches used is the Coulomb Counting Method of SOC estimation.

2.2.2 Coulomb Counting Method of SOC Estimation: The direct way to estimate the SOC of a battery is to collect charges during charging or discharging using Coulomb counting. The Coulomb counting method calculates SOC by integrating the amount of current flowing in and out of the battery over the time in seconds that the battery is charging or discharging. The mathematical representation of the equation [6].

$$SOC(T)\% = SOC(T_o)+1/(Q_{rated})\int I(dt)(S) * 100 \text{----------[6]}$$

From (2), the rated capacity of the battery is determined by the manufacturer's standards, whereas the current integration terms represent the total amount of charge transferred during charging and discharging situations. The Coulomb counting approach necessitates knowledge of the initial state of charge SOC [7]. This strategy utilizes less computational resources, but it produces a substantial number of errors due to the unpredictability of battery variables such as temperature and current, among others. Another disadvantage is that even minor differences in the initial SOC values can affect the integration process. Furthermore, various other parameters, such as current sensor accuracy and internal resistance, influence estimation accuracy [15].

2.3 Summary

In this chapter the concept of cell balancing methods and comparison between active and passive cell balancing is studied. The different methods used for Battery SOC estimation and SOC estimation using coulomb counting method are also discussed.

Chapter 3

METHODOLOGY AND BLOCK DIAGRAM

The methodology of Proposed Cell balancing Algorithm, SOC estimation Algorithm and block diagram of Battery Management System using Passive cell balancing implementation is discussed in this chapter.

3.1 Methodology

Figure 3.1 indicates the proposed passive cell balancing algorithm. Fundamentally, this includes monitoring the SOC of each cell in a battery pack B1 to B3 constantly. The cell with the highest SOC in a series-connected string of B1 to B3 cells is identified relative to the SOC of the other cells. MOSFET switch in that cell circuit is triggered on, only if SOC of one cell exceed that of another. Therefore, the bleeding resistor being connected across the cell, the cell discharges until it matches the remaining of the cells in the thread. An Optocoupler based on the 4N35 is used to trigger the MOSFET. MOSFET is until the voltage difference is < 20mV. If all cells are balanced the cell balancing algorithm terminates.

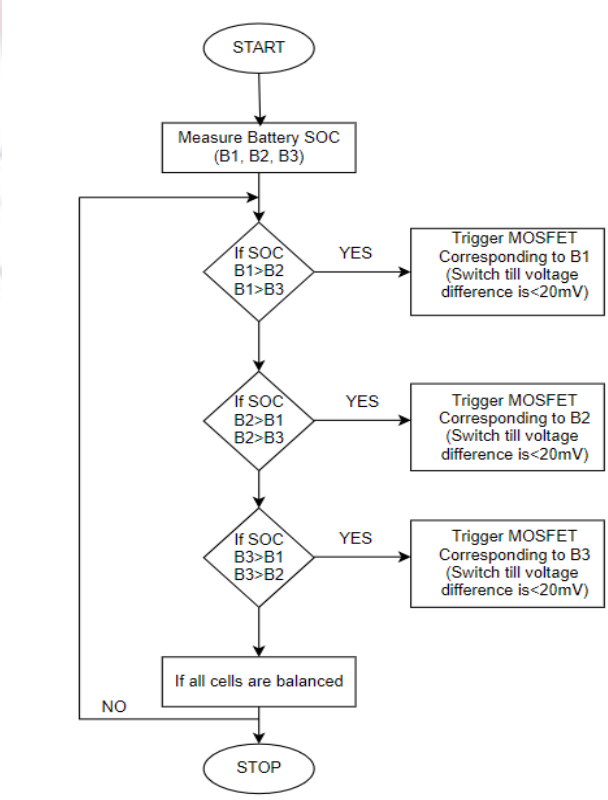

Figure 3.1: Methodology of Proposed Passive Cell balancing Algorithm.

3.2 Block Diagram

Figure 3.2 demonstrates the Block diagram of the Passive cell balancing module for 3 cells of Li-ion battery pack along with coulomb counting method-based SOC estimation algorithm using an Arduino-nano Controller. The passive cell balancing circuit was implemented with a switching resistor configuration to deliver a quick and effective cell balancing process. A regulated linear power supply is employed to simulate the operation of a charging battery cells. The voltage divider network is used to measure the voltage of each cell. The ACS712 Current sensor is used for measuring the current flowing through the Li-ion battery pack. The cell voltage and cell current are measured precisely on a discrete basis of 10 bits ADC of Arduino Nano controller.

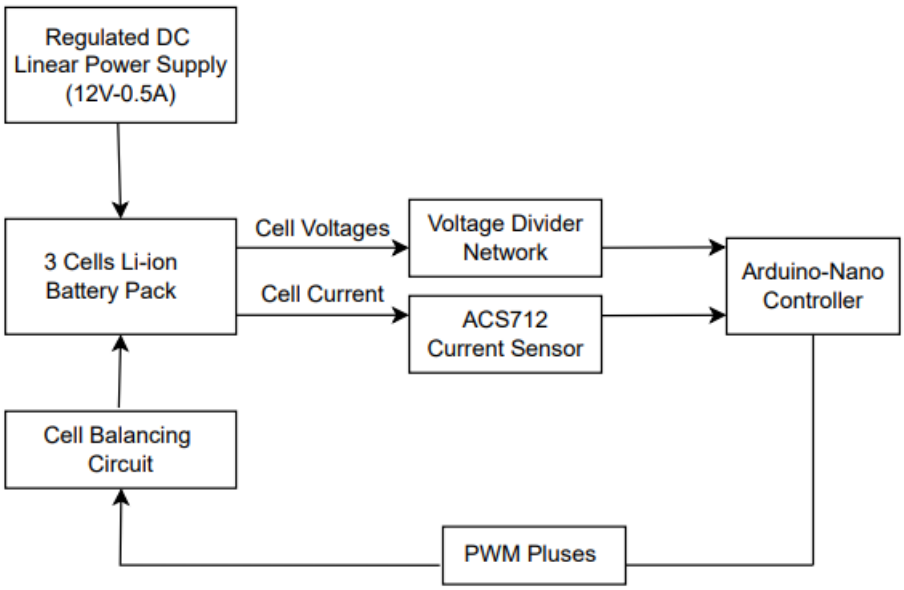

Figure 3.2: Block Diagram of Passive Cell Balancing Circuit.

3.3 SOC Estimation Algorithm

Figure 3.3 represents the SOC estimation algorithm using coulomb counting method. It primarily involves defining variables and Input parameters. If the collective cells voltage B1-B3 is less than 13, the cell SOC is determined using the current integration approach, is as described in [6].

$$SOC(T)\% = SOC(To)+1/(Q_{rated})\int I(dt)(S) * 100 \text{----------[6].}$$

This integration is achieved out using the numerical integration method carried out on Arduino-nano controller. It includes iteratively multiplying current by time and adding the result to the previous value of SOC. In the Coulomb counting technique,

reliable current measurement without noise is critical for accurate SOC estimation. The battery SOC is then determined by calculating power is transferred in it.

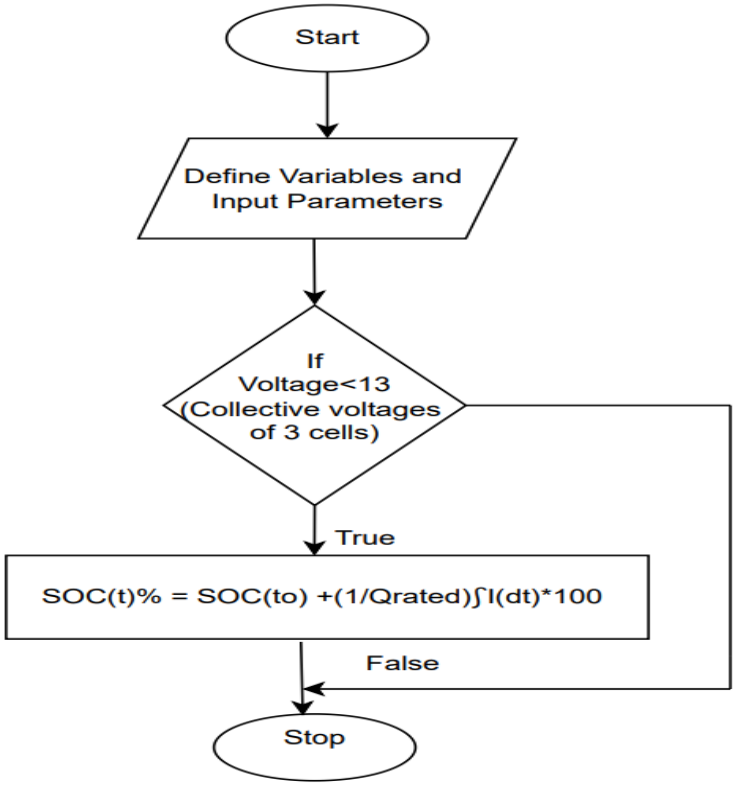

Figure 3.3: SOC estimation algorithm using coulomb counting method.

Based on these concepts the Battery management System using Passive Cell Balancing circuit is designed. Steps involved in the development and implementation of proposed system as shown in Figure 3.4

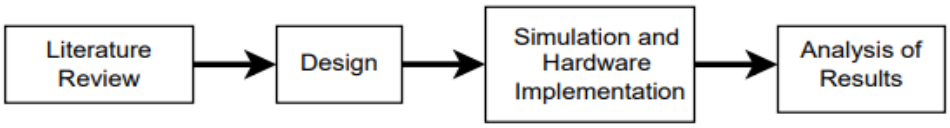

Figure 3.4: Methodology of Proposed Work

- Literature Survey - A detailed literature survey is carried out for selecting required cell balancing topology, SOC estimation algorithm and the Passive Cell Balancing technique employed with SOC estimation using coulomb counting method selected.
- Design - A Battery Management System using passive cell balancing circuit to

be designed. Designing of cell balancing circuit involves selection of the switching devices, design of bleeding resistors components and selection of the controller. The tool used for design of schematics is ALTIUM.

- Simulation and Hardware Implementation – The designed Passive Cell balancing circuit is simulated using the MATLAB/Simulink and the hardware prototype is developed using suitable components.
- Analysis of Result – Analysis of the Cell balancing circuit with different cell voltages and various SOC level of each cell in a Li-ion battery pack. The results are obtained using the Arduino-nano controller for balancing the voltage and SOC level of the battery pack.

3.3 Summary

The chapter gives detailed information regarding the block diagram, methodology of cell balancing algorithm, SOC estimation algorithm and the steps involved in the development and implementation of the Battery Management System using the Passive Cell Balancing circuit.

Chapter 4

SPECIFICATION AND DESIGN

There are numbers of components are involved in the process. The process is carried out smoothly only if all the components are interfaced and synchronized in the desired fashion. The process of selecting and designing the components as per the required specifications plays an important role. The chapter deals with the design and selection of various components needed for the operation.

4.1 Specifications

The parameters and the specifications for the passive cell balancing circuit is as specified in Table 4.1.

Table 4.1 Specifications of passive cell balancing Circuit.

Sl.no	Parameter	Specifications
1	Li-ion Battery Cells	LGABB41865
2	MOSFET Switch	BS170
3	Optocoupler	4N35
4	Bleeding resistors	10Ω
5	Current Sensor	ACS712
6	Controller	Arduino -Nano

4.1.1 Battery Pack

A battery pack comprises of Li-ion cells. These cells are rechargeable and are connected series. It has the advantages of pollution free, long cycle life, Built-in anti-explosion protection and short circuit protection [14]. The features of Li-ion battery cells are tabulated in Table 4.2.

Table 4.2 Features of Li-ion battery cells.

Battery Model	Li-ion 18650 Rechargeable Battery
Standard Voltage	3.7V
Capacity	1200mAh
Chemistry System	Li-ion
Cycle Life	More than 600 times cycles

4.1.2 MOSFET Selection

MOSFET is selected based on Drain to Source Voltage (Vds), Drain Current (Id) and Drain to Source ON state resistance RDS(ON). The drain to source ON state resistance is to be small for low losses.

1) Loss Calculation

The package and size of the MOSFET depend on the losses takes place in MOSFET. The following two types of losses are calculated while selecting the MOSFET

- Conduction losses
- Switching losses

Conduction losses and switching losses are calculated as per equations:

Conduction loss, $P_{cond}= \frac{1.25*R_{DS}*(I_{prms})^2}{2} = \frac{1.25*5*(200m)^2}{2*\sqrt{2}} = 65.5\text{mwatt}.$

Switching loss, $P_{sw}= \frac{1}{2}* Vin * Io * (tr + tf) * fsw$

$P_{sw}=\frac{1}{2}* 10 * 500m * (10n + 10n) * 1M = 500mwatt.$

The selected MOSFET is BS170, 10V, 500mA, 5Ohm.

4.1.3 Resistor

The bleeding resistors are connected in series with the cell. The value of the bleeding resistor is determined by R = V/I = 3.7/500m = 7.4Ω (8-10Ω Resistors are chosen). Power dissipated through the resistor= I^2 *R= (0.5)2*8 = 0.711 W.

4.1.4 Selection of Controller

The ATmega328P board Mini-B USB connector and pin headers. The CPU has a 16 MHz clock speed and 32 KB of Flash Memory (of 2 KB used by boot-loader). The Integrated Development Environment (IDE) for it is used to programme the 30 male I/O headers on the Arduino Nano.

The device is built with Microchip high-density non-volatile memory technology. The On-chip ISP Flash allows for in-system reprogramming of the programme memory through an SPI serial interface, a traditional non-volatile memory programmer, or an On-chip Boot application running on the AVR core. The boot programme downloads the application programme into the application Flash memory via any interface. While the application flash part is being updated, the software in the Boot Flash area continues to operate, allowing for real Read While-Write operation. The ATmega328P is a powerful microcontroller that combines an 8-bit RISC CPU with in-system Self-Programmable Flash on a monolithic device to provide a highly versatile and cost-effective solution to many embedded control applications.

4.6 Summary

The specification of individual component in terms of its rating was provided in this chapter. The simulations were carried out considering the designed values. The SOC estimation calculation was also discussed in this chapter.

Chapter 5

SIMULATION AND HARDWARE IMPLEMENTATION

This chapter presents the simulation analysis of the various models. All the simulations are performed using MATLAB software tool. The circuit model and its waveforms are explained in detail. The hardware approach for the project is also discussed.

5.1 Simulation Analysis

A simulation model is developed using the MALTAB/Simulink circuit for BMS using passive cell balancing. Initially, Cell-to-cell differences in the module create an imbalance in cell voltages in both charging and discharging conditions.

5.1.1 Charging of Battery Cells

The circuit diagram for charging of battery cells activated whenever DC bus is connected as shown in Figure 5.1(a).

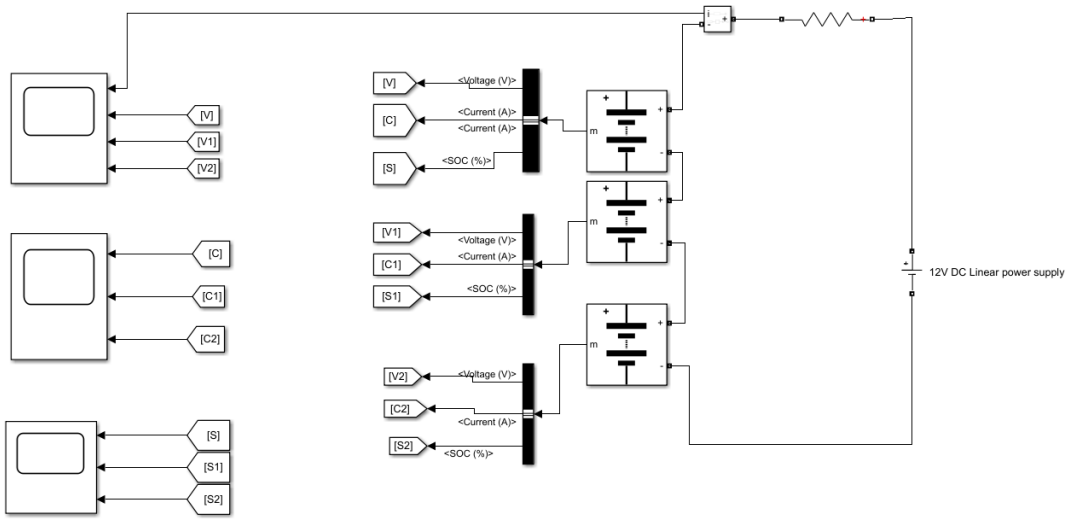

Figure 5.1(a): Circuit Diagram of Charging of Battery Cells.

5.1.2 Discharging of Battery Cells

Figure 5.1(b) represents the circuit diagram for discharging of Battery Cells. The circuit is automatically activated whenever DC bus is not connected, and the control objective becomes load voltage in order to maintain a constant load voltage during discharging.

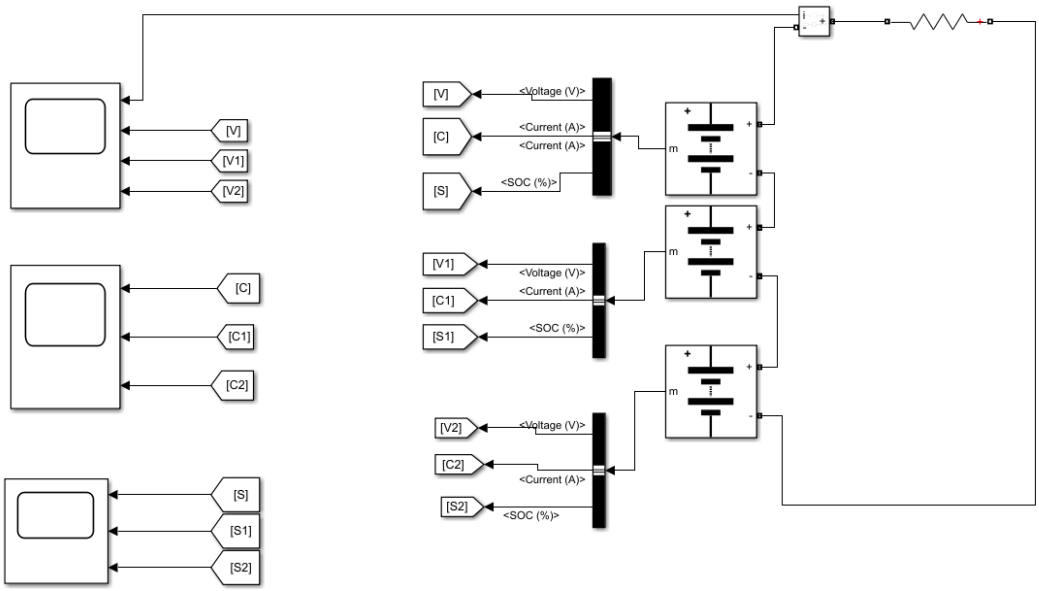

Figure 5.1(b): Circuit Diagram of Discharging of Battery Cells.

To overcome the imbalance creation during charging and discharging condition a circuit for passive cell balancing has been developed and simulated for charging and discharging conditions using MATLAB/Simulink. The SOC of the Li-ion battery cells is set at a difference of 5% to indicate cell balancing. The Li-ion battery cell's specifications are determined by the manufacturer's datasheet. Figure 5.2 depicts the SOC-based Passive cell balancing employing MOSFET as a switch with bleeding resistors positioned in parallel with each cell. If the voltage difference between the cells is more than < 20mV, the MOSFET switch connected with that battery cell is turned on. The passive cell balancing algorithm determines the following requirements. Whenever one cell voltage exceeds that of the other battery cells, the associated MOSFET switch is triggered, and if all cell voltages are equal, the triggering is STOP. To operate the circuit, the bleeding resistors are set to 10 ohms. If the cell voltage of B1 exceeds the cell voltage of B2, the MOSFET switch across B1 is activated. As a result, the logic for B2 and B3 is similar. The simulation results for the battery cells during charging and discharging circumstances were examined.

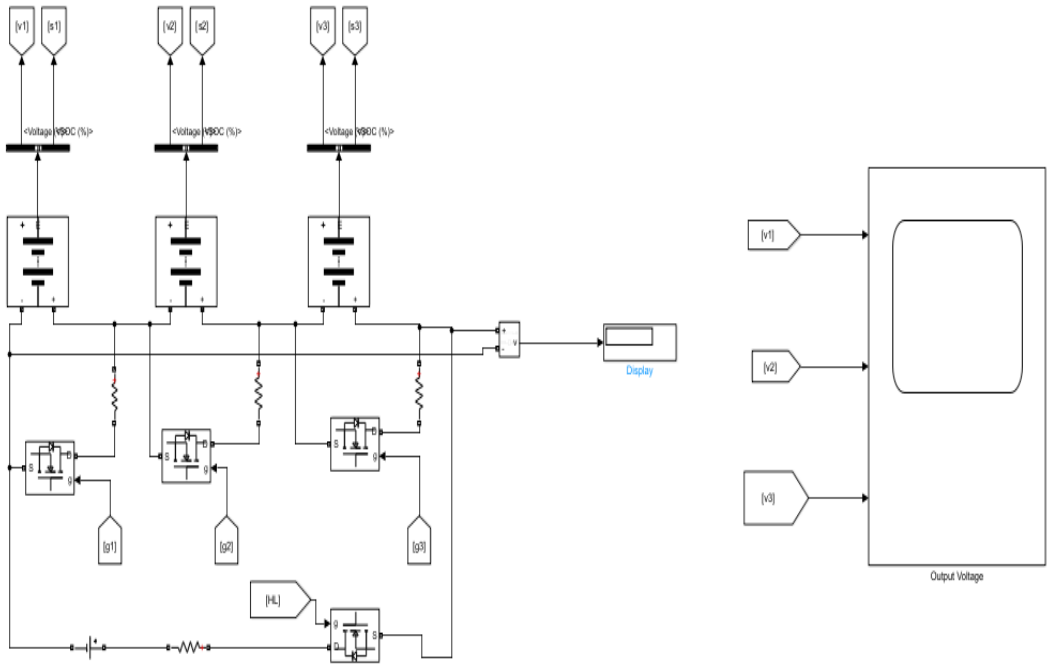

Figure 5.2: Passive Cell Balancing Circuit Simulated using MATLAB.

5.1.3 Battery SOC Estimation

Figure 5.3 represents the Coulomb Counting Method based SOC estimation simulated using MATLAB. It involves calculation of current over each sample and integrates with the currents during charging and discharging cycle over the period of operation. However, during the charging and discharging cycle the available charge is always lower than the stored charge.

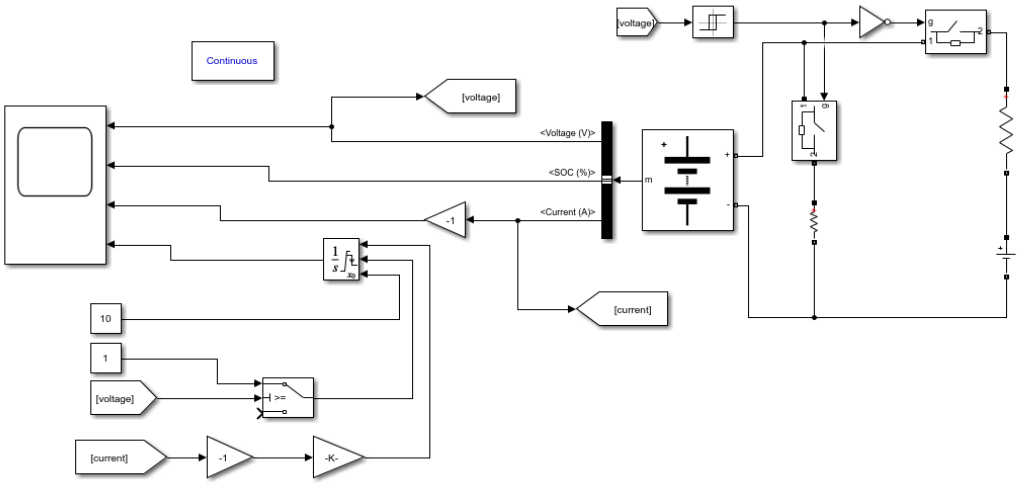

Figure 5.3: Coulomb Counting Method Based SOC Estimation of Battery simulated using MATLAB.

5.2 Hardware Implementation

Experimental results that depict Voltage of each cell, Current through the battery pack, SOC, and difference between maximum and minimum cell voltage. In the battery pack during charging and discharging conditions of Passive Cell Balancing circuit are presented. The hardware implementation of the balancing circuit includes various components:

- Li-ion Battery Cells
- MOSFET Switch
- Optocoupler
- Bleeding resistors
- Current Sensor
- Arduino-nano Controller

5.2.1 Schematic

From the designed values various components are selected. According to the Schematic representation as shown in Figure 5.4, the selected components like MOSFET Switch, Optocoupler, Bleeding resistors, Current Sensor and Arduino-nano are mounted on the printed circuit board. MOSFET is provided with heat sink, to absorb the heat dissipated by the MOSFET and the switch is provided by the Optocoupler, to provide the pulse to trigger the switch. Current sense circuitry senses the input current and provide the over current protection.

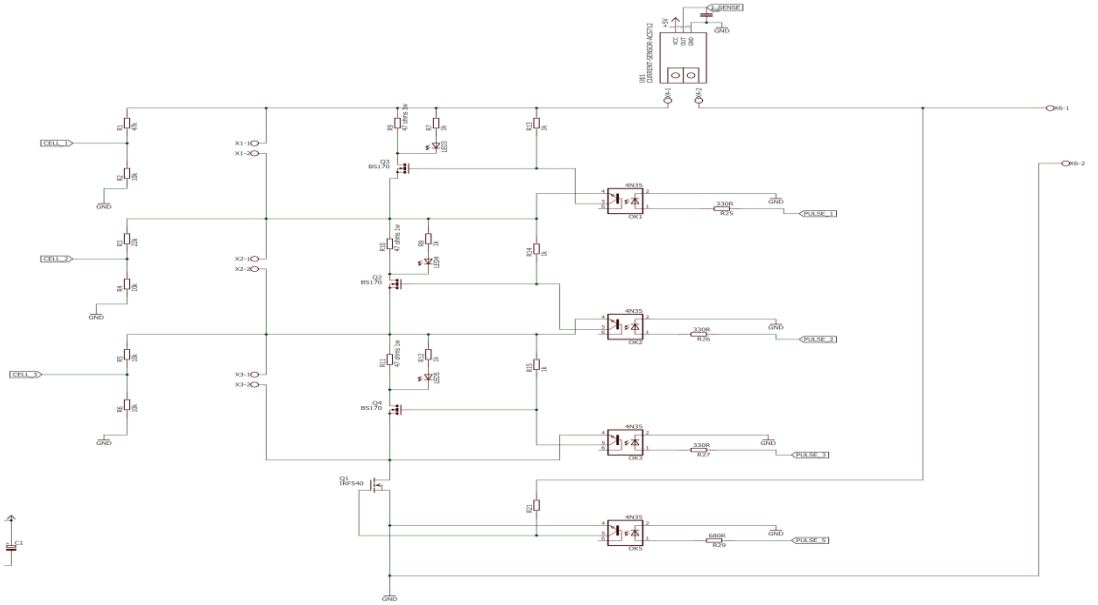

Figure 5.4: Schematic Representation of Passive Cell Balancing Circuit Designed in ALTIUM.

5.2.2 Proposed Hardware Module

The Hardware prototype of Passive Cell Balancing circuit with the SOC estimation algorithm coded on Arduino-nano controller was implemented for the 3 cells of Li-ion battery pack is as shown in Figure 5.5. A three-cell battery pack is made up of rechargeable lithium-ion cells connected in series. The passive cell balancing algorithm is used to operate MOSFET switches, as shown in Figure 3.1. The battery pack's charging and discharging conditions are monitored. The passive cell balancing algorithm is coded in the Arduino-nano controller.

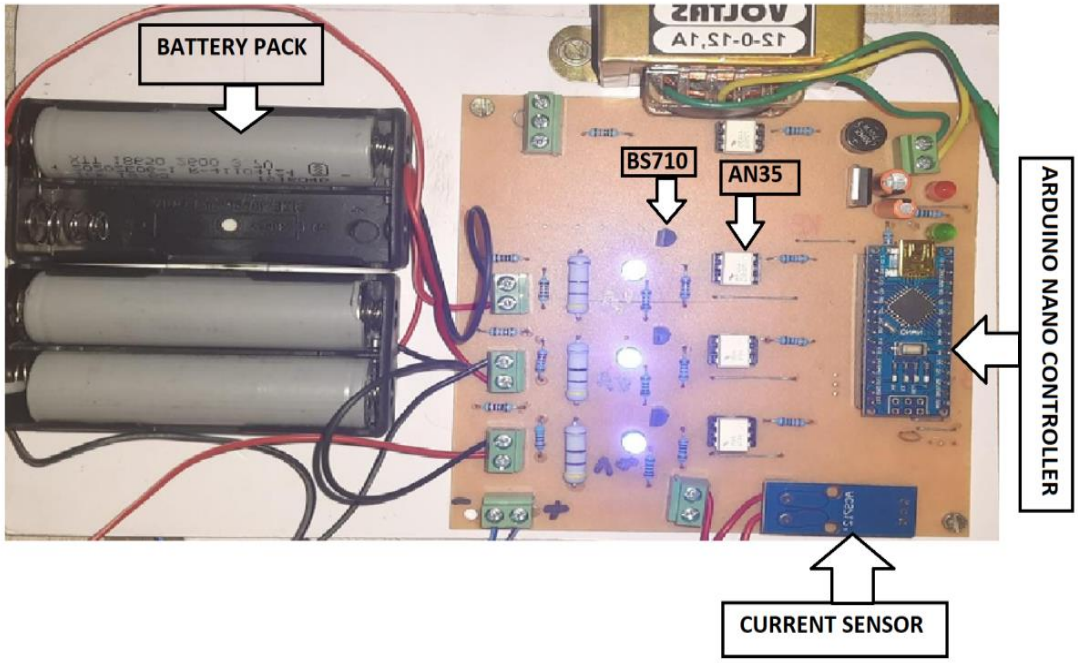

Figure 5.5: Hardware Implementation of Passive Cell Balancing Circuit.

5.3 Summary

The simulation of the Battery Management System using Passive cell balancing using MATLAB/SIMULINK was explained in this chapter. The chapter also describes the hardware components and the hardware implementation of the work.

Chapter 6

RESULTS AND DISCUSSION

In this chapter the simulation and the hardware results of the Passive Cell Balancing Circuit using the Coulomb Counting method of SOC estimation is discussed with its waveforms and results.

6.1 Simulation Results

Figure 5.1(a) represents the circuit diagram of charging of battery cells. The results observed from the circuits are explained. Initially, the Battery Cell Voltages are 3.6V, 3.7V and 3.8V. During charging of the Battery cells is able to charge till the maximum cell voltages of the battery pack (i.e., 4.2V), If the control over charging is not provided the battery cell voltages may reach up to 8V. Whenever a battery is charging, the exponential voltage raises independent of the battery's state of charge. And the current in the battery pack drops to zero, causing an imbalance in the BMS as shown in Figure 6.1(a).

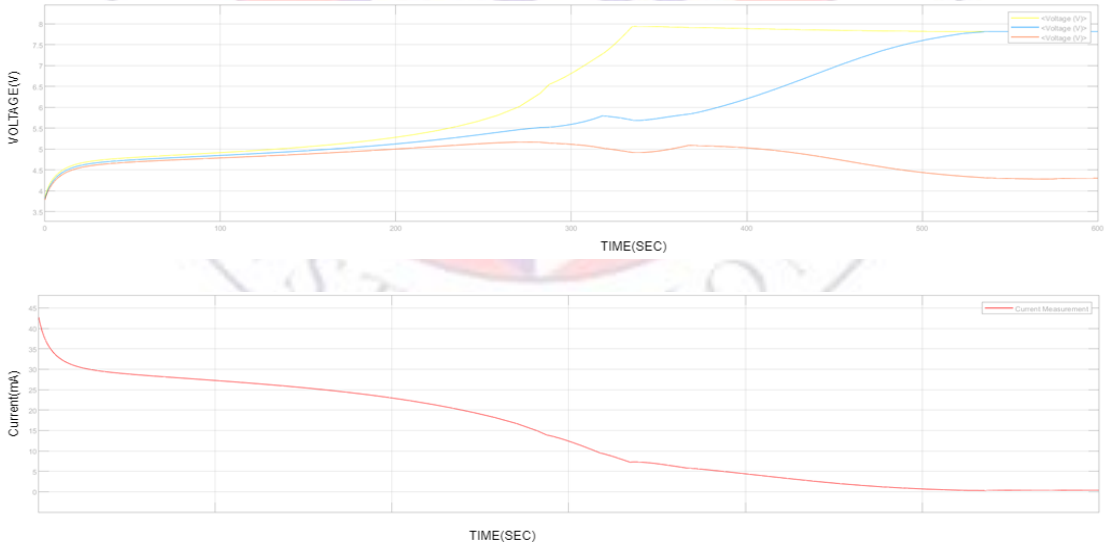

Figure 6.1(a): Battery cell Voltages and Current during Charging Condition.

Figure 5.1(b) shows the circuit diagram of discharging of battery cells. The results show that, whenever the battery discharges, the exponential voltage drops dramatically. And the current in the battery pack becomes negative, creating an imbalance in the BMS as shown in Figure 6.1(b).

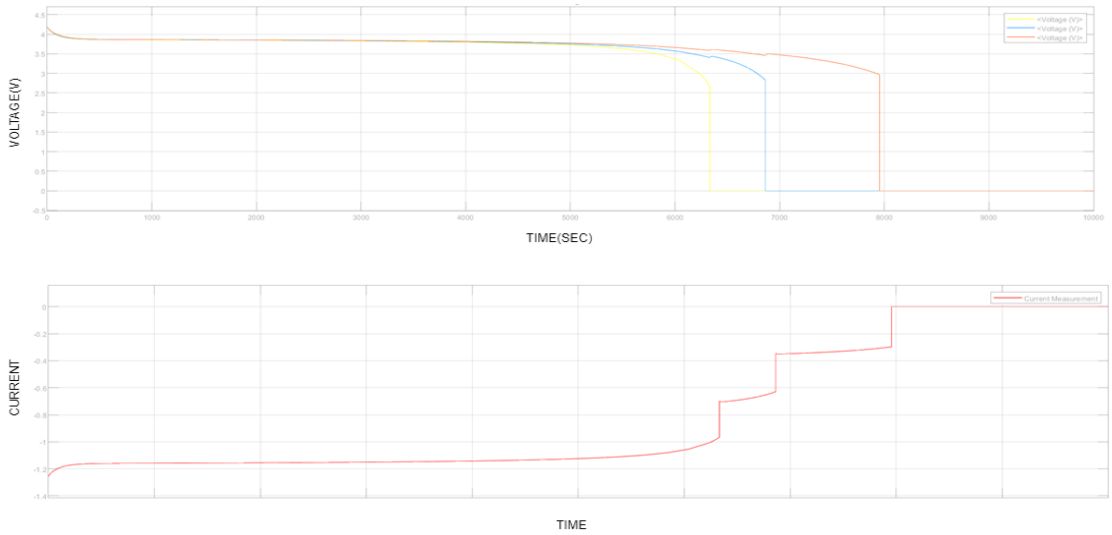

Figure 6.1(b): Battery cell Voltages and Current during Discharging Condition.

Figure 5.3 Passive Cell Balancing Circuit Simulated using MATLAB. The results observed from the circuits are explained. The cell voltages B1, B2 and B3 are initialized to 3.9, 3.93 and 3.97 and State of Charge to 65%, 70% and 75% respectively. The cells charges to its maximum voltage of 4.2V and SOC of the cells B1-B3 reaches to 97%. The time consumed during charging of cells was 1600sec. A bleeding resistor is linked across the battery cells while discharge. The battery cell voltages are compared. The battery cell with the lowest voltage level is determined, and the other two batteries are discharged to the same levels. The battery cells are balanced and the SOC of cells B1-B3reaches to 20%. The time consumed during the discharging of cells was 900sec. For the completion of overall operation, the time consumed was 2500sec is as shown in Figure 6.2.

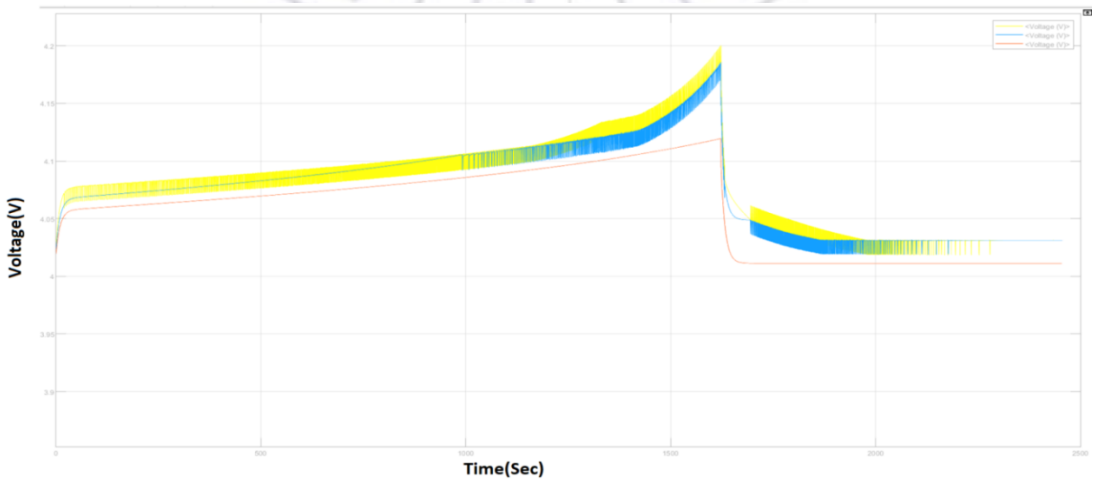

Figure 6.2: Battery Cell voltages During Charging and Discharging Operation.

Figure 5.4 coulomb counting method based soc estimation of battery simulated using MATLAB. The results observed from the circuits are explained. Figure 6.3(a) represents the Voltage cure during charging and discharging of battery cell, was the voltage is increased during charging till the maximum value 4.2 V and voltage decreased during discharging till the minimum value 2.6 V of Battery cells. Figure 6.3(b) indicates the SOC estimated curve during charging and discharging cycle of the battery pack. i.e., SOC is maintained at 20% initially, during charging the SOC of the battery increases approximately to 97% and during discharging the SOC level of the battery decreases to 8% and Figure 6.3(c) symbolize the current signal during the period of charging and discharging of battery cells. The current in the circuit is headed away from the positive terminal of the battery towards the negative terminal. Hence the current during charging of the battery is positive and during discharging cycle current is negative because, current in the circuit is headed away from the negative terminal and toward the positive terminal of the battery.

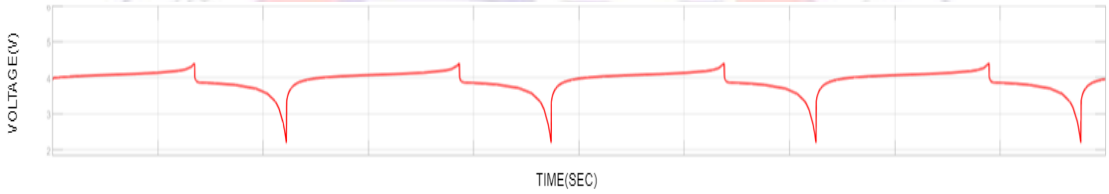

Figure 6.3(a): Voltage Curves during Charging and Discharging Operation of Battery Cells.

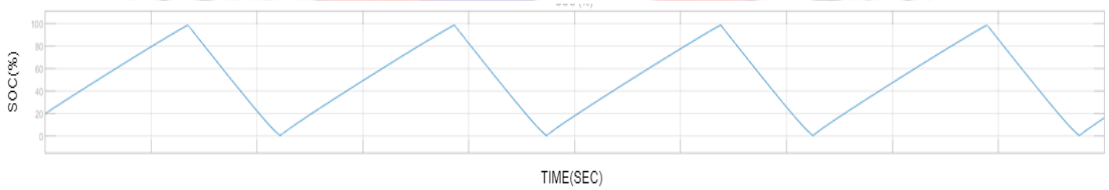

Figure 6.3(b): SOC estimated Curves during Charging and Discharging Operation Battery Cells.

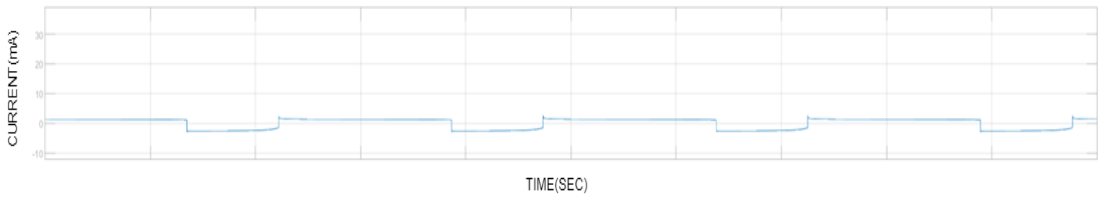

Figure 6.4(c): Current Waveforms during Charging and Discharging Operation Battery Cells.

6.3 Hardware Results

Figure 5.5(a) represents hardware setup of passive cell circuit during discharging of battery cells. The results observed from the prototype and explained. Arduino ID Software is used to code on Arduino-nano controller and for real-time monitoring the results. Serial monitoring display shows the individual battery cell voltage, denoted as V1, V2, and V3during discharging operation is as shown in Figure 6.5(a). The cell voltages before discharging were found to be around 3.81v, 3.85v, and 3.78v. After cell balancing, the voltages were almost equivalent to 3.81V, 3.82V, and 3.81V, with a SOC of around 87%.

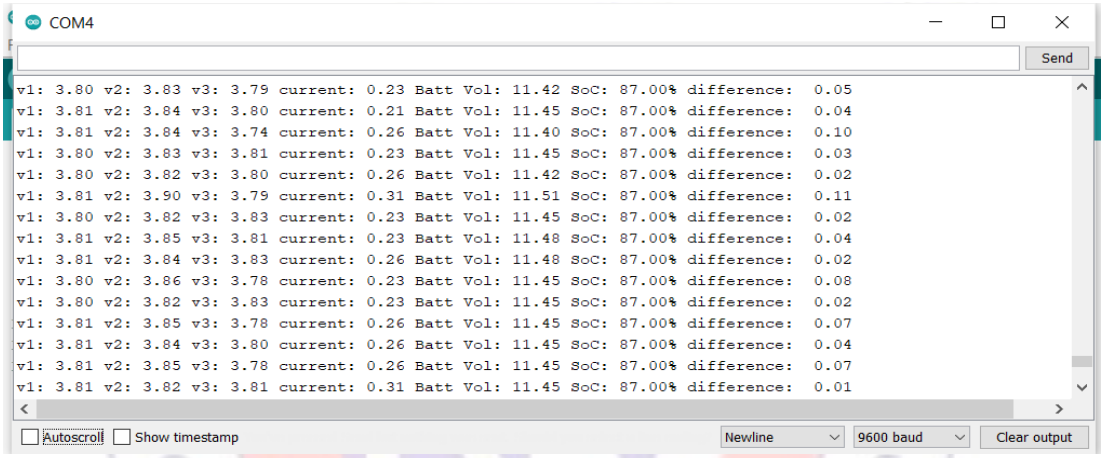

Figure 6.5(a): Values of Battery Cells Voltages, Current, SOC and Difference during Discharging of Battery Pack.

Figure 5.5(b) indicates hardware setup of passive cell circuit during charging of battery cellswith regulated dc linear power supply. The results were observed from the Serial monitoring display as shown in Figure 5.10. It is observed that before charging, the battery cell voltages were around 3.81V, 3.87V, and 3.77V. And after cell balancing, the voltages were around equal to3.81V, 3.83V, and 3.83V, with a SOC of around 87.02% is as shown in Figure 6.5(b).

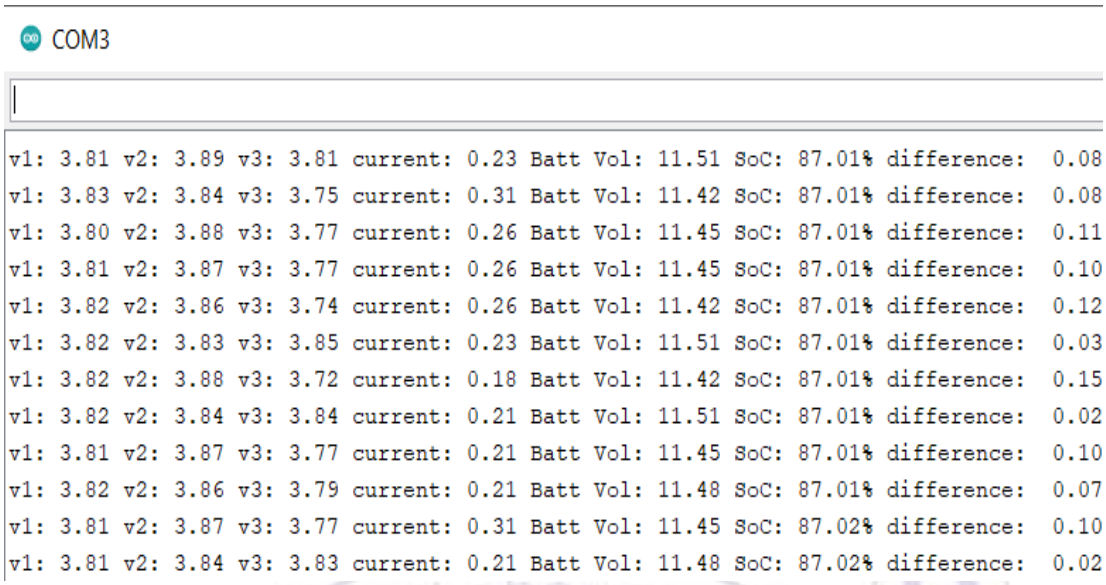

Figure 6.5(b): Values of Battery Cells Voltages, Current, SOC and Difference during Charging of Battery Pack.

6.4 Summary

The simulations of the circuits are performed and waveforms for the same are obtained. The designed components mounted on the PCB and hardware implementation is carried out. The readings for the circuit are noted.

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Chapter 7

CONCLUSION AND FUTURE SCOPE

The growing interest in EVs throughout the world is a result of techno-economic initiatives intended to reduce the problems associated with fossil fuels. Energy Storage is a crucial part of the EV powering system. Many battery cells are employed in the pack that stores energy in EVs linked in parallel and series. These battery cells require close monitoring and control systems whenever the EV is in operation. The cell voltage balancing coupled with the voltage and SOC monitoring are two of the essential features of BMS.

Balancing of the battery pack maintained the efficiency and safety of BMS. Balancing methods are frequently classified into two types. That is active cell balancing and passive cell balancing. The Active cell balancing method, the cell consists of more of charge is moved to the other battery cells with the least amount of charge. The Passive cell balancing method, the additional charge is dissipated through a bleeding resistor positioned in series to the battery cell. This method of charge equalization is simple, convenient, adaptable, and cost efficient. And for accurate estimation, SOC Coulombs counting is employed. Therefore, here in this project the BMS using passive cell balancing that is based on Arduino-nano controller is considered.

7.1 Conclusion

- The simulation of the Battery Management System using Passive Cell Balancing circuit was simulated using the MATLAB/Simulink software.
- A hardware prototype of 3 cells of Li-ion batteries with SOC estimation algorithm coded on Arduino-nano controller has been designed.
- It is observed that before charging, the battery cell voltages were 3.86V, 3.88V and 3.84V. And after cell balancing, the voltages were equal to 3.87V, 3.87V, and 3.87V, with a SOC of around 87.01%.
- The cells before discharging were found to be around 3.80V, 3.83V and 3.79V. And after cell balancing, the voltages were almost equivalent to 3.81V, 3.82V, and 3.81V, with a SOC of around 87%.

- From the results it is observed that by the use of passive balancing method the cell balancing and SOC estimation could be effectively achieved.

7.2 Future Scope

In a more advance design, shielded FETs could be used in parallel with each string to drain current from cells that are at or near the over-voltage threshold. The variable resistor could be used with a similar maintenance function, the resistor tune the rate of balancing throughout the circuit to obtain higher efficiencies. And Cell balance control would be accomplished by developing a rule-based algorithm generates a strategy based on fuzzy logic control.

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APPENDIX A

BCS712

FAIRCHILD SEMICONDUCTOR®

March 2010

BS170 / MMBF170
N-Channel Enhancement Mode Field Effect Transistor

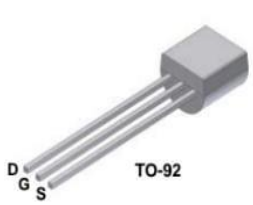
General Description

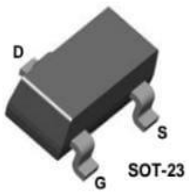
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 500mA DC. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

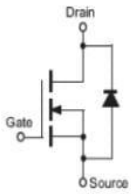
Features

- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.

BS170 **MMBF170**







Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1M\Omega$)	60		V
V_{GSS}	Gate-Source Voltage	± 20		V
I_D	Drain Current - Continuous	500	500	mA
	- Pulsed	1200	800	
T_J, T_{STG}	Operating and Storage Temperature Range	- 55 to 150		°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300		°C

Thermal Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
P_D	Maximum Power Dissipation	830	300	mW
	Derate above 25°C	6.6	2.4	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	150	417	°C/W

Electrical Characteristics T_A=25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 100μA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25V, V_{GS} = 0V	All			0.5	μA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15V, V_{DS} = 0V	All			10	nA
ON CHARACTERISTICS (Notes 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	All	0.8	2.1	3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 200mA	All		1.2	5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 200mA	BS170		320		mS
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200mA	MMBF170		320		
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz	All		24	40	pF
C_{oss}	Output Capacitance		All		17	30	pF
C_{rss}	Reverse Transfer Capacitance		All		7	10	pF
Switching Characteristics (Notes 1)							
t_{on}	Turn-On Time	V_{DD} = 25V, I_D = 200mA, V_{GS} = 10V, R_{GEN} = 25Ω	BS170			10	ns
		V_{DD} = 25V, I_D = 500mA, V_{GS} = 10V, R_{GEN} = 50Ω	MMBF170			10	
t_{off}	Turn-Off Time	V_{DD} = 25V, I_D = 200mA, V_{GS} = 10V, R_{GEN} = 25Ω	BS170			10	ns
		V_{DD} = 25V, I_D = 500mA, V_{GS} = 10V, R_{GEN} = 50Ω	MMBF170			10	

Note:
1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Ordering Information

Part Number	Package	Package Type	Lead Frame	Pin array
BS170	TO-92	BULK	STRAIGHT	D G S
BS170_D26Z	TO-92	Tape and Reel	FORMING	D G S
BS170_D27Z	TO-92	Tape and Reel	FORMING	D G S
BS170_D74Z	TO-92	AMMO	FORMING	D G S
BS170_D75Z	TO-92	AMMO	FORMING	D G S
MMBF170	SOT-23	Tape and Reel		

Typical Electrical Characteristics

BS170 / MMBF170

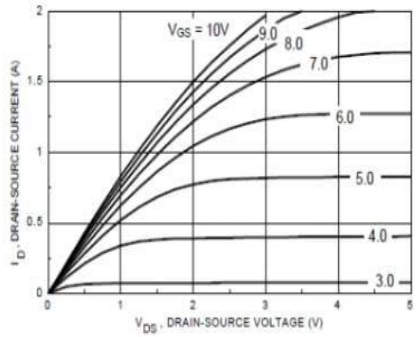


Figure 1. On-Region Characteristics.

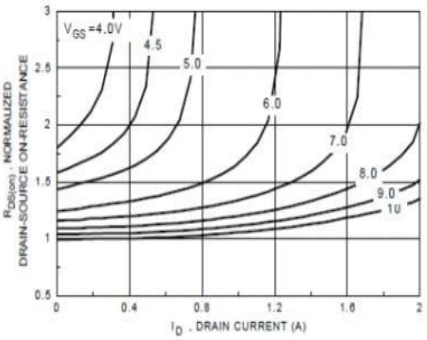


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

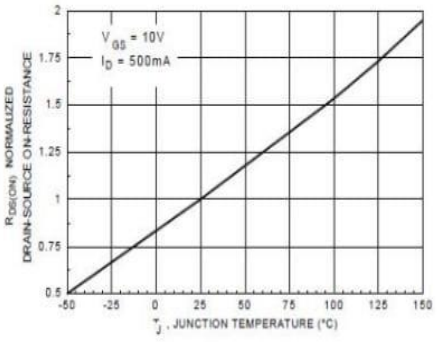


Figure 3. On-Resistance Variation with Temperature.

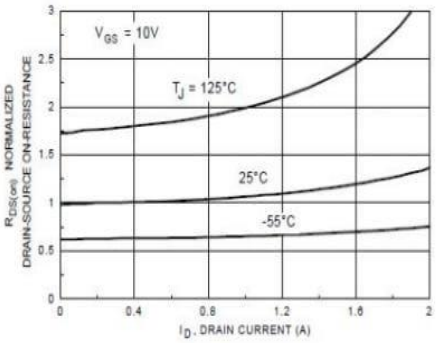


Figure 4. On-Resistance Variation with Drain Current and Temperature.

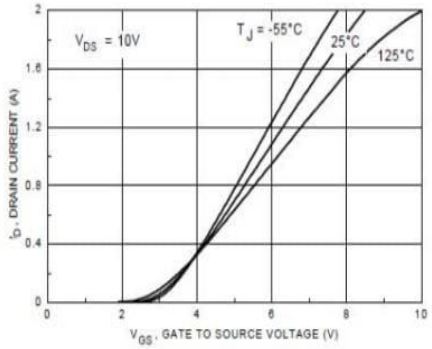


Figure 5. Transfer Characteristics.

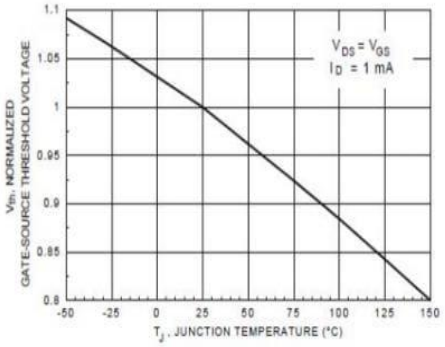


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

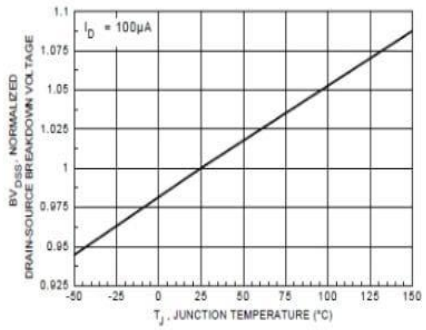


Figure 7. Breakdown Voltage Variation with Temperature.

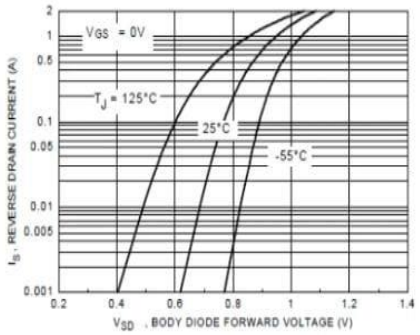


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

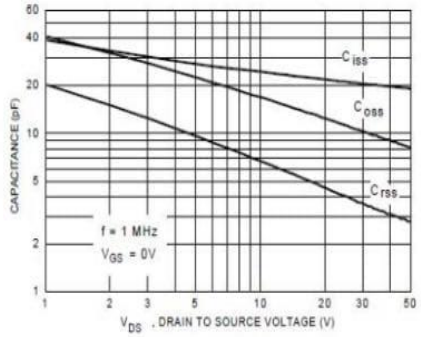


Figure 9. Capacitance Characteristics.

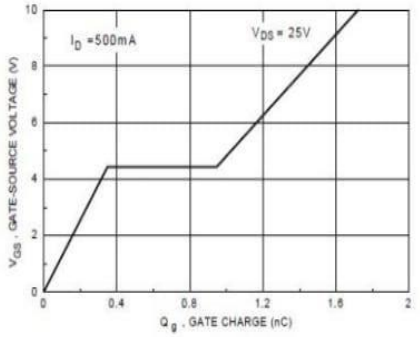


Figure 10. Gate Charge Characteristics.

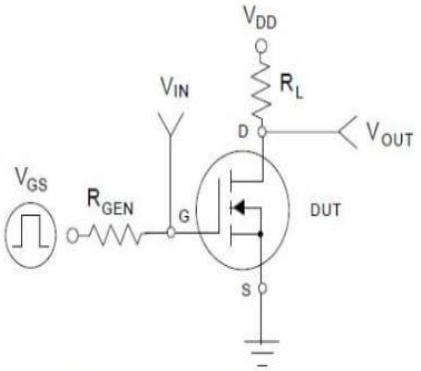


Figure 11. Switching Test Circuit.

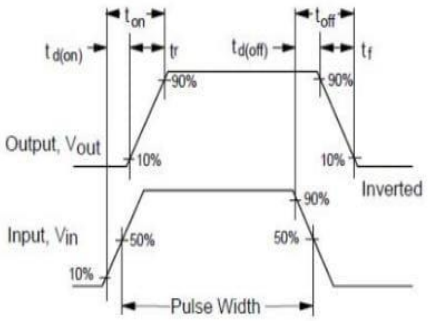


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

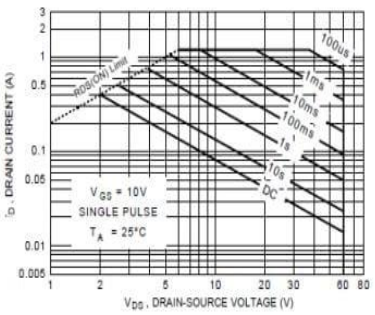


Figure 13. BS170 Maximum Safe Operating Area.

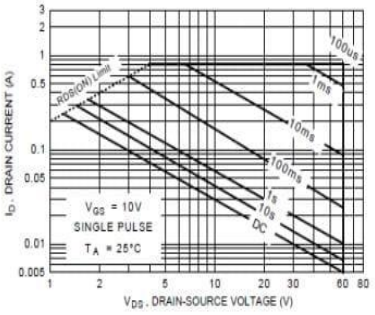


Figure 14. MMBF170 Maximum Safe Operating Area.

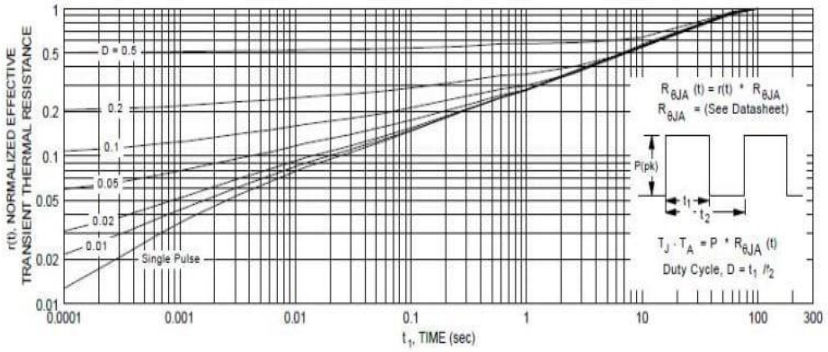


Figure 15. TO-92, BS170 Transient Thermal Response Curve.

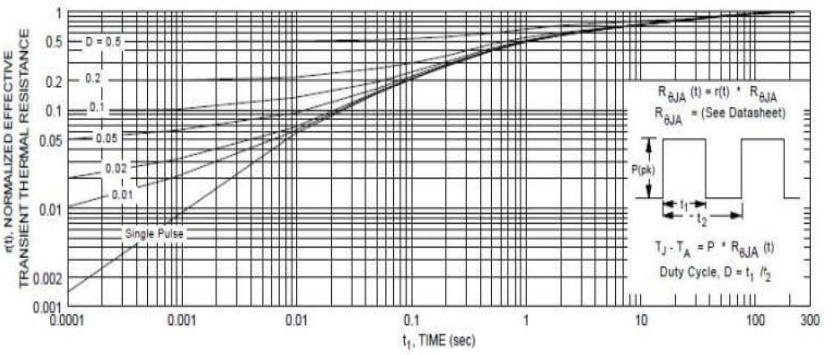


Figure 16. SOT-23, MMBF170 Transient Thermal Response Curve.

TO-92 Tape and Reel Data, continued

FAIRCHILD SEMICONDUCTOR®

TO-92 Packing
Information: Figure 2.0

TO-92 TNR/AMMO PACKING INFORMATION TABLE

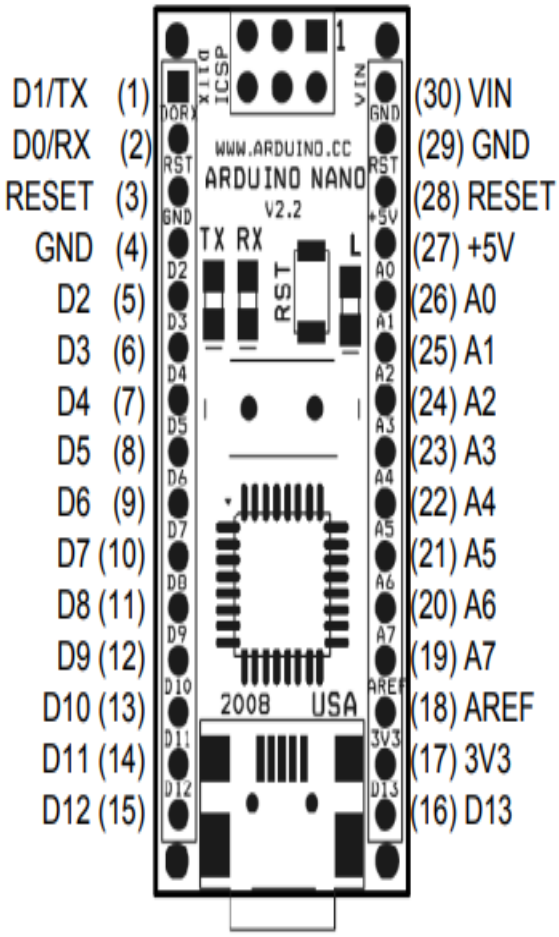
Packing	Style	Quantity	EOL code
Reel	A	2,000	D26Z
	B	2,000	D11Z
	C	2,000	D28Z
	D	2,000	D10Z
	E	2,000	D27Z
	F	2,000	D81Z
	G	2,000	D29Z
	H	2,000	D89Z
Ammo	M	2,000	D74Z
	P	2,000	D75Z

Unit weight = 0.22 gm
Reel weight with components = 1.04 kg
Ammo weight with components = 1.02 kg
Max quantity per intermediate box = 10,000 units

TO-92 BULK PACKING INFORMATION TABLE

EOL CODE / FLOW OPTION	DESCRIPTION	LEADCLIP DIMENSION	MINIMUM ORDER QTY	LEADFORM OULTINE
NO EOL CODE	STRAIGHT LEADS	NO LEAD CLIP	2.0K / BOX	
J18Z	TO-18 OPTION STD	NO LEAD CLIP	2.0K / BOX	
J35Z	TO-18 OPTION REVERSE	NO LEAD CLIP	2.0K / BOX	
J05Z	TO-5 OPTION STD	NO LEAD CLIP	1.5K / BOX	
J60Z	TO-5 OPTION REVERSE	NO LEAD CLIP	1.5K / BOX	
J61Z	IN LINE 0.200 SPACING	NO LEAD CLIP	1.5K / BOX	

Arduino-Nano Pinout Diagram



Pin No.	Name	Type	Description
1-2, 5-16	D0-D13	I/O	Digital input/output port 0 to 13
3, 28	RESET	Input	Reset (active low)
4, 29	GND	PWR	Supply ground
17	3V3	Output	+3.3V output (from FTDI)
18	AREF	Input	ADC reference
19-26	A7-A0	Input	Analog input channel 0 to 7
27	+5V	Output or Input	+5V output (from on-board regulator) or +5V (input from external power supply)
30	VIN	PWR	Supply voltage

Design and Implementation of Battery Management System Using Passive Cell Balancing

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Objective

Design and implementation of passive cell balancing circuit for 3 cells of Lithium-Ion batteries with SOC estimation algorithm coded on Aurdino-nano controller

Project Methodology

The concept of Passive Cell Balancing is used in the present work. In this method a resistor is used to dissipate the energy of the cell with the highest voltage in a series connected battery pack. Typically, the weakest cell achieves maximum voltage threshold faster than the rest of the cells in the pack for the same current. When the cell voltage exceeds the SOA (safe operational area), the switch is activated and the cell is allowed to discharge through the resistor, also known as the bleeding resistor, lowering the cell voltage and SOC to a safe level. This procedure is repeated until all the cells have the same voltage.

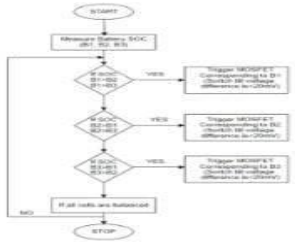

Fig 1: Proposed Cell balancing Algorithm.

Table 1. Summary of Components Specification.

Component Specifications	
Details	**Specification**
Li-ion Battery Cells	LGABB41865 1200mAH
MOSFET Switch	BS170 10V, 500mA, 5 ohm Rds(on)
Optocoupler	4N35, 6V, 600mA
Bleeding resistors	10Ω
Current Sensor	ACS712
Controller	Arduino -Nano

Analysis of Passive Cell Balancing

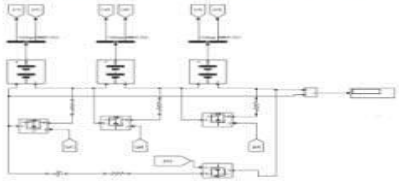

Fig 2: Circuit Diagram of Passive Cell Balancing.

It involves the continuous monitoring of the SOC of each cell B1-B3. In a string of series-connected cells B1-B3, the cell with the highest SOC is identified as compared to the SOC of other cells. Any cell having the positive differential SOC compared to other (i.e., ≤ 20mV), the MOSFET switch in that cell circuit is triggered ON. Thus, the resistor gets connected across the cell leading to the discharge of the cell until the time it matches with the voltage rest of the cells. To prevent the continuous switching operation of MOSFETs, the cell balancing algorithm is implemented such that MOSFETs will be turned on only when the SOC difference between any of the cells is more than the preset threshold value. Or else, the cell balancing operation is kept idle.

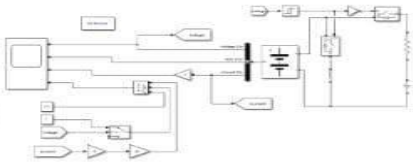

Fig 3: Circuit Diagram of SOC Estimation of Battery.

Fig 3 represents the simulation of SOC estimation using Coulomb Counting method in MATLAB. It involves calculation of current in each sample and integrates with the charging and discharging currents over the operating periods. However, the remaining charge is always less than the stored charge in the charging and discharging cycle.

Fig 4: Hardware prototype of Passive Cell.

Results and Discussions

Simulation Results

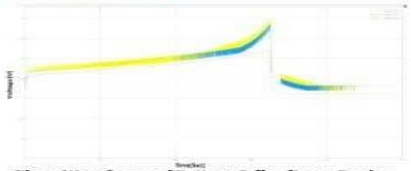

Fig 4: Waveforms of Battery Cell voltages During Charging and Discharging Operation.

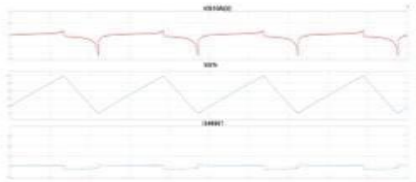

Fig 5: Waveforms Battery cell Voltage ,SOC, Current.

The initial voltages are 3.9, 3.93, 3.97 as shown in Fig 4 and SOC was initialized as 65%, 70% and 75% for cells B1, B2, and B3 respectively. When the cells were balanced the SOC of all cells reached 97%. To balance 5% variation at the beginning charging till the time reaches 4.2 i.e., cells reach the reset maximum value. The time taken was 1600sec. During discharging operation, a load resistor is shunted across the battery pack. The cell voltages are compared. The cell with least voltage level is identified and the remaining 2 battery cells are discharges to the same levels. When the cells were balanced with the SOC of all cells was reached 20%. To balance 5% variation with SOC and the time taken was 900sec in overall 2500sec of circuit operation.

The SOC estimation is done by coulomb counting method. The Fig 5 represents the waveforms Voltage ,SOC, Current of a battery pack.The voltage is increased during charging till the threshold value 4.2 V and decreased during discharging till the nominal voltage 3.6V of Battery cells. The SOC of the battery is maintained at 20% initially and during charging the SOC of the battery increases approximately to 97% and during discharging the SOC level of the battery decreases to 8% and the current waveform symbolize that during charging of the battery is positive and it is negative during discharging cycle.

Hardware Results

Fig 6: Values of Battery Cells Voltages, Current, SOC and Difference During Charging.

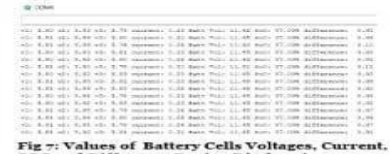

Fig 7: Values of Battery Cells Voltages, Current, SOC and Difference During Discharging.

- It can be observed that from Fig 6, the voltages of the cells before charging where around 3.81V, 3.87V and 3.77V. After balancing the voltages where approximately 3.81V, 3.82V, and 3.82V.
- From Fig 7, it can be observed that voltages of the cells before discharging where around 3.80V, 3.83V and 3.79V. And after balancing the voltages where approximately 3.81V, 3.82V, and 3.81V.

Conclusions

- The Battery Management System using Passive Cell Balancing for Electric Vehicle Application has been designed.
- The proposed passive balancing circuit with the Coulomb counting method of SOC estimation is simulated using MATLAB/Simulink modeling of three cells.
- A hardware prototype of 3 cells of Li-ion batteries with SOC estimation algorithm coded on Arduino-nano controller been designed.
- These results showed that battery balancing and SOC estimation will be effectively achieved using this topology.

Future Scope

- Advanced designs could use protected FETs in parallel with each string to drain the current from the cells that are at or near the over-voltage threshold.
- Potentially, The varied resistor could instead be used with a similar maintenance function to tune the rate of balancing throughout the circuit to obtain higher efficiencies.
- The cell balancing control can be done by establishing rule-based algorithm to determine a strategy using fuzzy logic control.

Acknowledgements

- I deeply express my sincere gratitude to my guide Suresha C, Assistant Professor, Dept. of EEE, RVCE, for his patience and valuable guidance throughout this project.
- I would like to express my deepest appreciation to Ampere Eclectic Vehicles Pvt. Ltd, Bengaluru, for providing me an opportunity to carry out my project in their organization.

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JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

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Design and Analysis of Battery Management System using Passive Cell Balancing

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Abstract: Due to the increasing demand for Electric Vehicles (EVs) worldwide is an implication of economic-technological efforts to reduce fossil fuel challenges. Energy storage which powers electric vehicles is a very important component. Battery packs used as energy storage for electric vehicles use many battery cells connected in series and in parallel. These battery cells require a close monitoring and management system while operating in an electric vehicle. Such a system, called the Battery Management System (BMS). BMS and battery packs play a very important role for EVs to become the best technical and commercial alternative to gasoline-based vehicles. BMS improves battery performance, and extends battery life while ensuring a safe operating range. Cell voltage balancing with State of Charge (SOC) monitoring is part of an important function of BMS. This paper focuses on the design and analysis of a passive cell balancing method for lithium-ion (Li-Ion) batteries based on the Arduino-Nano controller. This paper also deals with the simulation to demonstrate the SOC estimation using Coulomb counting method and passive cell balancing mechanism using MATLAB and results were analysed.

Index Terms **- Electric Vehicles, battery Management System, Passive Cell Balancing, State of Charge, Coulomb Counting, MATLAB.**

I. INTRODUCTION

In the recent years, EV's have gained considerable popularity. They are attractive mainly due to the integration of many smart applications and efficient energy saving technology, thereby addressing bigger problems associated with fossil fuels. EV Technology is considered as a potential solution to reduce emissions influence and depletion of petroleum resource reservoirs. As Electric Vehicle technology develops, many of its components and subsystems are getting better and better. Even then, mostly challenges are faced in design and development of Energy Storage Source (ESS). Frequently used ESS in EVs is the battery. Energy Storage Systems play a critical function within the fields of EVs. Li-ion batteries are more advantages as compared to the opposite rechargeable battery like Lead-acid, Nickel-Cadmium, Nickel-metal-hydride, etc. Lithium-ion batteries have the benefits of high energy density, long life, low self-discharge rate, no memory effect, non-toxic, comparatively low maintenance, fast charging, etc. over their contemporaries. They can supply large amounts of current for high-power applications, which has been traditional. For a Li-ion cell, the nominal voltage is 3.7V, maximum voltage is 4.2V and minimum voltage is 2.6V. If the intense battery limits are violated, i.e., any cell is overcharged to over 4.2V or discharged to but 2.7V, this will result in unstable battery condition and even causes fire hazard.

Therefore, the look of balancing system is essential to advance battery pack energy efficiency, cycle life and safety. The excess energy dissipation whether within the sort of heat, balancing mode are often divided into active balancing (non-dissipative) and passive balancing (dissipative). Active balancing can transfer energy to eliminate the inconsistencies between the batteries by employ inductors, capacitors, transformers, external power, and other modes. This sort of equalization method can achieve higher energy utilization, while the circuit is complex, and the cost is higher. Passive balancing dissipates excess energy within the type of heat through a parallel resistor. This equalization method is straightforward, convenient, flexible, low price and small, but this technology has disadvantages involving energy waste and causing burden to thermal management.

This article presents the design details of Arduino controlled BMS with passive cell balancing method. This system protects the Lithium-ion cells against the asymmetrical cell voltages and SOC. For effective functioning of BMS, an accurate SOC estimation of each battery cell of the pack is necessary. Multiple algorithms for estimation of SOC are suggested in literature. These are categorized into various types such as direct methods, Book-keeping methods, model-based methods, etc. In this article, an important method of SOC estimation using Coulombs counting has been considered.

II. BATTEY CELL BALANCING

Cell balancing methods can be classified into passive balancing and active balancing. The passive cell balancing method is simple, inexpensive, and easy to implement. It is therefore the most common and widely used method in industries today. Passive cell balancing is accomplished by dissipating the energy of overcharged cells with an external resistor until all cell voltages match. On the other hand, the active cell balancing circuit transfers excess energy from the cell with higher load to the cell with lower load. This excess cellular energy is transferred by the means of energy converters connected across each of the cells. Active

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cell balancing circuit provides higher battery efficiency and shorter cell balancing time compared to passive cell balancing. Due to the inclusion of converters in each cell, battery packs become very expensive and complex [6].
In this article, only the passive cell balanced method has been considered and is described in detail below.

2.1 Passive Cell balancing

Passive Cell Balancing, in this topology, excess charge is removed from the over charged cell by the controlled operation of power switches (SW1, SW2, and SW3) such as MOSFETs which is enabled via the microcontroller. When there is an imbalance between cells, the microcontroller decides which switch should be activated. When the switch is on, the resistor gets shunted across that cell and dissipates the excess of charge [4]. The circuit diagram of passive cell balancing is as shown in Fig. 2.1.

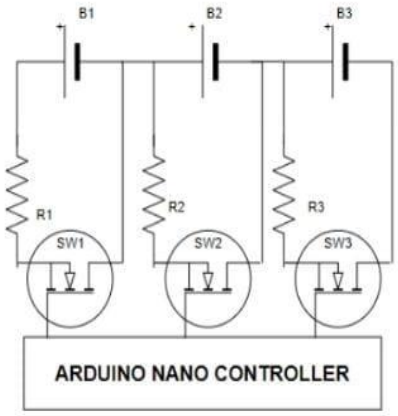

FIG.2.1 CIRCUIT SCHEMATIC OF PASSIVE CELL BALANCING.

Passive balancing method has a higher energy loss, but this method is still widely used in industries due to its reliability and simplicity. The control method is simple and cheaper when it is used for low power applications and is easy to implement with small size. This method is suitable for both Hybrid Electric Vehicle (HEV) and EV.

III. BATTERY SOC ESTIMATION

The SOC refers to the level available capacity of the battery as compared to its rated capacity. It is usually expressed as a percentage between 0% and 100%, recommended from a completely depleted battery to a fully charged one. To calculate SOC, the voltage at the cell terminals, the current in the cell and the temperature of each cell is necessary.

The various SOC estimation methods have been proposed which are classified mainly as Direct and Indirect methods. Coulomb Counting Method is considered as one of the direct methods implemented in this work is described below.

3.1 Coulomb counting Method of SOC Estimation

Coulomb counting method is also known as battery current integration method. In this method, SOC is estimated current integration terms represent the total amount of charge transferred during charging and discharging conditions.

This is represented mathematical representation as shown in the equation below [1].

$$SOC(T)\% = SOC(To) + \frac{1}{Qrated}\int_{to}^{to+t} I(dt)(s) * 100 \text{---------- (1)}$$

From (1), the rated capacity of the battery (Qrated) can be obtained from the manufacturer's specifications and sum to the initial state of charge SOC (To) [10].

IV. SOFTWARE IMPLEMENTATION

In simulation, the design of a passive cell balancing was realized for 3 cells of Lithium-Ion batteries with SOC estimation algorithm coded Aurdino-nano controller. Fig. 4.1, represents the SOC estimation algorithm. It primarily involves defining variables and Input parameters. In a string of series-connected cells B1-B3, if the cells voltage is less than 13, then the SOC is estimated by (1). If the condition goes false, then the SOC estimation is terminated.

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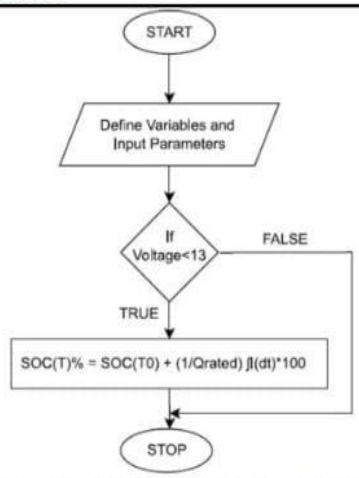

FIG. 4.1 SOC ESTIMATION ALGORITHM.

Fig. 4.2 represents the simulation of SOC estimation using Coulomb Counting method in MATLAB. It involves calculation of current in each sample and integrates with the charging and discharging currents over the operating periods. However, the remaining charge is always less than the stored charge in the charging and discharging cycle.

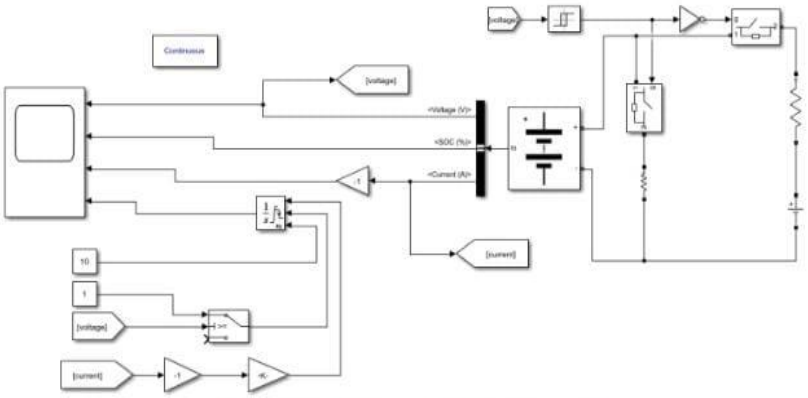

FIG.4.2.SIMULATION MODEL FOR SOC ESTIMATION.

Fig. 4.3(a) represents the Voltage cure were the voltage is increased during charging till the threshold value 4.2 V and voltage decreased during discharging till the minimum value 2.6 V of Battery cells. Fig. 4.3(b) indicates the SOC of the battery is maintained at 20% initially and during charging the SOC of the battery increases approximately to 97% and during discharging the SOC level of the battery decreases to 8% and Fig. 4.3(c) symbolize current during charging of the battery is positive and current is negative during discharging cycle.

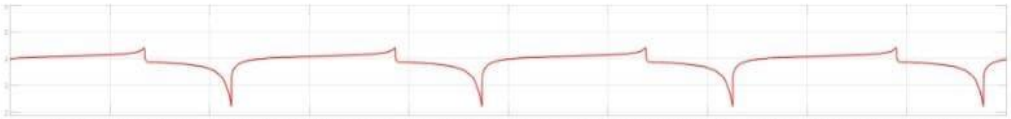

FIG. 4.3(A) VOLTAGE CURVES DURING CHARGING AND DISCHARGING OPERATION OF BATTERY CELLS.

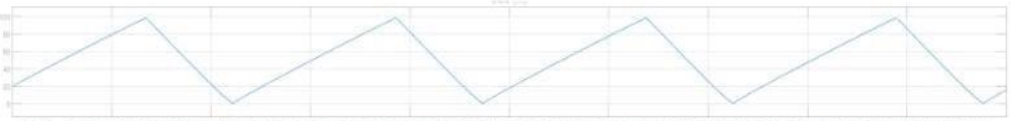

FIG. 4.3(B) SOC ESTIMATED CURVES DURING CHARGING AND DISCHARGING OPERATION BATTERY CELLS.

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FIG. 4.3(B) CURRENT WAVEFORMS DURING CHARGING AND DISCHARGING OPERATION BATTERY CELLS.

Fig. 4.4 shows the proposed cell balancing algorithm implemented. It involves the continuous monitoring of the SOC of each cell B1-B3. In a string of series-connected cells B1-B3, the cell with the highest SOC is identified as compared to the SOC of other cells. Any cell having the positive differential SOC compared to other, the MOSFET switch in that cell circuit is triggered ON. Thus, the resistor gets connected across the cell leading to the discharge of the cell until the time it matches with the voltage rest of the cells. To prevent the continuous switching operation of MOSFETs, the cell balancing algorithm is implemented such that MOSFETs will be turned on only when the voltage difference between any of the cells is ≤ 20mV. Or else, the cell balancing operation is kept idle.

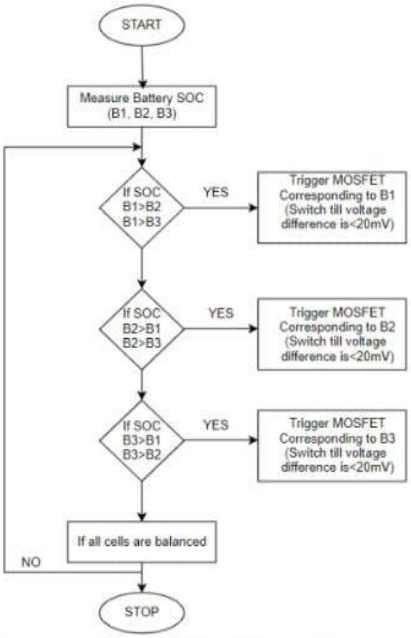

FIG. 4.4 CELL BALANCING ALGORITHM.

The proposed cell balancing circuit is simulated using MATLAB tool which carried out for two cases viz, during charging, discharging conditions as shown in Fig. 4.5(a). To demonstrate battery balancing, the State of Charge (SOC) of the cells is initialized with the difference of 5% between adjacent cells. MATLAB model was created for the 3cells Li-ion battery pack. Battery Cell specification was set according to the Li-Ion cell manufacturer datasheet. The simulation of SOC based cell balancing using a MOSFET and a resistor placed in parallel with each cell is realized. MOSFET corresponding to each battery is triggered ON when there is a voltage difference (i.e., ≤ 20mV) which determines the following condition based on the algorithm. Fig. 4.5(b) Voltage Function Block and Pulse Generation Block, MATLAB Simulation Model for Passive Cell Balancing. A Battery cell SOC is greater than other battery cells SOC in the string: MOSFET is triggered simultaneously and when all the cells are balanced, triggering is STOP corresponding to that MOSFET. The resistor value is taken as 10Ω to operate the circuit. These values have been calculated considering the losses occurring in MOSFETS and resistors. The circuit operation is based on a control algorithm as shown in Fig. 4.4. When the B1 SOC is greater than B2, the switch across the B1 is turned ON. Thus, similar logic is for B2 and B3. The simulation results were recorded for cells during charging, discharging conditions. The following section provides the simulation results obtained under the above-mentioned conditions and the discussion based on the same.

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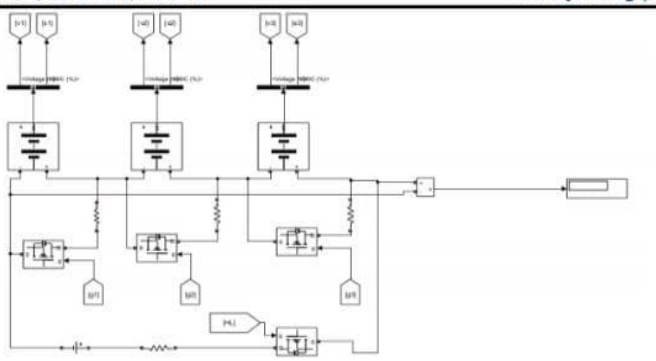

FIG. 4.5(A) MATLAB SIMULATION MODEL FOR PASSIVE CELL BALANCING.

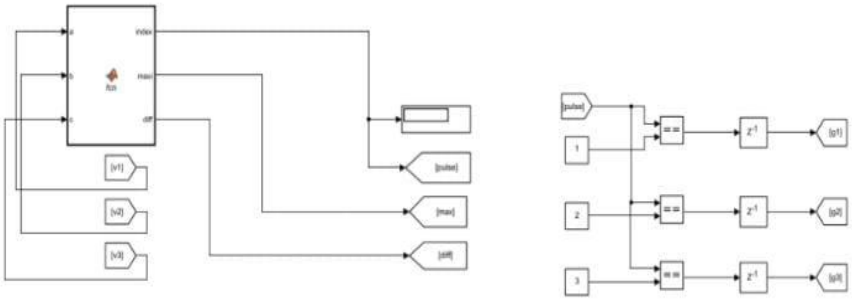

FIG. 4.5(B) VOLTAGE FUNCTION BLOCK AND PULSE GENERATION BLOCK, MATLAB SIMULATION MODEL FOR PASSIVE CELL BALANCING.

The initial cell voltages are 3.9, 3.93, 3.97 and SOC was initialized as 65%, 70% and 75% for cells B1, B2, and B3 respectively with a variation of 5% between B1 to B3. When the cells were balanced the SOC of all cells reached 97%. To balance 5% variation at the beginning charging till the time reaches 4.2 i.e., cells reach the maximum value. The time taken was 5000 sec in overall 1600sec. During discharging operation, a load resistor is shunted across the battery pack. The cell voltages are compared. The cell with least voltage level is identified and the remaining two battery cells are discharges to the same levels. When the cells were balanced with the SOC of all cells was reached 20%. To balance 5% variation with SOC and the time taken was 1600sec in overall 3000sec of circuit operation as shown in Fig. 4.6.

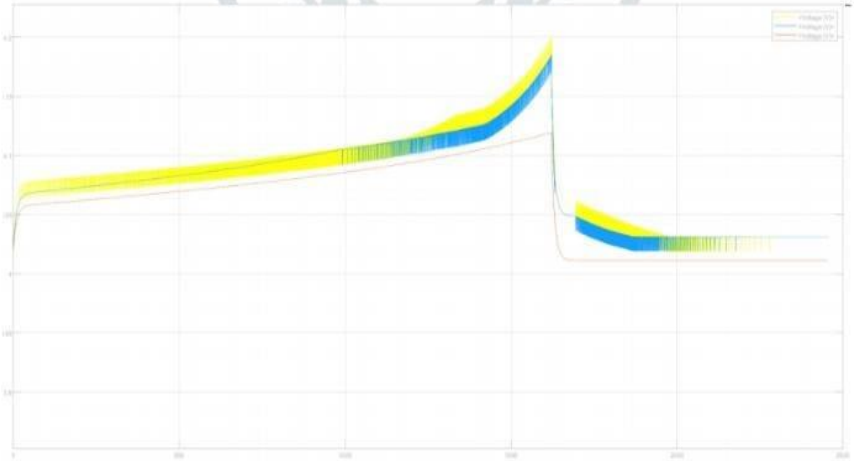

FIG. 4.6 CELL BALANCING CURVES DURING CHARGING AND DISCHARGING OPERATION OF BATTERY CELLS.

V. Conclusion

BMS is required for the EV battery pack to protect the battery and improve its life and performance. The work presented in this paper illustrates the use of Arduino-nano controller features, but the lower cost in BMS can provide the desired functionalities of the BMS. The passive cell balancing method is simple and cost-effective solution to be used in an EV battery pack. Therefore, it is one of the common methods which are followed by industries.

This paper presents the simulation results for BMS based passive cell balancing circuit with the Coulomb counting method of SOC estimation. This is followed by battery modelling using equivalent circuit and the charge and discharge graph, which is explained with the help of the equivalent circuit model. MATLAB/Simulink modelling of three cells and with their charge and discharge graphs are discussed after balancing techniques. These results showed that battery balancing, and SOC estimation will be effectively achieved using this topology.

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on
Design and Implementation of Digitally Controlled Cooler Drive Inverter for Temperature Control

18MPE41

Submitted by

Sachin J M

USN: 1RV20EPE11

Under the Guidance of

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Director
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Centum Electronics
Bengaluru-560064

Submitted in partial fulfillment of the requirements for the award of degree of

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in
POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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Sachin J M

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ABSTRACT

Cooler drives are widely used for cryocoolers, a cryocooler is a refrigerator designed to reach cryogenic temperatures and its main purpose is to cool objects quickly using extremely low temperatures. There are many common applications of Cryocoolers. One of the most common application is for the cooling of infrared sensors to temperatures of 80-150 K for use in military night vision equipment. The main objective was to capture the image from the space and fed to the FPGA and the signal received was converted to digital form using ADC.

The present work includes, design and implementation of digitally controlled cooler drive inverter for temperature control . The selected topology was H-Bridge inverter. The Main components includes ATmegaS128 Microcontroller, PID Controller, Protection Circuits, MOSFET Switches, Analog to Digital Converter, Driver Circuits, 2N2222A Transistor and Relays. The proposed inverter drives the cooler drive with 12V/6A, 50Hz AC output power via a PID control loop with input voltage range from 24V to 36V DC to control the cooling of detector array based upon the temperature signal feedback from the temperature sensor mounted on detector Focal Plane Array and in order to increase the relative accuracy of the thermal sensor, it was supplied with 1mA, 25uA constant current source to bias a temperature sensing diode and is connected to cooler PID control loop for temperature regulation. The voltage measured across the sensing diode was used by the control algorithm in the inverter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature.

The simulation analysis were carried out in PSIM, LTSpice and MATLAB/Simulink softwares, The design of the proposed inverter was carried out in SMath software and the Hardware Implementation was carried out in Printed Circuit board(PCB) and the PCB mainly consists of three cards namely Inverter(main), EMI and output cards and the interfacing of three cards were done to meet the design specifications for resistive and motor load conditions. The Hardware Implementation results shows that the efficiency of more than 90% were acheived at 3Ω Load Condition, 60W Load Condition, motor load condition and the effect of feedforward loop at 25º C ambient, 60º C Ambient and at Cold Tip Conditions were tabulated for input voltage range from 24 to 36V DC. The regulated output voltage and output current obtained were 12V and 6A respectively. The efficiency of more than 90% were achieved in all the cases and the obtained output ripple, frequency, DC offset, total harmonic distortion, load and line regulation were within the specified limits.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Sachin J M, Dr. Anitha G S, Dr. Ravichandran C, Prasanna Kumar R, Bhoopendra Kumar Singh, **"Design and Implementation of Digitally Controlled Cooler Drive Inverter for Temperature Control,"** International Journal of Emerging Technologies and Innovative Research, ISSN:2349-5162, Vol.9, Issue 6, pp. e549-e569, June-2022.

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GLOSSARY

ADC	:	Analog to digital converter
ATMEL	:	Advanced Technology for memory and logic
AVR	:	Alf and Vegard's RISC Processor
CE	:	Conducted emission
CRO	:	Cathode ray oscilloscope
D	:	Duty ratio
EEPROM	:	Electrically erasable programmable read only Memory
EMI	:	Electromagnetic Interference
EMC	:	Electromagnetic compatibility
EUT	:	Equipment under testing
ISR	:	Interrupt service routine
JTAG	:	Joint test action group
MOSFET	:	Metal oxide semiconductor field effect transistor
OCP	:	Over current protection
OVP	:	Over voltage protection
PCB	:	Printed circuit board
PID	:	Proportional integral derivative
PWM	:	Pulse width modulation
SPWM	:	Sinusoidal pulse width modulation
SRAM	:	Static random access memory
SPI	:	Serial peripheral interface
THD	:	Total Harmonic Distortion
TWI	:	Two-Wire interface
USART	:	Universal synchronous asynchronous receiver transmitter
UVP	:	Under voltage protection
VSI	:	Voltage Source Inverter

CHAPTER 1

INTRODUCTION

Power supply unit is an interface between power source and the electric load. The main function of the power supply unit is to modulate or convert the available electrical energy from the power supply into the form required by the load. It is quite rare that the power source directly matches the requirements of a particular load [1]. So, the power supply units find extensive applications in various industries. Input power source may be AC or DC, while the load may be a motor, an electronic equipment, or a computer[2]-[6].

Due to the growing need for low-cost cooling solutions for focal planes on short-duration (1-2 year), low-cost space flight experiments, both on spacecraft that fly in low Earth orbit as well as on landers and rovers for planetary investigation. Due to the significant temperature changes of the ambient environment and the limited available power, these applications place tremendous demands on both the cooler operating conditions and the thermal control of the cooler's surroundings[7]-[10].

A basic thermistor, a sensor whose resistance changes with temperature, is utilised in numerous applications. As an exponential function, this variation often introduces nonlinearity into the closed-loop control system. The open-loop plant's short time constants and the controller's relatively modest bandwidth demands, however, mean that this nonlinearity does not provide any specific control challenges[11]-[15].

The term cryogenic simply means very low temperature. Cryogenic cooling uses refrigerants, such as liquid nitrogen or solid carbon dioxide, directly. Cryogenic freezing is often treated as a specific type of freezing method on its own, however, it is essentially an immersion/spray system, depending on how the cryogen is utilized. Some gases are stored under “cryogenic conditions,” which means that they are stored at very low temperatures (-130 degrees Fahrenheit or less). Examples of gases that may be stored this way include air, argon, carbon monoxide, ethylene, fluorine, helium, hydrogen, methane, nitrogen, and oxygen[16].

A refrigerator designed to reach cryogenic temperatures is often called a cryocooler and its main purpose is to cool objects quickly using extremely low temperatures. There are many common applications of Cryocoolers. One of the most common application is for the cooling of infrared sensors to temperatures of 80-150 K for use in military night vision equipment. The term is most often used for smaller systems, typically table-top size, with input powers less than about 20 kW. Some can have input powers as low as 2-3 W. Large systems, such as those used for

cooling the superconducting magnets in particle accelerators are more often called cryogenic refrigerators. Their input powers can be as high as 1 MW[17]-[20].

In most cases cryocoolers use a cryogenic fluid as the working substance and employ moving parts to cycle the fluid around a thermodynamic cycle. The fluid is typically compressed at room temperature, precooled in a heat exchanger, then expanded at some low temperature. The returning low-pressure fluid passes through the heat exchanger to precool the high-pressure fluid before entering the compressor intake. The cycle is then repeated[20]-[32].

The Input to the cooler drives are AC, H-Bridge inverters are commonly used to convert DC Power into AC power and in order to generate sinusoidal PWM pulses for the single phase H-Bridge inverter, The microcontrollers are used because it is simpler and more flexible to change the real-time control algorithms without further modifications in a hardware with its reduced cost and also it reduces the complexity of the control circuit[33]-[36].

1.1 Overview

To meet the demand for the low-cost cooling options for local plane on very short duration, cooler drive inverter is designed for cryocoolers application. The output is controlled using duty cycle of the PID controller and accordingly the PWM waveforms are generated using ATmegaS128 microcontroller for controlling the output voltage. These applications place high demand on both cooler operating conditions and on the thermal control of the cooler environment because of the extreme temperature variation and because of limited available power[32].

The converter(DC-AC) has been employed with feed forward topology for fast response of closed loop control with changes in the input voltage ranging from 24V to 36V DC and voltage feed forward technique has been implemented for regulating both output voltage and temperature sensor voltage. Analog to Digital converter is used to convert analog signals to digital signals. The Switching frequency of 22KHz is used as per the design specification for the cooler drive. The converter is provided with two relays i.e., Main relay for Turning the converter ON-OFF and Launch lock relay is used to avoid the mechanical vibrations and secure moving during launching. The converter(DC-AC) is provided with protection circuits such as Over Voltage Protection (OVP), Under Voltage Protection (UVP) and Over Current Protection (OCP).

1.2 Specific Details

Digitally controlled H-Bridge inverter for cryocooler application with voltage feed forward technique for regulating output voltage and temperature sensor voltage is designed. The topology used is H-Bridge inverter. The input voltage range is 24V to 36V DC. The Main components includes ATmegaS128 Micro controller, PID Controller, Protection Circuits, MOSFET Switches,

Analog to Digital Converter, Driver Circuits, 2N2222A Transistor and Relays. The converter is designed with 22KHz switching frequency using ATmegaS128 Microcontroller. The output voltage to be obtained is 12V AC RMS and the output current is 6A. The Maximum permissible DC offset level at output is 0.2V and Maximum permissible harmonics in output signal for Secondary Harmonics is 10% and for Higher harmonics is 5%. The voltage for the over voltage protection circuit is 125% of the output voltage and for current is 125% .

1.3 Literature survey

Single-phase H-Bridge inverters are heavily used in home applications like uninterruptible power supplies (UPS), instant power supplies (IPS), induction heating, internet of things (IoT), renewable energy-based system. The input may come from a battery, rectified ac, fuel cell, solar cell, etc. It can be either standalone or grid-connected. Switch mode inverters are categorized mainly as a square wave and PWM inverters [1]. Square wave inverter is the simplest but comes with high harmonic contents close to the fundamental component. On the other hand, Sinusoidal Pulse Width Modulation (SPWM) scheme functions by comparing a modulating sinusoidal signal at desired output frequency with a high frequency (in kHz range) triangular signal acting as a carrier[2]. The advantage of this scheme is the shifting of harmonics at multiples of carrier frequency there by making the output more sinusoidal than square wave inverter. Besides, this characteristic enables the use of smaller, cheaper filters as the higher frequency harmonics are easier to filter out[3]-[10].

Recently, Voltage Source Inverters (VSIs) have become of more research interest in high power applications due to several features such as their power to get high quality of output voltage signal with reduced switching losses by semiconductor devices. The output signal of an ideal inverter is a sinusoidal waveform, however, the output for practical inverter is discontinuous and contains undesirable harmonics. The character of the output signal is normally evaluated in conditions of total harmonic distortion (THD). There are different modulation techniques utilized in inverters to generate the desired output voltage. Such inverters are classified according to switching frequency. A popular method that works with high switching frequencies is the Sinusoidal Pulse Width Modulation (SPWM)[6]-[14].

Pulse Width Modulation(PWM) techniques are applied to variable speed drives which are used in many increasingly in new industrial applications. The most widely used for voltage source inverters is Sinusoidal Pulse Width Modulation (SPWM). In Bipolar SPWM technique, the basic idea by comparing reference frequency signal with the triangular carrier to produce the bipolar PWM switching signal. When this signal is used, the upper switch and the lower switches operate

in complementary manner. In unipolar SPWM technique, the basic idea by comparing reference frequency signal with the triangular carrier to produce the bipolar PWM switching signal. When this signal is used, the upper switch and the lower switches operate in complementary manner compared with two sinusoidal reference signals that are positive and negative signals. The output voltage of the inverter transforms between zero and positive voltage or between zero and negative voltage of the fundamental frequency. In the unipolar voltage switching scheme the harmonic content of the output voltage signal is reduced compared to the result obtained in the case of bipolar switching[15]-[20].

In order to generate sinusoidal PWM pulses for the single phase inverter, The microcontroller is used because it is simpler and more flexible to change the real- time control algorithms without further modification in a hardware with its reduced cost and also it reduces the complexity of the control circuit[21]-[25].

Aircraft cabin temperature control is crucial in maintaining constant temperature inside the aircraft flying at high altitudes. In such altitudes, the atmospheric temperature and oxygen availability are very low in contrast to the requirements inside the aircraft. For constant monitoring and maintenance of temperature in real-time, the controller should be highly sensitive to parameter variations and hence require lower processing times for quick response. Traditional control method such as PID control offer faster response with lower computational overhead[26]-[32].

A Cryocooler is a refrigerator designed to reach cryogenic temperatures (below 120K / -153 °C) and its main purpose is to cool objects quickly using extremely low temperatures. There are many common applications of Cryocoolers. One of the most common is for the cooling of infrared sensors to temperatures of 80-150 K for use in military night vision equipment[29]-[32].

Cryogenic cooling systems have traditionally used cryogenic coolants like liquid nitrogen as well as specialized vapor compression systems. There are several challenges in using these technologies. For example, cryogenic coolants require periodic replacement which can be an issue especially in cases where they are located in remote areas. Vapor compression systems are limited by the coolant properties at cryogenic temperatures and extra heat addition into the system through the tubing[29]-[32].

The Electromagnetic compatibility (EMC) is the ability of electrical equipment and systems to function acceptably in their electromagnetic environment, by limiting the unintentional generation, propagation and reception of electromagnetic energy which may cause unwanted effects such as electromagnetic interference (EMI) or even physical damage in operational equipment. The goal of EMC is the correct operation of different equipment in a common

electromagnetic environment. EMI/EMC Filters are basically high pass filters that are mainly used to limit the input current fluctuations at the input stage[33].

The AVR microcontrollers such as the ATMEGA32 belong to Atmel. It provides an ATMEL Studio programming environment, which allows the programming of these microcontrollers in C language. The ATMEGA32 performs operations approaching 1 MIPS per MHZ allowing realizing systems with low power consumption and simple on the electronic level. The ATMEGA32 is a low-power circuit containing a microprocessor, 32K flash memory, 4 I / O ports and an internal oscillator. To program the ATMEGA32 microcontroller, Programmer and ATMEL studio is used. The generation of a sinusoidal wave centered on a zero voltage requires both a positive voltage and a negative voltage on the load. This can be obtained from a single source through the use of the H-bridge inverter[24]-[36].

The inverter is one of the devices for power conversion that is widely used in the world to convert the DC input voltage into alternating current output voltage. The output voltage waveform of the ideal inverters should be sinusoidal. However, the waveform of the practical inverter is non-sinusoidal and contains harmonics. The electronic devices, managed by this inverter, will be damaged by the content of the harmonic. The content of the harmonics in the output of the inverter depends on the number of pulses per cycle. Many researchers have studied that the wave of the output signal is distorted[34]-[36].

By switching the loss problem, the number of pulses per cycle is also affected. The use of high switching technology will contribute to high power losses. The main factors that must be considered in order to meet the requirements are, Cost of equipment , The size of the filter and The loss of power in the switching of the element. The most important problem to consider is the time-out control. The dead time period should be appropriate to avoid the problem of damaging the switch and the harmonic problem. If the dead time is short, it will cause damage to the switches and if it is long it will cause an increase in the total harmonic distortion[36].

1.4 Motivation

The use of conventional cooler drive inverters results in very high THD AC output voltage from a DC battery and has very poor line and load regulation, hence these drawbacks can be overcome by developing a prototype of cooler drive inverter by implementing voltage feed forward control technique and PID controller algorithm for the cooler drive inverter to maintain the constant output voltage and temperature(150K) for wide range of DC input and LC filter to get the low THD AC output voltage, that can be used for the control of temperature in the cryogenic cooler used in space and defence application.

In order to obtain clean noise free AC voltage and to improve the performance of the cooler drive, the inverter and cryogenic cooler drives plays an important role in providing low THD AC output voltage from a DC battery and to get the low temperature in the range of the liquid nitrogen temperature(150K) to cool down the temperature gradient sensitive infrared sensor.

1.5 Objectives

Following were the objectives of the proposed prototype.

- To design digitally controlled cooler drive inverter for temperature control.
- To Implement Voltage Feed-forward control technique for correcting voltage regulation at the output.
- To develop Controller algorithm using PID for temperature regulation.
- To Generate Sinusoidal PWM Pulses for the H-Bridge Inverter using ATmegaS128 microcontroller.
- To Analyse the efficiency of the cooler drive inverter.
- To Develop Hardware Prototype and testing for the cooler drive inverter.

1.6 Problem Statement

Design and Implementation of Digitally Controlled Cooler Drive Inverter for Temperature Control in Cryocoolers used for cooling of infrared sensors to temperatures of 80-150K for use in military night vision equipment for space and defence application.

1.7 Organization of the report

The project report consists of total seven chapters. An introduction to each phase in developing the work is listed as follows

Chapter-1 explains the brief introduction of Cooler Drive Using H-Bridge Inverter and relevant literature survey. It also includes objectives of the project, motivation, problem statement and the organization of the report.

Chapter-2 discusses the theory and concepts of H-Bridge Inverter topology, Bipolar and Unipolar PWM Techniques, ATmegaS128 Micro Controller Configurations, PIN Configurations and PIN Description, Inverter resolution, Launch lock procedure, Controlling techniques, Temperature sensing diode input, MIL-STD-461E, CE102 Testing.

Chapter-3 discusses the methodology, block diagram, Relay Sequencing, Implementation algorithm and Flow Chart of the proposed prototype.

Chapter-4 discusses the Specification and Design details of the proposed prototype.

Chapter-5 discusses the Simulation and Hardware Implementation of the proposed prototype.

Chapter-6 discuss the results of the proposed cooler drive inverter.

Chapter-7 discusses the overall conclusion drawn from the project and the future works that can be carried out.

Followed by the References consisting of list of papers referred for the understanding and analyzing the project work.

CHAPTER 2

H-BRIDGE INVERTER TOPOLOGY

The basics of H-Bridge Inverter topology, Bipolar and Unipolar PWM Techniques, ATmegaS128 Micro Controller Configurations, PIN Configurations and PIN Description, Inverter resolution, Launch lock procedure, Controlling techniques, Temperature sensing diode input, MIL-STD-461E, CE102 are discussed in this chapter.

2.1 Single phase H-Bridge Inverter

A full H-bridge topology contains of two legs, each branch takes in two power semiconductor switches (MOSFET or IGBT). The center stage of these legs is connected across the load . Fig 2.1 represents the single phase H-Bridge Inverter , The H-bridge inverter can work with bipolar or unipolar scheme. The output voltage waveform of the bipolar inverter between an output connection of DC voltages (+Vdc, - Vdc), while the output voltage signal of the unipolar system is between (+Vdc, 0, - Vdc) which named three level inverter. In the unipolar inverter topology, the Total Harmonic Distortion of the output waveforms is optimum and minimum compared to similar results in the case of bipolar inverter switching[6]-[12].

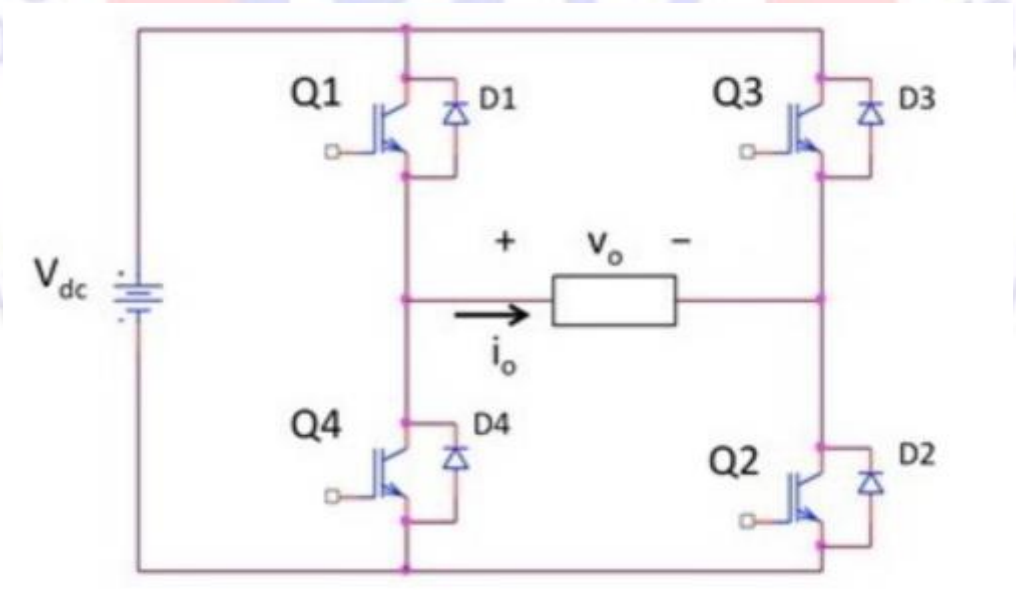

Fig 2.1 : Single phase H-Bridge Inverter

A low-pass filter has been widely used with a DC/AC inverter to mitigate the harmonics which caused by semiconductor switching. Hence LCL filter as shown in Fig. 2.2 is used to reduce high order harmonics. It can be applied at a lower switching frequency for the PWM inverter because its attenuation is 60 dB/decade for frequencies above the resonant frequency.

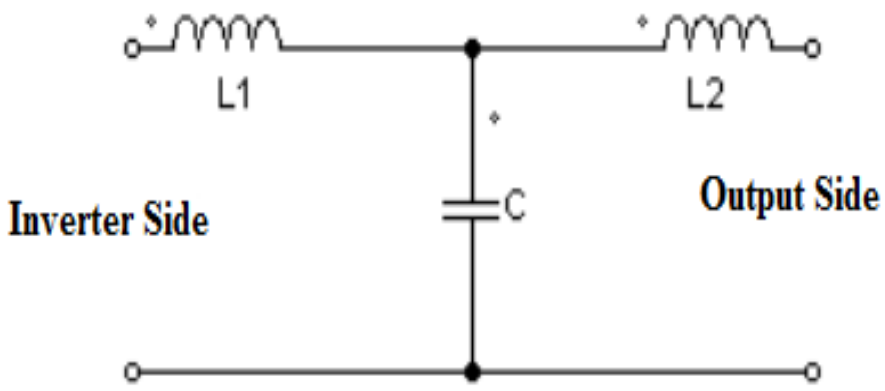

Fig. 2.2 : LCL filter circuit diagram.

2.2 Bipolar Pulse width modulation technique

The bipolar PWM modulation controls the inverter and generates the pulses for its gate driver by comparing the reference signal with the carrier-signals as shown in Fig. 2.3. The fundamental frequency or the reference signal, also known as modulating frequency, corresponds to the desired output voltage frequency and is 50 Hz for an inverter. In the bipolar PWM scheme the two switches of each leg are switched in a complementary way. Using this modulation technique in the H-bridge inverter shown in Fig. 2.3, the switch pairs T1, T4 (state S3) and T2, T3 (state S2) are switched simultaneously, Table 2.1 Represents Switching states of an H-bridge inverter using bipolar PWM technique , When the reference signal is higher than the carrier-signal i.e., vref > vcr, the first pair is switched on, otherwise the other pair is switched on as shown in Table 2.1. The H-bridge inverter output voltage contains only two levels ±Vbatt, therefore it is called bipolar PWM[11]-[14].

Table 2.1 : Switching states of an H-bridge inverter using bipolar PWM[11].

Condition	Switching state	T1	T2	T3	T4
$v_{ref} < v_{cr}$	S2	0	1	1	0
$v_{ref} > v_{cr}$	S3	1	0	0	1

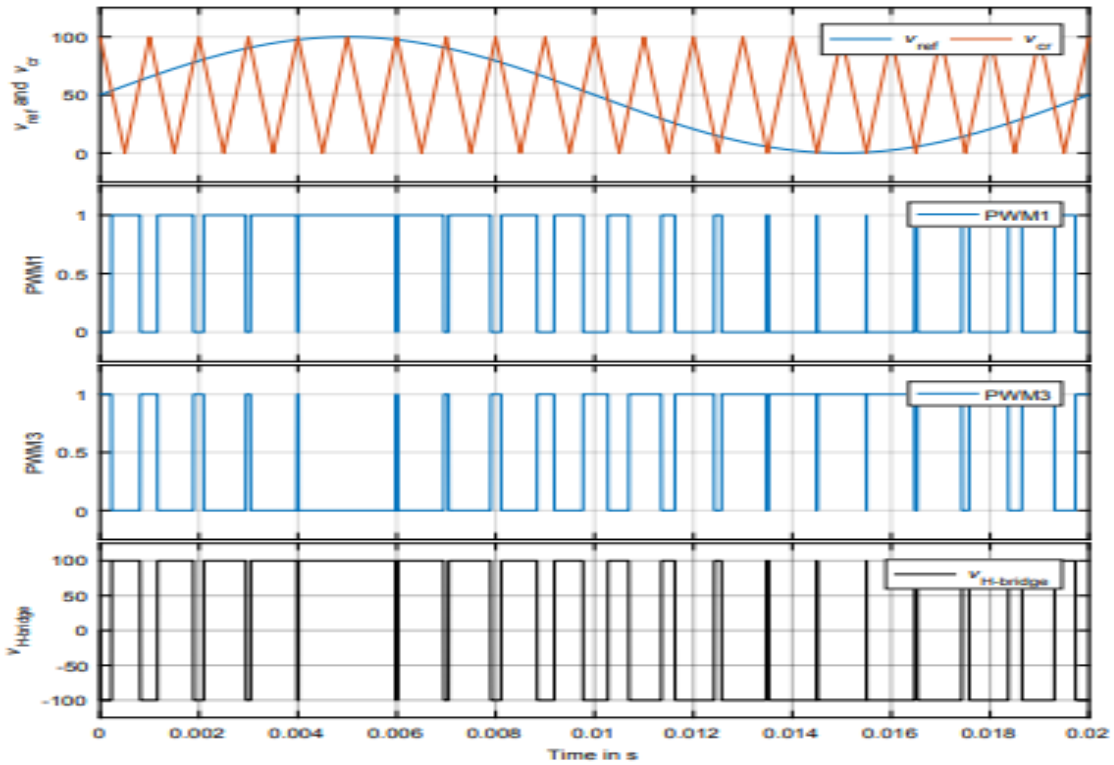

Fig 2.3 : H-bridge inverter bipolar PWM function principle using ideal sinusoidal signal with fundamental frequency Fref = 50 Hz and carrier-signal with switching frequency of Fsw = 1 kHz (top plot). Both plots in the middle represent pulse signals for switches S1 and S3. The bottom plot shows the resulting two-level H-bridge inverter output voltage using bipolar PWM.

2.3 Unipolar Pulse Width Modulation Technique

When unipolar PWM is used, under similar conditions as the previous bipolar PWM, the resulting switching states are shown in Table 2.2. Unlike the bipolar PWM, the power semiconductors are not switched simultaneously[11]. Fig. 2.4 represents the unipolar PWM function principle in an H-bridge inverter. Two signals are required and are compared to one other signal. Even the sinusoidal reference signal or the carrier-signal can be inverted. Fig. 2.4 shows that by using the unipolar PWM technique similar inverter operation is reached when the carrier-signal or the sinusoidal reference signal are inverted. The carrier-signal inversion is achieved using the multiplication with −1 (mirrored, |vref − 100|) or by shifting it with an offset of 180°, which is practically not easy to implement because modulators are generally implemented in one hardware component. The inversion of the reference signal is easier for possible implementation and is further followed[12]-[26].

The second and third plot in Fig. 2.4 represent the PWM signal for the power switch T1 and T3 respectively. The signal in the second plot is similar to the signal using the bipolar PWM.

The H-bridge inverter output voltage is shown in the fourth plot and contains three voltage steps at the AC-side while using unipolar PWM. The resulting inverter switching frequency, using unipolar PWM, is twice as high compared to the bipolar PWM. The resulting inverter voltage also has three levels instead of two as shown in Fig. 2.4 . Therefore, this modulation technique is used to present the operation of single-phase AC drives connected inverter[12]-[36].

Table 2.2 Switching states of a H-Bridge inverter using unipolar PWM[11].

Condition	Switching state
$v_{ref} > v_{cr}$	$T1 = 1; T2 = 0$
$v_{ref} < v_{cr}$	$T1 = 0; T2 = 1$
$-v_{ref} + 100 > v_{cr}$	$T3 = 1; T4 = 0$
$-v_{ref} + 100 < v_{cr}$	$T3 = 0; T4 = 1$

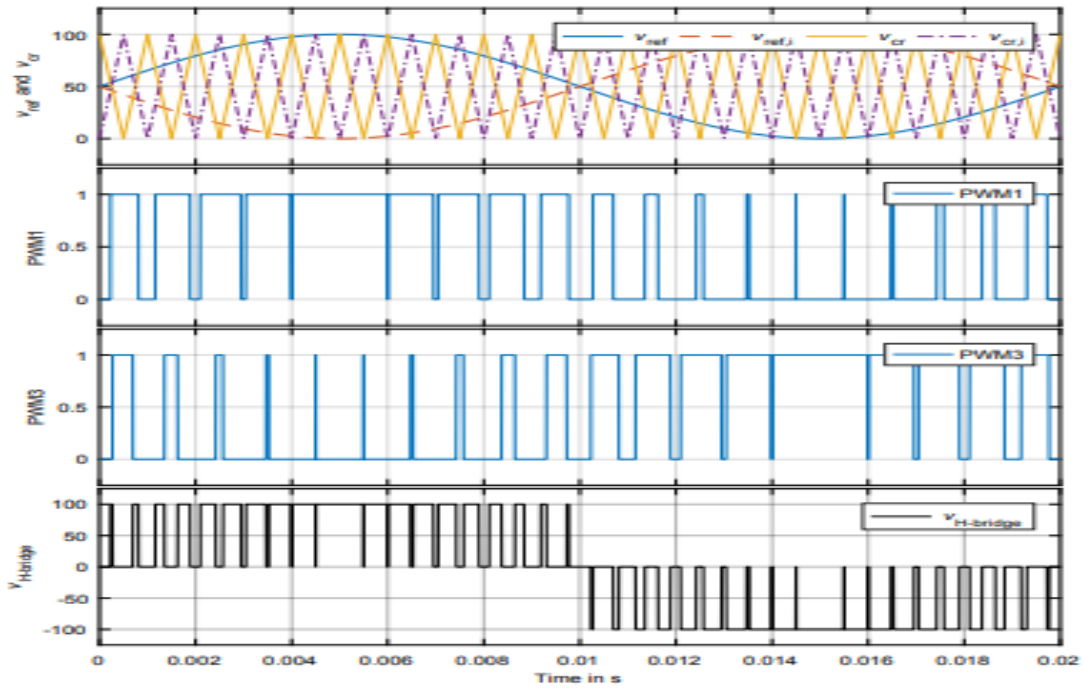

Fig 2.4 : H-bridge inverter unipolar PWM function principle using ideal sinusoidal signal with fundamental frequency fref = 50 Hz and carrier-signal with switching frequency of fsw = 1 kHz (top plot). Both plots in the middle represent pulse signals for switches S1 and S3. The bottom plot shows the resulting three-level H-bridge inverter output voltage using unipolar PWM [11].

2.4 ATmegaS128 MICRO CONTROLLER

The new Atmel® AVR® ATmegaS128 microcontroller (MCU) brings the industry-leading AVR core to the aerospace industry. The ATmegaS128 MCU is designed for enhanced radiation performance and increased reliability in space applications. Table 2.3 depicts the configuration of ATmegaS128 Micro Controller and Fig 2.5 shows the PIN Configuration of ATmegaS128 Microcontroller. It takes advantage of mature Atmel AVR tools designed and used in the mass market worldwide for many years. The ATmegaS128 microcontroller targets many of the most common space applications, which typically require a small footprint, low power and analog control of motors and sensors.

Table 2.3 : Configuration of ATmegaS128 Micro Controller

FEATURES	ATmegaS128
Pin count	64
Flash (KB)	128
SRAM (KB)	4
EEPROM (KB)	4
External Memory (KB)	64
General Purpose I/O pins	53
SPI	1
TWI (I^2C)	1
USART	2
ADC	10-bit, up to 76.9ksps (15ksps at max resolution)
ADC Channels	8
AC propagation delay	Typ 400ns
8-bit Timer/Counters	2
16-bit Timer/Counters	2
PWM channels	6
RC Oscillator	+/-3%
Operating voltage	3.0-3.6V
Max operating frequency	8 MHz
Temperature range	-55°C to 125°C
JTAG	Yes

2.4.1 ATmegaS128 Micro Controller PIN Configuration

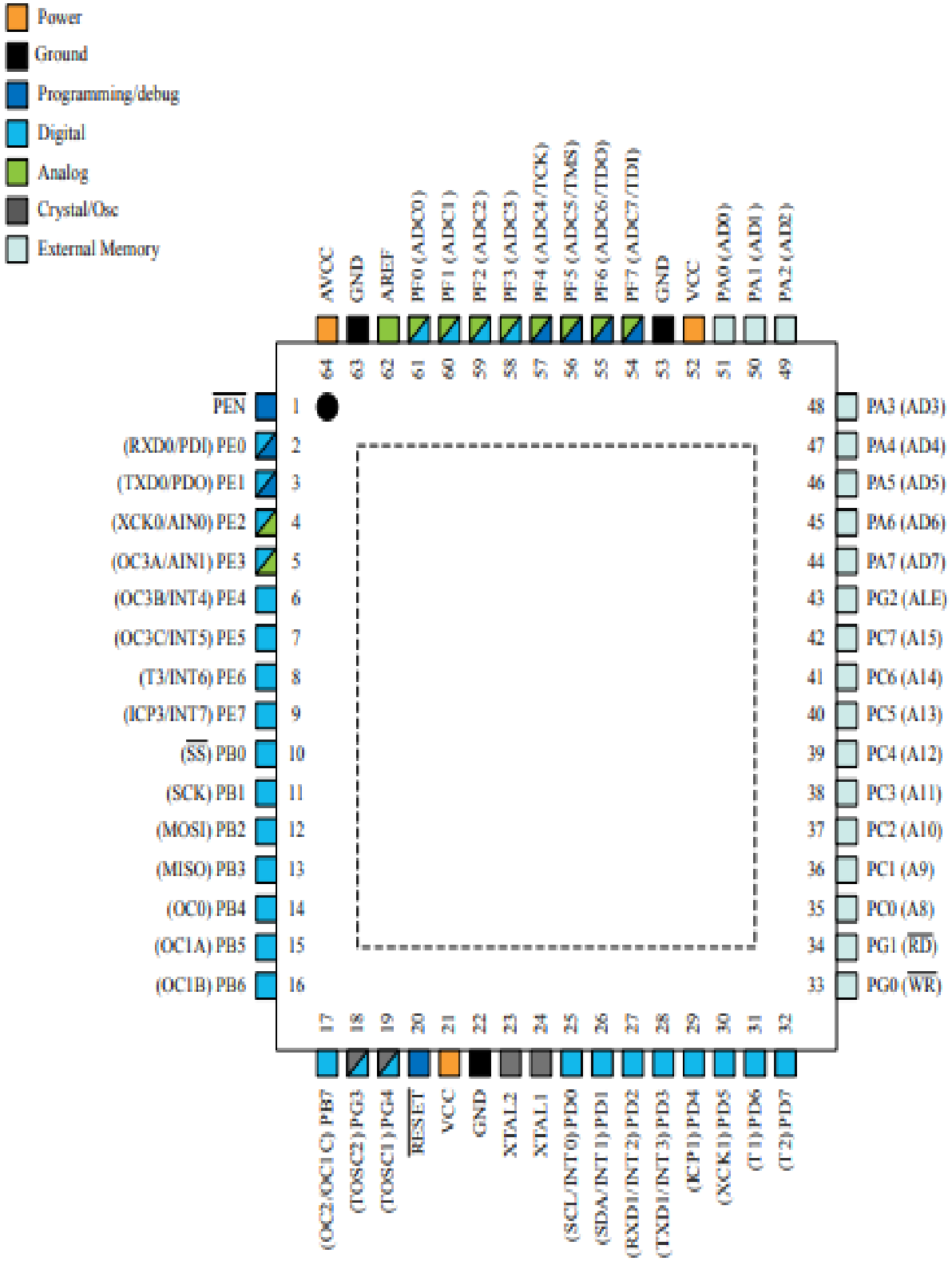

Fig 2.5 : PIN Configuration of ATmegaS128 Micro Controller

2.4.2 ATmegaS128 Micro Controller PIN Description

- **VCC** : Digital supply voltage.
- **GND** : Ground.
- **Port A (PA7:PA0)**

  Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tristated when a reset condition becomes active, even if the clock is not running.
- **Port B (PB7:PB0)**

  Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tristated when a reset condition becomes active, even if the clock is not running.
- **Port C (PC7:PC0)**

  Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tristated when a reset condition becomes active, even if the clock is not running.
- **Port D (PD7:PD0)**

  Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tristated when a reset condition becomes active, even if the clock is not running.
- **Port E (PE7:PE0)**

  Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tristated when a reset condition becomes active, even if the clock is not running.

- **Port F (PF7:PF0)**

  Port F serves as the analog inputs to the A/D Converter. Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a Reset occurs. The TDO pin is tri-stated unless TAP states that shift out data are entered. Port F also serves the functions of the JTAG interface. In ATmega103 compatibility mode, Port F is an input Port only.

- **Port G (PG4:PG0)**

  Port G is a 5-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tristated when a reset condition becomes active, even if the clock is not running. Port G also serves the functions of various special features. The port G pins are tri-stated when a reset condition becomes active, even if the clock is not running. In ATmega103 compatibility mode, these pins only serves as strobes signals to the external memory as well as input to the 32kHz Oscillator, and the pins are initialized to PG0 = 1, PG1 = 1, and PG2 = 0 asynchronously when a reset condition becomes active, even if the clock is not running. PG3 and PG4 are oscillator pins.

- **$\overline{\text{RESET}}$**

  Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in System and Reset Characteristics. Shorter pulses are not guaranteed to generate a reset.

- **XTAL1**

  Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

- **XTAL2**

  Output from the inverting Oscillator amplifier.

- **AVCC**

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to VCC, even if the ADC is not used. If the ADC is used, it should be connected to VCC through a low-pass filter.

- **AREF**

  AREF is the analog reference pin for the A/D Converter.

- **PEN**

  PEN is a programming enable pin for the SPI Serial Programming mode, and is internally pulled high. By holding this pin low during a Power-on Reset, the device will enter the SPI Serial Programming mode. $\overline{\text{PEN}}$ has no function during normal operation.

2.5 Control techniques

There are various control techniques like,

- Voltage mode control
- Current mode control
- Voltage feed forward control

2.5.1 Voltage mode control

Fig 2.6 shows a conventional voltage mode control circuit. The circuit has a voltage divider network, an error amplifier, a PWM modulator, a constant frequency saw tooth ramp and a reference voltage. Voltage divider network is used to scale down the output voltage so that an error signal can be generated using an error amplifier. This error is proportional to the error between the scaled output voltage and the reference voltage[8]-[10]. This error signal is compared with a fixed frequency fixed slope saw tooth ramp voltage to generate the desired PWM pulses and to drive the switch. Due to the negative feedback in the loop, error amplifier output changes such that duty cycle is modulated to maintain the constant output voltage. Impedances Z_1 and Z_2 are used to provide a proper gain, bandwidth and frequency compensation for the loop to be stable under all operating conditions.

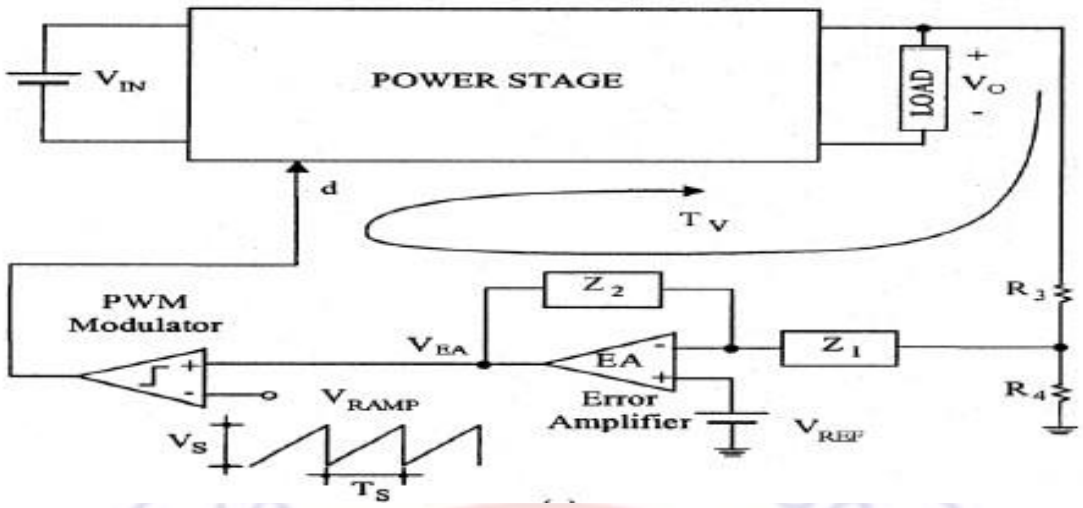

Fig 2.6 : Block diagram of voltage mode control method.

Fig 2.7 shows the transient response waveforms for the voltage mode control for a positive line voltage transient. At $t=T_o$, voltage V_{in} experiences a positive step change. Because of the slow response of the voltage feedback loop, the control voltage V_{EA} starts responding slowly after some time. The duty cycle remains unchanged in the event of sudden change in input voltage, thus the output voltage experiences a high voltage overshoot transient.

Thus, the voltage mode control technique suffers from a major drawback of slow response to input voltage transients. To fasten the response and to reduce the transient output voltage overshoot caused by the input voltage change, the duty cycle of the controller has to respond instantaneously to input voltage changes. This is accomplished by the voltage feed forward technique[8]-[10].

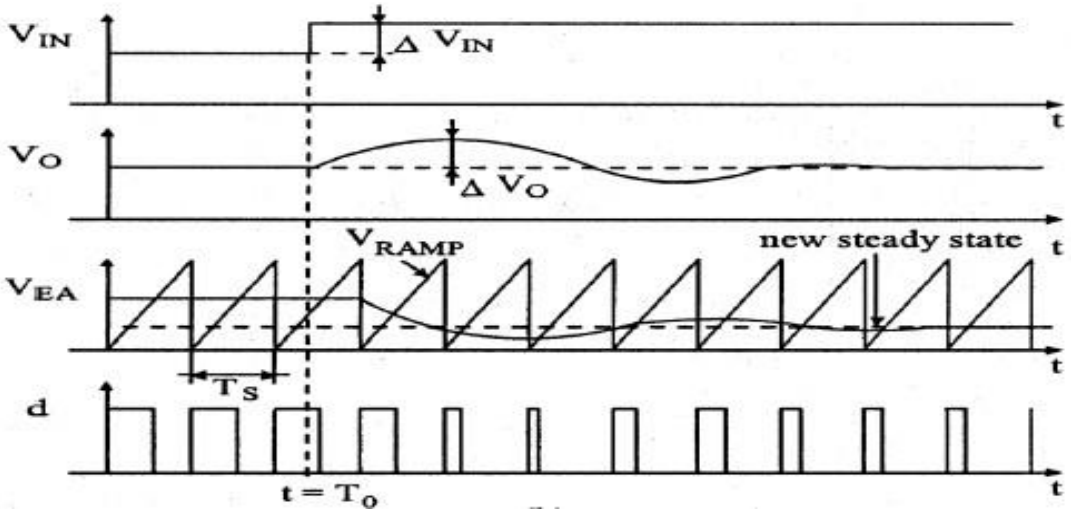

Fig 2.7 : Key waveforms during step change in V_{in} for voltage mode control.

2.5.2 Voltage feed forward control

Block diagram of voltage feed forward control is as shown in Fig. 2.8. In this method instead of fixed slope saw tooth ramp, a ramp whose slope varies in proportion to the input voltage variation is used at the PWM modulator input[8]-[10]. The input voltage is first sensed and attenuated using the voltage divider constituted of resistors R_1 and R_2. It is then inverted before being brought to the input of the integrator. Integrator is reset at the starting of each cycle by an external fixed frequency clock signal. Since in this control technique the slope of the ramp is proportional to the input voltage, and the output voltage of the error amplifier is compared with this ramp to generate duty cycle. Any change in the input voltage causes immediate change in the duty cycle even if the bandwidth of voltage loop is very low.

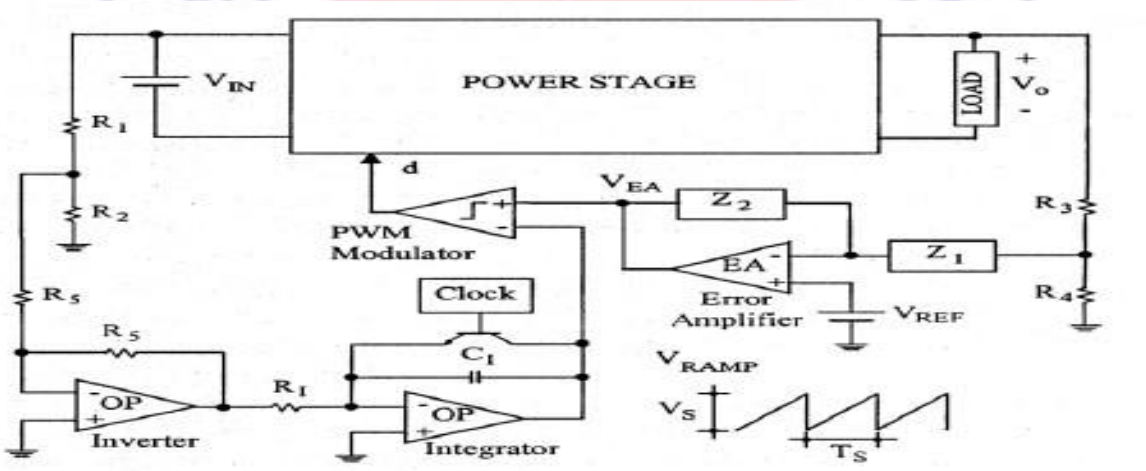

Fig. 2.8: Block diagram of voltage feed forward control.

After the input voltage is increased, at $t=T_o$, the slope of the ramp increases causing the duty cycle to reduce immediately so as to maintain the output voltage constant as shown in Fig. 2.9. Because of this instantaneous change in duty cycle, output voltage overshoot caused because of the input step change is decreased. Any increase in input causes the decrease in duty cycle. Thus good line regulation is achieved.

The operation of the feed forward scheme is described by following equations.

$$Vs = \left(\frac{Vin}{k}\right) \tag{2.1}$$

$$D = \left(\frac{Ton}{T}\right) = \left(\frac{Vc}{Vs}\right) = \left(\frac{KV_c}{Vin}\right) \tag{2.2}$$

Where,

D: Duty ratio

K: Constant

V_{in}: Input voltage

V_s: Peak-Peak Saw tooth Voltage

V_c: Control Voltage

Input Voltage feed forward technique provides the following advantages:

- Improved line transient performance.
- Freedom of V_o from V_{in} dependence minimizes the EA gain requirements while maintaining the adequate regulation.
- The audio susceptibility of the feed-forward method is good because of the cycle-by-cycle compensation for input voltage variations.
- The constant volts-second product of the main transformer primary allows the designer to optimize the size and cost.

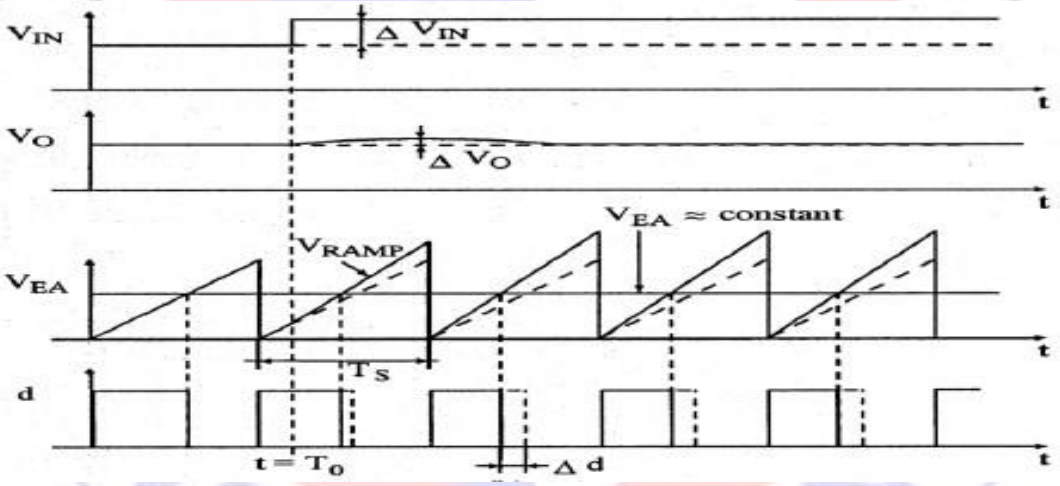

Fig. 2.9 : Key waveforms during step change in V_{in} for voltage mode feed forward control.

2.6 Temperature Sensing Diode Input

The converter (DC-AC) has been equipped with a separate 1mA current source to bias a temperature sensing diode. Fig. 2.10 and Fig. 2.11 represents the temperature sensing diode input and the Illustration of Temperature Sensing Diode Voltage versus Inverter Output Voltage . The voltage measured across the sensing diode is used by the control algorithm in the converter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature.

The temperature stability is strongly dependent on the correct measurement of the diode sensor voltage. The value for the diode set-point voltage should be programmed in the converter

by means of a software setting. This voltage "set-point" should be able to be adjusted within a range of 0.5 to 2 Volts.

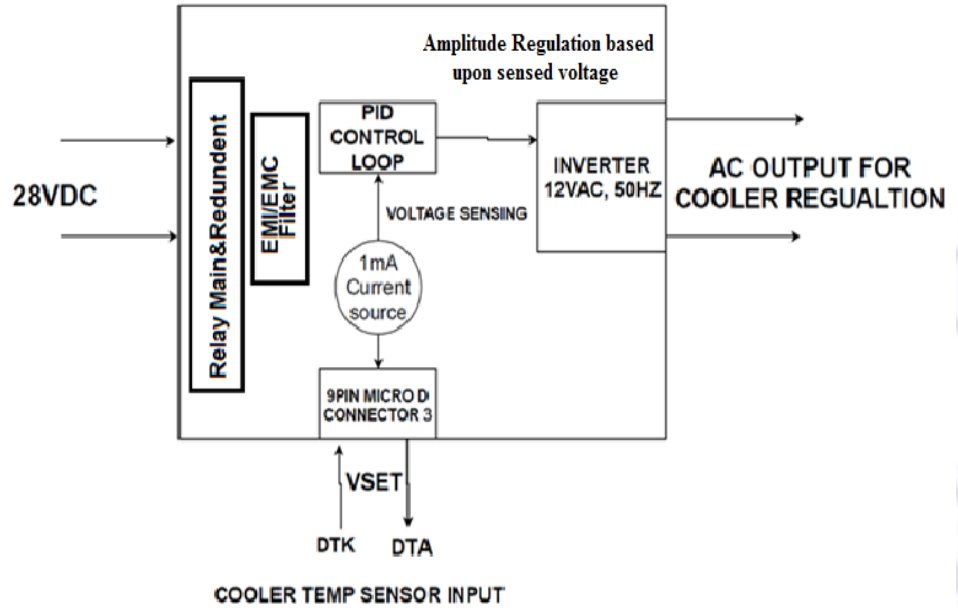

Fig 2.10 : Temperature Sensing Diode Input

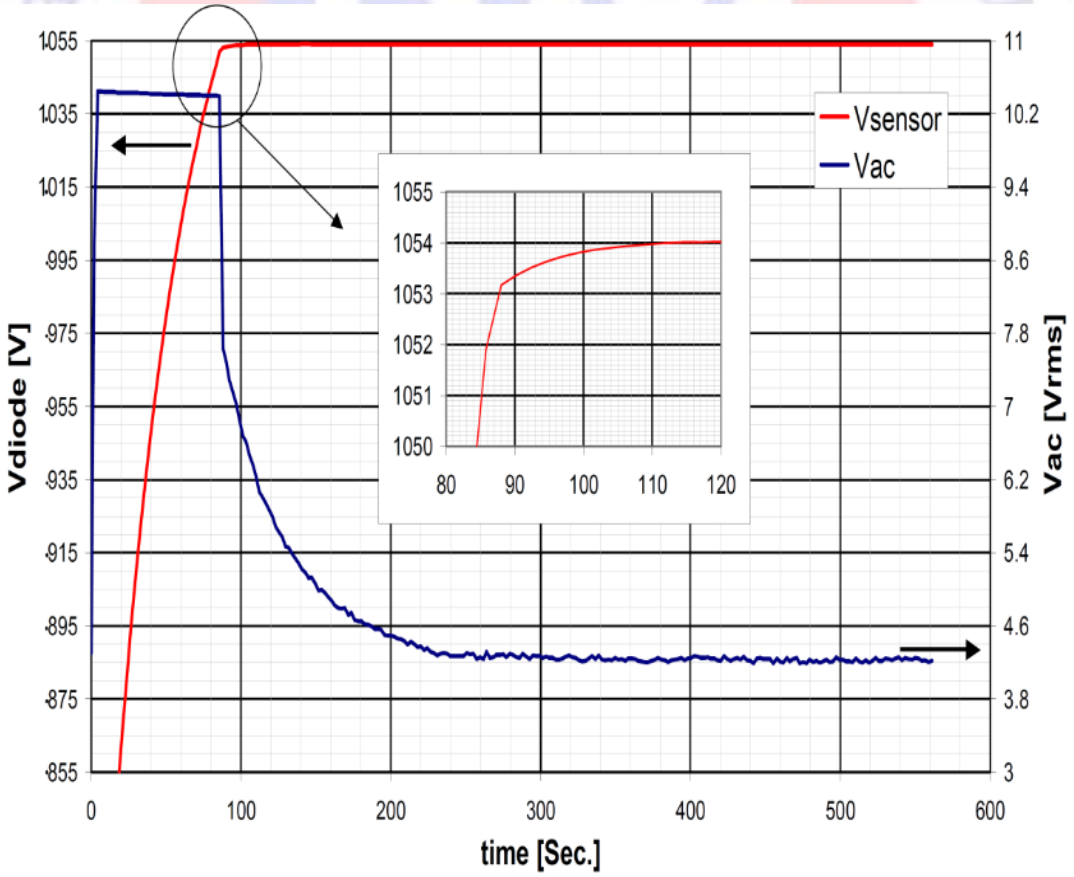

Fig 2.11 : Illustration of Temperature Sensing Diode Voltage versus Inverter Output Voltage

2.7 Launch Lock Procedure

The Launch lock procedure is aimed at maintaining the compressor during the launching phase. To protect the compressor pistons during shock and vibration loads, it is recommended to apply a launch lock connection. In launch lock mode, the wires of each coil are short-circuited. Due to the nature of the launch lock, the current running through the connection wires will be quite high. A current of twice the nominal current is expected The short circuit should have a resistance value as close as possible to zero ohms.

2.8 Inverter Resolution

The performance requirements for the inverter controller can be easily demonstrated as follows. The switching frequency should be higher than 15 kHz. Table 2.4 shows the prescalar and corresponding PWM Switching Frequency. When using 8 MHz clock frequency and 8-bit counter in the phase corrected PWM mode, the switching frequency is given by,

$$Fpwm = \frac{Fosc}{Prescalar * Countermax} \quad (2.3)$$

Table 2.4 : Prescalar & PWM Switching Frequency

Phase Corrected PWM Oscillator Frequency: f_{OSC} = 8MHz	
Prescalar (N)	PWM Switching Frequency f_{PWM} (Hz)
1	15686.27
8	1960.78
32	490.19
64	245.09
128	122.54
256	61.27
1024	15.32

When using the phase-correct mode, the modulation frequency will be 15.68 kHz. From Eq. (2.3), it is obvious that the core of the microcontroller will be forced to handle the interrupt from counter every 510 machine cycles.

One of the basic techniques for limiting calculations is the usage of a look-up table. This technique can be demonstrated on the calculation of the sine function. If we know that the input data will always be in the range from 0 to 255 - i.e., with an accuracy of 8 bits and the desired result will be also in the same range, the simplest solution is to allocate an array of 256 elements to which the individual results will be pre-calculated. The calculation functions can be then limited to a simple memory access, which is much faster.

2.9 Sine Wave Functions (Lookup Table)

The simplest way to generate sine waves is through a lookup table. One simply needs to determine the maximum allowable distortion along with the maximum operating frequency. Using these two criteria, the number of sample points needed can be determined.

Sample points = 100 / (% allowable voltage step inaccuracy)

Sample time = (Sample Points) • (Frequency)

- **Example:1**

2 kHz Sine wave, <8% voltage step inaccuracy,

Sample points = 100/5 = 20 points

Sample time = 20 • 2,000 = 40 kHz =25µs/Sample

- **Example:2**

50 Hz Sine wave, <0.2% voltage step inaccuracy

Sample points = 100/0.2 = 500 points

Sample time = 1/(500 • 50) = 1/25 kHz =40µs/Sample

- ✓ **For Finding Voltage Step inaccuracy:**

For 15KHz PWM Switching Frequency

Sampling points: f_{PWM}/f_O = 15000/50 = 300 Points

voltage step inaccuracy: 100/Sample points = 100/300 = 0.33%

Hence in 50 Hz Sine wave, <0.33% Voltage Step Inaccuracy.

Sample time = 300 • 50 = 15 kHz =66.67µs/Sample

- ✓ **For Maximum Sample:**

Voltage step inaccuracy: 100/Sample points = 100/500 = 0.2 %

Voltage step inaccuracy: 100/Sample points = 100/1000 = 0.1%

Sample time = 1/(1000 • 50 = 50kHz =66.67µs/Sample =20 µs/Sample

To generate a single sine wave, the user simply needs to create a lookup table with the correct number of sample points. Next the software steps through each sample point and moves this value to the register.

2.10 MIL-STD-461E CE102 EMI/EMC Testing

2.10.1 CE102 applicability.

This requirement is applicable from 10 kHz to 10 MHz for all power leads, including returns, that obtain power from other sources not part of the EUT.

2.10.2 CE102 limits.

Conducted emissions on power leads shall not exceed the applicable values as shown in Fig 2.12.

2.10.3 CE102 test procedure.

- **Purpose.**

This test procedure is used to verify that electromagnetic emissions from the EUT do not exceed the specified requirements for power input leads, including returns[5].

- **Test equipment.**

The test equipment shall be as follows:

a. Measurement receiver

b. Data recording device

c. Signal generator

d. Attenuator, 20 dB, 50 ohm

e. Oscilloscope

f. LISNs

- **Setup.**

The test setup shall be as follows:

a. Maintain a basic test setup for the EUT.

b. Calibration.

(1) Configure the test setup for the measurement system check as shown in Fig 2.13, CE102-2. Ensure that the EUT power source is turned off.

(2) Connect the measurement receiver to the 20 dB attenuator on the signal output port of the LISN.

c. EUT testing.

(1) Configure the test setup for compliance testing of the EUT as shown in Fig 2.14, CE102-3.

(2) Connect the measurement receiver to the 20 dB attenuator on the signal output port of the LISN.

- **Procedures.**

The test procedures shall be as follows:

a. Calibration. Perform the measurement system check using the measurement system check setup of Fig 2.13, CE102-2.

(1) Turn on the measurement equipment and allow a sufficient time for stabilization.

(2) Apply a signal level that is at least 6 dB below the limit at 10 kHz, 100 kHz, 2 MHz and 10 MHz to the power output terminal of the LISN. At 10 kHz and 100 kHz, use an oscilloscope to calibrate the signal level and verify that it is sinusoidal. At 2 MHz and 10 MHz, use a calibrated output level directly from a 50 signal generator.

(3) Scan the measurement receiver for each frequency in the same manner as a normal data scan. Verify that the measurement receiver indicates a level within ±3 dB of the injected level. Correction factors shall be applied for the 20 dB attenuator and the voltage drop due to the LISN 0.25 microfarad coupling capacitor.

(4) If readings are obtained which deviate by more than ±3 dB, locate the source of the error and correct the deficiency prior to proceeding with the testing.

(5) Repeat the above procedure for each LISN.

b. EUT testing. Perform emission data scans using the measurement setup of Fig 2.14, CE102-3.

(1) Turn on the EUT and allow a sufficient time for stabilization.

(2) Select an appropriate lead for testing.

(3) Scan the measurement receiver over the applicable frequency range, using the bandwidths and minimum measurement times.

(4) Repeat 2.9.3.4b(2) and 2.9.3.4b(3) for each power lead.

- **Data presentation.**

Data presentation shall be as follows:

a. Continuously and automatically plot amplitude versus frequency profiles on X-Y axis outputs. Manually gathered data is not acceptable except for plot verification.

b. Display the applicable limit on each plot.

c. Provide a minimum frequency resolution of 1% or twice the measurement receiver bandwidth, whichever is less stringent, and a minimum amplitude resolution of 1 dB for each plot.

d. Provide plots for both the measurement system check and measurement portions of the procedure.

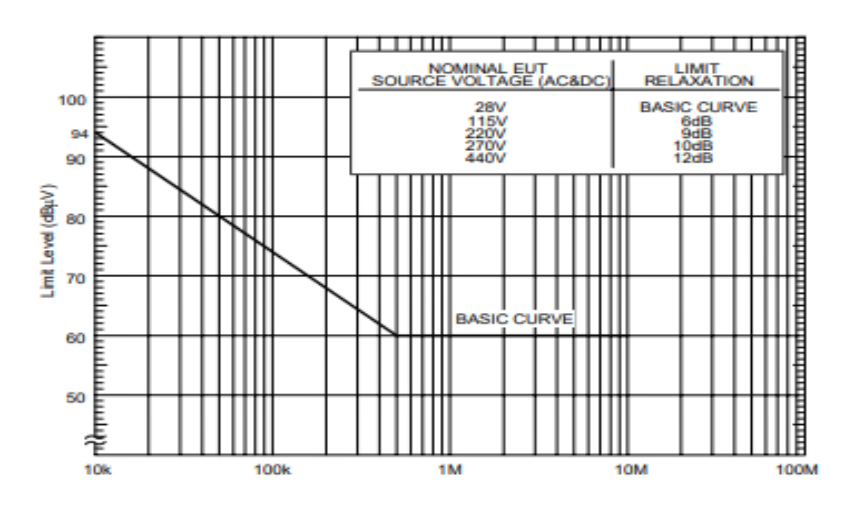

Fig 2.12 : CE102-1. CE102 limit (EUT power leads, AC and DC) for all applications.

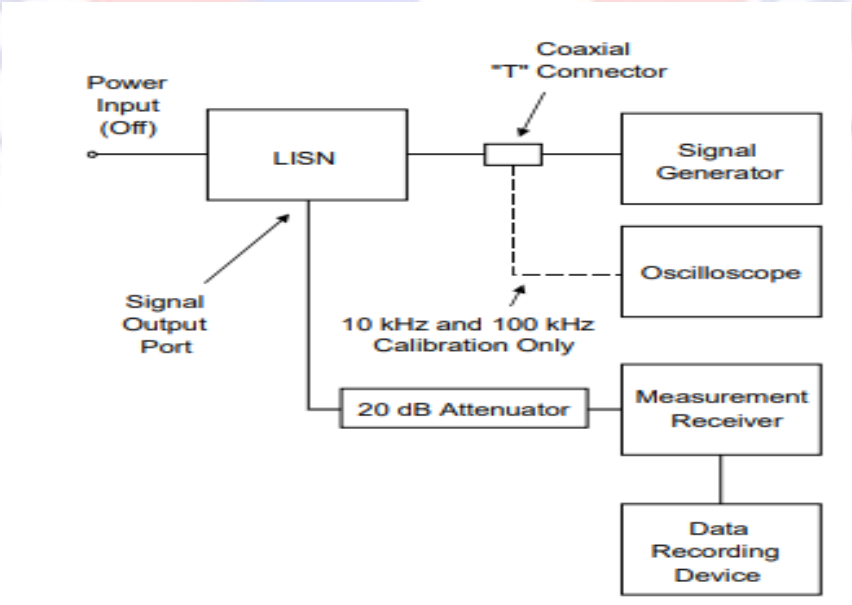

Fig 2.13 : CE102-2. Measurement system check setup

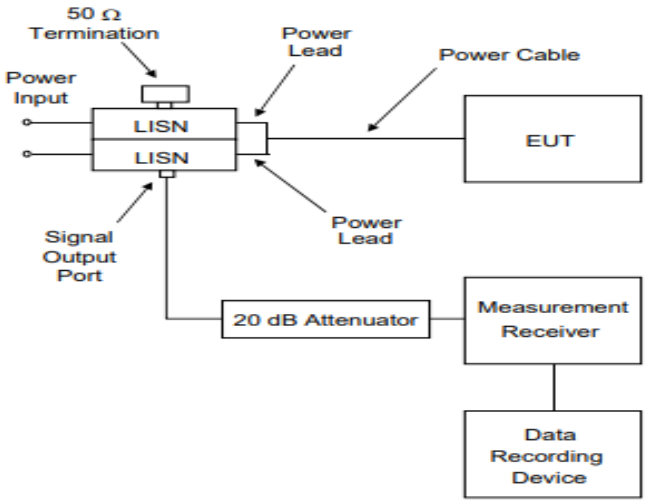

FIG 2.14 : CE102-3. Measurement setup.

2.11 Summary

In this chapter the concept of H-Bridge Inverter, Unipolar and bipolar PWM Techniques, ATmegaS128 Micro Controller Configurations, PIN Configurations and PIN Description, Inverter resolution, Launch lock procedure, Controlling techniques, Temperaure sensing diode input, MIL-STD-461E, CE102 Testing were studied in brief.

CHAPTER 3

METHODOLOGY AND BLOCK DIAGRAM

This chapter discusses about the methodology, block diagram, Relay Sequencing, Implementation algorithm and flow Chart of the proposed prototype.

3.1 Methodology

The methodology involved in developing the work is as shown in Fig 3.1

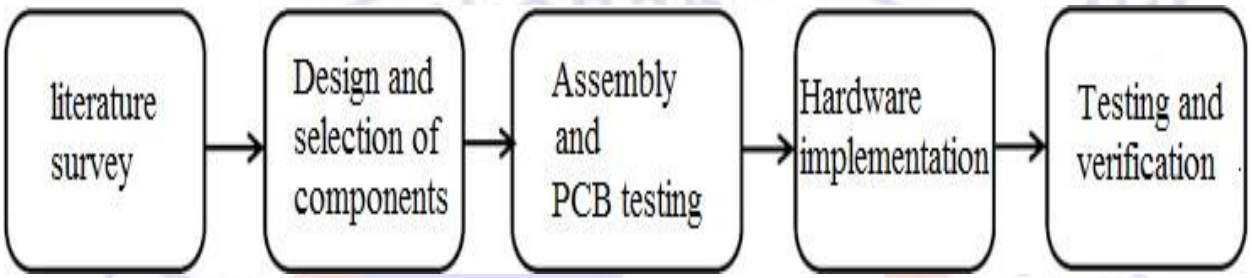

Fig 3.1: Methodology in design of converter(DC-AC)

- **Planning**

Efficient converter topology was selected by comparing with various topologies. The selected topology in this project was "H-Bridge Inverter".

- **Design and selection of components**

An H-Bridge inverter with single AC output for a wide-range of input was designed. The design of cooler drive inverter involves PID controller algorithm for temperature regulation, Controlling of PWM pulses for H-Bridge Inverter using ATmegaS128 Microcontroller, Design of filter components and design of inductor. The tools used for design were "SMath", and for schematics and simulations, "orcad" , "PSIM", "MATLAB/Simulink" and "LTspice" were used.

- **Assembly and PCB testing.**

PCB board was tested for the correct circuit paths and continuity is checked at different ground points etc. Selected components were assembled in the verified PCB according to the component designation.

- **Hardware Implementation.**

The assembled PCB was checked and the test setup was made for the analysis and testing purposes.

- **Testing and verification.**

The Hardware implemented Inverter was analyzed and the performance of cooler drive inverter were tested under input voltage range from 24-36V DC under resistive load of 3Ω and under motor load conditions.

3.2 Block Diagram

The General, Functional block diagram and interface block diagram of the proposed prototype is as shown in Fig 3.2, Fig 3.3 and Fig 3.4. The Hardware Prototype interfaces with the cooler by supplying it with an AC voltage. It takes 28V DC as input power supply. The prototype basically generates AC power via a PID control loop to control the cooling on detector array based upon the input from the temperature sensor mounted on detector Focal Plane Array(FPA). Three Latch Type relays(ON/OFF type Relays) are used namely, Relay main, Relay redundant and launch lock relay and their commands are controlled via the Relay command input connector.

Since the input current will be fluctuating , The EMI/EMC filters are used at the input stage to filter out the fluctuations in the input current. The filtered DC input is given to the H-bridge inverter. The ATmegaS128 microcontroller output signal drives an H-bridge, pulse-width modulated (PWM) output stage. Since the output from the H-bridge inverter is sinusoidally variable pulses and to minimize the amount of generated EMI, sufficient output filtering has been used and finally it is given to the output low pass filter to get pure sinusoidal pulses and finally is given to the cooler drive(Pure noise free AC power)[5]-[12].

The RMS output voltage is determined by the temperature control loop. Feedback for the control loop is provided by the temperature signal. The converter (DC-AC) has been equipped with a separate 1mA and 25uA constant current source to bias a temperature sensing diode . In order to increase the relative accuracy of the thermal sensor, it is supplied with 1mA, 25uA and is connected to cooler PID control loop.

Temperature sensor is a Base/Emitter silicon junction of a transistor 2N2222A .The voltage measured across the sensing diode is used by the control algorithm in the converter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature. The temperature stability is strongly dependent on the correct measurement of the diode sensor voltage. The value for the diode set-point voltage should be programmed in the converter by means of a software setting[29].

This voltage “set-point” should be able to be adjusted within a range of 0.5 to 2 Volts. During a cool down, the maximum RMS voltage can be limited depending on the ambient temperature, time after restart or the actual cold tip temperature. The maximum output voltage as

well as the limitation criteria are programmed in the converter and can be adjusted according to cooler and system parameters. The thermal transfer characteristics(time constant) of the cooler detector can be used in the design of feedback loop.

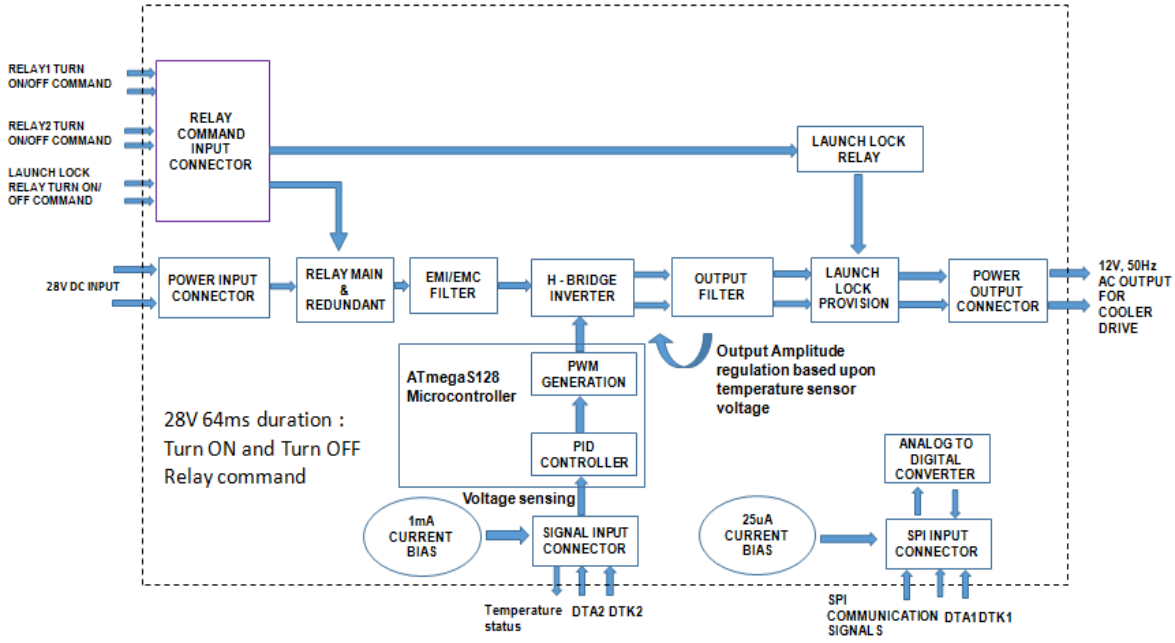

Fig 3.2 : General Block diagram of the Cooler Drive Inverter

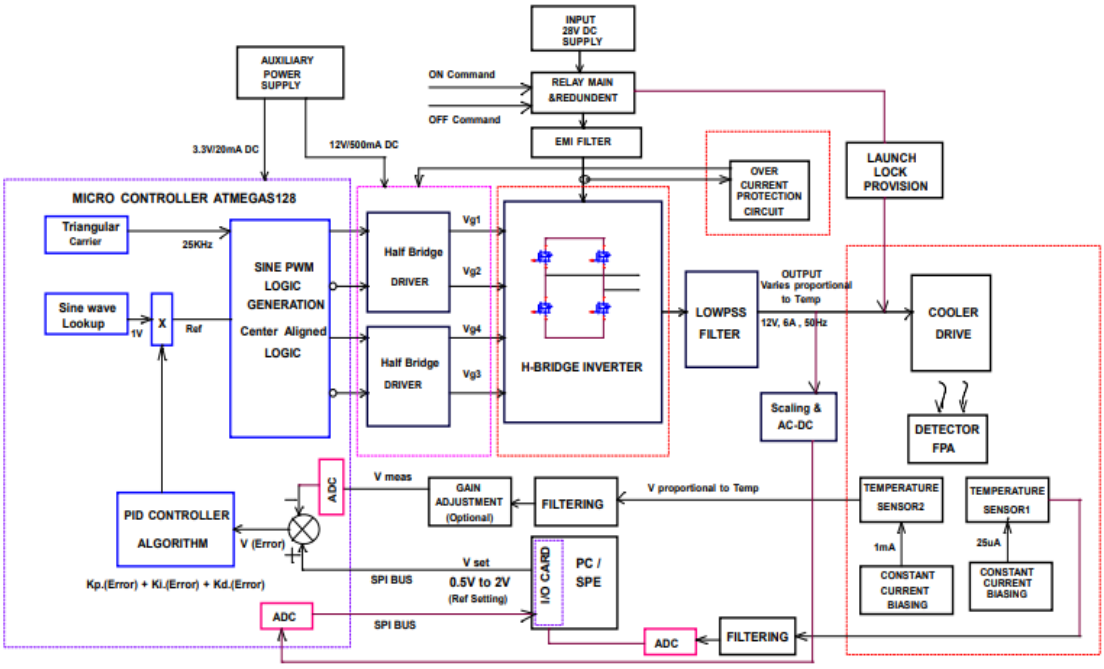

Fig 3.3 : Functional Block Diagram of the Cooler Drive Inverter

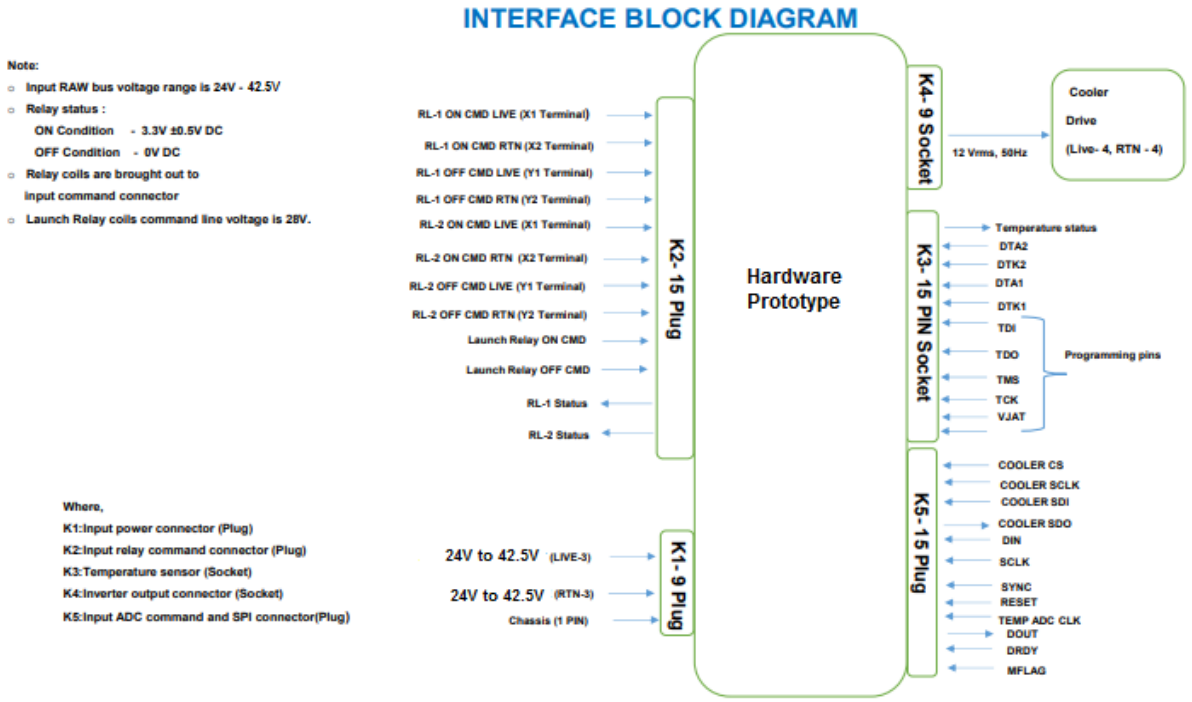

Fig 3.4 : Interface Block Diagram of Cooler Drive Inverter

3.3 Relay Sequencing for proposed prototype

- **Sequence of Operation for ON Condition:**

1. Launch lock relay (RL3) of cooler drive inverter : Initially the launch lock relay is in Normally ON condition (latch condition). Hence Output terminals are in short circuit condition. Supply the relay OFF command to RL3 to make the relay in OPEN Condition.
2. PSU main relay (RL1)/Redundant relay (RL2) is turned ON (latch condition) to switch on the Power Supply. PSU provides bias voltages (±5.5V and +12V) to Cooler drive inverter.
3. Turn ON (latch condition) the Power Relay main (RL1)/ Power relay Redundant (RL2) of Cooler drive inverter to provide AC output voltage ($12V_{rms}$, 6.5A) to cooler drive.

- **Sequence of Operation for OFF Condition:**

1. Turn OFF (OPEN Condition) the Power Relay main (RL1)/ Power relay Redundant (RL2) of Cooler drive inverter to turn OFF the AC output voltage ($12V_{rms}$, 6.5A) to cooler drive.
2. PSU main relay (RL1)/Redundant relay (RL2) is turned OFF (OPEN condition) to switch OFF the Power Supply to turn OFF the bias voltages (±5.5V and +12V) to Cooler drive inverter.
3. Launch lock relay (RL3) of cooler Electronics is turned ON (Latch Condition). RL3 will make Output terminals in short circuit condition.

ON : Specific Relay turned on; **OFF :** Specific Relay turned off.

These sequences were followed while switching ON and OFF of the Power Supply Unit and Cooler drive inverter.

Table 3.1 : Relay sequencing for cooler drive inverter

	PSU		Cooler			Remarks
Sequence	**Main Relay (RL1)**	**Redundancy (RL2)**	**Main (RL1)**	**Redundancy (RL2)**	**Launch (RL3)**	
1	OFF	OFF	OFF	OFF	OFF	Normal Condition.
2	OFF	OFF	OFF	OFF	ON	Output terminals are free from short.
3	ON	OFF	OFF	OFF	ON	1.Output power of PSU is available. 2.Output terminals free from short.
4	ON	OFF	ON	OFF	ON	1.Output power of PSU is available. 2.Output terminals free from short.
5	OFF	ON	ON	OFF	ON	1.Output power of PSU is available. 2.Output terminals free from short.
6	OFF	ON	OFF	ON	ON	1.Output power of PSU is available. 2.Output terminals free from short.

3.4 Implementation Algorithm and Flow Chart

3.4.1 Implementation Algorithm

1. Set the reference value of voltage (0.5 to 2.5V) corresponding to cold tip temperature to microcontroller through SPI. This range (0.5 to 2.5V) depends on the actual sensor voltage and reference voltage of ADC. If the set point is finalized means, which is internally programmed via the reference voltage.

2. ADC is configured to read the analog temperature sensor voltages.
3. Reading the temperature sensor voltage and feed to ADC channel.
4. Read the values of PID controller gains *Kp*, K_i and K_d.
5. Execute the ISR for discrete algorithm (sampling time).
6. Execute the Discrete PID algorithm and set the maximum and minimum limits.
7. Initialized sine table in which the values of a complete sine wave are stored (we generated a sine table in range of 0-359 degrees whereas, zero of sine wave is set at decimal.
8. Read the Look up table sine values and multiply each sine sample magnitude with the PID output value to get the sine reference voltage for generation of SPWM.
9. Reference value of sine decides the Modulation index value, which in turns decide the Output AC voltage. The Maximum Output voltage is limited by limiting the Modulation index value to the 0.6 in all conditions.
10. Initialize Timer x which starts from 0 and peaks to xxx (it gives a triangular carrier output).
11. The SPWM generation follows the logic of phase corrected PWM (the sine reference is compared with the 8-bit counter register values). Set the maximum value of PWM frequency(15.618kHz) with a clock frequency of 8-MHz and suitable pre-scalar value.
12. When Timer reaches xxx then interrupt overflow is generated.
13. Enabling timer overflow interrupt enable bit.
14. Configure the generated PWM to OCRx register to interface to the external Hardware circuits. SPWM from the controller is fed to the suitable logic compatibility H-bridge Inverter MOSFET drivers through Logic Buffers.
15. Connect the leg of the H-bridge inverter to load terminals through suitable low pass LC filter with a cut- off frequency of $1/10^{th}$ of the PWM frequency.
16. Apply the 24V to 36V DC bus voltage to the H-bridge inverter. The nominal voltage is set 28V.
17. Working of an H-bridge for pure sine wave inverter can be divided into two modes.

- ✓ In Mode1, the input signal at the gate of S1and S4 is high and at the gate of S2 and S3 is low. This causes conduction from S1and S4 and we achieve a +12V signal (positive peak of the AC output).
- ✓ In Mode2, the input signal at the gate of S2 and S3 is high and at the gate of S1and S4 is low. This causes conduction from S2 and S3 and we achieve a -12V signal (negative peak of the AC output). And thus, we obtain a 24V peak-peak signal at the output.

18. In H-bridge circuit we have obtained amplitude modulating signal frequency (reference sine signal). Modulating signal frequency does not change at the output, which means the output frequency remains constant. Only the power of the signal increases in terms of current.
19. If the output cooler motor consumes more current (1.5 times higher than the nominal load current) than the maximum load current, then the over current protection circuit should activate to shut down the converter.

3.4.2 Flow Chart

Fig 3.5 shows the Flow chart of the Sine PWM Logic Generation and PID Controller for the cooler drive inverter.

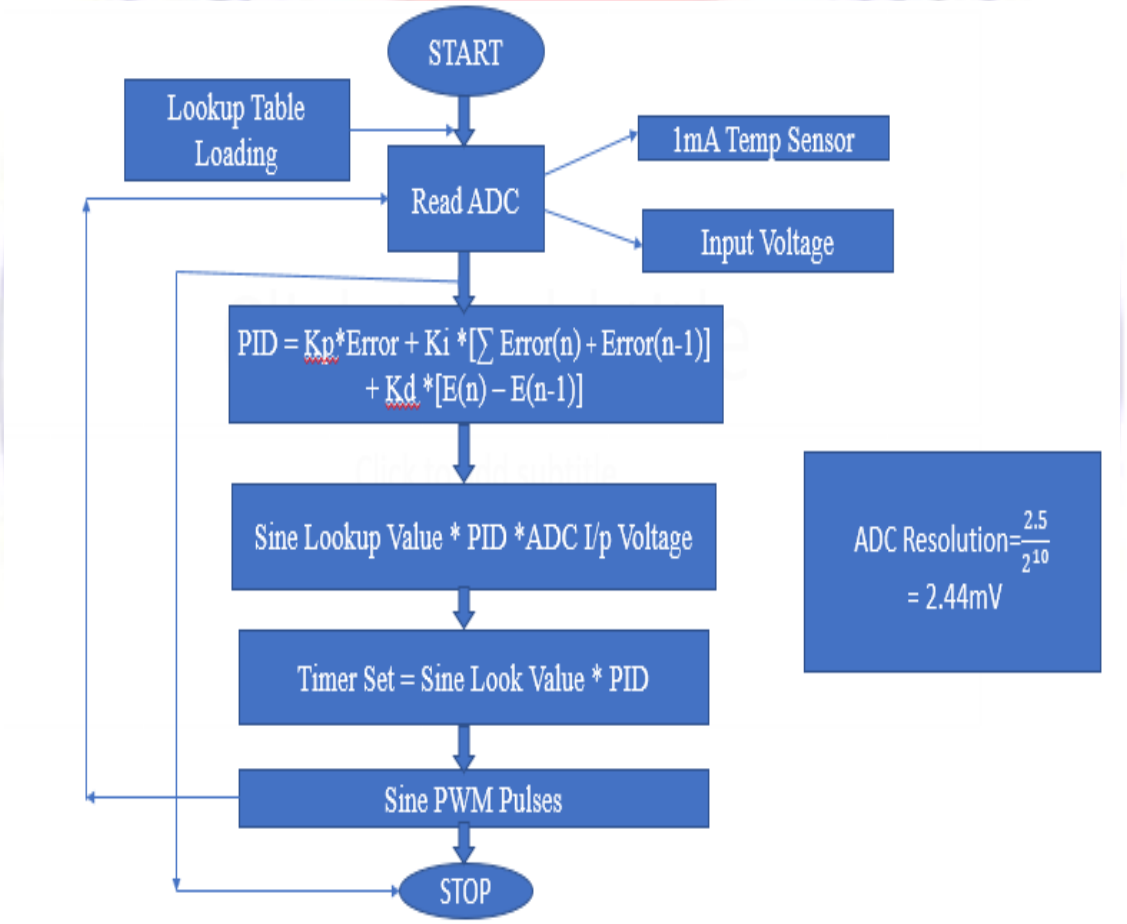

Fig 3.5 : Flow Chart of Sine PWM Logic Generation and PID Controller

3.5 Summary

In this chapter the methodology, block diagram, Relay Sequencing, Implementation algorithm and flow Chart of the proposed prototype were discussed in brief.

CHAPTER 4

SPECIFICATIONS AND DESIGN DETAILS

This chapter discusses about the specification and design details which includes input power and current calculation, output filter design, output inductor design, power loss calculations, MOSFET selection and snubber design, PID controller design and efficiency calculations of the proposed prototype.

4.1 Specifications

The Table 4.1 shows the specifications of the Cooler Drive Inverter using ATmegaS128 Micro Controller.

Table 4.1 : Specifications for the proposed prototype

Sl.no	Parameter	Specifications
1	Input Voltage Range	24V - 36V DC
2	Nominal Input Voltage	28V DC
3	Nominal Output Voltage (RMS)	12V AC
4	Maximum Output Voltage (RMS)	15.7V AC
5	Maximum AC Power Output	78 W
6	Topology	H-Bridge Inverter
7	Maximum AC Output Current	6.5 A
8	Nominal Output Current	6A
9	Modulation	Sine PWM
10	Switching Frequency	22KHz
11	AC Output Power	72W
12	Output Frequency	50Hz ,+/- 1%
13	Protections	OCP, UVP and OVP
14	Controller used	ATmegaS128 Microcontroller (10MHz, 8 channel 10-bit ADC, 30k Radiation, 6 PWM channels, 53 GPIO,4KB EEPROM and 64KB External memory).
15	Efficiency (%)	> 90% at 60W (@R load 3Ω)
16	Bias current temperature sensing diode	1 mA,25uA +/-4%
17	Maximum permissible DC offset level at output	0.2V
18	THD (Total Harmonic Distortion) Maximum permissible harmonics in output signal 1.Secondary Harmonics 2.Higher Harmonics	 10% 5%

4.2 Design Details

1. Input Power and Current Calculation

Maximum Output Power : $P0_{max} = \frac{V0_{MAX}^2}{RL} = 82.1633W$ at linear load natur (4.1)

Maximum input Power : $Pin_{max} = \frac{P0_{max}}{\eta} = 91.2926W$ (4.2)

Voltage across switch : $Vsw = Vin_{Max} = 36V$ (4.3)

Peak Switch Current : $Ip = \frac{Vin_{max}}{RL} = 12A$ (4.4)

Average switch current : $IA_{sw} = \frac{Ip}{2} = 6A$ (4.5)

Average input current : $Is = \frac{Pin_{max}}{Vin_{max}} = 2.5359A$ (4.6)

Let Assume maximum output current is peak current for input OCP

$Is_{rms} = 6.5A$ (4.7)

2. Output Filter Design

Output filter consist of inductor and capacitor.

(1) Output Inductor

The primary role of the output filter inductor (Lo) is to filter out the switching frequency harmonics. The design of an inductor, amongst other factors, depends on the calculation of the current ripple and choosing a material for the core that can tolerate the calculated current ripple.

When designing filters, the value of inductance is usually designed first. The selection of inductance is related to the ripple current and the power consumption of the system. In general, the ripple current on the inductor is selected to be 15% - 25 % of the rated current.

For this design, the rating is 75 W, the switching frequency is 20 kHz, and the bus voltage is 32 V.Assume that the ripple is 20% and is tolerable by the inductor core,and the minimum inductance required is calculated as:

Peak to Peak Ripple Current is : $\Delta IL = \frac{20}{100} * I0rms_{max} = 1.3A$ (4.8)

Hence Output Inductor Value is

$L = \frac{Vin_{max}}{4 * Fsw * \Delta IL} = 3.4615 * 10^{-4} H$ (4.9)

(2) Output Capacitor Filter

Assume $L0 = 0.5 * 10^{-3}$ (4.10)

Cutoff Frequency : $Fc = \frac{Fsw}{10} = 2000Hz$ (4.11)

$$C0 = \frac{1}{4 * \pi^2 * L0 * Fc^2} = 1.2665 * 10^{-5}F \quad (4.12)$$

3. Output Inductor Design

Let $K = 0.3$ $Kw = 0.5$ $Bm = 0.33$ $J = 4$
Using Area Product Method

$$Ap_{L0} = Lo * I0rms_{max} * I0rms_{max} * \frac{\left(1 + \frac{K}{2}\right)}{Kw * Bm * J * 10^{-6}} = 36808.7121 \quad (4.13)$$

Requirement of Core selection

An appropriate core will be selected which must have area product greater than the calculated Ap. Area product (Ap) is given as the product of the core cross section (Ac) and the window area (Aw).

Selected Ferrite Toroid Core: ZW-422120,Material:R, AL: 12080mH/1000T

$Ac = 51.1\ mm^2$ $Aw = 147.9\ mm^2$ $AL = 12080.10 * 10^{-9}H$

$Ap = Ac * Aw$ $Ap = 7557.69\ mm^4$

Cross sectional area of wiregauge selected $Aw_{28AWG} = 0.111\ mm^2$ (4.14)

Number of Turns : $N = \sqrt{\frac{L0}{AL}} = 6.4336$ N=10 (4.15)

Possible number of turns possible in the core

Outer Diameter of selected wire gauge $dw_{CM} = 0.366\ mm$ For 28 AWG Wire Gauge

$$Toroid_{inner_{dia_{CM}}} = 13.7\ mm \quad (4.16)$$

$$Possible_{turns_{for_{core}}} = \pi * \frac{Toroid_{inner_{dia_{CM}}}}{dw_{CM}} = 117.5951 \quad (4.17)$$

Required cross sectional Area of wire : $Awp = \frac{I0rms_{max}}{J} = 1.625$ $Awp = 1.625$ (4.18)

Number of parallel strand required : $nparp = \frac{Awp}{Aw_{28AWG}} = 14.6396$: 6*28AWG (4.19)

4. Power Loss Calculations

Copper Loss calculations

AC resistance of wire gauge selected $\mathrm{Rac_{28AWG}} = 0.222\ \mathrm{Ohm}$ (4.20)

Length of wire required : $\mathrm{L} = \frac{(22.1-13.7)+2.12*7}{1000} = 0.0338\ \mathrm{meter}$ (4.21)

$\mathrm{L_N} = \mathrm{N} * \mathrm{L} + 0.02 = 0.358\ \mathrm{meter}$ (4.22)

- **Copper loss**

$\mathrm{P_N} = \left(\mathrm{L_N} * \mathrm{Rac_{28AWG}} * \mathrm{I0rms}_{\mathrm{max}}^{2}\right) * \frac{1}{6} = 0.5596\ \mathrm{watt}$ (4.23)

- **Core Loss Calculations**

$\mathrm{a} = 0.30 \quad \mathrm{c} = 1.26 \quad \mathrm{d} = 2.60 \quad \mathrm{Ve} = 2.77\ \mathrm{cm^3}$

$\mathrm{Bm} = 0.33$

$\mathrm{B} = \left(\frac{\mathrm{Bm}}{2}\right) * 10 \qquad \mathrm{B} = 1.65 \qquad \mathrm{f} = \frac{\mathrm{Fsw}}{1000} = 20$

$\mathrm{Pcore} = \mathrm{a} * \mathrm{f^c} * \mathrm{B^d} * \frac{\mathrm{Ve}}{1000} \qquad \mathrm{Pcore} = 0.1332\mathrm{W}$ (4.24)

Where: 1. Ve is core Volume
2. B is core calcated flux density
3. Pcore is the power loss in the selected core

Total Loss

$\mathrm{P_{L0}} = 2 * (\mathrm{Pcore} + \mathrm{P_N}) = 1.3856\ \mathrm{watt}$ (For 2 Inductor) (4.25)

5. MOSFET Selection And Snubber Design

FQA70N15 , 0.028 Ohm, 70A@ 25 Deg. Vds:150V (Industrial)

$\mathrm{R_{DS}} = 0.028\ \mathrm{ohm} \qquad \mathrm{R_{Gate}} = 3.3\ \mathrm{ohm}$

$\mathrm{Q_{GATE}} = 25 * 10^{-9}\mathrm{C} \quad \mathrm{V_{TH}} = 6\mathrm{V}$

$\mathrm{V_{GATE}} = 12\mathrm{V} \qquad \mathrm{V_{OFF}} = 2.5 * \mathrm{Vin_{max}} = 90\mathrm{V}$

$\mathrm{Coss} = 1100 * 10^{-12}\ \mathrm{F}$

$\mathrm{Tr} = \mathrm{Q_{GATE}} * \frac{\mathrm{R_{GATE}}}{\mathrm{V_{GATE}} - \mathrm{V_{TH}}} = 1.375 * 10^{-8}\mathrm{Sec}$ (4.26)

$$Tf = Q_{GATE} * \frac{R_{GATE}}{V_{TH}} = 1.375 * 10^{-8} \text{ sec} \quad (4.27)$$

$$P_{CONDUCTION} = 1.25 * R_{DS} * IS_{rms}^2 = 1.4788 \text{ Watt} \quad (4.28)$$

$$P_{GATE} = Q_{GATE} * V_{GATE} * Fsw = 0.006 \text{ Watt} \quad (4.29)$$

$$P_{Coss} = Coss * V_{OFF}^2 * \frac{Fsw}{2} = 0.0891 \text{ Watt} \quad (4.30)$$

$$P_{Switching_{ON}} = Vin_{min} * Is_{rms} * (Tr) * \frac{(Fsw)}{3} = 0.0143 \text{ Watt} \quad (4.31)$$

$$P_{Switching_{OFF}} = V_{OFF} * IS_{rms} * (Tf) * \frac{Fsw}{3} = 0.0536 \text{ Watt} \quad (4.32)$$

MOSFET Gate Charge loss takes place in Gate Resistor and this loss is not added in the MOSFET power losses.

RC snubber is connected across MOSFET to reduce switching loss.

Let $Csnubber = 1 * 10^{-9}F$

$$P_{Switching_{OFF_{WITH_{SNUBBER}}}} = \left(\frac{Coss}{Coss + Csnubber}\right) * P_{Switching_{OFF}} = 0.0281 \text{ Watt} \quad (4.33)$$

$$P_{MOSFET_{LOSS_1}} = P_{conduction} + P_{Coss} + P_{Switching_{ON}} + P_{Switching_{OFF_{with_{Snubber}}}} \quad (4.34)$$

$$P_{MOSFET_{LOSS_1}} = 2 * P_{MOSFET_{LOSS_1}} = 3.2205 \text{ Watt for 2 MOSFET} \quad (4.35)$$

6. PID Controller Design

As we know, an analog compensator is usually implemented with RC network and an operational amplifier. Let us consider a type III PID compensator and its network is shown in Fig 4.1 and the associated frequency response in equation 4.36

Type III compensator has one pole *fp*o at DC, other two high frequency poles *fp*1, *fp*2 and two zeros *fz*1, *fz*2. First pole *fp*1 at 0 frequency is able to improve the DC gain resulting in smaller steady state error. And first zero *fz*1 is recommended to place around 1/10 of crossover frequency of loop response since the phase lag due to the integrator pole will not be completely cancelled out by this zero until 10 times of *fz*1 reaches. That means to make the phase not be degraded at the crossover frequency *f z*1 must be greater than 1/10 of crossover frequency.

However, the lower *fz*1 will give the higher dc gain, which benefits the loop performance. The second zero is recommended to locate around or less than crossover frequency to improve the phase margin and make the response magnitude achieve $-20dB$ attenuation at crossover frequency.

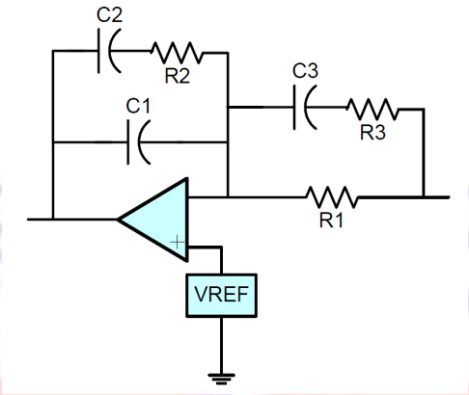

Fig 4.1 : PID controller circuit

$$G_c(s) = G_{oc} * \frac{\left(\frac{s}{wz1}+1\right)\left(\frac{s}{wz2}+1\right)}{s * \left(\frac{s}{wp1}+1\right) * \left(\frac{s}{wp2}+1\right)} \quad (4.36)$$

Parallel form of PID can be given as:

✓ **Discrete-time PID algorithm**

The PID mathematical equation must be transferred to digital equation which will be understandable for the PIC. It can be changed with a good approximation like the below equation, for digital implementation, we are more interested in a Z-transform of (*):

$$\mathrm{U(Z)} = \left[\mathrm{Kp} + \frac{\mathrm{Ki}}{1-\mathrm{Z}^{-1}} + \mathrm{Kd}(1-\mathrm{Z}^{-1})\right]\mathrm{E(Z)} \quad (4.37)$$

By rearranging once again:

$$\mathrm{U(Z)} = \frac{[(\mathrm{Kp}+\mathrm{Ki}+\mathrm{Kd})+(-\mathrm{Kp}-2\mathrm{Kd})*\mathrm{Z}^{-1})+\mathrm{Kd}*\mathrm{Z}^{-2}]}{1-\mathrm{Z}^{-1}} * \mathrm{E(z)} \quad (4.38)$$

$$\mathrm{K1} = \mathrm{Kp} + \mathrm{Ki} + \mathrm{Kd} \quad (4.39)$$

$$\mathrm{K2} = -\mathrm{Kp} - 2\mathrm{Kd} \quad (4.40)$$

$$\mathrm{K3} = \mathrm{Kd} \quad (4.41)$$

It can be written as.

$$\mathrm{U(Z)} - \mathrm{Z}^{-1} * \mathrm{U(Z)} = [\mathrm{K1} + \mathrm{K2} * \mathrm{Z}^{-1} + \mathrm{K3} * \mathrm{Z}^{-2}] * \mathrm{E(Z)} \quad (4.42)$$

Which can be converted to:

$$U[K] = U[K-1] + K1 * U[K] + K2 * U[K-1] + K3 * U[K-2] \quad (4.43)$$

Now a digital output must be transferred to an analogue output, to be understandable.

7. Efficiency Calculations

Total Power Losses

Let other losses be 20% of Total Loss

$$P_{loss_1} = P_{MOSFET_{Loss_1}} + P_{L0} + P_{EMI} = 5.3273 \text{ Watt} \quad (4.44)$$

$$P_{loss} = 0.2 * P_{loss_1} + P_{loss_1} = 6.3928 \text{ Watt} \quad (4.45)$$

$$P0_{max} = 82.1633 \text{ Watt} \quad (4.46)$$

$$\text{Efficiency} = \frac{P0_{max}}{(P0_{max+}P_{loss})} * 100 = 92.7811 \text{ Watt} \quad (4.47)$$

4.3 Summary

In this chapter the specification and design details which includes input power and current calculation, output filter design, output inductor design, power loss calculations, MOSFET selection and snubber design, PID controller design and efficiency calculations of the proposed prototype were discussed in brief.

CHAPTER 5

SIMULATION AND HARDWARE IMPLEMENTATION

This chapter discusses about the simulation and hardware analysis which includes logic implementation in temperature Control, PWM Control Logic, H-Bridge inverter power circuit and waveforms, constant current source biasing circuit, protection circuits, Hardware CRO waveforms, MIL-STD 461E CE102 EMI/EMC Testing, Hardware PCB under testing and experimental setup of the proposed prototype.

5.1 Logic Implementation in Temperature Control

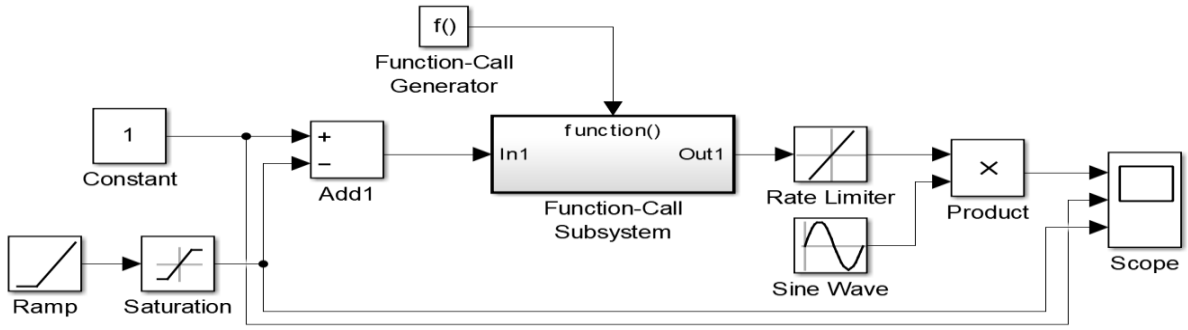

Fig 5.1 : MATLAB Simulation (Logic implementation in Temp control)

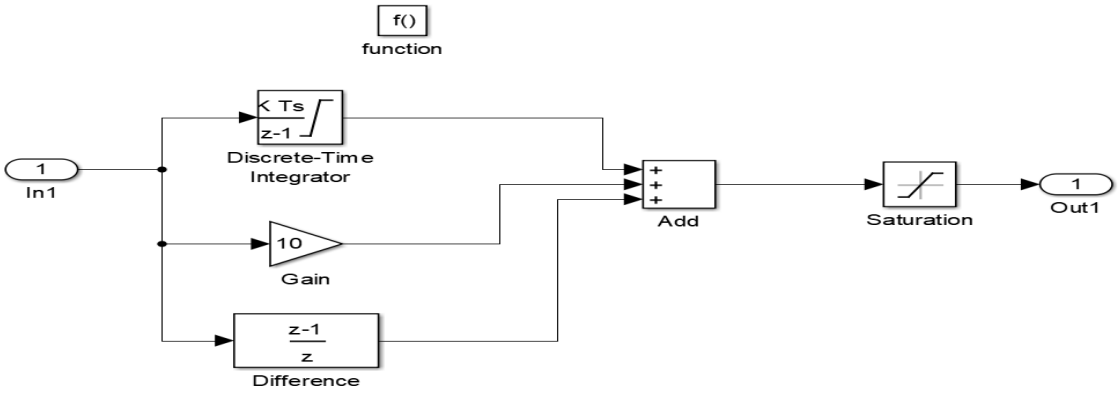

Fig 5.2 : PID Controller

Fig 5.1 and Fig 5.2 depicts the MATLAB simulation of logic implementation in temperature control, Fig 5.3 shows the simulated output waveform of output voltage, reference and temperature sensor voltage, here when the temperature sensor voltage starts increasing, the output voltage also starts increasing by means of soft start principle and until the sensor voltage reaches 1V, the output voltage will be 12V. and when the sensor voltage reaches 1V, the output voltage starts decreasing and will maintain 4.5 to 5V and this same logic is implemented in the hardware implementation of digitally controlled cooler drive inverter.

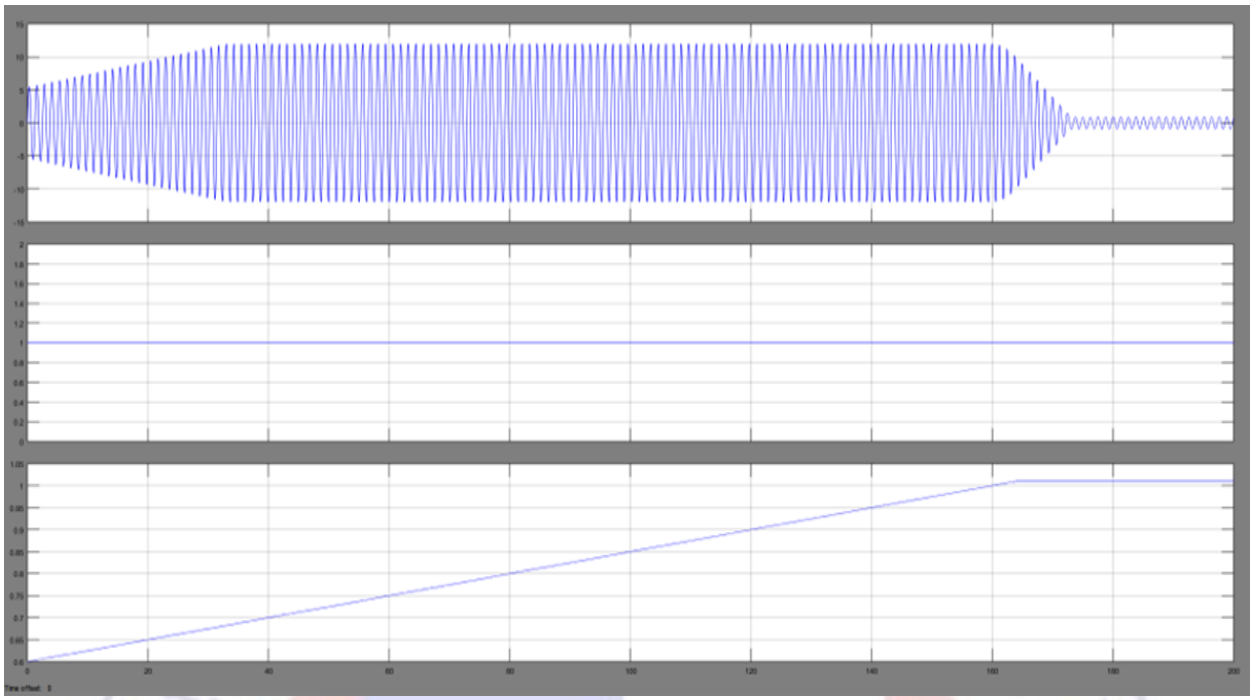

Fig 5.3 : simulated output waveform (Output voltage, reference and Temp sensor output)

5.2 PWM Control Logic

Fig 5.4 shows the PWM control logic used in ATmegaS128 Microcontroller for H-Bridge Inverter.

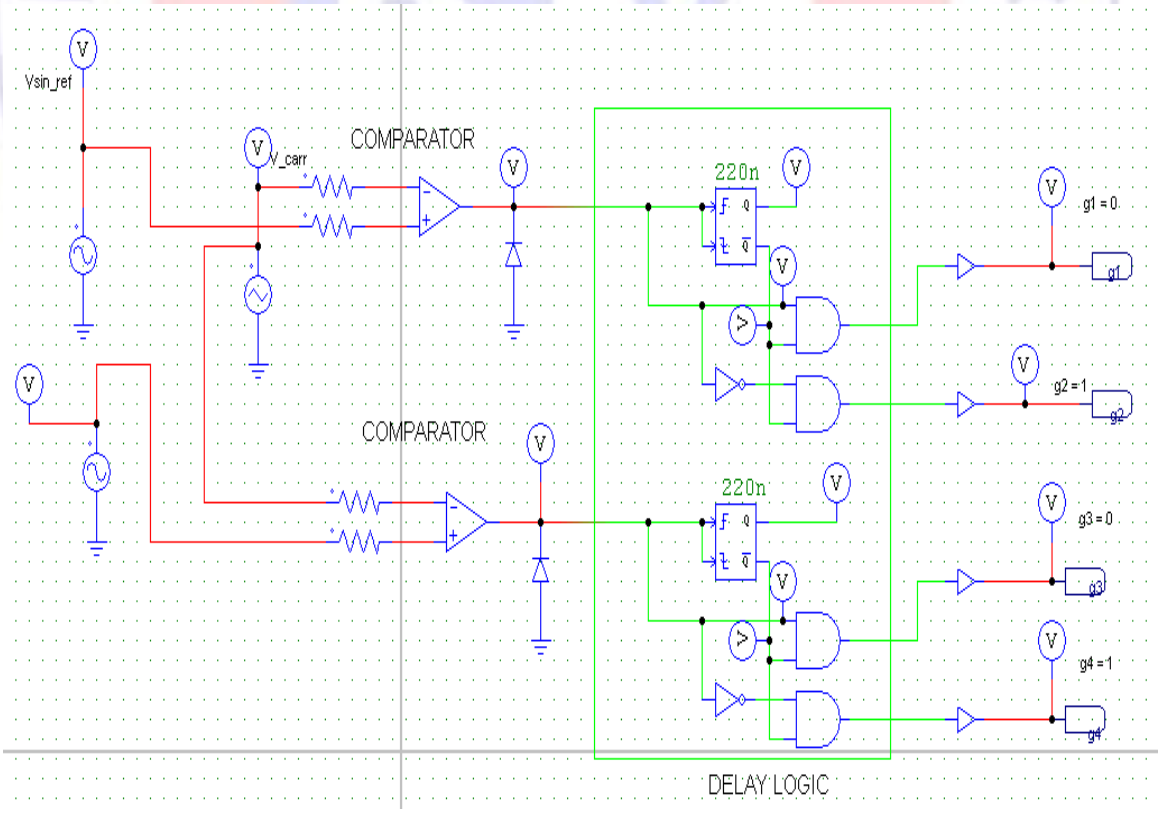

Fig 5.4 : PWM control logic used in Microcontroller for H-Bridge Inverter

5.3 H-Bridge Inverter Power Circuit

Fig 5.5 shows the H-bridge inverter power circuit, It mainly consists of 4 MOSFETs, DC source, gating pulses, LC filter at the output side to obtain pure sine wave.

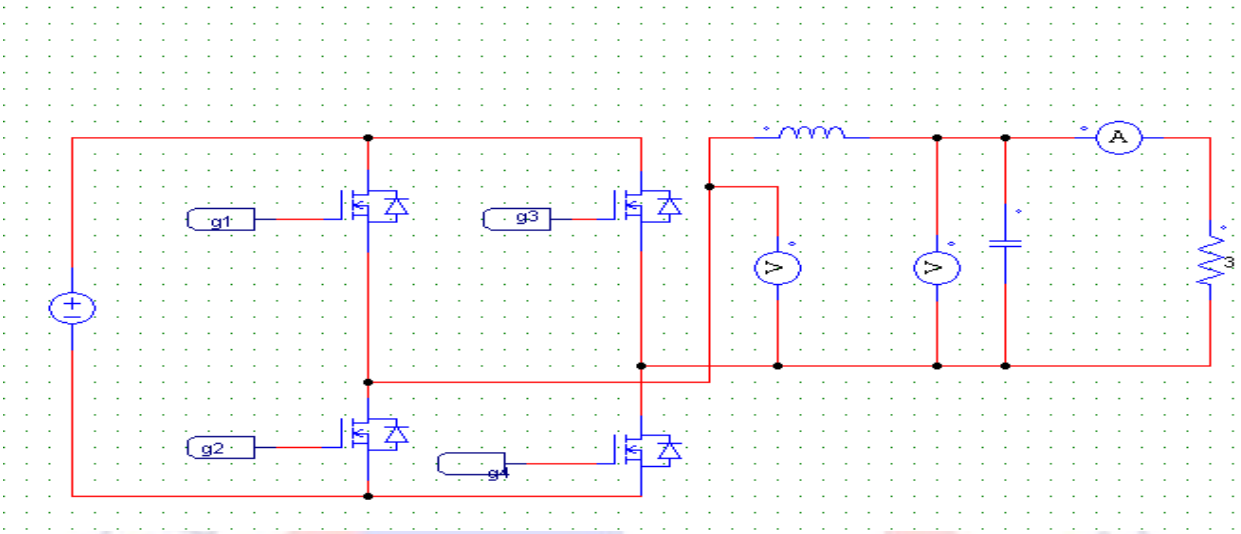

Fig 5.5 : H-Bridge Inverter Power Circuit

5.4 H-Bridge Inverter Waveforms

Fig 5.6 shows the H-bridge inverter output voltage before LC filter(above waveform) and after LC filter(below waveform) and it is observed from the waveform that, 12V AC RMS is obtained after the sinusoidally variable pulses are passed through low pass LC filter.

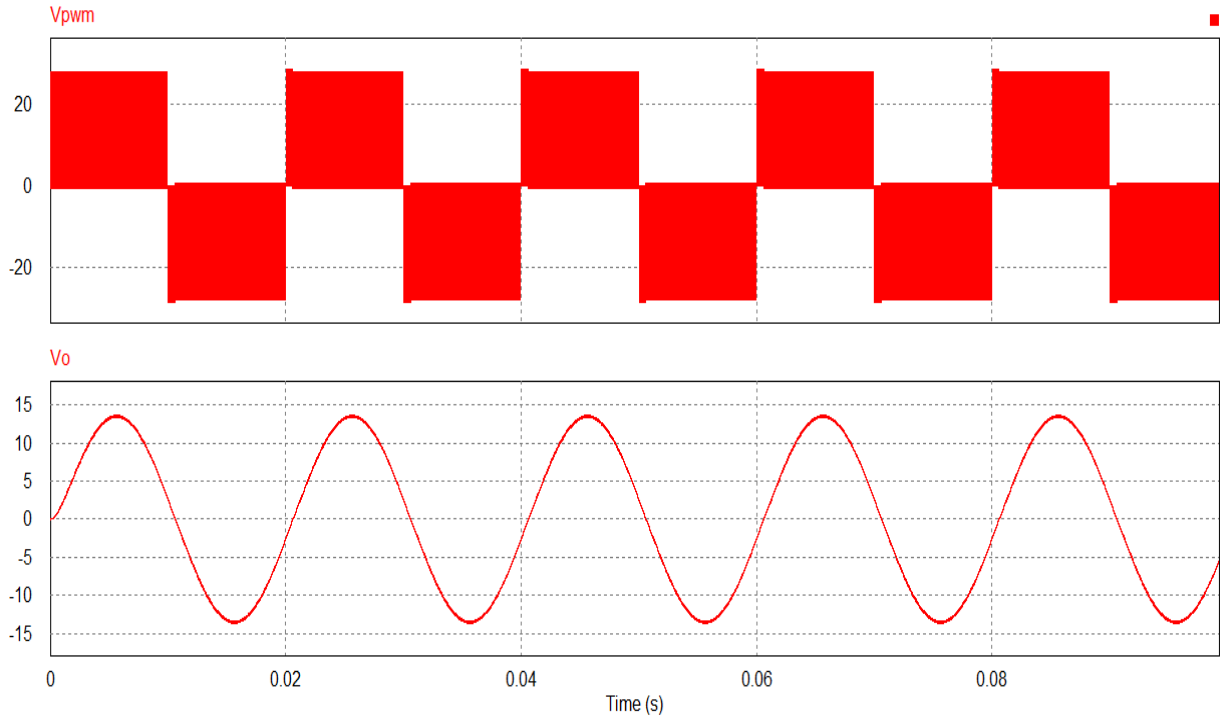

Fig 5.6 : H bridge inverter output voltage (Before filtering and After filtering)

Fig 5.7, Fig 5.8 and Fig 5.9 represents generation of PWM signals (switches 1 and 2) During half cycle of time duration 0 to 0.01 second.

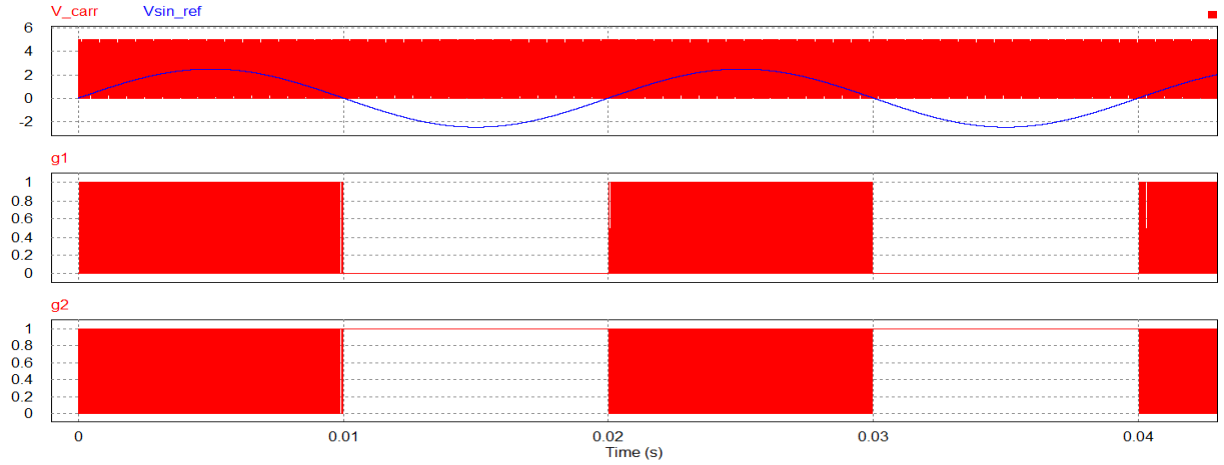

Fig 5.7 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0 to 0.01 second.

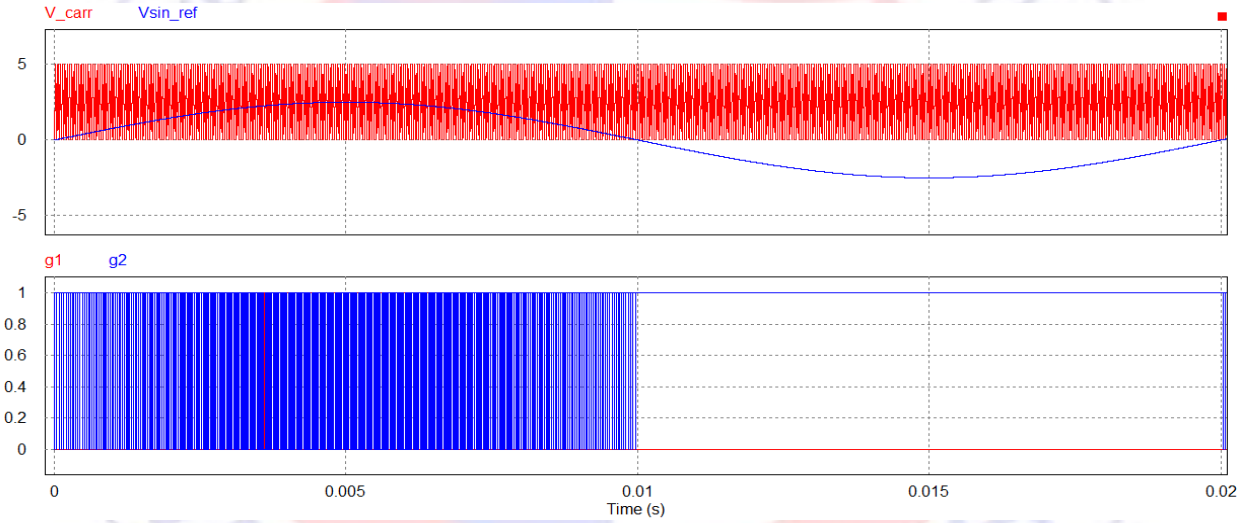

Fig 5.8 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0 to 0.01 second.

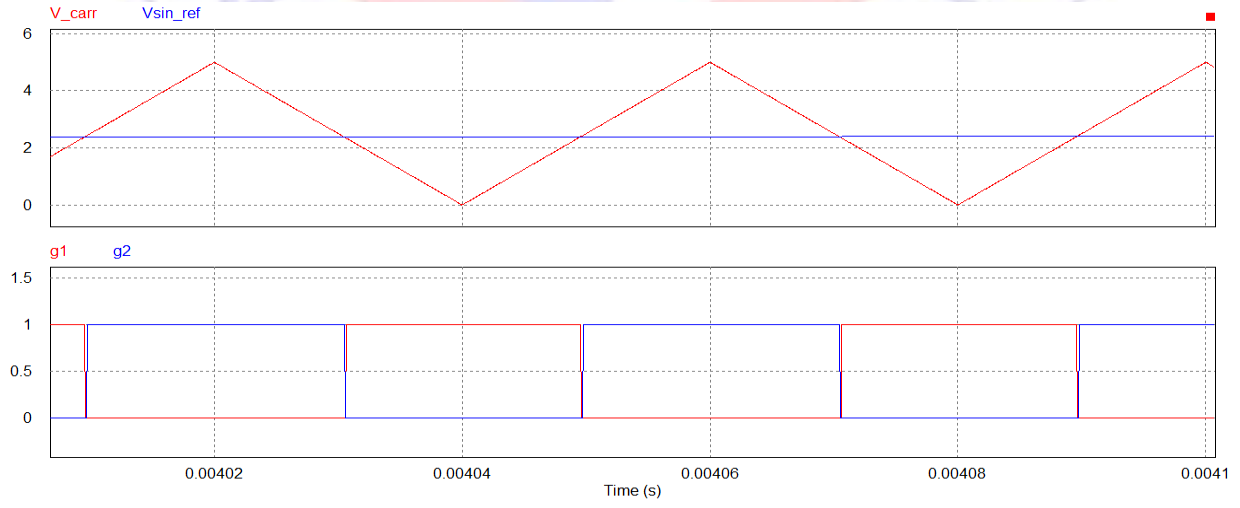

Fig 5.9 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0 to 0.01 second.

Fig 5.10 and Fig 5.11 represents generation of PWM signals (switches 3 and 4) During half cycle of time duration 0.01to 0.02 second.

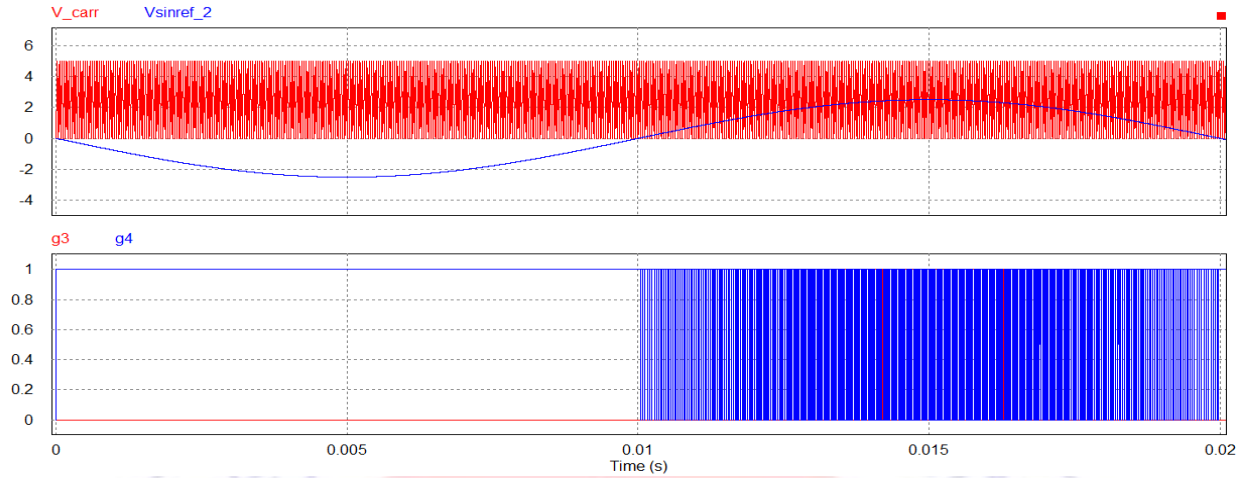

Fig 5.10 : Generation of PWM signal (switches 3 and 4) During half cycle of time duration 0.01to 0.02 second.

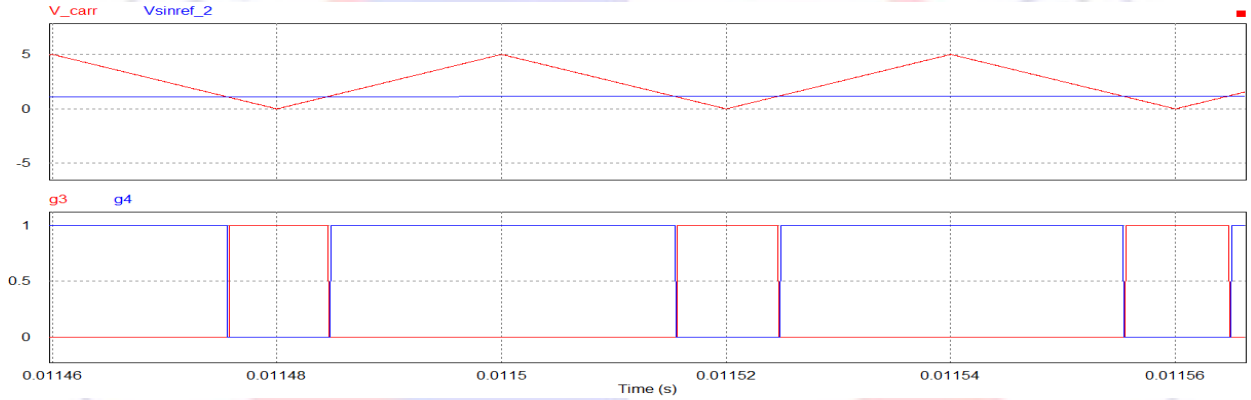

Fig 5.11 : Generation of PWM signal (switches 3 and 4) During half cycle of time duration 0.01to 0.02 second.

5.5 Constant Current Source Biasing Circuit

Fig 5.12 represents the simulation of 1mA constant current source biasing. The constant current source circuit is kept in thermal chamber and variation of the current with respect to chamber temperature was observed. The temperature sensor is kept at ambient condition.

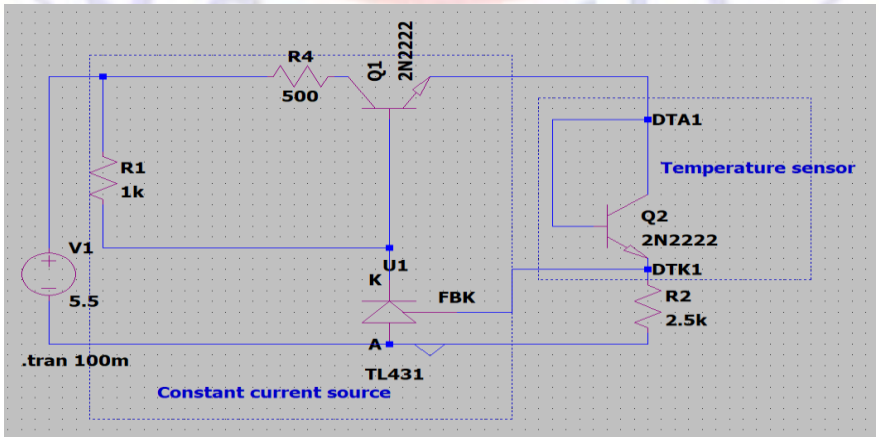

Fig 5.12 : 1mAConstant Current Source Biasing Circuit

5.6 Protection Circuits

Input side has protection circuits such as Over voltage protection (OVP), Under voltage protection (UVP), Over current protection (OCP).

5.6.1 Over Voltage Protection

Fig 5.13 represents over voltage protection circuit. The over voltage protection is used to avoid the damage of any device from the maximum voltage or over voltage, if the voltage exceeds more than the specification, the components may get damage, to avoid those damage, over voltage protection circuit is used. The value of the resistor is designed on the bases of maximum differential voltage at the highest expected current. The voltage sensing element will be placed in the device if the voltage reaches above the maximum voltage or 125% of the rated primary voltage then the U1 pin gets high and shutdown pin of PWM IC gets high. Thus turns off the device.

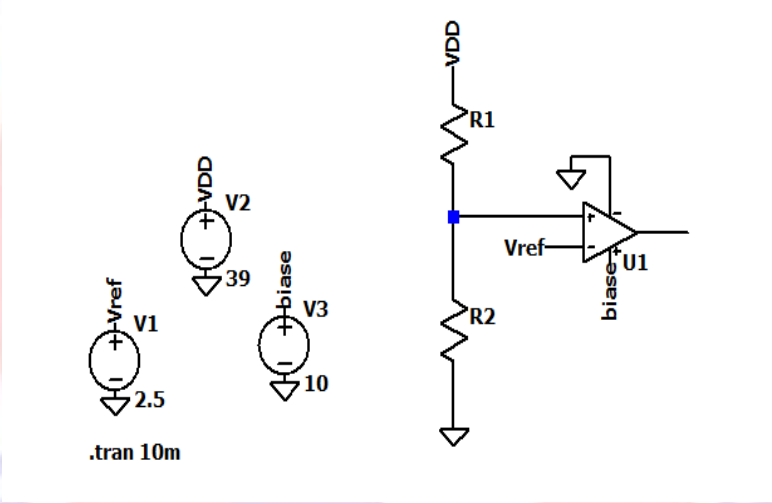

Fig 5.13 : Circuit of Over Voltage Protection

5.6.2 Under voltage Protection

Fig 5.14 represents under voltage protection circuit. The under voltage is used to avoid the damage of any device from the voltage rated below the specification, In DC-AC converter the under-voltage range is below 22V, so when the voltage reaches below 22V then, current drawing will be more from the input supply, this causes power losses, then the voltage sensing element gets sensed and the shutdown pin of PWM IC gets high and converter gets turn off. the voltage should be of 125% of the rated primary voltage. By this we can avoid the damage of components in the converter.

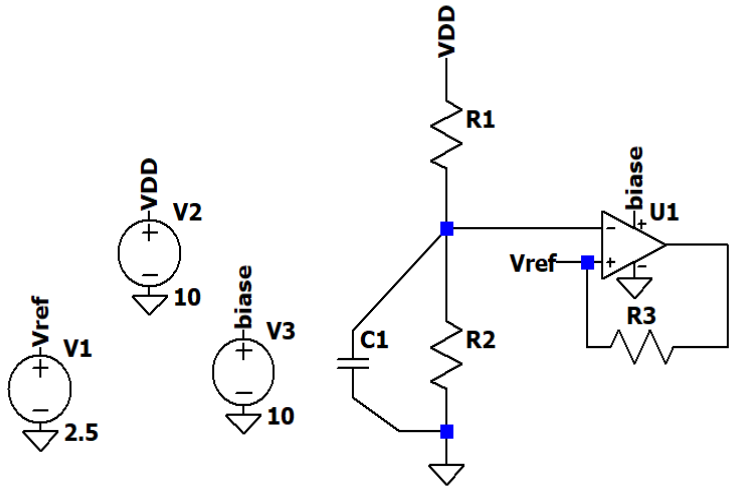

Fig 5.14 : Circuit of Under Voltage Protection

5.6.3 Over current Protection

Fig 5.15 represents over current protection circuit. The over current protection is used to avoid the converter from the damage. If the current reaches above the specification, then the components in converter may get damage. So the value of the voltage divider resistor is designed according to the input voltage supply, here the input voltage range is from 24 - 42.5V, The current limiting resistor is designed according to the input and output current, when the current exceeds 125% of designed value, The shutdown pin of PWM IC gets high and converter gets turn off.

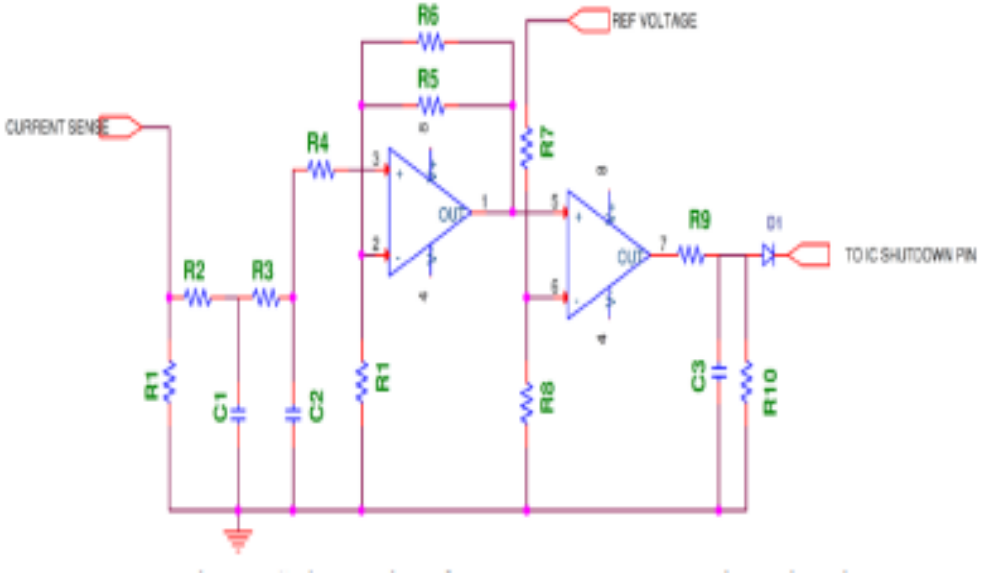

Fig 5.15 : Circuit of Over current Protection

5.7 Hardware CRO waveforms of Cooler Drive Inverter

Fig 5.16 shows the hardware CRO waveforms of Gate Main pulses(Upper MOSFETs) of MOSFETs 1 and 3.

Fig 5.16 : Gate Main pulses(Upper MOSFETs) of MOSFETs 1 and 3.

Fig 5.17 shows the hardware CRO waveforms of Gate Main pulse and its complementary pulses of MOSFETs 1 and 2.

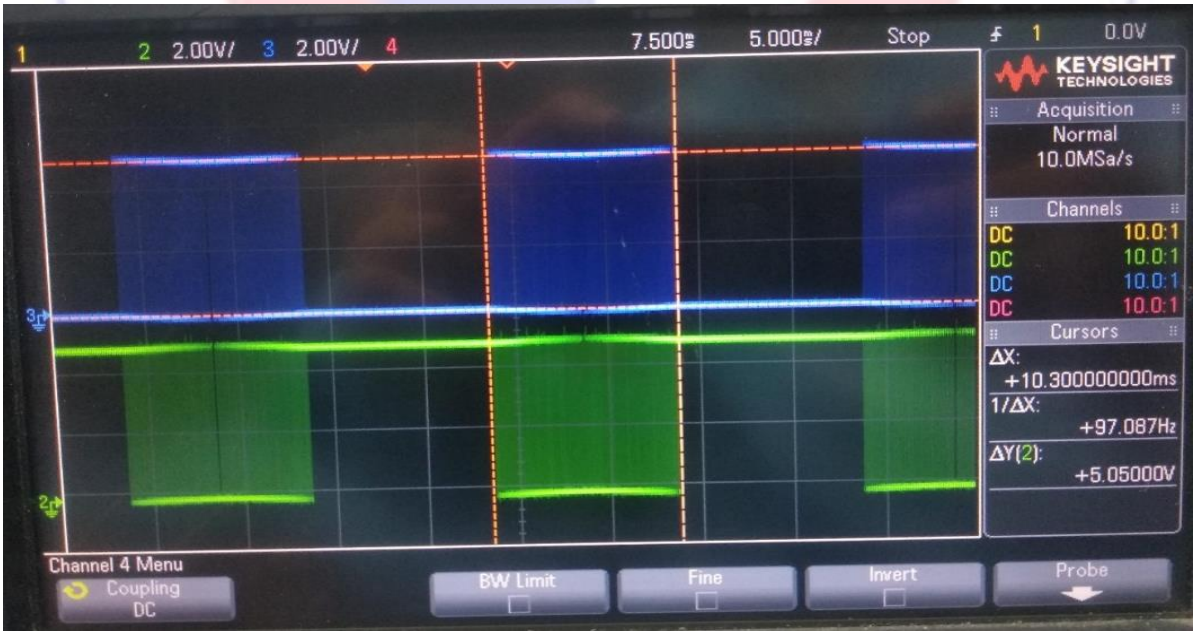

Fig 5.17 : Gate Main pulse and its complementary pulses of MOSFETs 1 and 2.

Fig 5.18 shows the hardware CRO waveforms of Main pulse and its complementary pulses of MOSFETs 3 and 4.

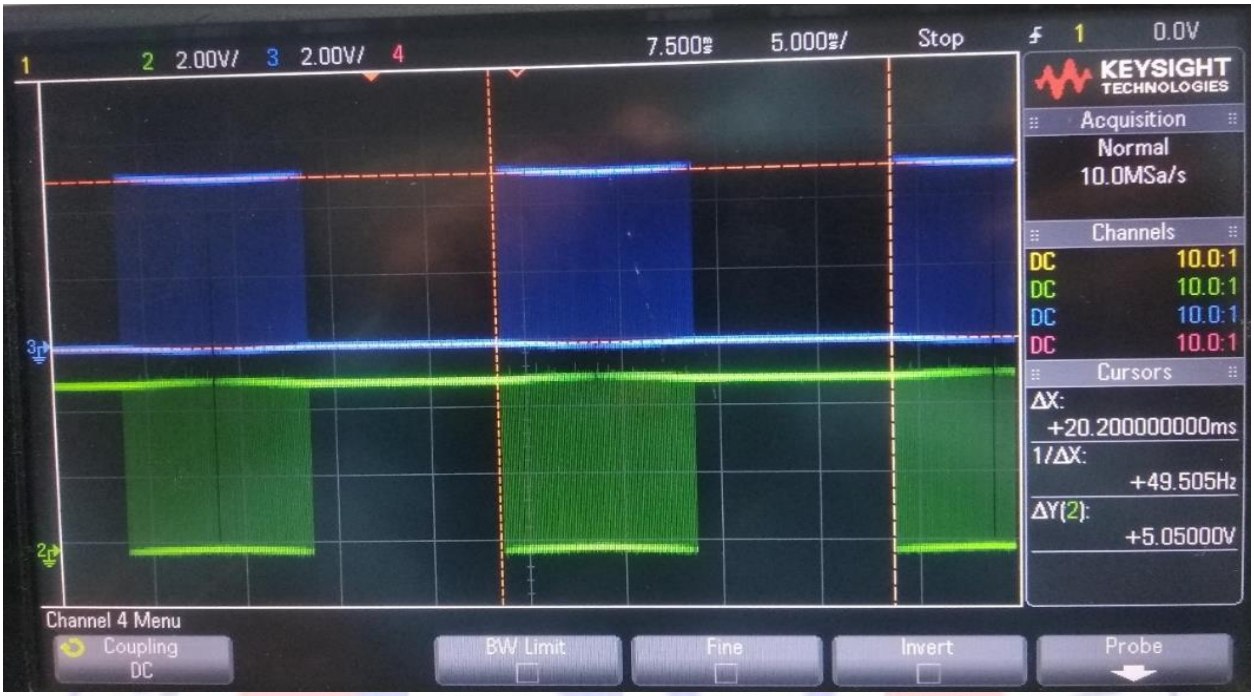

Fig 5.18 : Main pulse and its complementary pulses of MOSFETs 3 and 4.

Fig 5.19 shows the hardware CRO waveforms of Sinusoidal PWM variation pulses of the main pulses.

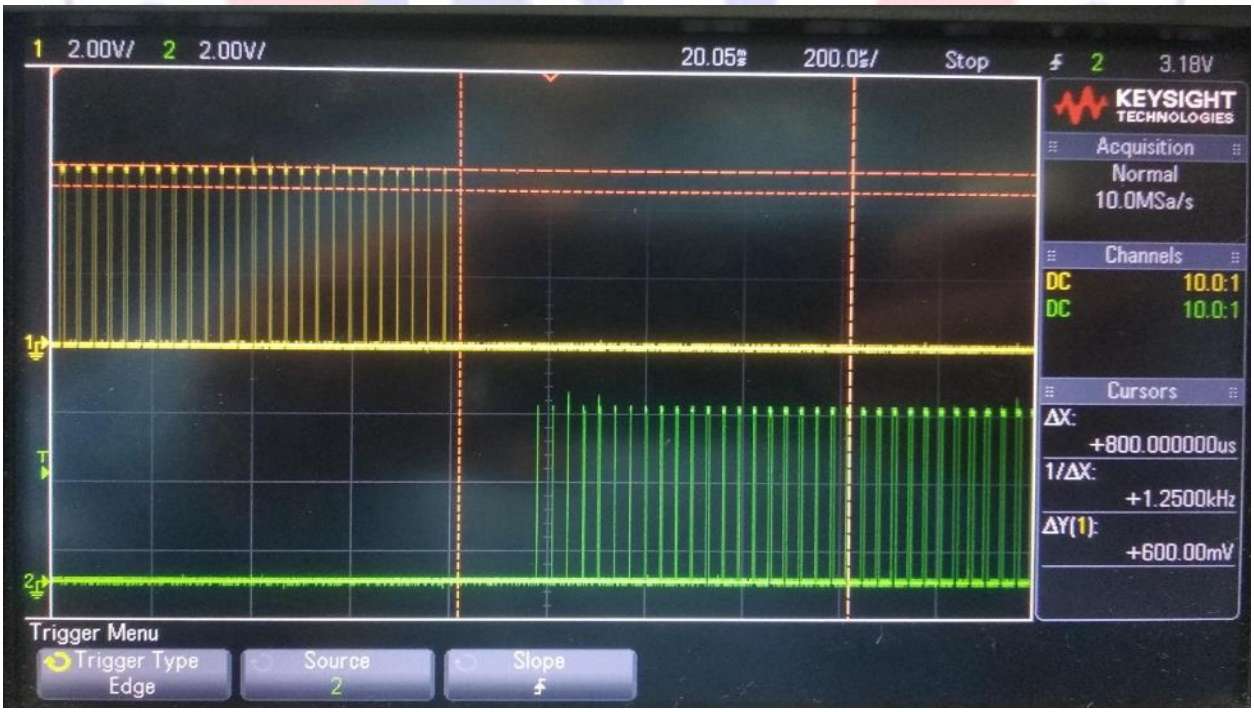

Fig 5.19 : Sinusoidal PWM variation of the Main pulses

Fig 5.20 shows the hardware CRO waveforms of Sinusoidal waveform after main pulses are passed through RC low pass filter with cutoff frequency of 1.59kHz.

Fig 5.20 : Sinusoidal waveform after main pulses are passed through RC low pass filter(cutoff frequency = 1.59kHz)

Fig 5.21 shows the hardware CRO waveforms of Sinusoidal waveform after main pulses are passed through RC low pass filter with cutoff frequency of 1.59kHz.

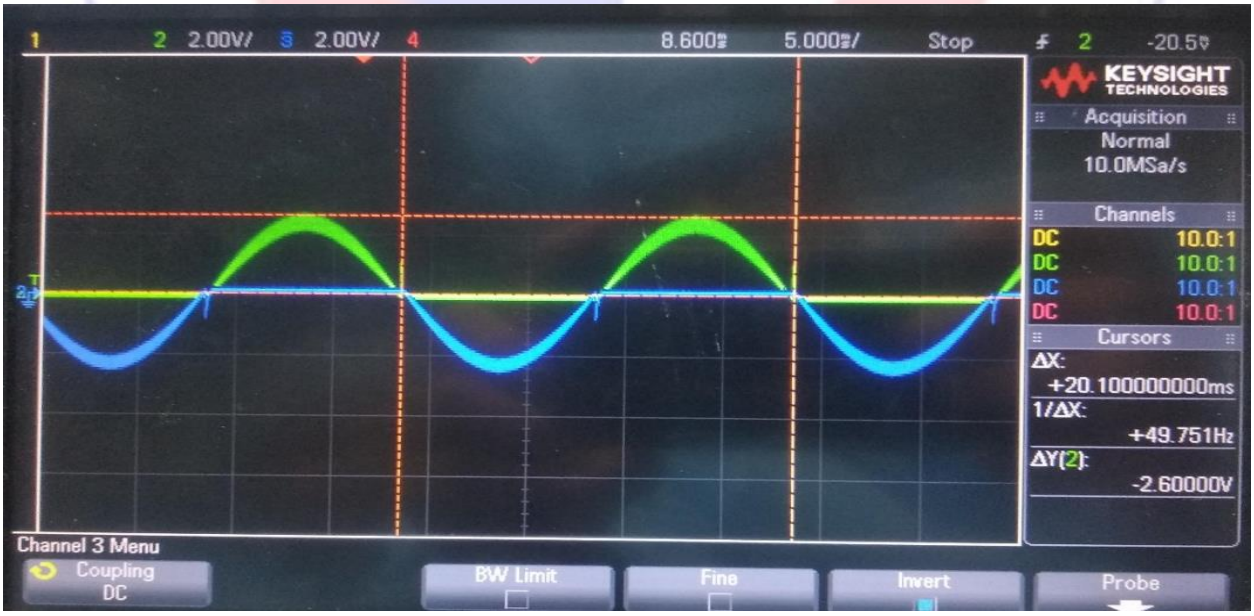

Fig 5.21 : Sinusoidal waveform after main pulses are passed through RC low pass filter (cutoff frequency = 1.59kHz)

Fig 5.22 shows the hardware CRO waveforms of Sinusoidal waveform after main pulses are passed through RC low pass filter with cutoff frequency of 1.59kHz and by increasing the voltage modulation index.

Fig 5.22 : Sinusoidal waveform after main pulses are passed through RC low pass filter (cutoff frequency = 1.59kHz) and by increasing the Voltage modulation index.

Fig 5.23 shows the hardware CRO waveforms of Generated inverter output without Output filter

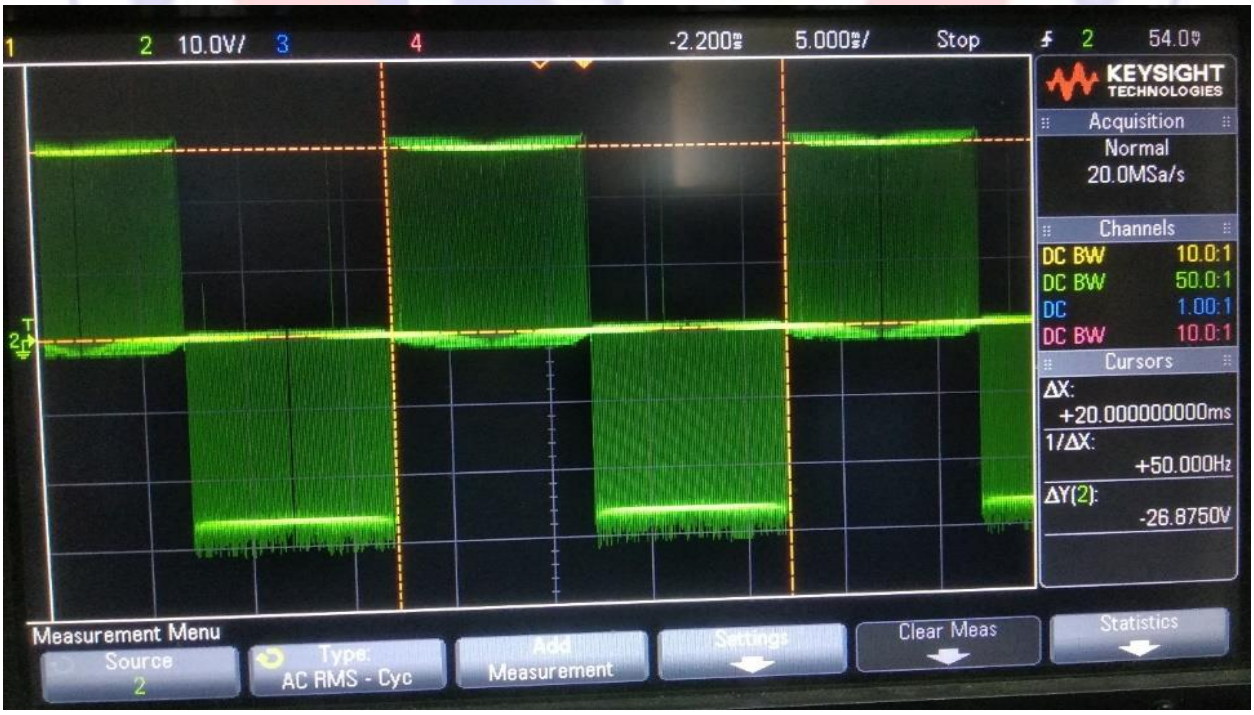

Fig 5.23 : Generated inverter output without Output filter

Fig 5.24 shows the hardware CRO waveforms of Generated inverter output with Output LC filter

Fig 5.24 : Generated Inverter output with output LC filter

Fig 5.25, Fig 5.26 and Fig 5.27 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for motor load.

Test method : Measured by dipping Temperature sensor in Liquid Nitrogen Cylinder.

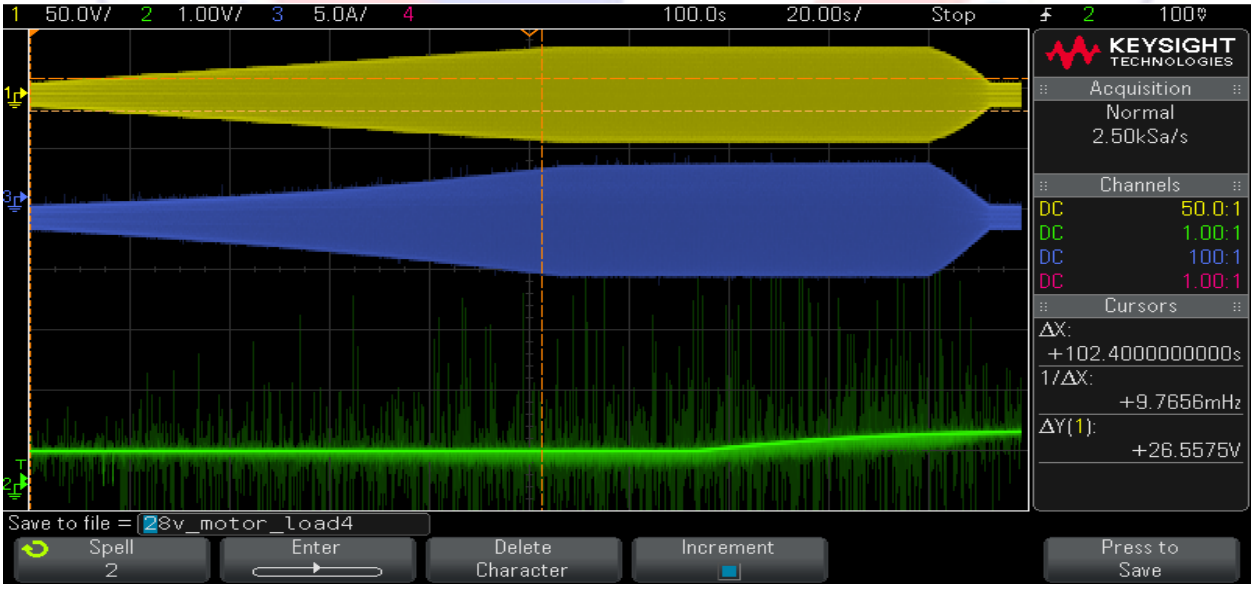

Fig 5.25 : Output voltage, output current and Temperature sensor at 28VDC for Motor load

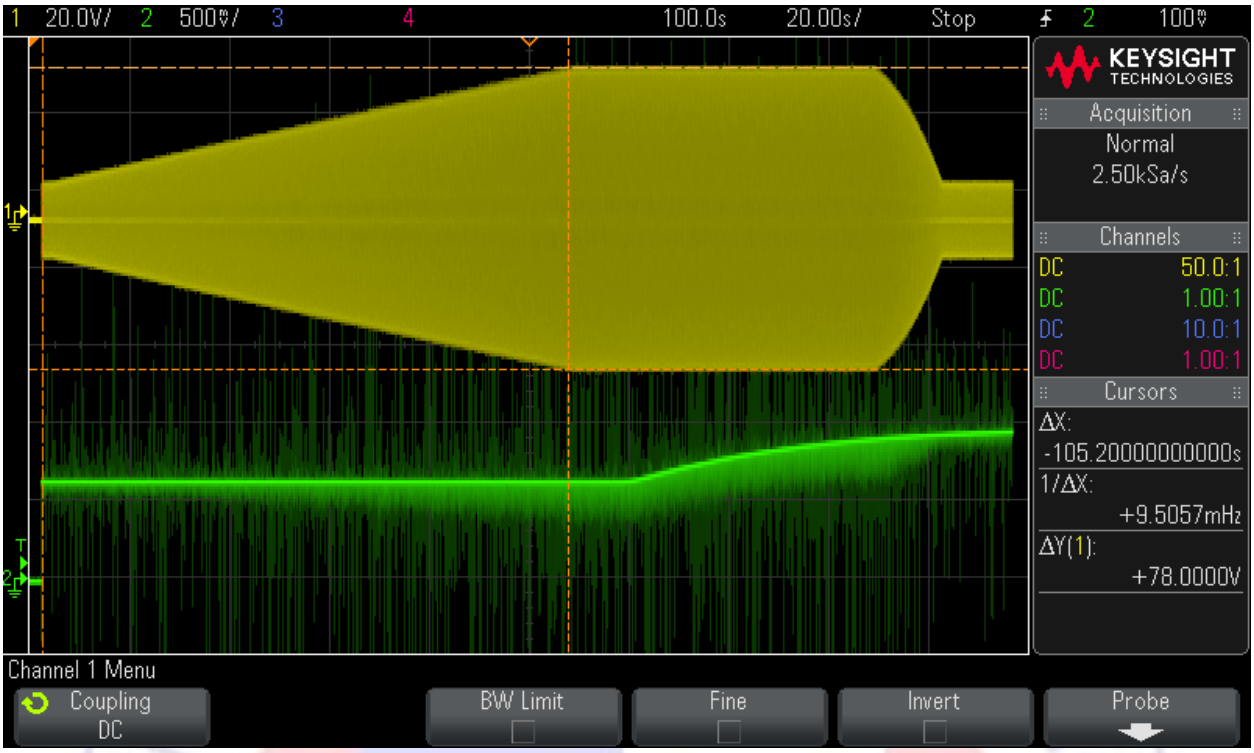

Fig 5.26 : Output voltage and Temperature sensor output voltage for motor load

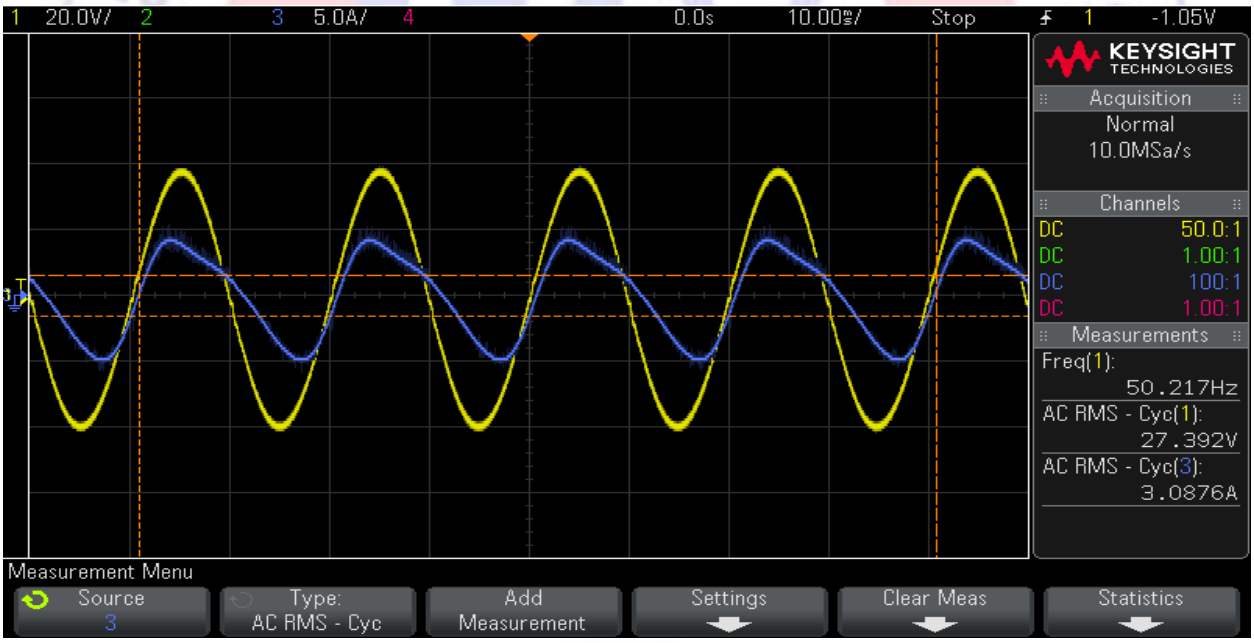

Fig 5.27 : Output voltage and output current for Motor load

Fig 5.28 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for 3-ohm Resistive load condition, here The temperature sensor voltage channel was set at high resolution mode to observe the waveform clearly.

Test method: Measured by dipping Temperature sensor in Liquid Nitrogen Cylinder.

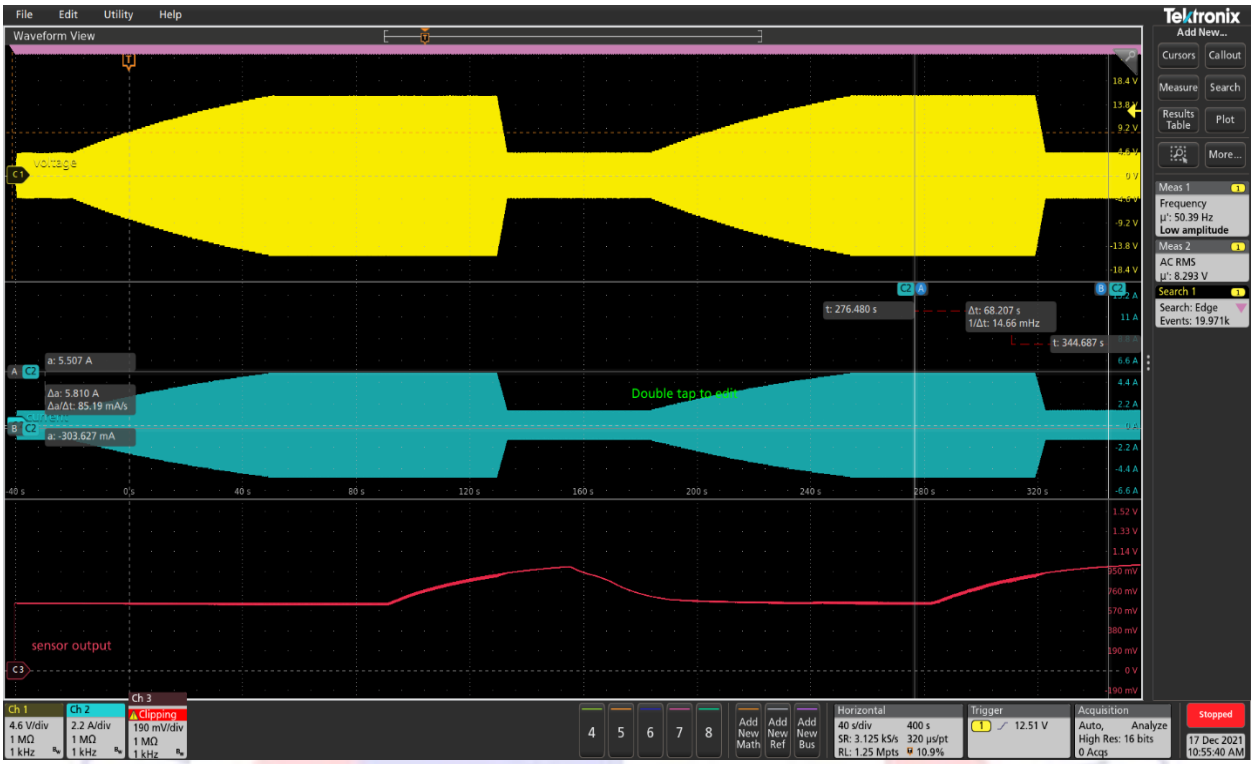

Fig 5.28 : Output voltage, output current and Temperature sensor voltage at 28VDC for 3-ohm resistive load condition

Fig 5.29 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for motor load.

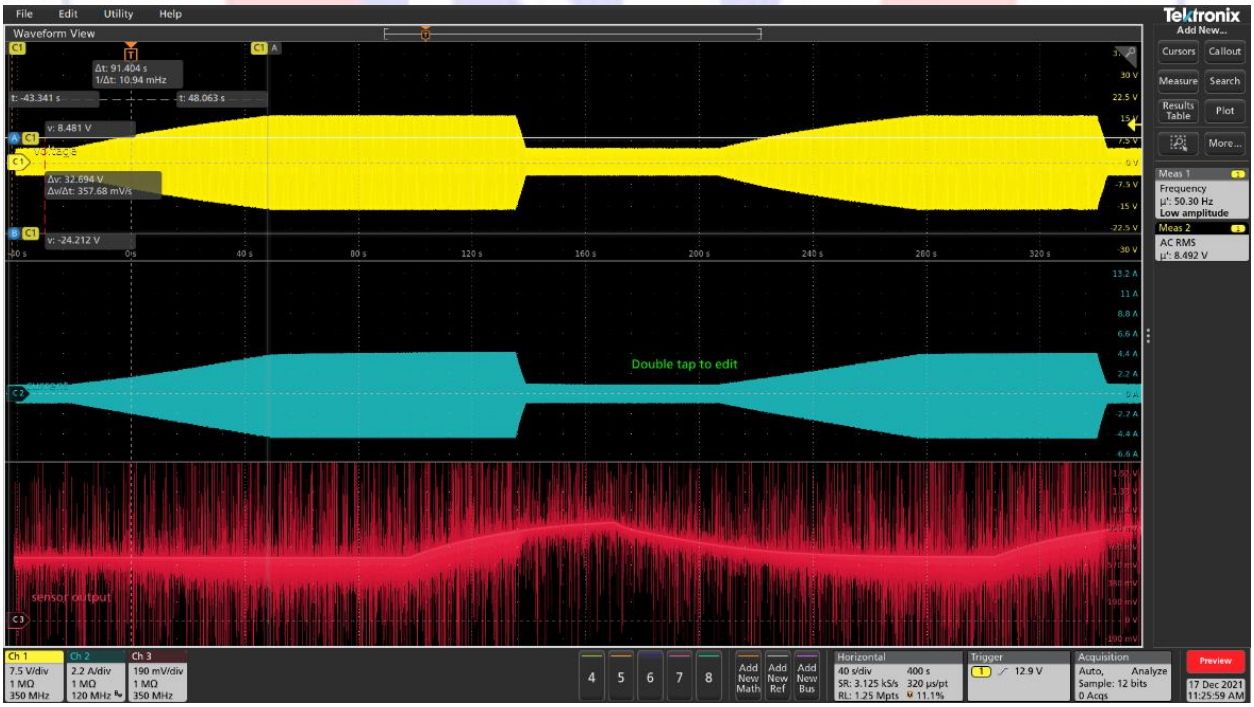

Fig 5.29 : Output voltage, output current and Temperature sensor voltage at 28VDC for Motor load

5.8 MIL-STD-461E CE102 EMI/EMC Testing

5.8.1 CE 102 : LIVE TO CHASSIS

Fig 5.30 represents the MIL-STD-461E EMI/EMC Live to Chassis Testing for the proposed prototype.

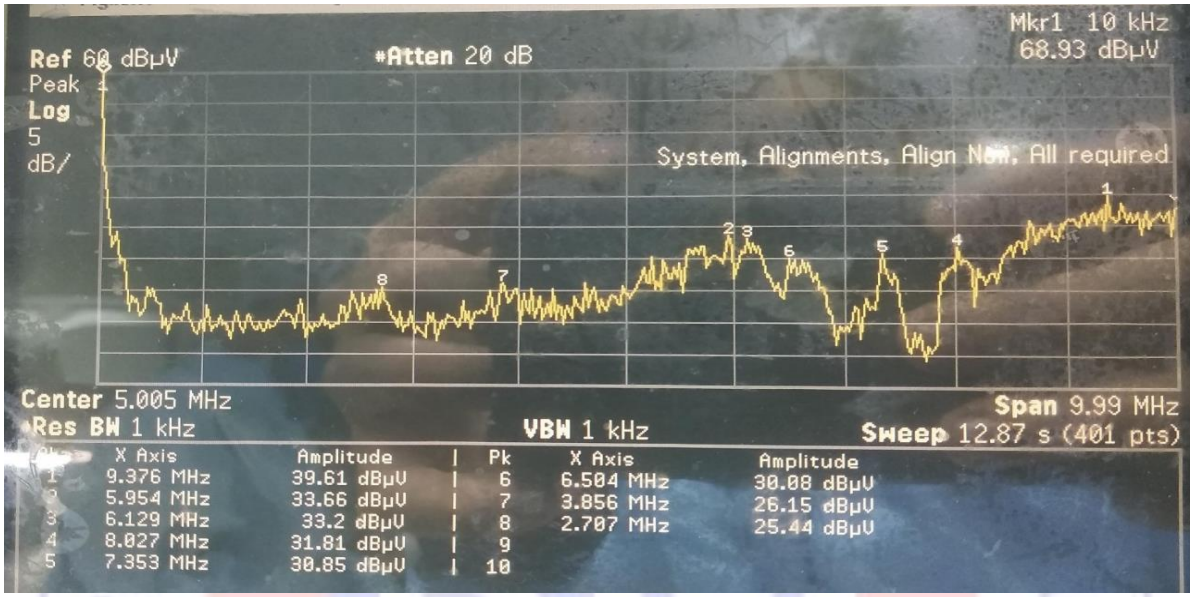

Fig 5.30 : CE 102 : LIVE TO CHASSIS

5.8.2 CE 102 : RETURN TO CHASSIS

Fig 5.31 represents the MIL-STD-461E EMI/EMC Return to Chassis Testing for the proposed prototype.

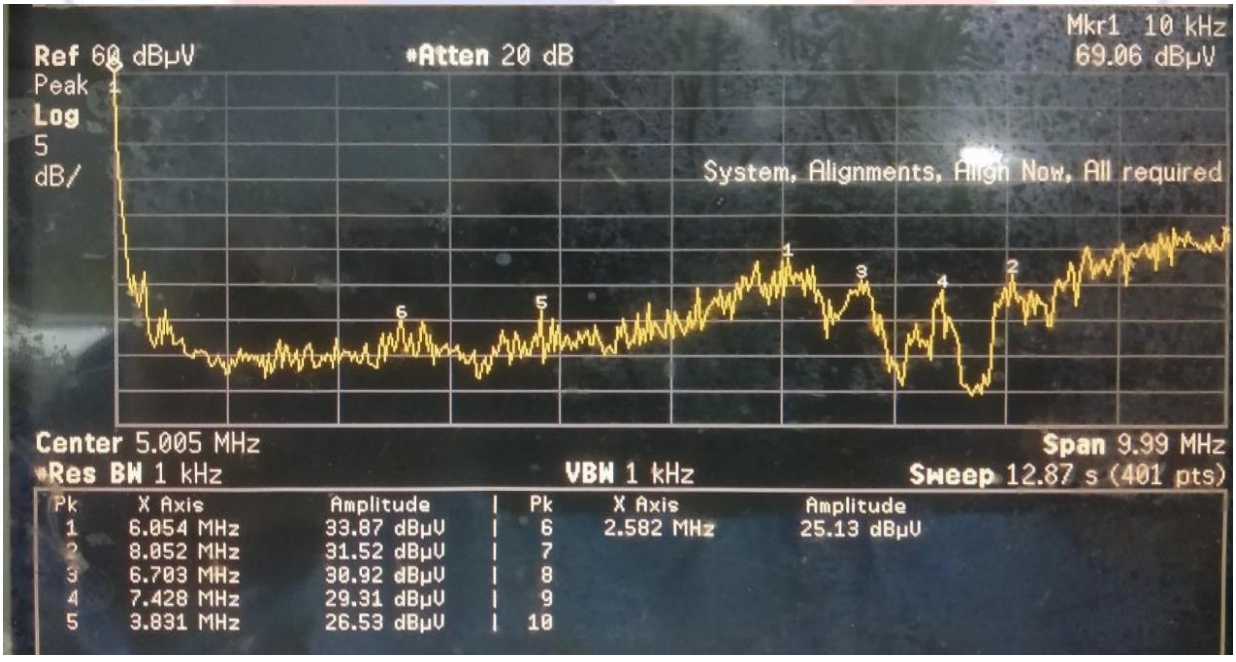

Fig 5.31 : CE 102 RETURN TO CHASSIS

5.9 Hardware PCB under testing

Fig 5.32 shows the Hardware Experimental Setup Under Testing for the proposed prototype.

Fig 5.32 : Hardware Experimental Setup Under Testing

Fig 5.33 shows the Hardware Experimental Setup Under Testing with Liquid Nitrogen Cylinder for the proposed prototype.

Fig 5.33 : Hardware Experimental Setup Under Testing with Liquid Nitrogen Cylinder

5.10 Hardware PCB and Experimental Setup of Cooler Drive Inverter

Fig 5.34 shows the hardware Printed Circuit Board(PCB) of the cooler drive inverter, here the main components are Main card(Inverter card), EMI card and Output card.

1.Main Card(Inverter Card)

2.Output Card

3.EMI Card

4.Relays(Main, Redundant and Launch lock Relays)

5.ATmegaS128 Microcontroller

6.Bulk Capactitor

7.MOSFET Driver ICs

8.EMI Filters

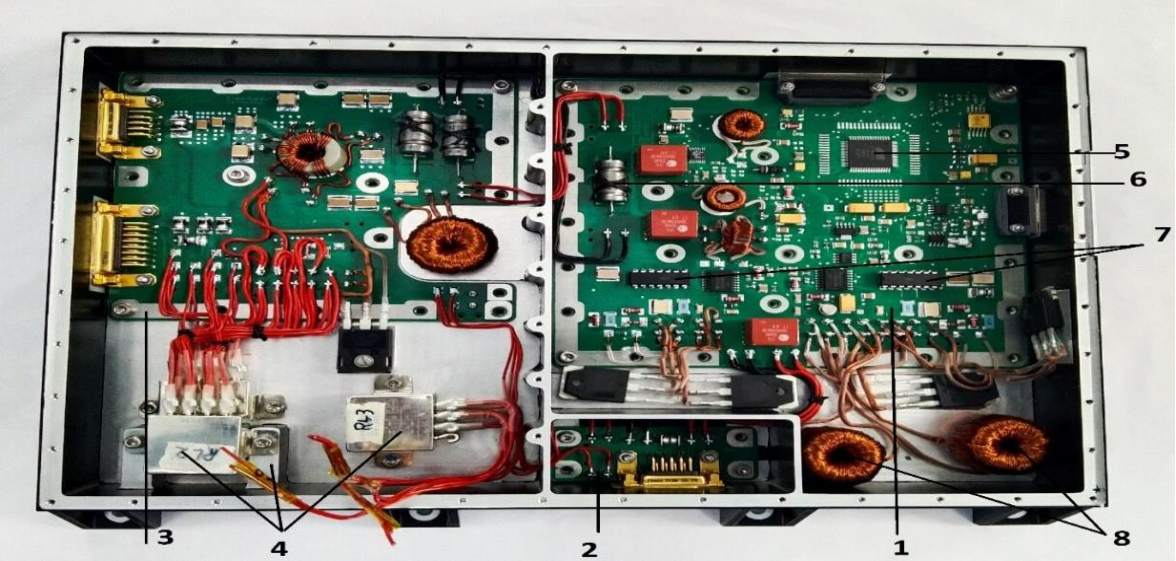

Fig 5.34 : Hardware PCB

Fig 5.35 shows the Hardware Experimental Setup of the cooler drive inverter with chassis.

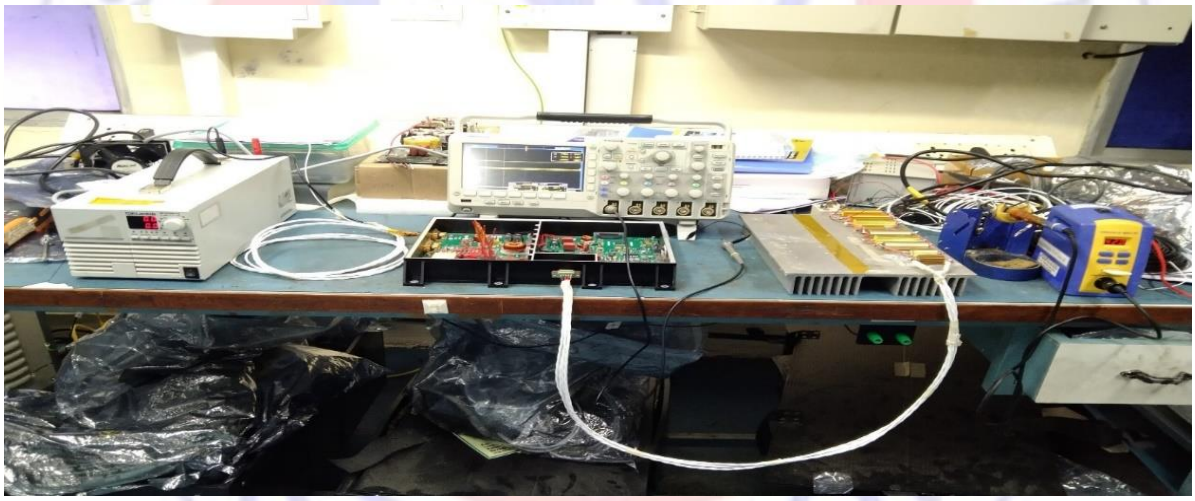

Fig 5.35 : Hardware Experimental Setup

5.11 Summary

In this chapter the simulation and hardware analysis which includes logic implementation in temperature Control, PWM Control Logic, H-Bridge inverter power circuit and waveforms, constant current source biasing circuit, protection circuits, Hardware CRO waveforms, MIL-STD 461E CE102 EMI/EMC Testing, Hardware PCB under testing and experimental setup of the proposed prototype were discussed in brief.

CHAPTER 6

RESULTS AND DISCUSSION

This chapter discusses about the hardware experimental results and discussion which includes tabulated results of output voltages, load regulation, line regulation, frequency, DC offset, THD, efficiency at 3Ω load condition and 60W load condition, ripple voltage, OCP, effect of feed forward loop at 25ºC ambient, 60ºC ambient and at cold tip conditions, measured experimental results of thermal sensor and slow and soft start measured results of cooler drive inverter.

6.1 Hardware Results of output voltage

Table 6.1 Shows the hardware implemented results of output voltages of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table 6.1 : OUTPUT VOLTAGES (VRMS)

VIN (V)	OUTPUT VOLTAGES (VRMS)		
	(12-15.7 VRMS) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	10.56	10.54	10.66
28	10.74	10.83	10.90
32	10.94	10.77	10.97
36	11.43	11.48	11.59

6.2 Hardware Results of load regulation

Table 6.2 Shows the hardware implemented results of load regulation of cooler drive inverter at 2.5ohm and 3.5ohm resistive load.

Table 6.2 : LOAD REGULATION

VIN (V)	LOAD REGULATION % for 2.5 Ohm resistor	LOAD REGULATION % for 3.5 Ohm resistor
24	0.61	-1.37
28	0.23	-1.47
32	0.35	-3.13
36	-0.96	-3.49

6.3 Hardware Results of Line regulation

Table 6.3 Shows the hardware implemented results of line regulation of cooler drive inverter for 28VDC input voltage.

Table 6.3 : LINE REGULATION

VIN (V)	LINE REGULATION % for 28VDC input voltage
24	4.02
32	-1.20
36	-6.34

6.4 Hardware Results of Frequency

Table 6.4 Shows the hardware implemented results of frequency of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table 6.4 : Frequency

VIN (V)	Frequency(Hz)		
	12VRMS (49.5 - 50.5) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	12VRMS (49.5 - 50.5) at 3.5 Ohm load
24	51.79	51.73	51.72
28	51.82	51.75	51.69
32	51.66	51.69	51.75
36	51.88	51.74	51.83

6.5 Hardware Results of DC offset

Table 6.5 Shows the hardware implemented results of DC offset(V) of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table 6.5 : DC offset

VIN (V)	DC offset (V)		
	12VRMS at 3.0 Ohm load(< 0.2V)	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	0.095	0.100	0.100
28	0.100	0.100	0.100
32	0.100	0.100	0.100
36	0.100	0.100	0.100

6.6 Hardware Results of THD

Table 6.6 Shows the hardware implemented results of Total Harmonic Distortion(THD) of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table 6.6 : Total Harmonic Distortion(THD)

VIN(V)	Total Harmonic Distortion(THD) %					
	12VRMS at 3.0 Ohm load		12VRMS at 2.5 Ohm load		12VRMS at 3.5 Ohm load	
	Secondary harmonics	Higher Harmonics	Secondary harmonics	Higher Harmonics	Secondary harmonics	Higher Harmonics
	<10%	<5%	<10%	<5%	<10%	<5%
28	0.425	3.250	0.32	3.510	0.19	3.450

6.7 Hardware Results of Efficiency at 3Ω Load Condition

Table 6.7 Shows the hardware implemented results of efficiency of cooler drive inverter at 3ohm resistive load.

Table 6.7 : Efficiency@3 ohm Load condition

At 3 ohm Load condition						
VIN (V)	Input current (A)	Input power (W)	Output Voltage (Vrms)	Output current (Irms)	Output power (W)	Efficiency (%) > 90% 60W @Rload 3 ohm
24	1.674	40.18	10.91	3.40	37.05	92.22
28	1.570	43.96	11.36	3.72	42.27	96.15
32	1.419	45.41	11.50	3.75	43.08	94.86
36	1.419	51.10	12.08	3.94	47.56	93.07

6.8 Hardware Results of Efficiency at 60W Load Condition

Table 6.8 Shows the hardware implemented results of efficiency of cooler drive inverter at 60W load condition.

Table 6.8 : Efficiency@60W Load condition

At 60W Load Condition						
VIN (V)	Input current (A)	Input power (W)	Output Voltage Vrms	Output current Irms	Output power (W)	Efficiency (%) > 90% 60W load condition

24	2.72	65.28	10.54	5.83	61.46	94.14
28	2.30	64.40	11.03	5.51	60.70	94.26
32	2.00	64.00	11.28	5.37	60.53	94.57
36	1.81	65.16	12.46	5.02	62.57	96.03

6.9 Hardware Results of Ripple Voltage

Table 6.9 Shows the hardware implemented results of ripple voltage of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table 6.9 : Vripple

VIN (V)	Vripple		
	(12-15.7 VRMS) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	1.30	1.30	1.20
28	1.30	1.20	1.20
32	1.80	1.30	1.50
36	1.70	1.50	1.60

6.10 Hardware Results of OCP

Table 6.10 Shows the hardware implemented results of Over Current Protection of cooler drive inverter.

Table 6.10 : Over Current Protection

OCP Limit	OCP Limit Spec : Min : 112.5% Max : 137.5%	Percentage %
24V	5.99	92.15
28V	7.00	107.69
32V	7.50	115.38
36V	8.12	124.92

6.11 Effect of Feedforward loop@25 deg Ambient conditions

Table 6.11 Shows the hardware implemented results of the Effect of Feedforward loop at 25 deg Ambient Conditions.

Table 6.11 : Effect of Feedforward loop@ 25 deg Ambient Conditions

At 25 deg Ambient conditions								
S.No	**Vin V**	**Iin A**	**Temp voltage V**	**Vo rms**	**Io A**	**Pin W**	**Po W**	**Efficiency %**
1	24	2.3348	0.3	12.56	4.19	56.0352	52.62137	93.91
2	25	2.3327	0.3	12.76	4.305	58.3175	54.9318	94.19
3	26	2.3037	0.3	12.92	4.357	59.8962	56.31335	94.02
4	27	2.3961	0.3	13.41	4.526	64.6947	60.69185	93.81
5	28	2.3689	0.3	13.56	4.597	66.3292	62.34819	94.00
6	29	2.3176	0.3	13.65	4.633	67.2104	63.24786	94.10
7	30	2.253	0.3	13.69	4.64	67.59	63.50861	93.96
8	31	2.1942	0.3	13.72	4.642	68.0202	63.70866	93.66
9	32	2.146	0.3	13.82	4.67	68.672	64.55808	94.01
10	33	2.07	0.3	13.77	4.653	68.31	64.07367	93.80
11	34	2.003	0.3	13.72	4.63	68.102	63.51064	93.26
12	35	1.9435	0.3	13.88	4.65	68.0225	64.56432	94.92
13	36	1.9982	0.3	14.10	4.779	71.9352	67.3839	93.67

6.12 Effect of Feedforward loop@60 deg Ambient conditions

Table 6.12 Shows the hardware implemented results of the Effect of Feedforward loop at 60 deg Ambient Conditions.

Table 6.12 : Effect of Feedforward loop@ 60 deg Ambient Conditions

At 60 deg Ambient conditions								
S.No	**Vin V**	**Iin A**	**Temp voltage V**	**Vo rms**	**Io A**	**Pin W**	**Po W**	**Efficiency %**
1	24	2.187	0.6	12.16	4.099	52.488	49.834	94.94
2	25	2.159	0.6	12.28	4.16	53.975	51.09312	94.66
3	26	2.0324	0.6	12.09	4.11	52.8424	49.68168	94.02

4	27	2.1067	0.6	12.55	4.253	56.8809	53.35814	93.81
5	28	2.063	0.6	12.73	4.31	57.764	54.85768	94.97
6	29	2.024	0.6	12.76	4.33	58.696	55.23348	94.10
7	30	1.9517	0.6	12.75	4.33	58.551	55.19884	94.27
8	31	1.8985	0.6	12.78	4.38	58.8535	55.95888	95.08
9	32	1.85	0.6	12.80	4.35	59.2	55.70088	94.09
10	33	1.769	0.6	12.74	4.319	58.377	55.02406	94.26
11	34	1.696	0.6	12.66	4.298	57.664	54.39549	94.33
12	35	1.646	0.6	12.62	4.301	57.61	54.27862	94.22
13	36	1.6901	0.6	12.98	4.415	60.8436	57.3067	94.19

6.13 Effect of Feedforward loop@Cold Tip Conditions

Table 6.13 Shows the hardware implemented results of the Effect of Feedforward loop at cold tip conditions.

Table-6.13 : Effect of Feedforward loop@Cold Tip Conditions

At cold tip conditions								
S.No	**Vin V**	**Iin A**	**Temp voltage V**	**Vo rms**	**Io A**	**Pin W**	**Po W**	**Efficiency %**
1	24	0.2792	1.5	4.29	1.443	6.7008	6.196819	92.48
2	25	0.2519	1.5	4.16	1.397	6.2975	5.806491	92.20
3	26	0.2225	1.5	3.98	1.331	5.785	5.297912	91.58
4	27	0.2266	1.5	4.09	1.376	6.1182	5.634445	92.09
5	28	0.2058	1.5	3.96	1.336	5.7624	5.293766	91.87
6	29	0.1752	1.5	3.71	1.246	5.0808	4.618673	90.90
7	30	0.1418	1.5	3.38	1.14	4.254	3.854568	90.61
8	31	0.1146	1.5	3.07	1.041	3.5526	3.19587	89.96
9	32	0.1069	1.5	3.01	1.017	3.4208	3.059543	89.44
10	33	0.068	1.5	2.41	0.818	2.244	1.973016	87.92
11	34	0.0473	1.5	2.11	0.684	1.6082	1.441872	89.66
12	35	0.0346	1.5	1.76	0.586	1.211	1.0285	84.93

13	36	0.0335	1.5	1.75	0.589	1.206	1.028865	85.31

6.14 Measured Experimental Results of Thermal Sensor

Table 6.14 Shows the Measured Experimental Results of Thermal Sensor of 1mA and 25uA constant current source.

Table-6.14 : Measured Experimental Results of Thermal Sensor

Temperature ° C	1mA current source		25uA current source	
	ICE (mA)	DTA2-DTK2 (V)	ICE (uA)	DTA1-DTK1 (V)
-50	0.993	0.6631	25.76	0.5431
-40	0.995	0.6651	25.77	0.5481
-30	0.997	0.6631	25.77	0.5441
-20	0.996	0.6629	25.78	0.5445
-10	0.998	0.6629	25.77	0.5431
0	0.995	0.6631	25.76	0.5431
10	0.994	0.6629	25.77	0.5481
20	0.995	0.6631	25.77	0.5441
30	0.996	0.6629	25.78	0.5445
40	0.994	0.6631	25.77	0.5431
50	0.995	0.6651	25.78	0.5445
60	0.995	0.6631	25.76	0.5431

6.15 Slow and Soft Start Measured Results of cooler drive inverter:

Table 6.15 shows the measured experimental results of slow start procedure implemented for the proposed prototype as per the appendix A.

Table-6.15 : Measured Experimental results of slow and soft start procedure implemented

S. No	Parameters	Time	Duration	Remarks
1	Soft start	T1	2.859 s	Adjustable
2	Ramp slow start	T2	93s	Adjustable. At present case 80s to 90s optimum.
3	Maximum voltage saturation (During cool down)	T3	100s	Not adjustable. Depends on the ADC and actual temperature sensor during cool down phase.
4	Fall down time	T4	5s	Adjustable as per real system.
5	Output Voltage during cool down phase	11.83 V	--	Adjustable as per actual drive.
6	Output Voltage during steady state phase	4.75V	--	Adjustable as per actual drive (Power is less than 20W as per data sheet) $P=V^2/R$. V= 5.5, R=3 ohms, P=10Watts.

6.16 Summary

In this chapter the hardware experimental results and discussion which includes tabulated results of output voltages, load regulation, line regulation, frequency, DC offset, THD, efficiency at 3Ω load condition and 60W load condition, ripple voltage, OCP, effect of feed forward loop at 25ºC ambient, 60ºC ambient and at cold tip conditions, measured experimental results of thermal sensor and slow and soft start measured results of cooler drive inverter were discussed in brief.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

The sensor used in many applications was a simple thermistor, a device whose resistance varies with temperature. This variation was typically an exponential function, and hence introduces a non linearity into the closed-loop control system. However, given the slow time constants of the open-loop plant and the relatively low bandwidth requirements of the controller, this nonlinearity caused difficulty from a control point of view.

In order to overcome the problems, a cooler drive inverter with regulated output followed by feed-forward control was designed. Voltage feed forward control technique was used to control the duty cycle. This control technique was simple to design and resulted in better line regulation. The converter was designed with 22KHz switching frequency using ATmegaS128 Microcontroller. It had functional benefits such as, simpler and more flexible to change the real-time control algorithms without further modification in a hardware with its reduced cost and also it reduced the complexity of the control circuit and better efficiency were acheived. Various protection circuits such as short circuit protection, over voltage protection and under voltage protection were implemented for the proposed cooler drive inverter.

7.1 Conclusion

Digitally controlled cooler drive inverter with feed-forward control for space application has been designed, simulated and implemented in hardware. The selected topology was H-Bridge inverter. The simulation analysis were carried out in MATLAB/Simulink, LTspice and PSIM platform. The Main components include ATmegaS128 Microcontroller, PID Controller, Protection Circuits, MOSFET Switches, Analog to Digital Converter, Driver Circuits, 2N2222A Transistor and Relays. The major conclusions drawn from hardware analysis are,

- The efficiency of cooler drive inverter were found to be more than 90% at 3Ω Load condition, 60W load condition and motor load condition.
- The effect of feedforward loop at 25º C, 60º C ambient and at Cold Tip Conditions were tabulated and efficiency was found to be more than 90% for various range of input voltage from 24V to 36V DC.
- The regulated output voltage of the cooler drive inverter was found to be 12V AC RMS with +/- 1% variation, for various range of input voltage from 24V to 36V DC.

- The regulated output current of the cooler drive inverter was found to be 6A AC RMS with +/- 1% variation, for various range of input voltage from 24V to 36V DC.
- The obtained output ripple, frequency, DC offset, Total Harmonic Distortion, load and line regulation were within the specified limits.

7.2 Future Scope

There is scope for future improvement of the converter. They are as listed below

- PWM Pulses for the H-Bridge Inverter can be controlled by using Op-Amps.
- GaN(Gallium Nitride) Material switch can be used instead of silicon material MOSFET switch to reduce losses and to further improve the efficiency of cooler drive inverter.
- TMP36 Thermal Sensor can be used to get more accurate sensor voltage readings.

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APPENDIX A
Datasheets

3.3 Slow Start

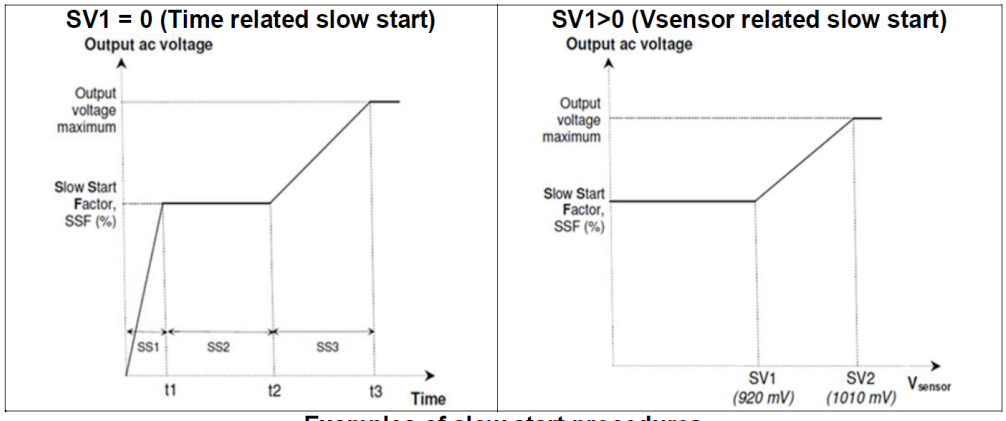
3.3.1 Slow Start Definition

"Slow start" is a procedure aimed at protecting and preserving the compressor from potential internal shocks while limiting the vibrations induced on system. This procedure consists in a starting at low input power followed by a ramp-up to max power. The only side effect of this procedure is that it increases the cool down time.

3.3.2 Example of Slow Start Correction (for information only)

The slow start function gradually increases the ac output voltage after start-up to the programmed maximum output voltage. This function is required to achieve quick cooldown times while preventing the cooler from hitting its end stops. Hitting the end stops can damage the cooler.

The gradual increase can consist of 1, 2 or 3 timed phases or can be made dependable on the actual temperature diode voltage. In the figure below the slow start principles for both time and temperature diode dependencies are depicted.



Examples of slow start procedures

3.3.3 Slow Start Correction for Saturn Coolers

The completion of both design and qualification phases have permitted to demonstrate that slow start procedure was not required at all. The required voltage can thus be put on from the start when the cooler is warm. No further limiting of the input voltage is required.

FAIRCHILD

June 2014

FQA70N15

N-Channel QFET® MOSFET

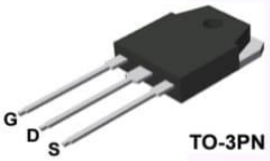
150 V, 70 A, 28 mΩ

Description

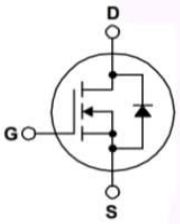
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 70 A, 100 V, $R_{DS(on)}$ = 28 mΩ (Max)@V_{GS} = 10 V, I_D = 35 A
- Low Gate Charge (Typ. 135 nC)
- Low Crss (Typ.135 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



TO-3PN



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQA70N15	Unit
V_{DSS}	Drain-Source Voltage		150	V
I_D	Drain Current - Continuous (T_C = 25°C)		70	A
	- Continuous (T_C = 100°C)		50	A
I_{DM}	Drain Curent - Pulsed	(Note 1)	280	A
V_{GSS}	Gate-Source Voltage		± 25	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1000	mJ
I_{AR}	Avalanche Current	(Note 1)	70	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	33	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		330	W
	- Derate above 25°C		2.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQA70N15	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

2N2222 / 2N2222A

NPN Silicon Epitaxial Planar Transistor
for switching and AF amplifier applications.

The transistor is subdivided into one group according to its DC current gain.

On special request, these transistors can be manufactured in different pin configurations.

1. Emitter 2. Base 3. Collector
TO-92 Plastic Package

Absolute Maximum Ratings (T_a = 25 °C)

Parameter		Symbol	Value	Unit
Collector Base Voltage	2N2222 2N2222A	V_{CBO}	60 75	V
Collector Emitter Voltage	2N2222 2N2222A	V_{CEO}	30 40	V
Emitter Base Voltage	2N2222 2N2222A	V_{EBO}	5 6	V
Collector Current		I_C	600	mA
Power Dissipation		P_{tot}	625	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	- 55 to + 150	°C

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2N2222 / 2N2222A

Characteristics at T_a = 25 °C

Parameter		Symbol	Min.	Max.	Unit
DC Current Gain					
at V_{CE} = 10 V, I_C = 0.1 mA		h_{FE}	35	-	-
at V_{CE} = 10 V, I_C = 1 mA		h_{FE}	50	-	-
at V_{CE} = 10 V, I_C = 10 mA		h_{FE}	75	-	-
at V_{CE} = 10 V, I_C = 150 mA		h_{FE}	100	300	-
at V_{CE} = 10 V, I_C = 500 mA	2N2222	h_{FE}	30	-	-
	2N2222A	h_{FE}	40	-	-
Collector Base Cutoff Current					
at V_{CB} = 50 V	2N2222	I_{CBO}	-	10	nA
at V_{CB} = 60 V	2N2222A		-	10	
Collector Base Breakdown Voltage					
at I_C = 10 µA	2N2222	$V_{(BR)CBO}$	60	-	V
	2N2222A		75	-	
Collector Emitter Breakdown Voltage					
at I_C = 10 mA	2N2222	$V_{(BR)CEO}$	30	-	V
	2N2222A		40	-	
Emitter Base Breakdown Voltage					
at I_E = 10 µA	2N2222	$V_{(BR)EBO}$	5	-	V
	2N2222A		6	-	
Collector Emitter Saturation Voltage					
at I_C = 150 mA, I_B = 15 mA	2N2222		-	0.4	
	2N2222A	$V_{CE(sat)}$	-	0.3	V
at I_C = 500 mA, I_B = 50 mA	2N2222		-	1.6	
	2N2222A		-	1	
Base Emitter Saturation Voltage					
at I_C = 150 mA, I_B = 15 mA	2N2222		-	1.3	
	2N2222A	$V_{BE(sat)}$	0.6	1.2	V
at I_C = 500 mA, I_B = 50 mA	2N2222		-	2.6	
	2N2222A		-	2	
Gain Bandwidth Product					
at I_C = 20 mA, V_{CE} = 20 V, f = 100 MHz		f_T	250	-	MHz
Collector Output Capacitance					
at V_{CB} = 10 V, f = 1 MHz		C_{ob}	-	8	pF

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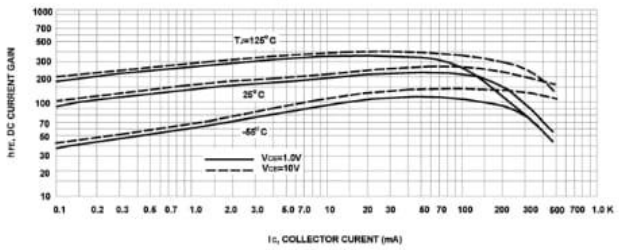
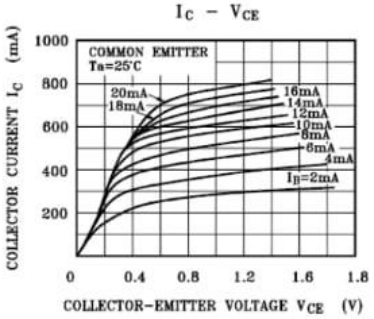
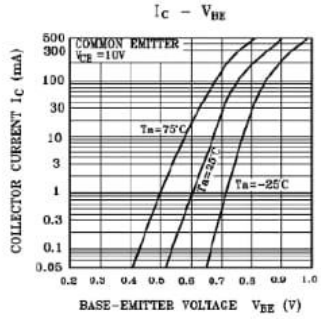
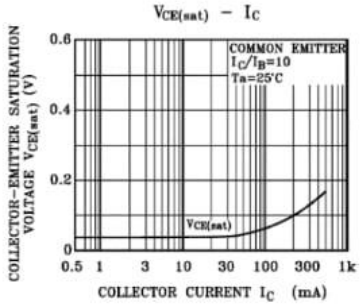
2N2222 / 2N2222A

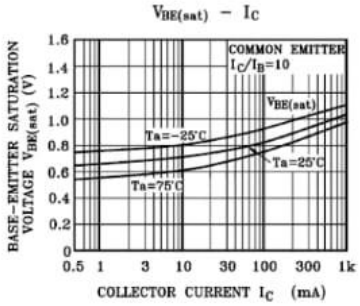
Figure 1. DC Current Gain

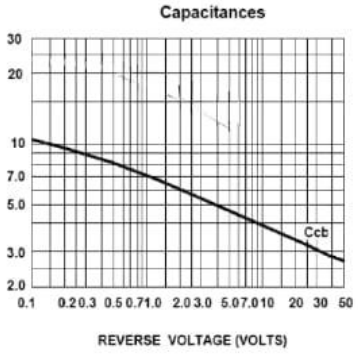


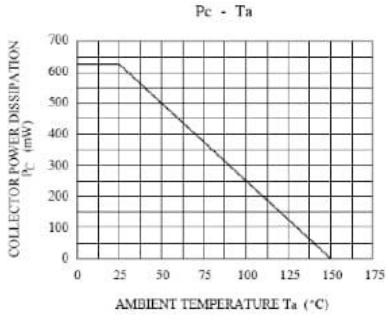












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Dated : 12/06/2016 Rev:02

Design and Implementation of Digitally Controlled Cooler Drive Inverter for Temperature Control

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OBJECTIVE

To design and implement digitally controlled cooler drive inverter for the control of temperature in the Cryocoolers via a PID control loop based upon the temperature signal feedback from the temperature sensor used for space and defence application.

Project Methodology

The **Prototype** interfaces with the cooler by supplying it with an AC voltage. It takes 28V DC as input power supply. It basically generates AC power via a PID control loop to control the cooling on detector array based upon the input from the temperature sensor mounted on detector Focal Plane Array (FPA). Feedback for the control loop is provided by the temperature signal. Temperature sensor is a Base/Emitter silicon junction of a transistor 2N2222A. In order to increase the relative accuracy of the thermal sensor, it is supplied with 1mA and is connected to cooler PID control loop.

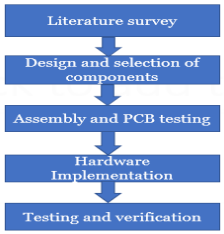

Fig 1 : Methodology

Specifications

Specifications of Cooler Drive Inverter	
Parameter	**Specifications**
I/P Voltage Range, Nominal Input Voltage	24V – 36V DC, 28V DC
Topology	H-Bridge Inverter
Nominal O/P Voltage and O/P Current	12V/6A AC
Switching Frequency	22KHz
AC Output Power	72W
Output Frequency	50Hz ,+/- 1%
Controller used	ATmegaS128 Microcontroller

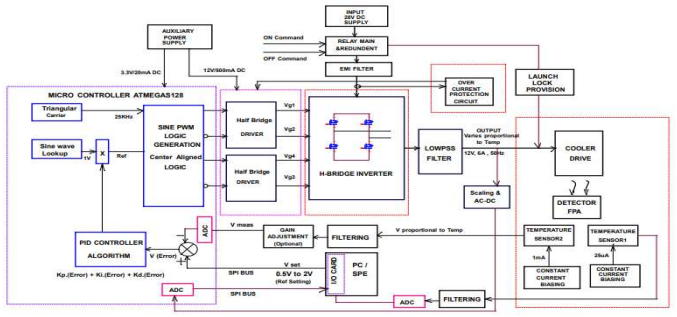

Fig 2 : Functional Block Diagram of Proposed Prototype

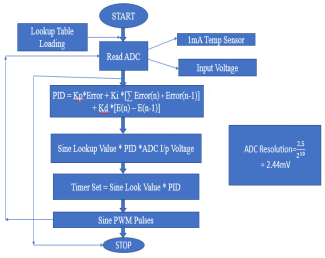

Fig 3 : Logic Implementation Flow Chart

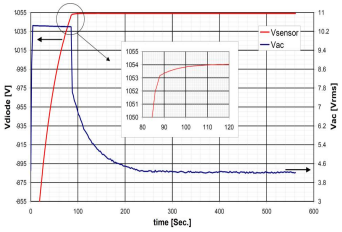

Fig 4 : Illustration of Temperature Sensing Diode Voltage versus Inverter Output Voltage

The converter (DC-AC) has been equipped with a separate 1mA current source to bias a temperature sensing diode. The voltage measured across the sensing diode is used by the control algorithm in the converter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature. The temperature stability is strongly dependent on the correct measurement of the diode sensor voltage. The value for the diode set-point voltage is programmed in the converter by means of a software setting. This voltage "set-point" can be adjusted within a range of 0.5 to 2 Volts.

Results and Discussions

Fig 5 : Output voltage, Output current and Temperature sensor voltage at 28VDC for 3-ohm resistive load

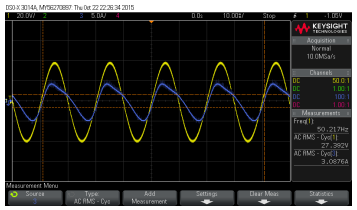

Fig 6 : Output voltage & output current for Motor load

VIN (V)	OUTPUT VOLTAGES (VRMS)		
	(12-15.7 VRMS) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	10.56	10.54	10.66
28	10.74	10.83	10.90
32	10.94	10.77	10.97
36	11.43	11.48	11.59

VIN (V)	Frequency(Hz)		
	12VRMS (49.5 - 50.5) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	12VRMS (49.5 - 50.5) at 3.5 Ohm load
24	50.27	50.27	50.23
28	50.22	50.28	50.25
32	50.29	50.21	50.24
36	50.27	50.11	50.19

At 3 ohm Load condition						
VIN (V)	Input current (A)	Input power (W)	Output Voltage (Vrms)	Output current(Irms)	Output power (W)	Efficiency (%) > 90% 60W @Rload 3 ohm
24	1.610	38.64	10.56	3.50	36.97	95.67
28	1.450	40.60	10.74	3.56	38.27	94.26
32	1.310	41.92	10.94	3.63	39.77	94.87
36	1.278	46.01	11.43	3.79	43.35	94.22

Fig 5 & Fig 6 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for 3-ohm Resistive load and motor load condition, here The temperature sensor voltage channel was set at high resolution mode to observe the waveform clearly and the tables shows the readings of output voltage, Frequency and efficiency at 3 ohm load condition.

Test method : Measured by dipping Temperature sensor in Liquid Nitrogen Cylinder.

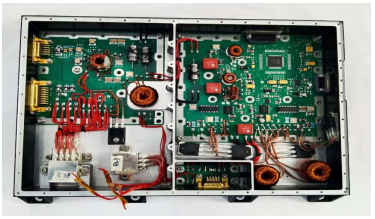

Fig 7 : Hardware PCB of Cooler Drive Inverter

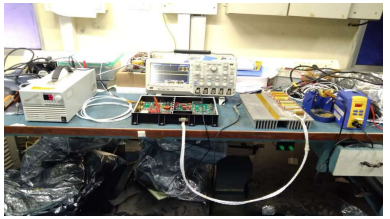

Fig 8 : Hardware Experimental Setup of Cooler Drive Inverter

Conclusions

Digitally controlled cooler drive inverter with feed-forward control for space application has been designed. The selected topology was H-Bridge inverter. The Main components include ATmegaS128 Micro controller, PID Controller, Protection Circuits, MOSFET Switches, Analog to Digital Converter, Driver Circuit, 2N2222A Transistor and Relays. The Hardware Implementation results shows that the output voltage obtained was 12V and the output current obtained was 6A. The obtained efficiency was more than 90% and obtained output ripple, Frequency, DC offset, Total Harmonic Distortion, Load and Line regulation were within the specified limits.

Future Scope

There is scope for future improvement of the inverter and they are as follows

- PWM Pulses for the H-Bridge Inverter can be controlled by using Op-Amps.
- GaN(Gallium Nitride) Material switch can be used instead of silicon material MOSFET switch to reduce losses and to further improve the efficiency of cooler drive inverter.
- TMP36 Thermal Sensor can be used to get more accurate sensor voltage readings.

Acknowledgements

- **I deeply express my sincere gratitude to my guide Dr. Anitha G S, Associate professor, Dept. of EEE, RVCE, Principal and HOD, Dept. of EEE, RVCE and Panel members for their patience and valuable guidance throughout this project.**
- **I would like to express my deepest appreciation to Centum Electronics Limited, Bengaluru, for providing me an opportunity to carry out the project in their organization.**

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Design and Implementation of Digitally Controlled Cooler Drive Inverter for Temperature Control

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Abstract : Cooler drives are widely used for cryocoolers, a cryocooler is a refrigerator designed to reach cryogenic temperatures and its main purpose is to cool objects quickly using extremely low temperatures. The main objective is to capture the image from the Space and fed to the FPGA and the signal received is converted to Digital form using Analog to Digital converter (ADC). The proposed inverter drives the cooler drive with 12V/6.5A, 50Hz AC output power via a PID control loop with input voltage range from 24V to 42.5V DC to control the cooling of detector array based upon the temperature signal feedback from the temperature sensor mounted on detector Focal Plane Array. Efficiency of more than 90% is achieved for different range of input DC Voltage and in order to increase the relative accuracy of the thermal sensor, it is supplied with 1mA, 25uA constant current source to bias a temperature sensing diode and is connected to cooler PID control loop for temperature regulation. The voltage measured across the sensing diode is used by the control algorithm in the inverter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature.

Keywords : ATmegaS128 Microcontroller, H-Bridge Inverter, 2N2222A Transistor, ADC, Sine PWM, PID Controller.

I. INTRODUCTION

Power supply unit is an interface between power source and the electric load. The main function of the power supply unit is to modulate or convert the available electrical energy from the power supply into the form required by the load. It is quite rare that the power source directly matches the requirements of a particular load [1]. So, the power supply units find extensive applications in various industries. Input power source may be AC or DC, while the load may be a motor, an electronic equipment, or a computer [8-10]. Since the Input to the cooler drives are AC, H-Bridge inverters are commonly used to convert DC Power into AC power and In order to generate sinusoidal PWM pulses for the single phase H-Bridge inverter, ATmegaS128 Microcontroller is used because it is simpler and more flexible to change the real-time control algorithms without further modification in a hardware with its reduced cost and also it reduces the complexity of the control circuit[1-2].

Cooler drive Inverter is designed to meet demand for the low-cost cooling options for local plane on very short duration. The output is controlled using Duty cycle of the PID Controller and accordingly the PWM waveforms are generated for controlling the output voltage. These applications place high demand on both cooler operating conditions and on the thermal control of the cooler environment because of the extreme temperature variation and because of limited available power. The converter uses Feed forward topology for fast response of closed loop control with changes in the input voltage and Feedback technique is implemented for regulating both output voltage and temperature sensor voltage . Analog to Digital converter is used to convert analog signals to digital signals. The Switching frequency of 22KHz is used to reduce the size of the converter. The converter is provided with two relays i.e., Main relay for Turning the converter ON-OFF and Launch lock relay is used to avoid the mechanical vibrations and secure moving

during launching. The converter is provided with protection circuits such as Over Voltage Protection (OVP), Under Voltage Protection (UVP) and Over Current Protection (OCP).

1.1 ATmegaS128 MICRO CONTROLLER

In microcontroller-based design, ATmegaS128 is operated at 8MHz frequency. It has Internal 10-bit ADC and pre-scalar. So maximum ADC sampling clock is 50KHz to 200KHz, so it supports maximum resolution of 15KSPS only and the features of ATmegaS128 microcontroller are as follows

- Advanced RISC architecture /Up to 8MIPS
- 3V-3.6V / 0 - 8MHz operating voltages & speed grades
- Two 8-bit and two 16-bit timers/counters
- 6 PWM channels
- 8-channel, 10-bit ADC
- TWI/USARTs/SPI serial interface
- Programmable watchdog timer
- On-chip analog comparator
- 128 Kbytes of Flash program memory
- 4 Kbytes EEPROM – 4 Kbytes internal SRAM
- Up to 64 Kbytes optional external memory space.
- SPI interface for in-system Programming (ISP).

II. VOLTAGE FEED FORWARD CONTROL

Block diagram of voltage feed forward control is as shown in Fig - 1 . In this method instead of fixed slope saw tooth ramp, a ramp whose slope varies in proportion to the input voltage variation is used at the PWM modulator input[8-10]. The input voltage is first sensed and attenuated using the voltage divider constituted of resistors R_1 and R_2. It is then inverted before being brought to the input of the integrator. Integrator is reset at the starting of each cycle by an external fixed frequency clock signal. Since in this control technique the slope of the ramp is proportional to the input voltage, and the output voltage of the error amplifier is compared with this ramp to generate duty cycle. Any change in the input voltage causes immediate change in the duty cycle even if the bandwidth of voltage loop is very low.

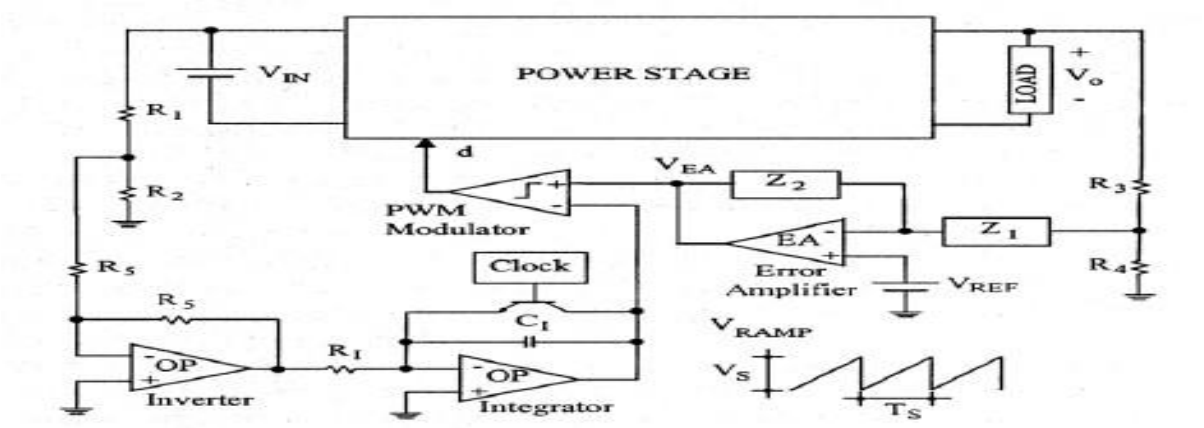

Fig – 1 : Block diagram of voltage feed forward control.

After the input voltage is increased, at $t=T_o$, the slope of the ramp increases causing the duty cycle to reduce immediately so as to maintain the output voltage constant as shown in Fig-2. Because of this instantaneous change in duty cycle, output voltage overshoot caused because of the input step change is decreased. Any increase in input causes the decrease in duty cycle. Thus good line regulation is achieved.

The operation of the feed forward scheme is described by following equations.

$$Vs = \left(\frac{V_{in}}{K}\right) \quad \text{.....(2.1)}$$

$$D = \left(\frac{T_{on}}{T}\right) = \left(\frac{V_c}{V_s}\right) = \left(\frac{KV_c}{V_{in}}\right) \quad \text{.....(2.2)}$$

Where,

D: Duty ratio

K: constant

V_{in}: Input voltage

V_s: Peak-Peak Saw tooth Voltage

V_c: Control Voltage

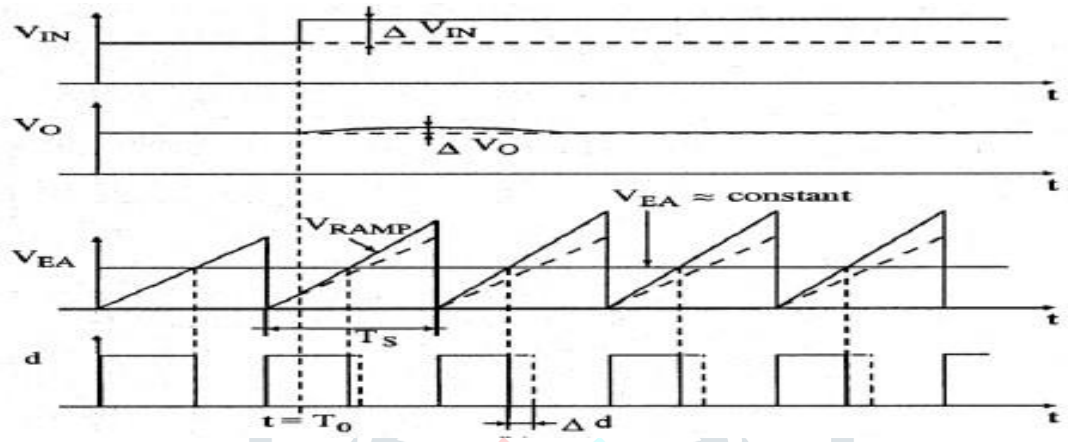

Fig-2 : Key waveforms during step change in V_{in} for voltage mode feed forward control.

2.2 Temperature Sensing Diode Input

The converter (DC-AC) has been equipped with a separate 1mA current source to bias a temperature sensing diode. Fig-3 and Fig-4 represents the temperature sensing diode input and the Illustration of Temperature Sensing Diode Voltage versus Inverter Output Voltage . The voltage measured across the sensing diode is used by the control algorithm in the converter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature.

The temperature stability is strongly dependent on the correct measurement of the diode sensor voltage. The value for the diode set-point voltage should be programmed in the converter by means of a software setting. This voltage "set-point" should be able to be adjusted within a range of 0.5 to 2 Volts.

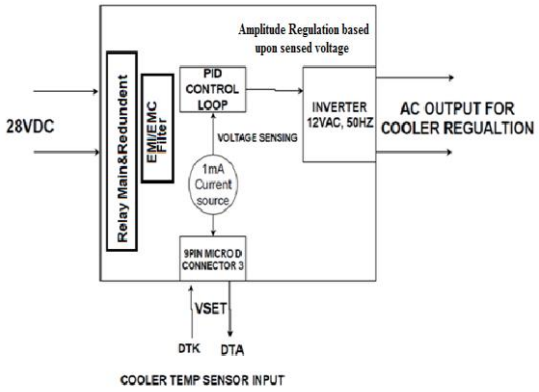

Fig-3 : Temperature Sensing Diode Input

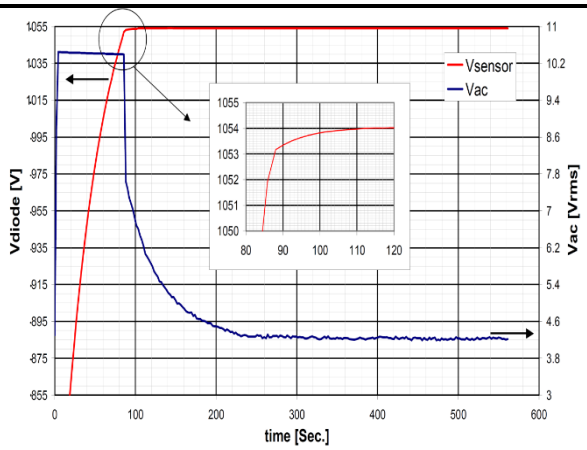

Fig-4 : Illustration of Temperature Sensing Diode Voltage versus Inverter Output Voltage

III. FUNCTIONAL BLOCK DIAGRAM AND METHODOLOGY

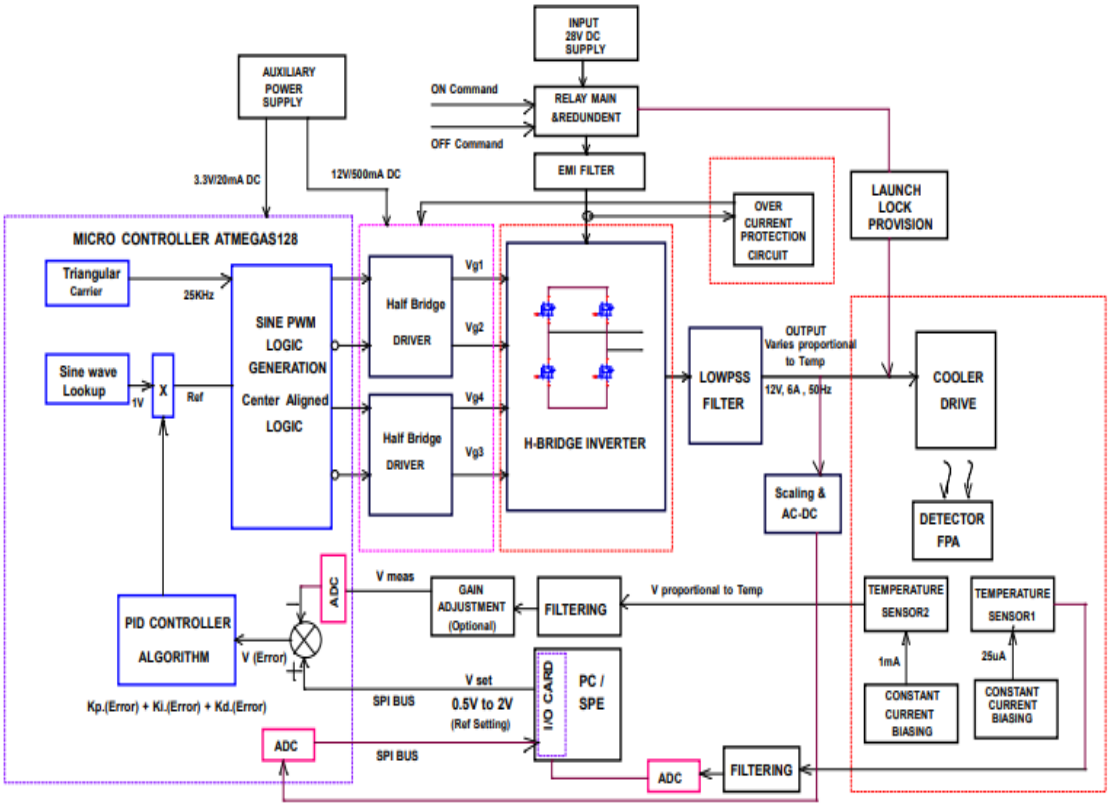

Fig-5 : Functional Block Diagram of the Cooler Drive Inverter

Functional block diagram of the proposed prototype is as shown in Fig-5. The Hardware Prototype interfaces with the cooler by supplying it with an AC voltage. It takes 28V DC as input power supply. The prototype basically generates AC power via a PID control loop to control the cooling on detector array based upon the input from the temperature sensor mounted on detector Focal Plane Array(FPA). Three Latch Type relays(ON/OFF type Relays) are used namely, Relay main, Relay redundant and launch lock relay and their commands are controlled via the Relay command input connector.

Since the input current will be fluctuating , The EMI/EMC filters are used at the input stage to filter out the fluctuations in the input current. The filtered DC input is given to the H-bridge inverter. The ATmegaS128 microcontroller output signal drives an H-bridge, pulse-width modulated (PWM) output stage. Since the output from the H-bridge inverter is sinusoidally variable pulses and to minimize the amount of generated EMI, sufficient output filtering has been used and finally it is given to the output low pass filter to get pure sinusoidal pulses and finally is given to the cooler drive(Pure noise free AC power).

The RMS output voltage is determined by the temperature control loop. Feedback for the control loop is provided by the temperature signal. The converter (DC-AC) has been equipped with a separate 1mA and 25uA constant current source to bias a temperature sensing diode . In order to increase the relative accuracy of the thermal sensor, it is supplied with 1mA, 25uA and is connected to cooler PID control loop.

Temperature sensor is a Base/Emitter silicon junction of a transistor 2N2222A .The voltage measured across the sensing diode is used by the control algorithm in the converter to regulate the AC output voltage so that the cooler will maintain a stable cold tip temperature. The temperature stability is strongly dependent on the correct measurement of the diode sensor voltage. The value for the diode set-point voltage should be programmed in the converter by means of a software setting.

This voltage "set-point" should be able to be adjusted within a range of 0.5 to 2 Volts. During a cool down, the maximum RMS voltage can be limited depending on the ambient temperature, time after restart or the actual cold tip temperature. The maximum output voltage as well as the limitation criteria are programmed in the converter and can be adjusted according to cooler and system parameters.

IV. SPECIFICATIONS AND DESIGN DETAILS

4.1 SPECIFICATIONS

Table 1 shows the specifications of the Cooler Drive Inverter using ATmegaS128 Micro Controller.

Table 1 : Specifications for the proposed prototype

Sl.no	Parameter	Specifications
1	Input Voltage Range	24V - 42.5V DC
2	Nominal Input Voltage	28V DC
3	Nominal Output Voltage (RMS)	12V AC
4	Maximum Output Voltage (RMS)	15.7V AC
5	Maximum AC Power Output	78 W
6	Topology	H-Bridge Inverter
7	Maximum AC Output Current	6.5 A
8	Nominal Output Current	6A
9	Modulation	Sine PWM
10	Switching Frequency	22KHz
11	AC Output Power	72W
12	Output Frequency	50Hz ,+/- 1%
13	Protections	OCP, UVP and OVP
14	Controller used	ATmegaS128 Microcontroller (10MHz, 8 channel 10-bit ADC, 30k Radiation, 6 PWM channels, 53 GPIO,4KB EEPROM and 64KB External memory).
15	Efficiency (%)	> 90% at 60W (@R load 3Ω)
16	Bias current temperature sensing diode	1 mA,25uA +/-4%
17	Maximum permissible DC offset level at output	0.2V
18	THD (Total Harmonic Distortion) Maximum permissible harmonics in output signal 1.Secondary Harmonics 2.Higher Harmonics	 10% 5%

4.2 DESIGN DETAILS

1. Input Power and Current Calculation

Maximum Output Power : $P0_{max} = \frac{V0^2_{MAX}}{RL} = 82.1633W$ at linear load nature……(4.1)

Maximum input Power : $Pin_{max} = \frac{P0_{max}}{\eta} = 91.2926W$……(4.2)

Voltage across switch : $Vsw = Vin_{Max} = 36V$……(4.3)

Peak Switch Current : $Ip = \frac{Vin_{max}}{RL} = 12A$……(4.4)

Average switch current : $IA_{sw} = \frac{Ip}{2} = 6A$……..……...…(4.5)

Average input current : $Is = \frac{Pin_{max}}{Vin_{max}} = 2.5359A$……..…..…(4.6)

Let Assume maximum output current is peak current for input OCP

$Is_{rms} = 6.5A$……...……(4.7)

2. Output Filter Design

Output filter consist of inductor and capacitor.

a. Output Inductor

The primary role of the output filter inductor (Lo) is to filter out the switching frequency harmonics. The design of an inductor, amongst other factors, depends on the calculation of the current ripple and choosing a material for the core that can tolerate the calculated current ripple.

When designing filters, the value of inductance is usually designed first. The selection of inductance is related to the ripple current and the power consumption of the system. In general, the ripple current on the inductor is selected to be 15% - 25 % of the rated current.

For this design, the rating is 75 W, the switching frequency is 20 kHz, and the bus voltage is 32 V.Assume that the ripple is 20% and is tolerable by the inductor core,and the minimum inductance required is calculated as:

$Peak\ to\ Peak\ Ripple\ Current\ is:\ \Delta IL = \frac{20}{100} * I0rms_{max} = 1.3A$……..……(4.8)

Hence Output Inductor Value is

$L = \frac{Vin_{max}}{4*Fsw*\Delta IL} = 3.4615 * 10^{-4}\ H$……..…….(4.9)

b. Output Capacitor Filter

Assume $L0 = 0.5 * 10^{-3}$……(4.10)

Cutoff Frequency : $Fc = \frac{Fsw}{10} = 2000Hz$……(4.11)

$C0 = \frac{1}{4*\pi^2*L0*Fc^2} = 1.2665 * 10^{-5}F$……..…..(4.12)

c. Output Inductor Design

Let $K = 0.3$ $Kw = 0.5$ $Bm = 0.33$ $J = 4$

Using Area Product Method

$Ap_{L0} = Lo * I0rms_{max} * I0rms_{max} * \frac{\left(1+\frac{K}{2}\right)}{Kw*Bm*J*10^{-6}} = 36808.7121$……(4.13)

Requirement of Core selection

An appropriate core will be selected which must have area product greater than the calculated Ap. Area product (Ap) is given as the product of the core cross section (Ac) and the window area (Aw). These data is avalable in ferrite magnetic core design catalog.

Selected Ferrite Toroid Core: ZW-422120,Material:R, AL: 12080mH/1000T

$Ac = 51.1\ mm^2$ $Aw = 147.9\ mm^2$ $AL = 12080.10 * 10^{-9}H$

$Ap = Ac * Aw$ $Ap = 7557.69\ mm^4$

Cross sectional area of wiregauge selected $Aw_{28AWG} = 0.111\ mm^2$……..……(4.14)

Number of Turns : $N = \sqrt{\frac{L0}{AL}} = 6.4336$ N=10……(4.15)

Possible number of turns possible in the core

Outer Diameter of selected wire gauge $dw_{CM} = 0.366\ mm$ For 28 AWG Wire Gauge

$Toroid_{inner_{dia_{CM}}} = 13.7\ mm$……..(4.16)

$Possible_{turns_{for_{core}}} = \pi * \frac{Toroid_{inner_{dia_{CM}}}}{dw_{CM}} = 117.5951$……(4.17)

Required cross sectional Area of wire $Awp = \frac{I0rms_{max}}{J} = 1.625 \quad Awp = 1.625$……..…(4.18)

Number of parallel strand required $nparp = \frac{Awp}{Aw_{28AWG}} = 14.6396$: 6*28AWG……..(4.19)

3. Power Loss Calculations

Copper Loss calculations

AC resistance of wire gauge selected $Rac_{28AWG} = 0.222\ Ohm$……..……..…(4.20)

Length of wire required : $L = \frac{(22.1-13.7)+2.12*7}{1000} = 0.0338\ meter$……..……(4.21)

$L_N = N * L + 0.02 = 0.358\ meter$……..…(4.22)

Copper loss

$P_N = \left(L_N * Rac_{28AWG} * I0rms_{\max}^{\ 2}\right) * \frac{1}{6} = 0.5596\ watt$……..…(4.23)

Core Loss Calculations

$a = 0.30 \quad c = 1.26 \quad d = 2.60 \quad Ve = 2.77\ cm^3$

$Bm = 0.33$

$B = \left(\frac{Bm}{2}\right) * 10 \qquad B = 1.65 \qquad f = \frac{Fsw}{1000} = 20$

$Pcore = a * f^c * B^d * \frac{Ve}{1000} \qquad Pcore = 0.1332W$……..……(4.24)

Where: 1. Ve is core Volume
2. B is core calcated flux density
3. Pcore is the power loss in the selected core

Total Loss

$P_{L0} = 2 * (Pcore + P_N) = 1.3856\ watt$ (For 2 Inductor)……(4.25)

4. MOSFET Selection and Snubber Design

FQA70N15 , 0.028 Ohm, 70A@ 25 Deg. Vds:150V (Industrial)

$R_{DS} = 0.028$ ohm $\quad R_{Gate} = 3.3$ ohm

$Q_{GATE} = 25 * 10^{-9}C \quad V_{TH} = 6V$

$V_{GATE} = 12V \qquad V_{OFF} = 2.5 * Vin_{max} = 90V$

$Coss = 1100 * 10^{-12}$ F

$Tr = Q_{GATE} * \frac{R_{GATE}}{V_{GATE}-V_{TH}} = 1.375 * 10^{-8}$sec……..……(4.26)

$$Tf = Q_{GATE} * \frac{R_{GATE}}{V_{TH}} = 1.375 * 10^{-8} \text{ sec} \quad (4.27)$$

$$P_{CONDUCTION} = 1.25 * R_{DS} * IS_{rms}^2 = 1.4788 \text{ Watt} \quad (4.28)$$

$$P_{GATE} = Q_{GATE} * V_{GATE} * Fsw = 0.006 \text{ Watt} \quad (4.29)$$

$$P_{Coss} = Coss * V_{OFF}^2 * \frac{Fsw}{2} = 0.0891 \text{ Watt} \quad (4.30)$$

$$P_{Switching_{ON}} = Vin_{min} * Is_{rms} * (Tr) * \frac{(Fsw)}{3} = 0.0143 \text{ Watt} \quad (4.31)$$

$$P_{Switching_{OFF}} = V_{OFF} * IS_{rms} * (Tf) * \frac{Fsw}{3} = 0.0536 \text{ Watt} \quad (4.32)$$

MOSFET Gate Charge loss takes place in Gate Resistor and this loss is not added in the MOSFET power losses.

RC snubber is connected across MOSFET to reduce switching loss.

Let $Csnubber = 1 * 10^{-9}$F

$$P_{Switching_{OFF_{WITH_{SNUBBER}}}} = \left(\frac{Coss}{Coss+Csnubber}\right) * P_{Switching_{OFF}} = 0.0281\ Watt \quad (4.33)$$

$$P_{MOSFET_{LOSS_1}} = P_{conduction} + P_{Coss} + P_{Switching_{ON}} + P\_Switching\_OFF\_with\_Snubber \quad (4.34)$$

$$P_{MOSFET_{LOSS_1}} = 2 * P_{MOSFET_{LOSS_1}} = 3.2205\ Watt\ for\ 2\ MOSFET \quad (4.35)$$

5. Efficiency Calculations

$$P_{loss_1} = P_{MOSFET_{LOSS_1}} + P_{L0} + P_{EMI} = 5.3273\ Watt \quad (4.36)$$

$$P_{loss} = 0.2 * P_{loss_1} + P_{loss_1} = 6.3928\ Watt \quad (4.37)$$

$$P0_{max} = 82.1633\ Watt \quad (4.38)$$

$$Efficiency = \frac{P0_{max}}{(P0_{max}+P_{loss})} * 100 = 92.7811\ Watt \quad (4.39)$$

V. IMPLEMENTATION ALGORITHM AND FLOW CHART

5.1 Implementation Algorithm

1. Set the reference value of voltage (0.5 to 2.5V) corresponding to cold tip temperature to microcontroller through SPI. This range (0.5 to 2.5V) depends on the actual sensor voltage and reference voltage of ADC. If the set point is finalized means, which is internally programmed via the reference voltage.
2. ADC is configured to read the analog temperature sensor voltages.
3. Reading the temperature sensor voltage and feed to ADC channel.
4. Read the values of PID controller gains *Kp*, K_i and K_d.
5. Execute the ISR for discrete algorithm (sampling time).
6. Execute the Discrete PID algorithm and set the maximum and minimum limits.
7. Initialized sine table in which the values of a complete sine wave are stored (we generated a sine table in range of 0-359 degrees whereas, zero of sine wave is set at decimal.
8. Read the Look up table sine values and multiply each sine sample magnitude with the PID output value to get the sine reference voltage for generation of SPWM.
9. Reference value of sine decides the Modulation index value, which in turns decide the Output AC voltage. The Maximum Output voltage is limited by limiting the Modulation index value to the 0.6 in all conditions.

10. Initialize Timer x which starts from 0 and peaks to xxx (it gives a triangular carrier output).
11. The SPWM generation follows the logic of phase corrected PWM (the sine reference is compared with the 8-bit counter register values). Set the maximum value of PWM frequency(15.618kHz) with a clock frequency of 8-MHz and suitable pre-scalar value.
12. When Timer reaches xxx then interrupt overflow is generated.
13. Enabling timer overflow interrupt enable bit.
14. Configure the generated PWM to OCRx register to interface to the external Hardware circuits. SPWM from the controller is fed to the suitable logic compatibility H-bridge Inverter MOSFET drivers through Logic Buffers.
15. Connect the leg of the H-bridge inverter to load terminals through suitable low pass LC filter with a cut- off frequency of $1/10^{th}$ of the PWM frequency.
16. Apply the 24V to 28V DC bus voltage to the H-bridge inverter. The nominal voltage is set 28V.
17. Working of an H-bridge for pure sine wave inverter can be divided into two modes.

✓ In Mode1, the input signal at the gate of S1and S4 is high and at the gate of S2 and S3 is low. This causes conduction from S1and S4 and we achieve a +12V signal (positive peak of the AC output).

✓ In Mode2, the input signal at the gate of S2 and S3 is high and at the gate of S1and S4 is low. This causes conduction from S2 and S3 and we achieve a -12V signal (negative peak of the AC output). And thus, we obtain a 24V peak-peak signal at the output.

18. In H-bridge circuit we have obtained amplitude modulating signal frequency (reference sine signal). Modulating signal frequency does not change at the output, which means the output frequency remains constant. Only the power of the signal increases in terms of current.
19. If the output cooler motor consumes more current (1.5 times higher than the nominal load current) than the maximum load current, then the over current protection circuit should activate to shut down the converter.

5.2 Flow Chart

Fig-6 shows the Flow chart of the Sine PWM Logic Generation and PID Controller for the cooler drive inverter.

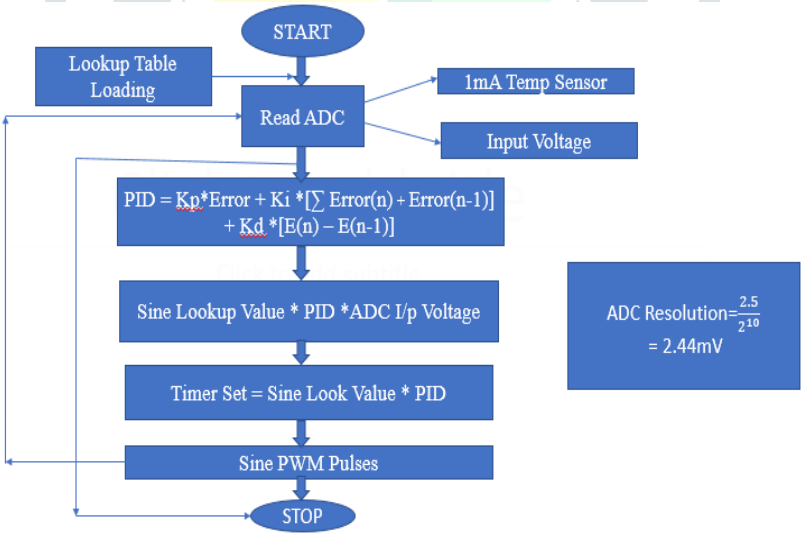

Fig-6 : Flow Chart of Sine PWM Logic Generation and PID Controller

VI. SIMULATION ANALYSIS AND DISCUSSION

6.1 Logic Implementation in Temperature Control

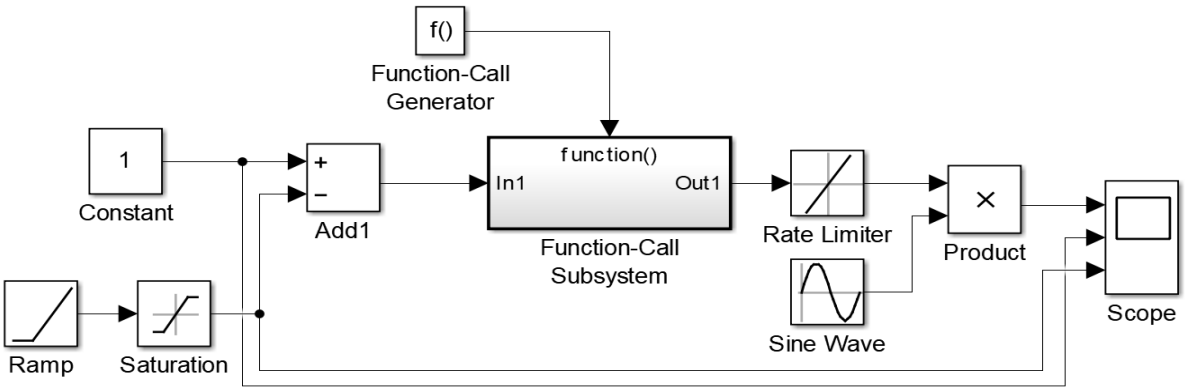

Fig-7 : MATLAB Simulation (Logic implementation in Temp control)

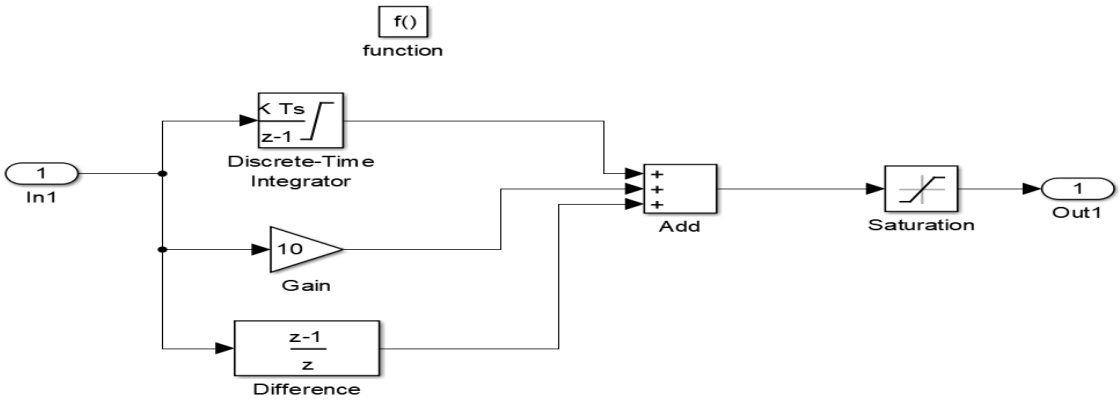

Fig-8 : PID Controller

Fig-9 shows the simulated output waveform of output voltage, Reference and Temperature sensor voltage, Here when the temperature sensor voltage starts increasing the output voltage also starts increasing by means of soft start principle and until the sensor voltage reaches 1V, the output voltage will be 12V. and when the sensor voltage reaches 1V, the output voltage starts decreasing and will maintain 4.5 to 5V and this same logic is implemented in the hardware implementation of digitally controlled cooler drive inverter.

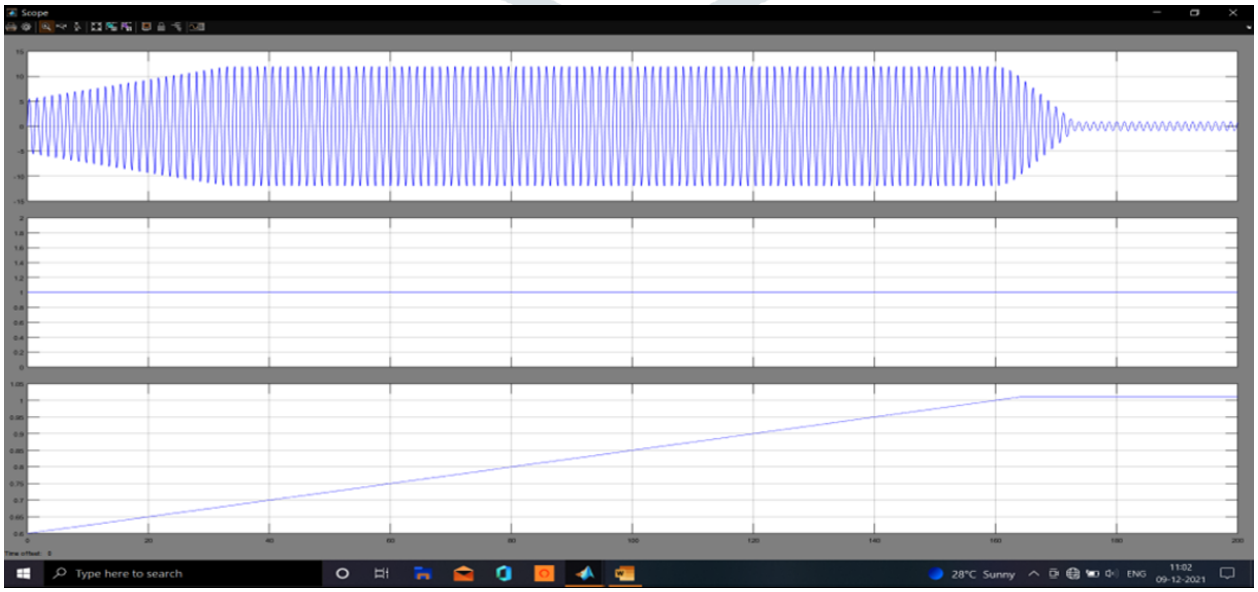

Fig-9 : simulated output waveform (Output voltage, reference and Temp sensor output)

6.2 PWM Control Logic

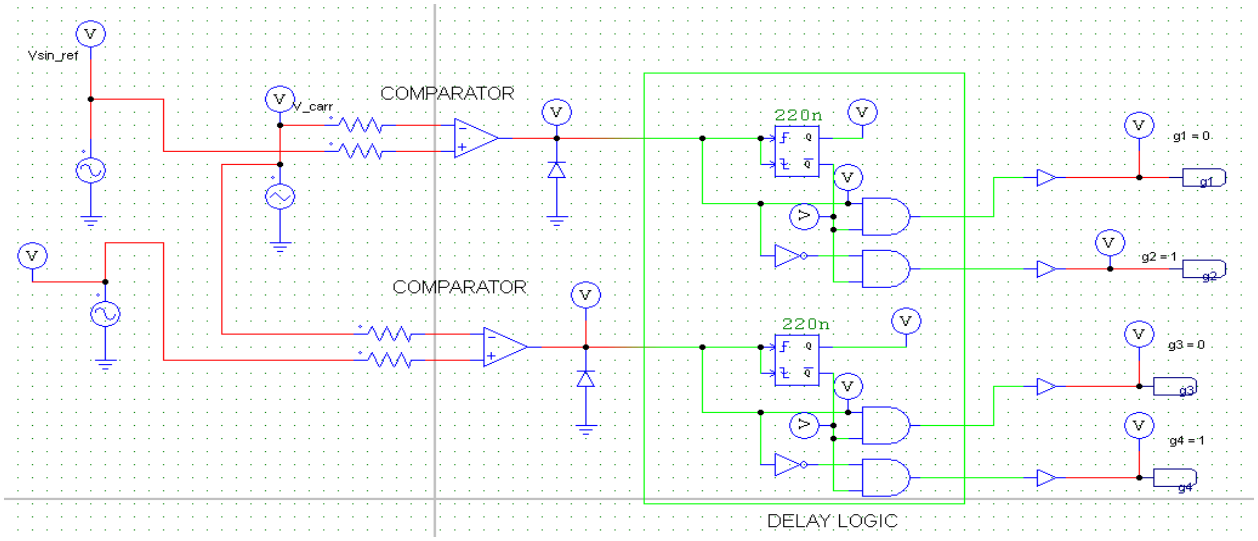

Fig-10 : PWM control logic used in Microcontroller for H-Bridge Inverter

6.3 H-Bridge Inverter Power Circuit

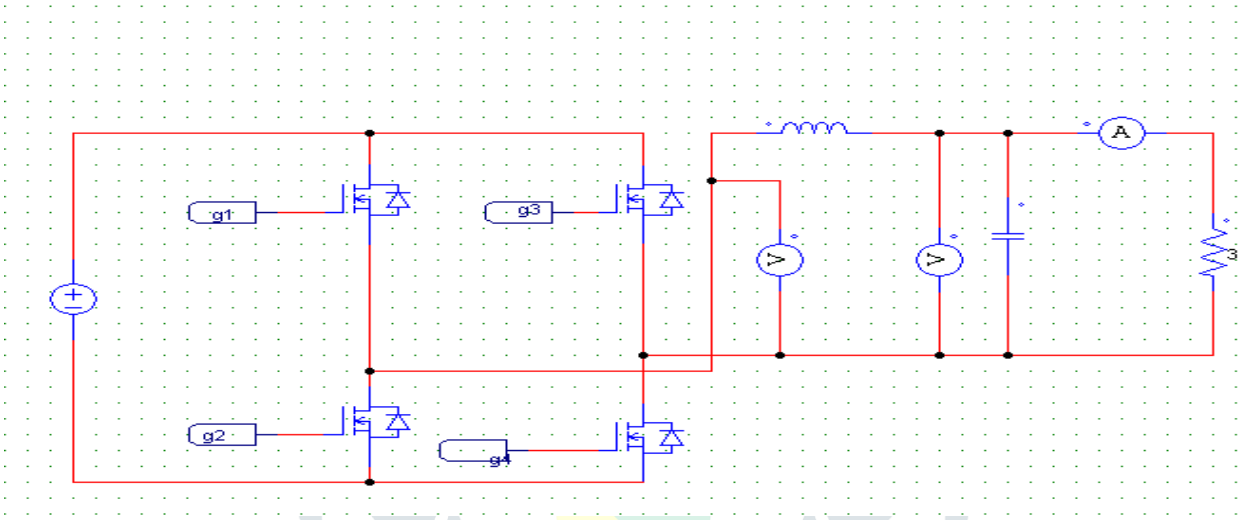

Fig-11 : H-Bridge Inverter Power Circuit

6.4 H-Bridge Inverter Waveforms

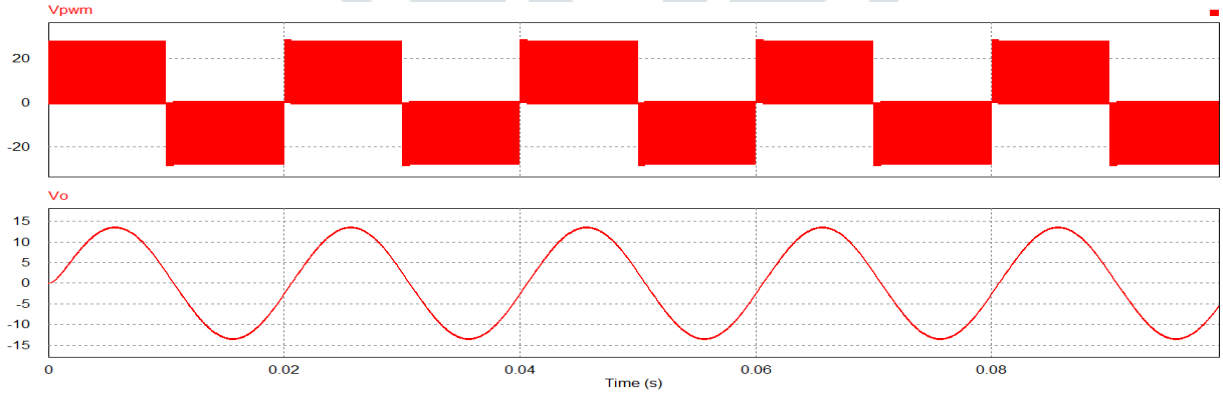

Fig-12 : H bridge inverter output voltage (Before filtering and After filtering)

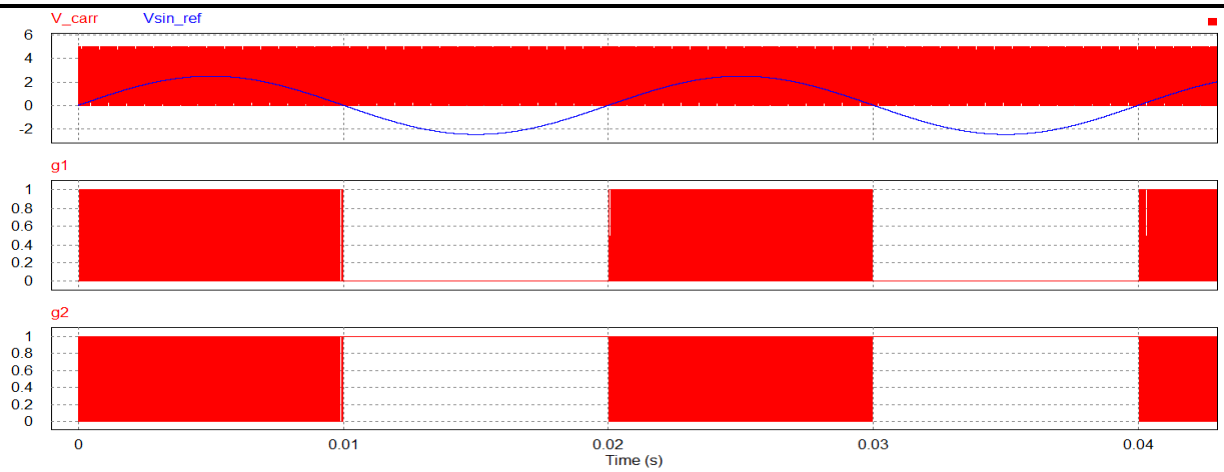

Fig-13 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0 to 0.01 second.

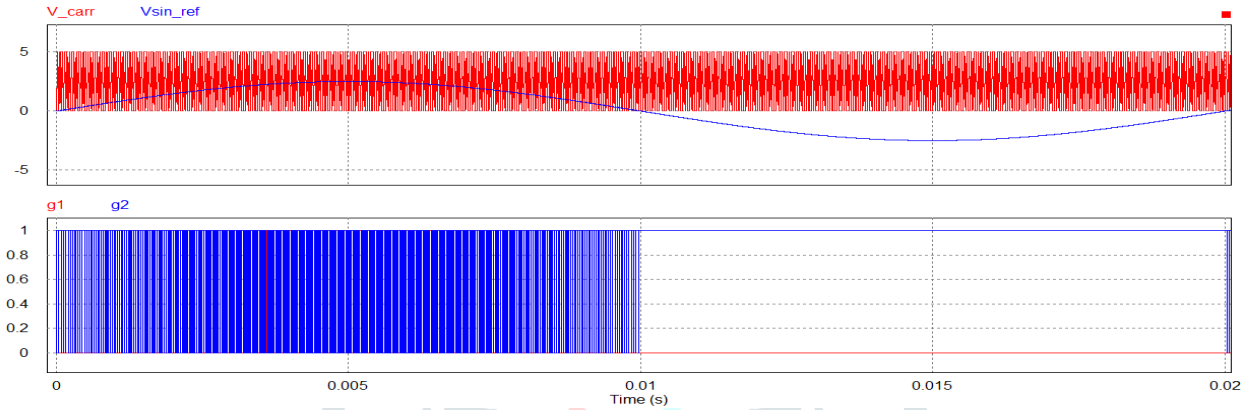

Fig-14 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0 to 0.01 second.

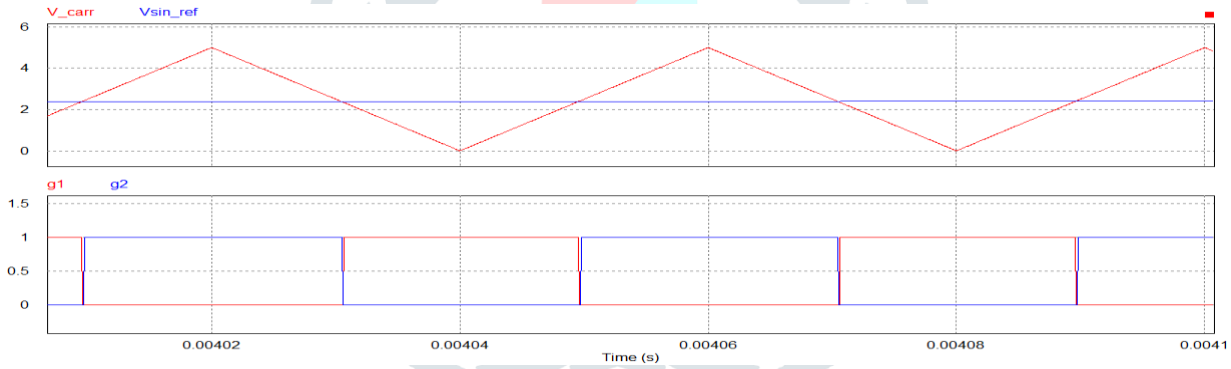

Fig-15 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0 to 0.01 second.

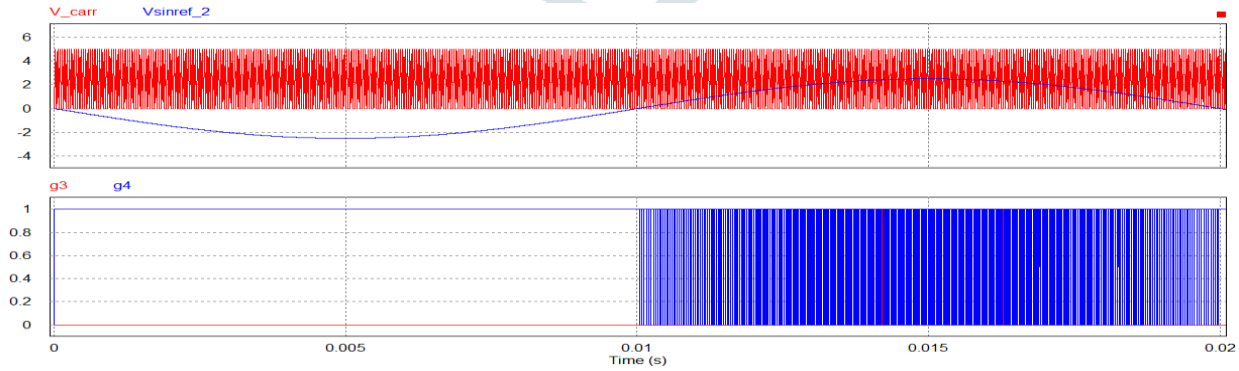

Fig-16 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0.01to 0.02 second.

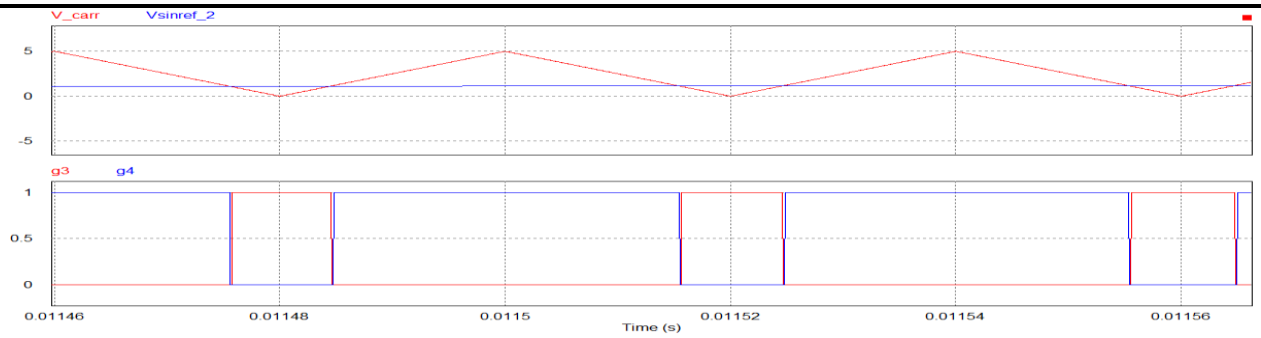

Fig-17 : Generation of PWM signal (switches 1 and 2) During half cycle of time duration 0.01to 0.02 second.

6.5 Protection Circuits

Input side has protection circuits such as Over voltage protection (OVP), Under voltage protection (UVP), Over current protection (OCP).

- **Over Voltage Protection**

The over voltage protection is used to avoid the damage of any device from the maximum voltage or over voltage, if the voltage exceeds more than the specification, the components may get damage, to avoid those damage, over voltage protection circuit is used. The value of the resistor is designed on the bases of maximum differential voltage at the highest expected current. The voltage sensing element will be placed in the device if the voltage reaches above the maximum voltage or 125% of the rated primary voltage then the U1 pin gets high and shutdown pin of PWM IC gets high. Thus turns off the device

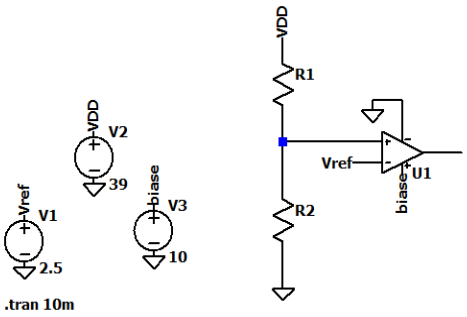

Fig – 18 : circuit of Over Voltage Protection

- **Under voltage Protection**

The under voltage is used to avoid the damage of any device from the voltage rated below the specification, In DC-AC converter the under-voltage range is below 22V, so when the voltage reaches below 22V then, current drawing will be more from the input supply, this causes power losses, then the voltage sensing element gets sensed and the shutdown pin of PWM IC gets high and converter gets turn off. the voltage should be of 125% of the rated primary voltage. By this we can avoid the damage of components in the converter.

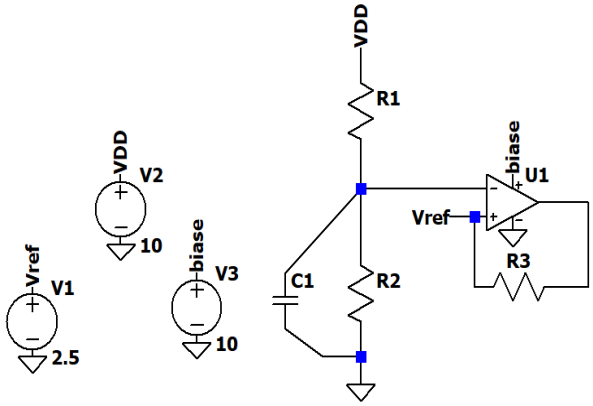

Fig – 19 : circuit of Over Voltage Protection

- **Over current Protection**

The over current protection is used to avoid the converter from the damage. If the current reaches above the specification, then the components in converter may get damage. So the value of the voltage divider resistor is designed according to the input voltage supply, here the input voltage range is from 24 - 42.5V, The current limiting resistor is designed according to the input and output current, when the current exceeds 125% of designed value, The shutdown pin of PWM IC gets high and converter gets turn off.

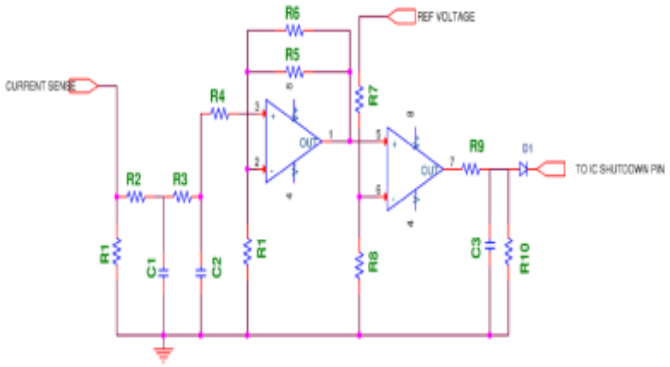

Fig – 20 : circuit of Over current Protection

VII. HARDWARE IMPLEMENTATION RESULTS AND DISCUSSION

7.1 Hardware Results of output voltage

Table-2 Shows the hardware implemented results of output voltages of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-2 : OUTPUT VOLTAGES (VRMS)

VIN (V)	OUTPUT VOLTAGES (VRMS)		
	(12-15.7 VRMS) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	10.56	10.54	10.66
28	10.74	10.83	10.90
32	10.94	10.77	10.97
36	11.43	11.48	11.59

7.2 Hardware Results of load regulation

Table-3 Shows the hardware implemented results of load regulation of cooler drive inverter at 2.5ohm and 3.5ohm resistive load.

Table-3 : LOAD REGULATION

VIN (V)	LOAD REGULATION % for 2.5 Ohm resistor	LOAD REGULATION % for 3.5 Ohm resistor
24	0.61	-1.37
28	0.23	-1.47
32	0.35	-3.13
36	-0.96	-3.49

7.3 Hardware Results of Line regulation

Table-4 Shows the hardware implemented results of line regulation of cooler drive inverter for 28VDC input voltage.

Table-4 : LINE REGULATION

VIN (V)	LINE REGULATION % for 28VDC input voltage
24	4.02
32	-1.20
36	-6.34

7.4 Hardware Results of Frequency

Table-5 Shows the hardware implemented results of Frequency of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-5 : Frequency

VIN (V)	Frequency(Hz)		
	12VRMS (49.5 - 50.5) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	12VRMS (49.5 - 50.5) at 3.5 Ohm load
24	51.79	51.73	51.72
28	51.82	51.75	51.69
32	51.66	51.69	51.75
36	51.88	51.74	51.83

7.5 Hardware Results of DC offset

Table-6 Shows the hardware implemented results of DC offset(V) of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-6 : DC offset

VIN (V)	DC offset (V)		
	12VRMS at 3.0 Ohm load(< 0.2V)	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	0.095	0.100	0.100
28	0.100	0.100	0.100
32	0.100	0.100	0.100
36	0.100	0.100	0.100

7.6 Hardware Results of THD

Table-7 Shows the hardware implemented results of Total Harmonic Distortion(THD) of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-7 : Total Harmonic Distortion(THD)

VIN(V)	Total Harmonic Distortion(THD) %					
	12VRMS at 3.0 Ohm load		12VRMS at 2.5 Ohm load		12VRMS at 3.5 Ohm load	
	Secondary harmonics	Higher Harmonics	Secondary harmonics	Higher Harmonics	Secondary harmonics	Higher Harmonics
	<10%	<5%	<10%	<5%	<10%	<5%
28	0.425	3.250	0.32	3.510	0.19	3.450

7.7 Hardware Results of Efficiency at 3 ohm Load Condition

Table-8 Shows the hardware implemented results of efficiency of cooler drive inverter at 3ohm resistive load.

Table-8 : Efficiency@3 ohm Load condition

At 3 ohm Load condition						
VIN (V)	Input current (A)	Input power (W)	Output Voltage (Vrms)	Output current (Irms)	Output power (W)	Efficiency (%) > 90% 60W @Rload 3 ohm
24	1.674	40.18	10.91	3.40	37.05	92.22
28	1.570	43.96	11.36	3.72	42.27	96.15
32	1.419	45.41	11.50	3.75	43.08	94.86
36	1.419	51.10	12.08	3.94	47.56	93.07

7.8 Hardware Results of Efficiency at 60W Load Condition

Table-9 Shows the hardware implemented results of efficiency of cooler drive inverter at 60W load condition

Table-9 : Efficiency@60W Load condition

At 60W Load Condition						
VIN (V)	Input current (A)	Input power (W)	Output Voltage Vrms	Output current Irms	Output power (W)	Efficiency (%) > 90% 60W load condition
24	2.72	65.28	10.54	5.83	61.46	94.14
28	2.30	64.40	11.03	5.51	60.70	94.26
32	2.00	64.00	11.28	5.37	60.53	94.57
36	1.81	65.16	12.46	5.02	62.57	96.03

7.9 Hardware Results of Ripple Voltage

Table-10 Shows the hardware implemented results of ripple voltage of cooler drive inverter at 2.5ohm, 3ohm and 3.5ohm resistive load.

Table-10 : Vripple

VIN (V)	Vripple		
	(12-15.7 VRMS) at 3.0 Ohm load	(12-15.7 VRMS) at 2.5 Ohm load	(12-15.7 VRMS) at 3.5 Ohm load
24	1.30	1.30	1.20
28	1.30	1.20	1.20
32	1.80	1.30	1.50
36	1.70	1.50	1.60

7.10 Effect of Feedforward loop@Cold Tip Conditions

Table-11 Shows the hardware implemented results of the Effect of Feedforward loop at cold tip conditions.

Table-11 : Effect of Feedforward loop@Cold Tip Conditions

At cold tip conditions								
S.No	Vin V	Iin A	Temp voltage V	Vo rms	Io A	Pin W	Po W	Efficiency %
1	24	0.2792	1.5	4.29	1.443	6.7008	6.196819	92.48
2	25	0.2519	1.5	4.16	1.397	6.2975	5.806491	92.20
3	26	0.2225	1.5	3.98	1.331	5.785	5.297912	91.58
4	27	0.2266	1.5	4.09	1.376	6.1182	5.634445	92.09
5	28	0.2058	1.5	3.96	1.336	5.7624	5.293766	91.87
6	29	0.1752	1.5	3.71	1.246	5.0808	4.618673	90.90
7	30	0.1418	1.5	3.38	1.14	4.254	3.854568	90.61
8	31	0.1146	1.5	3.07	1.041	3.5526	3.19587	89.96
9	32	0.1069	1.5	3.01	1.017	3.4208	3.059543	89.44
10	33	0.068	1.5	2.41	0.818	2.244	1.973016	87.92
11	34	0.0473	1.5	2.11	0.684	1.6082	1.441872	89.66
12	35	0.0346	1.5	1.76	0.586	1.211	1.0285	84.93
13	36	0.0335	1.5	1.75	0.589	1.206	1.028865	85.31

7.11Measured Experimental Results of Thermal Sensor

Table-12 Shows the Measured Experimental Results of Thermal Sensor of 1mA and 25uA constant current source.

Table-12 : Measured Experimental Results of Thermal Sensor

Temperature ° C	1mA current source		25uA current source	
	ICE (mA)	DTA2-DTK2 (V)	ICE (uA)	DTA1-DTK1 (V)
-50	0.993	0.6631	25.76	0.5431
-40	0.995	0.6651	25.77	0.5481
-30	0.997	0.6631	25.77	0.5441
-20	0.996	0.6629	25.78	0.5445
-10	0.998	0.6629	25.77	0.5431
0	0.995	0.6631	25.76	0.5431
10	0.994	0.6629	25.77	0.5481
20	0.995	0.6631	25.77	0.5441
30	0.996	0.6629	25.78	0.5445
40	0.994	0.6631	25.77	0.5431
50	0.995	0.6651	25.78	0.5445
60	0.995	0.6631	25.76	0.5431

7.12Hardware CRO waveforms of cooler drive inverter

Fig-21 and Fig-22 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for motor load.
Test method: Measured by dipping Temperature sensor in Liquid Nitrogen Cylinder.

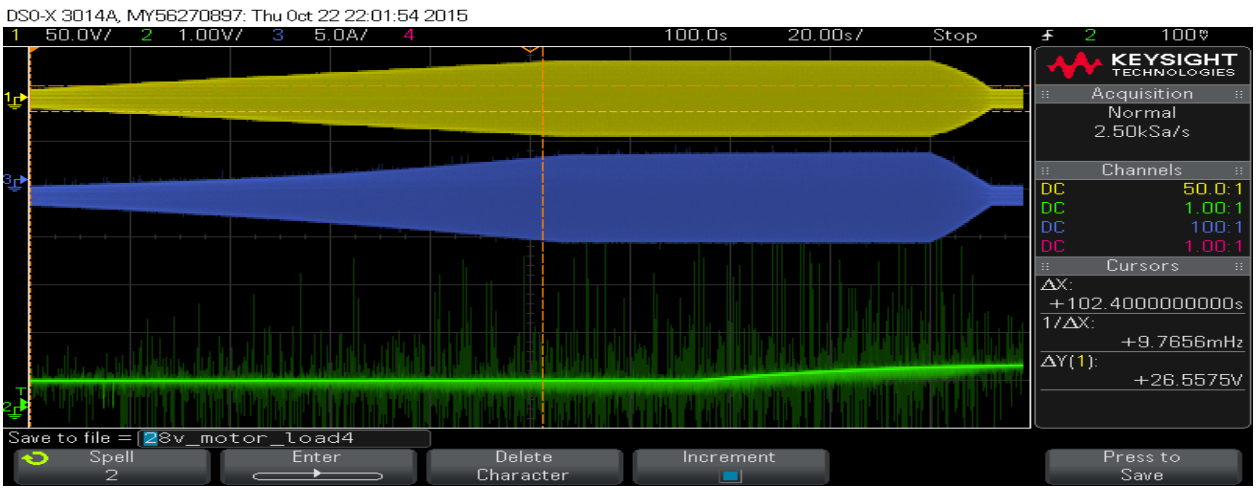

Fig-21 : Output voltage : Yellow, output current : Blue and Temperature sensor : Green at 28VDC for Motor load

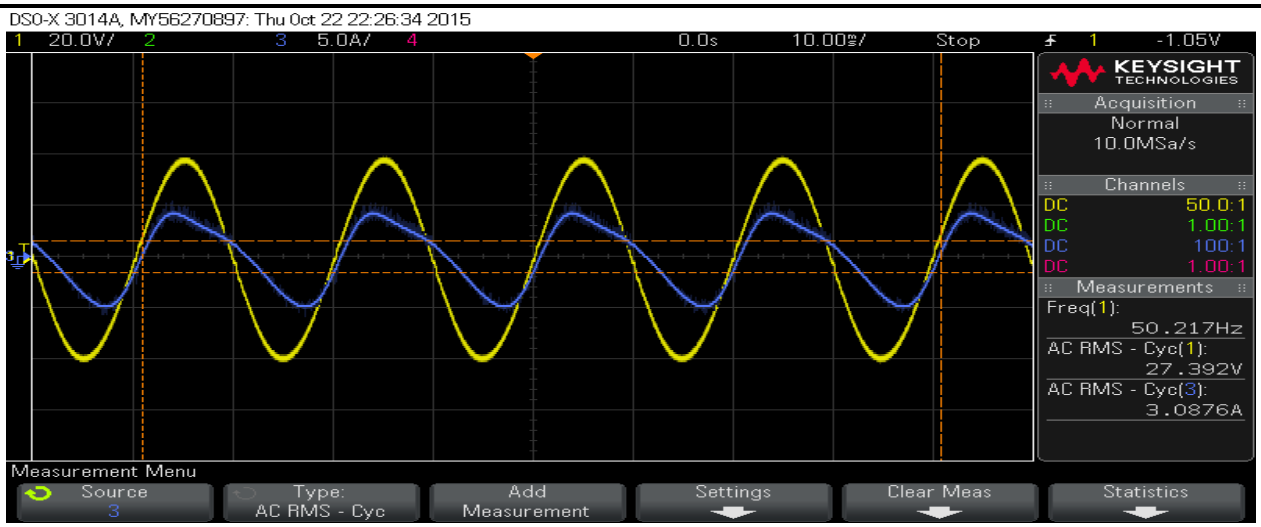

Fig-22 : Output voltage : Yellow and output current : Blue for Motor load

Fig-23 Shows the Hardware CRO waveforms of output voltage, output current and Temperature sensor voltage at 28VDC for 3-ohm Resistive load condition, here The temperature sensor voltage channel was set at high resolution mode to observe the waveform clearly.

Test method: Measured by dipping Temperature sensor in Liquid Nitrogen Cylinder.

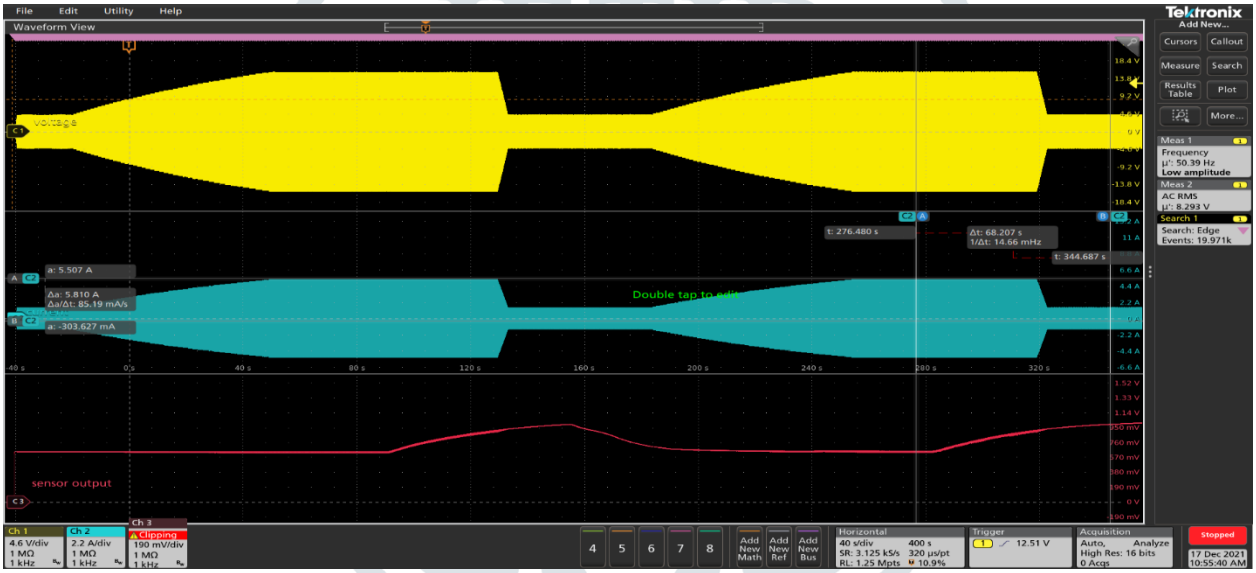

Fig-23 : Output voltage : Yellow, output current : Blue and Temperature sensor : Red at 28VDC for 3-ohm resistive load condition

7.13 Hardware PCB and Experimental Setup of Cooler Drive Inverter

Fig-24 shows the hardware Printed Circuit Board(PCB) of the cooler drive inverter, here the main components are Main card(inverter card), EMI card and output card.

1.Main Card(Inverter Card)

2.Output Card

3.EMI Card

4.Relays(Main, Redundant and Launch lock Relays)

5.ATmegaS128 Microcontroller

6.Bulk Capactitor

7.MOSFET Driver ICs

8.EMI Filters

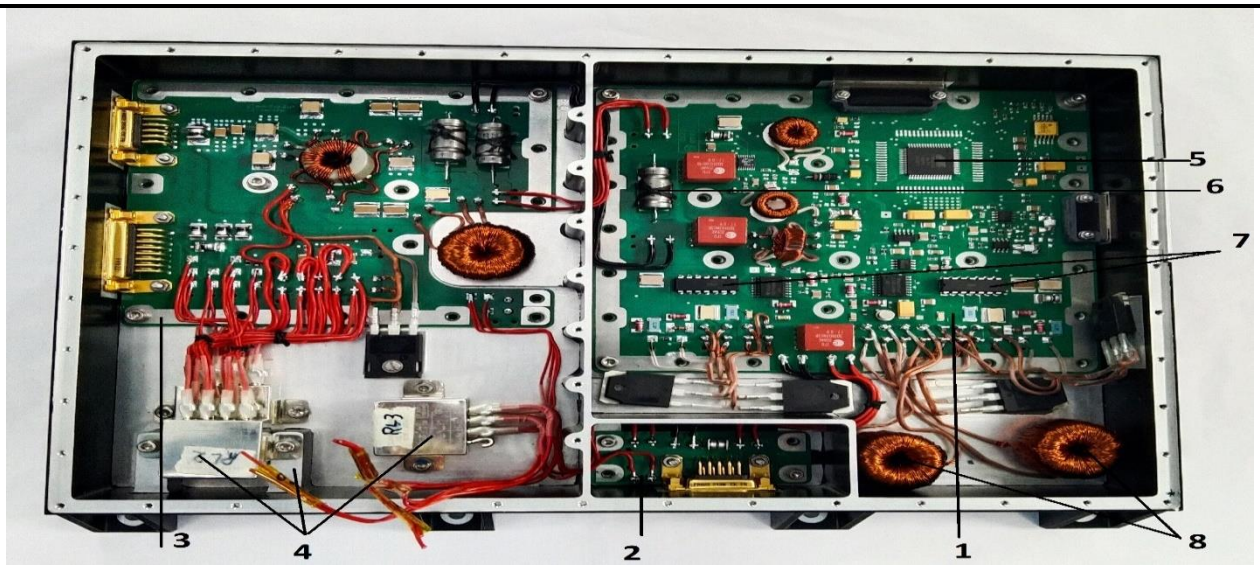

Fig-24 : Hardware PCB

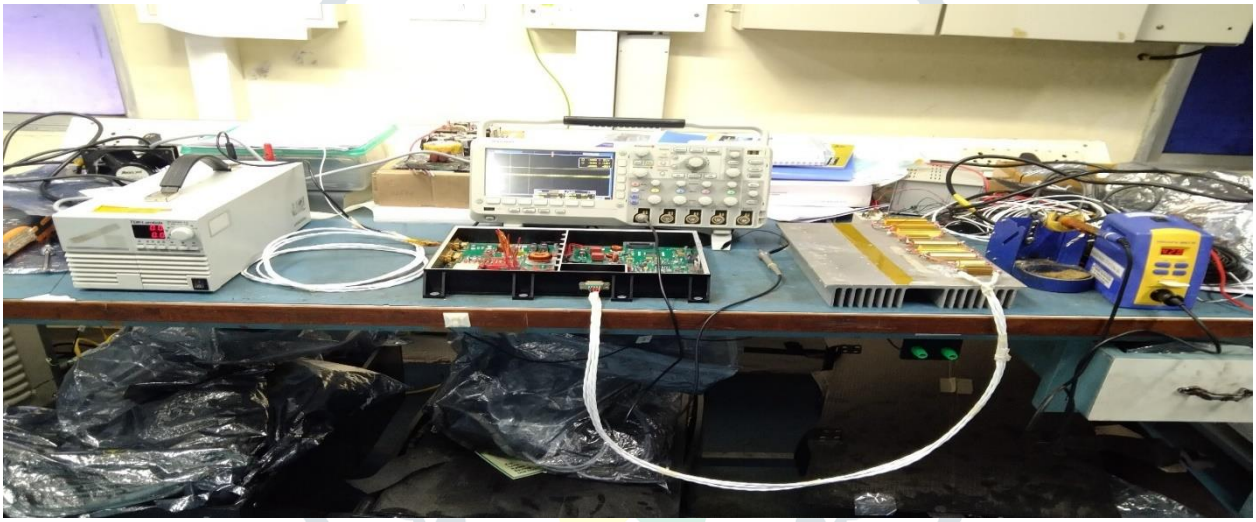

Fig-25 : Hardware Experimental Setup

VIII. CONCLUSION

Digitally controlled cooler drive inverter with feed-forward control for space application has been designed. The selected topology was H-Bridge inverter. The Main components include ATmegaS128 Micro controller, PID Controller, Protection Circuits, MOSFET Switches, Analog to Digital Converter, Driver Circuit, 2N2222A Transistor and Relays. The Hardware Implementation results shows that the output voltage obtained was 12V and the output current obtained was 6.5A. The obtained efficiency was more than 90% and obtained output ripple, Frequency, DC offset, Total Harmonic Distortion, Load and Line regulation was within the specified limits.

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USN: 1RV20EPE14

Under the Guidance
of

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Submitted in partial fulfillment of the requirements for the award of degree of

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2021-22

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DECLARATION

I, **Shreelakshmi N**, student of fourth semester M.Tech in **Power Electronics, Department of Electrical and Electronics Engineering,** RV College of Engineering®, Bengaluru declare that the project titled **"Design and Implementation of Fuzzy Logic Controller for Speed Control of BLDC Motor"**, has been carried out by me. It has been submitted in partial fulfilment of the course requirements for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

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Her Project Title is "Design and Implementation of Fuzzy Logic Controller for Speed Control of BLDC Motor" and has completed the project under the guidance of Kappala Venkateswarlu, R&D.

During the tenure of the internship at Ampere, her conduct, character, and interest to learn were found good.

We wish her all the best in her future endeavors.

Thanks & regards,

Vithal Acharya
Head – Human Resources
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ABSTRACT

According to a recent survey globally, the number of Electric Vehicles (EVs) sold are increasing gradually indicating the likeliness among people to buy and use EVs daily. The selection of right electric motor and its controller is very important. The various advantages of Brush Less DC (BLDC) motors including noiseless operation, a longer lifespan, improved speed torque characteristics, and a higher speed range make it more feasible in automotive industries. In classical control techniques, obtaining the solution of mathematical models is tedious and valid for linear systems only. Modern control techniques including Artificial Intelligence (AI) and Fuzzy Logic (FL) are gaining importance and lot of research is being conducted. A rule- based FL controller seems to be a better approach for the control of BLDC motors as it increases the performance of the drive system by using linguistic variables.

The project deals with controlling the speed of the motor using the Fuzzy Logic Controller (FLC). The speed of the BLDC motor is initialized and by using hall effect sensors, the actual speed of the BLDC motor is sensed. If the actual speed and the set speed of the motor are same, then PWM pulses are generated directly and is fed to the 3-phase inverter for speed control. If the actual speed and the set speed are not same, then the error and change in error are estimated and fed as input to the FLC. FLC processes these inputs with the rule base table and generates the input to regulate the duty cycle of the PWM pulses, fed to the 3-phase inverter for speed control. The designed controller, that is based on the Mamdani Inference System with triangular membership functions and 49 rules, a switching frequency of 1 KHz, and reference speed of 1500 rpm, is simulated using MATLAB/Simulink. The results are compared with the PI, PID Controller, and a hardware prototype is implemented using an Arduino Uno Controller, IR sensor and the Electronic Speed Controller (ESC) by taking small drone BLDC motor.

From the results of the simulation, it is observed that the BLDC motor reaches its reference speed with a settling time, rising time, and overshoot of 2.801ms, 3.309ms, and 2.577 percent, respectively, using FLC and 4.228, 3.010, and 5.851 percent, respectively, in PI controller. So, in terms of overshoot and settling time, the fuzzy logic controller performs better than the PI Controller, however, it appears that the PI Controller performs better in terms of rising time.

LIST OF PUBLICATIONS

Publication Type	Publication Details
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GLOSSARY

AC	Alternating Current
AI	Artificial Intelligence
ANN	Artificial Neural Network
AQI	Air Quality Index
BLDC	Brush Less Direct Current
BMS	Battery Management System
DC	Direct Current
EV	Electric Vehicle
FIS	Fuzzy Inference System
FLC	Fuzzy Logic Controller
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
VR	Variable Reluctance

Chapter 1

INTRODUCTION

Energy, environment, and health have been the three major problems in recent years. While the use of fossil fuels is escalating quickly, their supplies are rapidly running out. This has a negative influence on the ecology as well as the depletion of natural fuels.[1]-[3]

According to a World Health Organization (WHO) assessment, 91% of people worldwide reside in areas with pollution levels that are much higher than the defined threshold. Since the Air Quality Index (AQI) numbers are steadily increasing at densely populated areas one may categorise the impact of air pollution on personal health. As a result, incorporating new technologies to cut down on emissions has emerged as a key automotive technology trend.[4]-[9] The first step towards green transportation is hybrid vehicles. However, these vehicles do not totally reduce CO_2 emissions. As an alternative, pure Electric Vehicle (EV) technology has shown to be the possible solution in reducing overall emission and low energy usage without damaging the health of both the environment and human life. As a result, EV technology is emerging as one of the most attractive choices for energy saving and pollution reduction.[2]-[14]

The core components of the EV's power train are the motor that is used to propel the vehicle, motor controller, battery, Battery Management System (BMS) and the power electronics converters. The selection of right electric motor for the EV application is very essential. There are various types of motors used in EV applications like DC motor, Induction motor, Switched Reluctance Motor, Brush Less Direct Current (BLDC) motor etc.[14]-[17] The BLDCM have various advantages like noiseless operation, longer life, better speed torque characteristics, higher speed range and hence used in many applications like automobile industries, home appliances, Aircraft, computers, robots and many more.[3][4]

Over the past few decades, control applications have been using traditional controllers like P, PI, and PID. The limitations of conventional controllers, such PI and PID, include their incapacity to operate in non-linear circumstances that arise in daily life. [23]-[28]

The suggested study focuses on using an advanced control technology, like Fuzzy Logic Controller (FLC), to regulate the speed of a BLDC motor in order to overcome the conventional controller limitations to increase the performance, inability to operate in the non-linear circumstances .[29]-[33]

1.1 Overview

A motor controller is primarily an electronic module that links between the battery pack and the motor to manage the speed and acceleration of an electric vehicle depending on throttle input.

The inverter circuit power the BLDC motor and the speed of the motor is controlled by controlling the supply voltage given to the motor. At the beginning the motor speed is initialised, and the actual speed of the motor is detected using sensors. If the actual and set speeds of the motor are the same, pulse width modulation (PWM) pulses are generated using the PWM generator and supplied to the 3-phase inverter for speed control. If the actual and set speeds differ, the error and change in error are calculated and sent to the FLC as input. FLC processes these inputs using a specified rule base table and generates a controlled output to regulate the motor's speed by suppling the required supply voltage via the inverter circuit. The controlled output is used to generate the PWM pulses of the required duty cycle to control the motor speed. Analysis of this circuit is carried out using the MATLAB Simulink and a hardware prototype is fabricated.

1.2 Specific Details

The FLC controller is designed with two input variables and one output variable. The error (i.e., the difference between the actual and set speed) and change in error (i.e., the difference between the previous and current error) are the two inputs. With triangular membership functions, error input and change in error have 7 membership values, and the degree of membership function is obtained using the triangular rule. The range of error and change in error for the input is -5 to +5, and -1 to +1 for the output. The rule base, that consists of 49 rules, is employed.

To obtain the regulated output, a Mamdani-based Fuzzy Inference System (FIS) is used with the AND operator and the defuzzification is done using the weighted average approach. The BLDC motor with 4Poles pairs, Stator Resistance of 10.91 Ohms, Stator

Inductance of 30.01mH, Inertia of motor is taken as $2x10^{-4}$ kgm^2, back EMF of 120^o.This regulated output controls a supply voltage of 132V. The MATLAB Simulink software is used to simulate this FLC controller for controlling the speed of a BLDC motor.

1.3 Literature Survey

The growth of human civilisation in the twenty-first century is hampered by two key challenges: energy and the environment. In recent years, energy costs have continued to rise, volatility has become more severe, public opinion on environmental protection has risen, applicable rules and regulations are more stringent, and "energy conservation" and "emission reduction" has become an urgent practical concern.[1]-[3]

As a result, using new technologies to cut down on energy use and emissions has become a key area of focus for the automotive industry. The hybrid electric vehicles and electric vehicles are the most appropriate solutions to the problem. Hybrid electric vehicles, without a question, aid in lowering fuel consumption and emissions, but pure electric vehicles prove to be superior and are seen to be the most promising solution. As a result, for the past several years, the automobile industry has identified EVs as its primary focus of study.[4]-[8]

The motor and motor controller are the two most important components of an electric vehicle power train. The selection of the motor is critical and needs to be done with care in order to optimise the vehicle's performance. DC motors, induction motors, BLDC motors, PMSMs (Permanent Magnet Synchronous Motor), and other types of motors are used in present day EVs. Compared to DC motors, the BLDC motor has a better power density, higher torque, lower operating and mechanical noise, no electromagnetic interference, and high efficiency. As a result, this motor is the most often used for EV applications.[9]-[11]

Because of the limited number of parameters to be set, traditional controllers such as P, PI, and PID have been employed for control applications for decades. It is necessary to know the exact mathematical model of the system or the response of the system in order to develop these controllers, however in reality, systems are discovered to be nonlinear and complicated.[12]-[16]

New control techniques such as Artificial Intelligence (AI) and FLC are gaining prominence, and much research is being conducted to address nonlinear events that occur in real time. FLCs provide the following benefits over traditional controllers: they are less expensive to create, cover a broader variety of operating situations, and are more easily adaptable in natural language concepts. Hence a rule based FLC appears to be a better technique for controlling BLDC motors in EV applications.[17]-[20]

Fuzzy logic is a type of logic that uses "degree of truth" to calculate rather than the standard "true or false" (1 or 0) Boolean logic. It is a very successful control system since it offers the optimum solutions for its applications. Fuzzy logic is a subset of Boolean logic that deals with partial truth and provide exact answers from approximate knowledge.[21]-[25]

A FLC is a rule-based controller that has four key components: fuzzification, inference engine, rule base/database, and defuzzification. The Mamdani fuzzy inference system and the Takagi-Sugeno-Kang fuzzy inference system are two types of fuzzy inference systems.[26]-[27]

BLDCM speed control is possible in sensor-based and sensor-less modes. Hall-Effect position sensors, optical position sensors, and electromagnetic variable reluctance (VR) sensors are frequently employed in sensor-based techniques to determine the position of the rotor. The most commonly utilised of them are Hall-Effect sensors. Techniques for sensor-less control, such as the Back-EMF method, magnetic flux linkage method, and inductive approach, implicitly sense the location of the rotor by employing the motor voltages or currents and the back-EMF approach is most frequently preferred. Despite many advantages of sensor less technique it has many disadvantages like it is more complicated, consumes more computational time and requires processors with large amount of memory. Hence the sensor-based techniques are more preferable in the low speed and variable load conditions.[28]-[30]

The vector control, pulse width modulation (PWM) control, hysteresis current control, etc. are some of the several algorithms used to regulate the speed of the BLDC motors. However, from a safety perspective, the drive train controller needs to be robust. Because of its simplicity and robust nature PWM control is the most effective and widely used technology.[30][32]

Typically, the terminal voltage of the BLDCM, that is supplied by a voltage source inverter (VSI), determines the speed of the device. In the PWM method, switching signals from the VSI are multiplied by a high frequency chopper signal with a predetermined duty cycle. Therefore, by adjusting the duty cycle of the inverter's switching pulses, the output voltage may be changed. In this study, the duty cycle of the PWM signals is controlled using an FLC controller.[33]-[35]

This paper illustrates the simulation of FLC using MATLAB. MATLAB Simulink has a feature to simulate the fuzzy logic using Fuzzy Logic Toolbox. FLC must first be designed using the FIS editor before being transferred to the workspace. Then, in the modelling of a BLDC motor drive, the Simulink environment offers a direct connection to the FLC via the MATLAB Workspace.[36]

1.4 Motivation

The motor and its controller are critical components in the design and development of an electric vehicle. The advantages of BLDC motors over AC induction motors, such as their small size, ease of speed control, high specific power, and thermal efficiency, make them more practical for automotive applications. The FLC is chosen over other traditional controllers because of its several advantages, including

- FLC is simple to use and takes less time to design because it does not involve complex mathematical equations.
- FLC has the ability to simulate nonlinear situations in real time.
- Using FLC in combination with traditional controllers enhances efficiency further.

1.5 Problem Statement

To design and implement the Fuzzy Logic based controller for a BLDC motor and compare the simulation results of the FLC with a traditional PI, PID controller, as well as to check the FLC's operation for speed variations throughout the period of a drive cycle.

1.6 Objectives

The main objective of the project is to design and implement a Fuzzy Logic based controller for speed control of BLDC motor through these steps

- To design the fuzzy logic-based controller for the speed control of BLDC motor.
- To simulate and analyse the FLC.
- To analyse the behaviour of FLC for different drive cycle.
- To compare the simulation results obtained using PID controller and fuzzy logic controller.
- Implementation of FLC based controller for speed control of BLDC.

1.7 Organization of Thesis

The project report consists of total seven chapters. An introduction to each phase in developing the work is listed as follows.

Chapter- 1: Consists of a literature survey that was carried out to understand the different types of controllers and their drawbacks and the advantages of FLC. It includes the problem definition, objectives of the project, motivation behind carrying out this project.

Chapter- 2: Consists of the basic concepts of the BLDC motor including construction, operating principle and the controllers used to control the BLDC motor.

Chapter -3: Consists of the block diagram, methodology and flow of the proposed work in detail.

Chapter- 4: Involves the design of the FLC for the speed control of the BLDC motor and the specifications of the motor and the FLC used for the simulation sre described.

Chapter-5: Consists of the simulation analysis of the proposed work , hardware components used for the implementation and the hardware implementation is depicted.

Chapter-6: Discusses about the simulation results obtained, the comparative analysis of the conventional PI and PID controller and the hardware implementation results.

Chapter -7: includes the overall conclusion drawn from the project and the future works that can be carried out.

Followed by References consisting of list of papers referred for understanding and analysing the project work.

Chapter 2

BLDC MOTOR AND CONTROL TECHNIQUES

The chapter provides overall basic concepts required to carry out the project work. Chapter includes the introduction to BLDC motors, construction, operating principle, and some controllers used to control the BLDC motors.

2.1 BLDC Motor

Motors are devices that transform electrical energy into mechanical energy in general. Most electric motors operate through the interaction between the motor's magnetic field and winding currents to generate force in the form of rotation. Electric motors are powered by either direct current (DC) or alternating current (AC) sources.[7]

The BLDC motor is a three-phase synchronous motor with permanent magnets on the rotor rather than a commutator or brushes.[7] As the name implies BLDC motors do not contain brushes or commutators and the role of the brushes is replaced by an electronic control or a drive circuit that rotates the motor.[8]

2.1.1 Construction

A BLDC motor, like any other electric motor, is made up of a stator and a rotor. Permanent magnets are mounted on the rotor of a BLDC motor, and the stator is wound with a specified number of poles.[7]. Figure 2.1 depicts the construction of BLDC. motor.

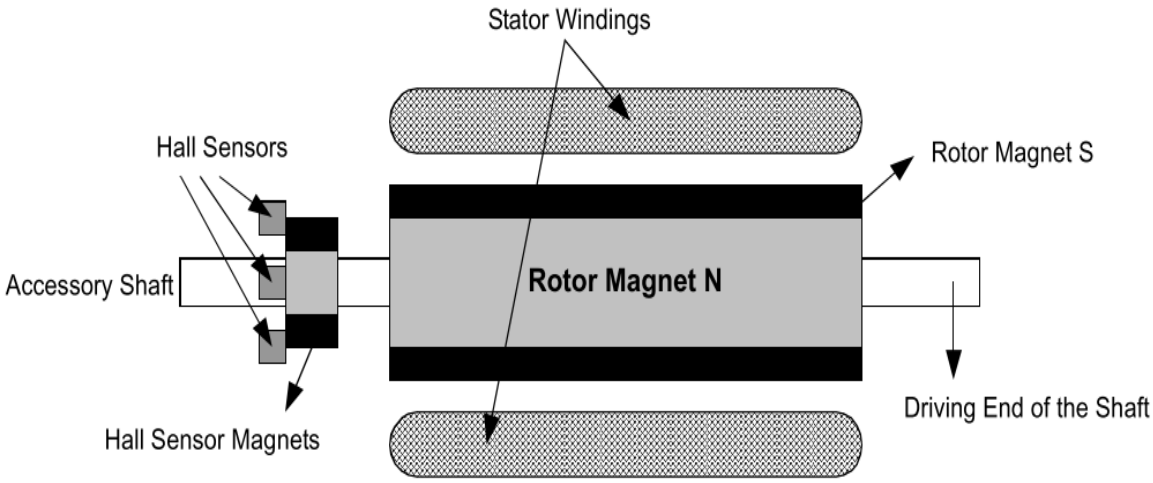

Figure 2.1 Construction of BLDC Motor [9]

2.1.1.1 Stator

A BLDC motor's stator is made of stacked steel laminations with windings positioned in slots axially cut along the inner perimeter. Traditionally, the stator is similar to that of an induction motor; however, the windings are placed differently. Most BLDC motors have three stator windings coupled in a star pattern. Each of these windings is made up of several coils that are joined to make a winding.[7], [9]

2.1.1.2 Rotor

The rotor is comprised of permanent magnets and have two to eight pole pairs with alternate North (N) and South (S) poles. The magnetic material used to manufacture the rotor is selected based on the desired magnetic field density in the rotor. Permanent magnets are usually made with ferrite magnets but rare earth alloys such as Neodymium (Nd), Samarium Cobalt (SmCo), and the alloy of Neodymium, Ferrite, and Boron (NdFeB) are increasing prominence as technology progresses.[10]

2.1.1.3 Hall Sensors

The commutation of a BLDC motor is regulated electronically, as compared to a brushed DC motor. The stator windings must be activated in a certain order to rotate the BLDC motor. It is necessary to understand the rotor position in order to determine that winding is energised after the energising procedure. The location of the rotor is determined via Hall effect sensors integrated in the stator.[10]

2.1.2 Operating Principle

BLDC motor works on the principle similar to that of a conventional DC motor, i.e., the Lorentz force law states that whenever a current carrying conductor placed in a magnetic field it experiences a force.[9] As a consequence of reaction force, the magnet experiences an equal and opposite force. In case BLDC motor, the current carrying conductor is stationary while the permanent magnet moves.[10]

Hall sensors are used by the BLDC motor to determine the location of the rotor. For location data, three sensors H_A, H_B, and H_C are needed. Six potential valid commutation sequences are obtained with three sensors. One of the Hall sensors changes its states every 60 electrical degrees of rotation. An electrical cycle is therefore completed in six phases. The motor's switching pattern for clockwise rotation with the hall sensor signals and the back EMF is shown in Table 2.1.[11]

Table 2.1 Switching Pattern for Motor Rotation [12]

Sequence	H_A	H_B	H_C	Active Switches	EMF A	EMF B	EMF C
1	0	0	1	S4, S5	0	-1	1
2	0	1	0	S2, S3	-1	1	0
3	0	1	1	S2, S5	-1	0	1
4	1	0	0	S1, S6	1	0	-1
5	1	0	1	S1, S4	1	-1	0
6	1	1	0	S3, S6	0	1	-1

Figure 2.2 shows the Back EMF and the hall sensor waveforms for the different operating conditions of the switches and the Hall sensor signals.

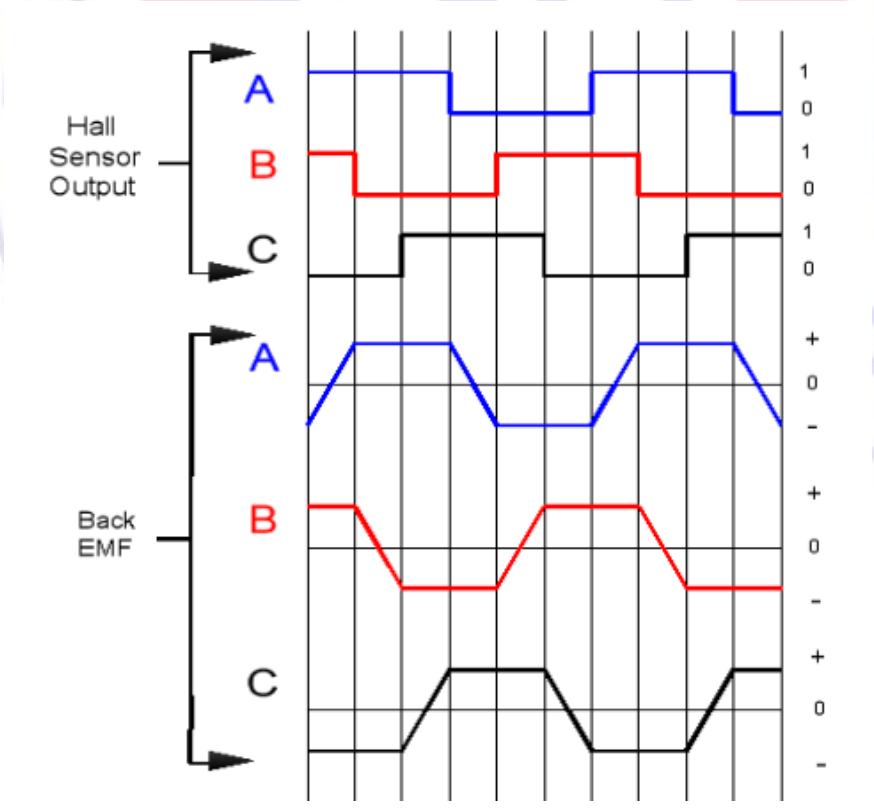

Figure 2.2 Back EMF and Hall Sensor Waveforms [11]

2.2 Control Techniques

There are several brushless motor control methods available today. They are broadly categorised into three groups: Trapezoidal, Sinusoidal, and Field Oriented Control.

2.2.1 Trapezoidal Control

One of the simplest and common methods for controlling Brushless DC motors (BLDC) is Trapezoidal Control and it is also known as Square-wave control. Square-wave control uses Hall sensor or sensor less estimation algorithm to obtain the position of the motor rotor, and then commutates six times in the 360° electrical cycle according to the position of the rotor (commutate per 60°). The current waveform for each winding is therefore a staircase from zero, to positive, to zero, and then to negative current as shown in Figure 2.3.

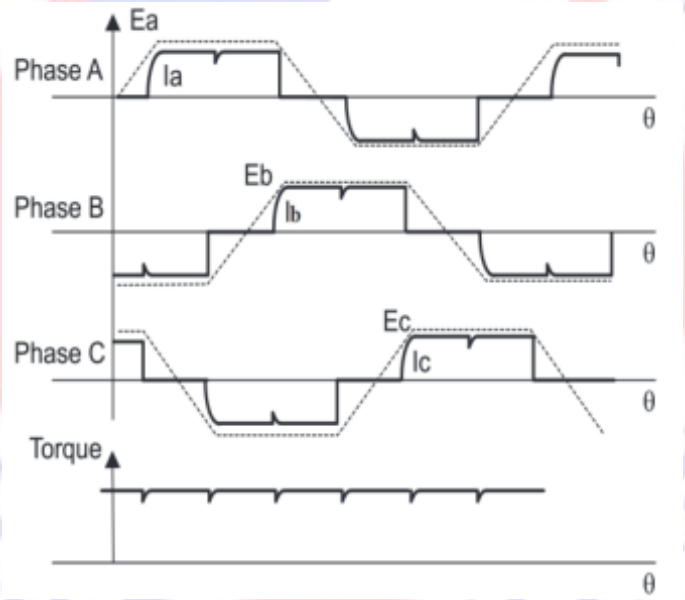

Figure 2.3 The Current Waveforms in the Trapezoidal Control

Advantages of square-wave control include: simple control algorithm, low hardware cost, and higher motor speed is obtained by using ordinary controller. Disadvantage of square-wave control include: large torque ripple, a certain current noise, efficiency is not up to the maximum. Square-wave control is suitable for occasions of motor rotation performance is not very high.[17]

2.2.2 Sinusoidal Control

The principle of Sinusoidal Control is to drive all the three motor windings with three currents that vary smoothly and sinusoidally as the motor rotates. This requires modulation of the three winding currents such that the resulting space vector is always in the quadrature direction with respect to the rotor and has constant magnitude. In order to achieve this, accurate measurement of rotor position is required and is provided by Resolver or Quadrature Pulse Encoders. Since the windings are star connected, the current in one of the windings is the negative sum of the currents in the other two windings. Hence, this scheme requires a current control loop for the first two windings. Figure 2.4 shows the typical block diagram of a sinusoidal control scheme.[14]

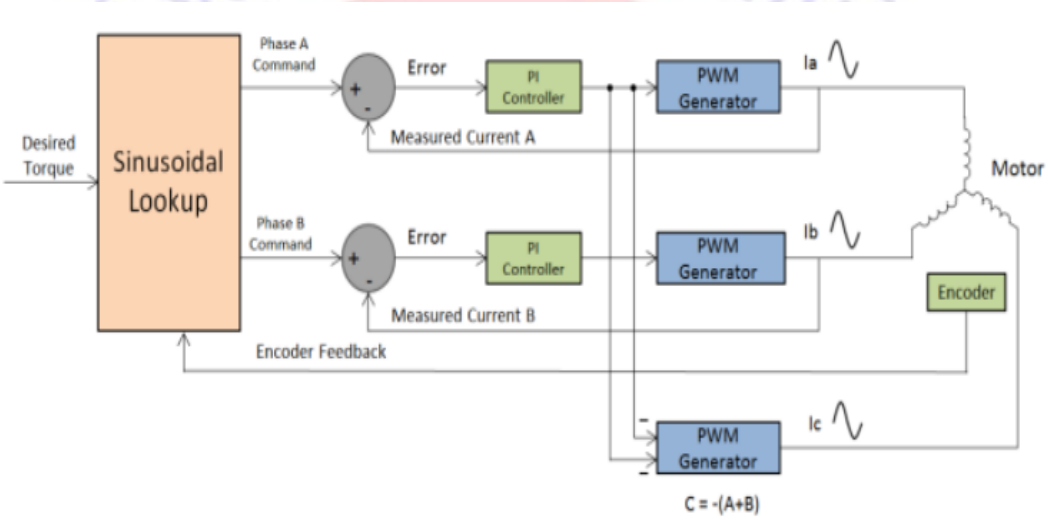

Figure 2.4 Block Diagram of Sinusoidal Control Scheme [36]

2.2.3 Field Oriented Control

FOC control is regarded as an upgraded sine wave control, it realizes the control of current vector, namely realizing the vector control of motor's stator magnetic field This control scheme revolves around Clarke and Park Transformations, and their inverse. By applying these transformations, the 3Φ currents of the stator into the rotating frame of the rotor. By using Clarke Transformation, three-phase quantities are translated from the three-phase reference frame to the two-axis orthogonal stationary reference. However, the quantities are still in a stationary reference frame while the rotor reference frame is constantly rotating. Park's Transformation converts these quantities into an

orthogonal reference frame consisting of the direct and quadrature axis. Figure 2.5 shows the block diagram of the Field Oriented Control.[16]

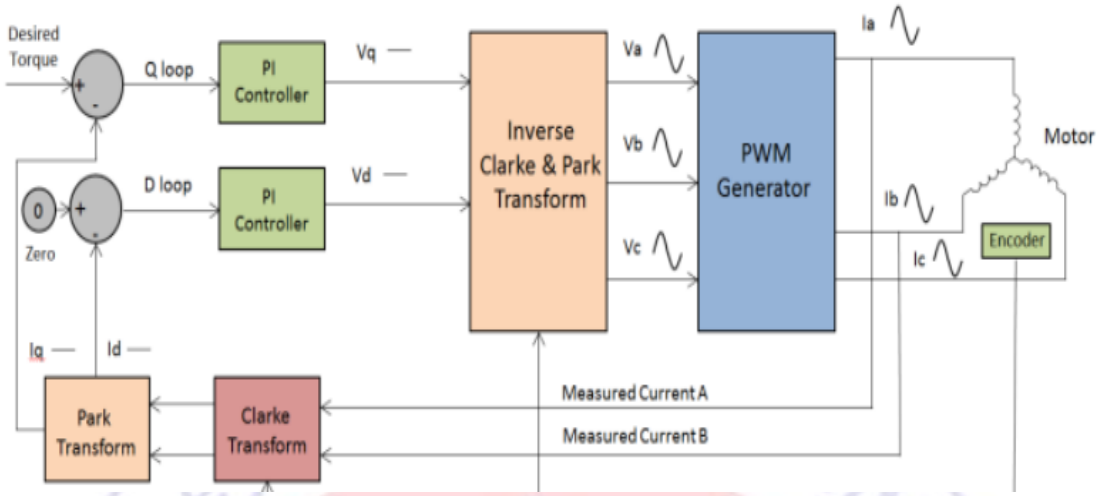

Figure 2.5 Block Diagram of FOC [36]

Advantages of FOC control include: small torque ripple, high efficiency, low noise and fast dynamic response. Disadvantages include: high hardware cost, higher requirement for the controller performance, and motor parameters need to be matched.[15]

2.3 Controllers

A controller circuit is critical for improving the performance of BLDC motors. For this, several controller circuits and algorithms are used. A few of them include P controllers, PI controllers, PID controllers, fuzzy logic controllers, fuzzy PID controllers, Artificial Neural Network (ANN) based controllers, etc.[7]

2.3.1 PI Controller

It is a type of controller that uses proportional and integral control operations. Using the gain Kp, the P controller generates an output that is proportionate to the current error value. High proportional gain causes the system to become unstable. To make the system stable, integral action comes into the action. It lacks the ability to forecast potential system problems because it cannot reduce rise time and eliminate oscillations. Figure 2.6 depicts the block diagram of PI Controller.[11]

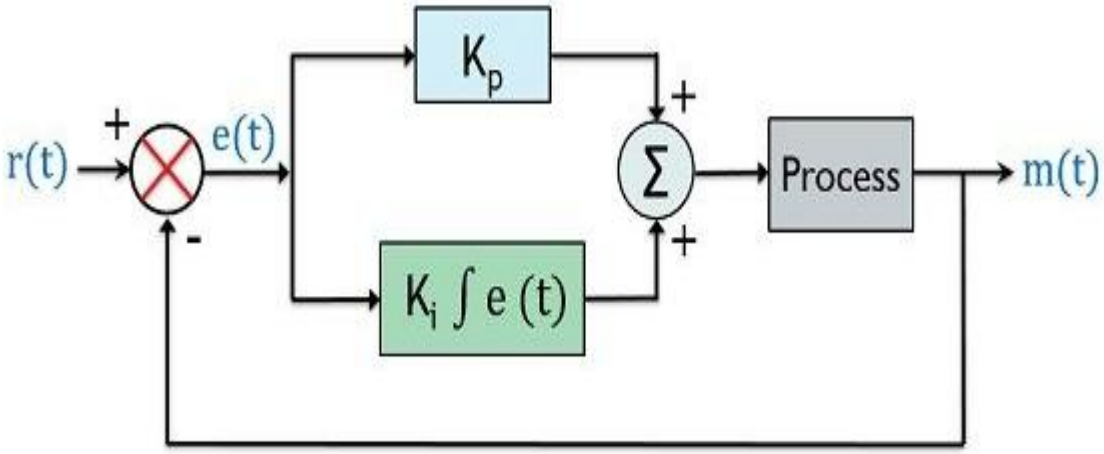

Figure 2.6 Block Diagram of PI Controller

The mathematical equation of PI controller is as shown

$$m(t) = kp\ e(t) + ki\ \int e(t) \quad \text{..... (2.1)}$$

Here m(t) is the PI output, e(t) is the error, k_p and k_i are the proportional and the integral gain respectively.

2.3.2 PID Controller

To prevent oscillations and overshoot in the system's output response, the derivative gain component is added to the PI controller in the PID controller. Three terms a proportional, integral, and derivative term are added together to form the output. The controller provides great stability, no oscillations, quick response times, and zero steady error. Figure 2.7 represents the block diagram of PID controller.[11]

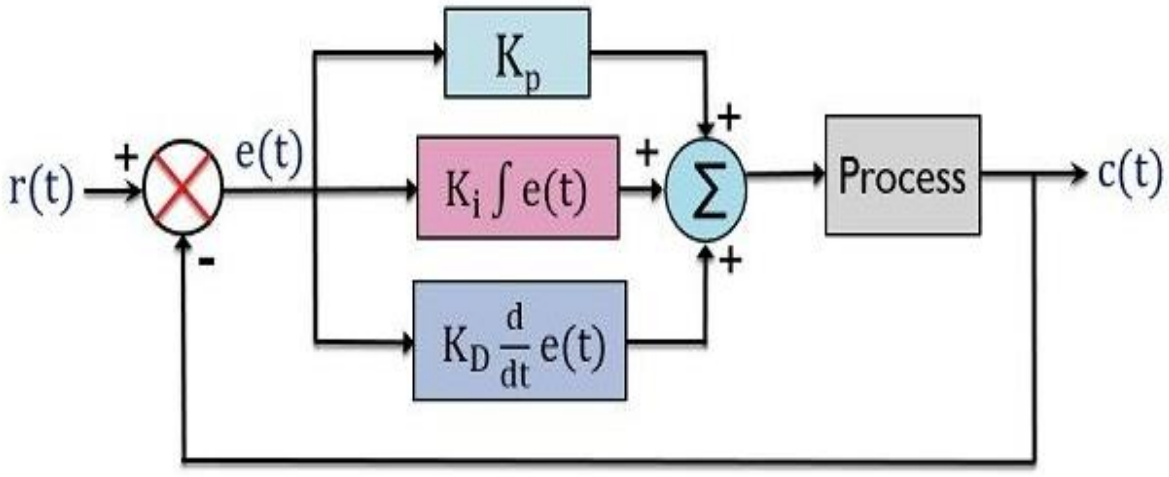

Figure 2.7 Block Diagram of PID Controller

The mathematical equation of PI controller is as shown

$$c(t) = kp\, e(t) + ki \int e(t) + kd \frac{d}{dt} e(t) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.2)$$

Here c(t) is the PID output, k_p is the proportional gain, k_i is the integral gain and k_d is the derivative gain.

2.3.3 Fuzzy Logic Controller

Complicated mathematical models and complex mathematical equations are needed for conventional controls. On the other hand, a fuzzy logic controller doesn't require complex mathematical modelling to cater the non-linearities. Operational laws in fuzzy logic controllers are expressed in linguistic words as alternative to mathematical formulae. There are numerous sophisticated controllers exist that are difficult to design. Fuzzy logic is therefore preferable for nonlinear controllers since it is simpler and much more feasible. Figure 2.8 represents the block diagram of the FLC.[20]-[22]

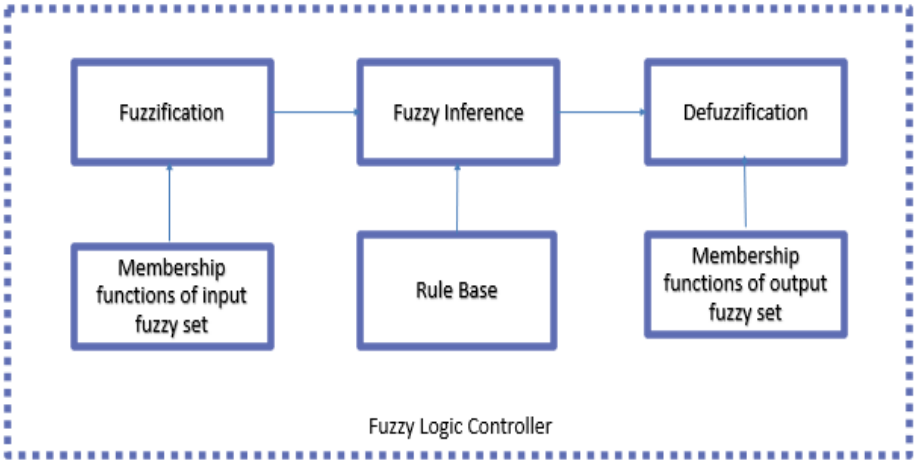

Figure 2.8 Block Diagram of FLC [13]

2.3.3.1 Fuzzification

The method of "fuzzification" involves transforming the controller's input values from crisp to fuzzy or linguistic variables based on membership functions. The selection of the state variables (also known as input variables) and control variables (also known as output variables) is the most crucial stage in the fuzzification. There are various membership function types, including gaussian, triangular, and trapezoidal. Figure 2.9, Figure 2.10 shows the representation of triangular and trapezoidal membership function respectively.[13]-[15]

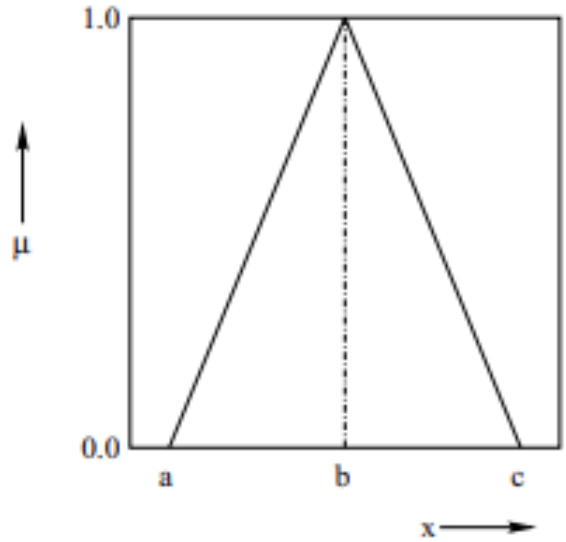

Figure 2.9 Triangular Membership Function [15]

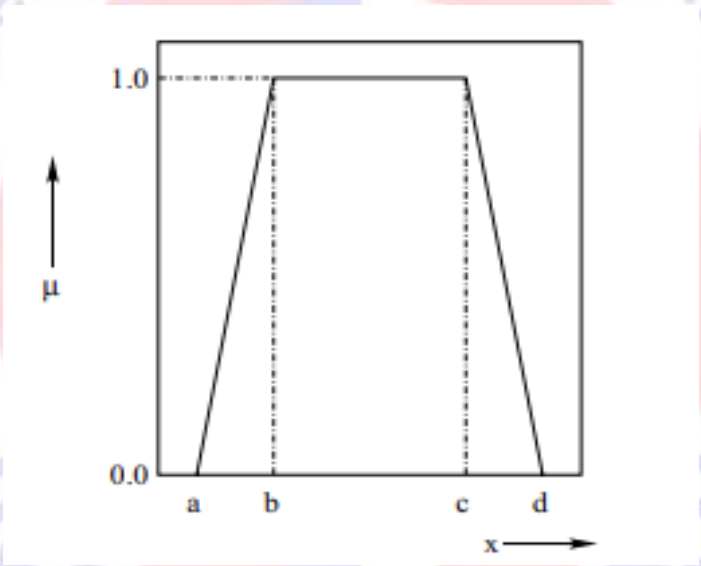

Figure 2.10 Trapezoidal Membership Function [15]

2.3.3.2 Inference Engine

The fuzzy output is produced by the inference engine by applying the inference rules to the fuzzy input. In particular, the inference rules are used to assess linguistic values and map them to a fuzzy set, it then needs to be defuzzified to become a crisp value. Mamdani and Sugeno approach are the two types of inference systems. These guidelines may be derived from prior information, observations, and experiences. The fundamental components of each fuzzy inference rule are if-then statements and

linguistic variables. The verbal input serves as the antecedent in the if-then rules, and the linguistic output serves as the consequence and is dependent on the input.[13][16]

2.3.3.3 Defuzzification

The output of the inference system is in the form of fuzzy variables. The defuzzification is required to convert the fuzzy output into the defuzzified or the crisp output. Some of the types of defuzzification methods are Centroid method, weighted average method, height method etc [15]

2.4 Summary

This chapter discussed the BLDC motor theory, its construction and operating principle, control techniques and various controllers like PI, PID and FLC. Particularly the block diagram of FLC and the basic structure that shows the different steps of the process like fuzzification, inference and the defuzzification process is illustrated.

Chapter 3

METHODOLOGY AND BLOCK DIAGRAM

The chapter gives a comprehensive overview of the FLC's project methodology and briefly explains the block diagram of the proposed work, process flow for the simulation.

3.1 Methodology

A BLDC motor is driven by voltage coupled by rotor position. The rotor position is measured using Hall sensors. By varying the voltage across the motor, the speed of the motor is controlled. The PWM is used to control the six switches of the three-phase bridge, variation of the motor voltage is obtained by varying the duty cycle of the PWM signal. The speed and torque of the motor depend on the strength of the magnetic field generated by the energized windings of the motor, it depends on the current through them. Hence adjusting the rotor voltage and current changes motor speed. Commutation ensures only proper rotation of the rotor.

Figure 3.1 represents the flowchart for the methodology of the proposed control technique.

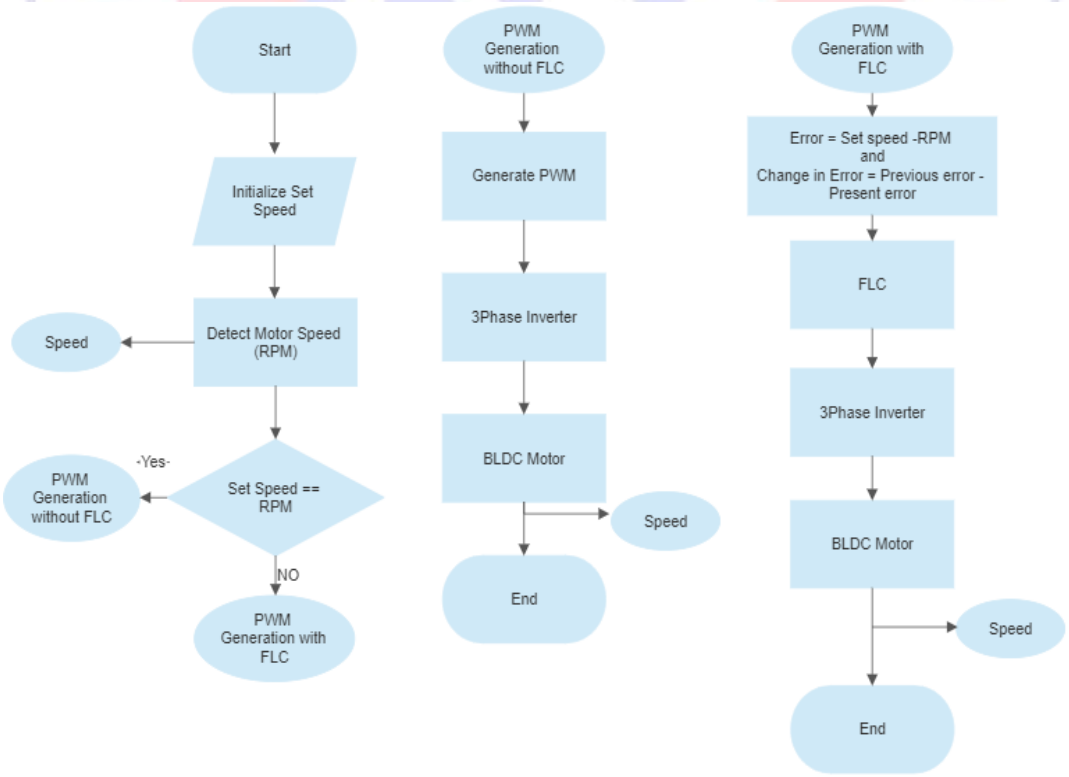

Figure 3.1 Flowchart for the Methodology of the Proposed Controller

The motor speed depends on the amplitude of the applied voltage. This is adjusted using PWM technique. The required speed is controlled by a speed controller. This is implemented as a advanced Fuzzy Logic controller. The difference between the actual and required speeds is given as input to the controller. Based on this data FLC controls the duty cycle of the PWM pulses that correspond to the voltage amplitude required to maintain the desired speed. When using PWM outputs to control the six switches of the three-phase bridge, variation of the motor voltage is achieved easily by changing the duty cycle of the PWM signal.

The process is initiated by setting the BLDC motor's required speed (set speed),and the sensor is used to determine the motor's actual speed. Then the system compares the set speed and the actual speed of the motor. If the motor's set speed and actual speed are the same, the PWM generator provides the pulses required for the inverter to supply the necessary amount of power to the BLDC motor.

The FLC receives two inputs - the error and the change in error of the speed if the motor's actual speed and the set speed are not the same. The error and the change in error is calculated using the equations as shown

$$Error = Set\ speed - Actual\ Speed$$

$$Change\ in\ Error = Previous\ Error - Present\ Error$$

The FLC takes these two as the input and the fuzzification process converts these two crisp inputs into the fuzzy or the linguistic variables based on membership functions. The membership function used here is the triangular membership function.

The fuzzy input from the fuzzification step gets processed in the fuzzy inference system and the inference rules are used to assess linguistic values and map them to a fuzzy set. The Mamdani based fuzzy inference system is used in the proposed work.

The output of the inference system is in the form of fuzzy variables. The defuzzification is required to convert the fuzzy output into the defuzzified or the crisp output. The weighted average method of defuzzification is used in the proposed work.

Based on these concepts the fuzzy logic controller for speed control of BLDC motor is designed. Steps involved in the development and implementation of proposed system as shown in Figure 3.2.

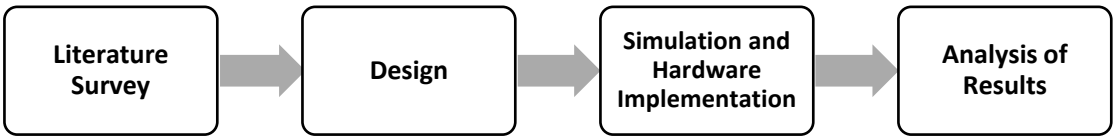

Figure 3.2 Methodology of Proposed Work

- Literature Survey - A detailed literature survey is carried out for selecting required topology of the controller and the FLC is selected.
- Design - The FLC controller is designed by using Mamdani Fuzzy Inference System and triangular membership functions and the weighted average method of defuzzification is adopted.
- Simulation and Hardware Implementation – Speed control of BLDC motor using FLC is simulated using the MATLAB Simulink and the implementation is done using suitable components.
- Analysis of Result – Analysis of the FLC controller with different speeds and for the drive cycle and the results obtained using the FLC controller is compared with the conventional PI and PID Controller.

3.2 Block Diagram

The block diagram of the FLC for the speed control of BLDC motor consisting of the BLDC motor, a sensor, commutation logic block, 3 phase inverter, PWM generator, FLC is depicted as shown in Figure 3.3.

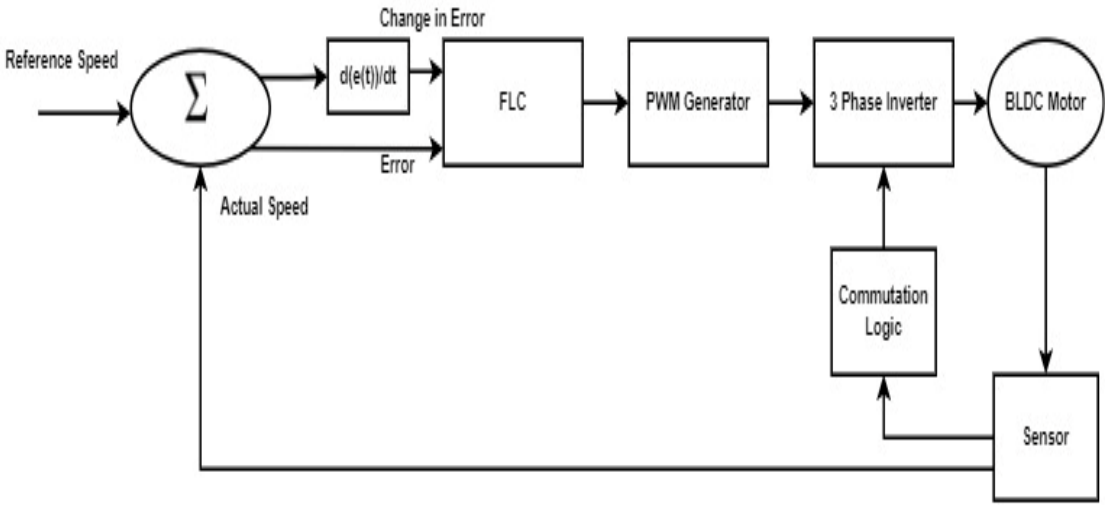

Figure 3.3 Block Diagram of FLC for Speed Control of BLDC motor

- Sensor: The speed and rotor position of the BLDC motor are sensed by a sensor. The sensor determines the right rotor position in order to calculate the correct time to drive the motor.
- Error and change in error block: The sensed speed from the sensor and the reference speed is compared to find the error in the speed and change in error and these two parameters are fed as the input to the controller.
- FLC: The FLC takes these two as the input and the fuzzification process converts these two crisp inputs into the fuzzy or the linguistic variables based on triangular membership functions and gets processed using the Mamdani Fuzzy Inference System and the defuzzified output is generated using the weighted average method.
    - PWM generator: The defuzzified output from the controller is fed to the PWM generator to generate the PWM pulses with the necessary duty cycle for a three-phase inverter.
    - 3 Phase Inverter: The voltage required for the operation of the BLDC motor at the desired speed is supplied by the 3 Phase Inverter using PWM pulses from the PWM generator.
    - Commutation Logic: The commutation logic block provides the rotor position for starting and for providing proper commutation sequence to turn on the power switches in the inverter bridge. Instead of commutating the armature current using brushes, electronic commutation is used and based on the rotor position, the power devices are commutated sequentially every 60 degrees.

3.3 Summary

The chapter gives the detailed information regarding the block diagram, methodology and the steps involved in the development and implementation of the speed control of BLDC motor using the FLC.

Chapter 4

SPECIFICATION AND DESIGN

This chapter discusses the specifications of the BLDC motor and the FLC used in the simulation. The FLC's design requirements and the hardware components' specifications utilised for the suggested work are shown.

4.1 Specifications

The specifications of the BLDC motor and the FLC selected for the simulation after extensive literature review are depicted in Table 4.1.

Table 4.1 Specifications of BLDC motor and FLC

Parameter	Value
FLC Type	Mamdani
Number Of Inputs, output	2,1
Type Of membership function used	Triangular
Rule Evaluation Done Using	AND(Min)
Defuzzification Type	Weighted Average
Type of Motor	BLDC
Back EMF area (degree) of the Motor	120
Stator Phase Resistance (Rs) of the Motor	10.91 Ohm
Stator Phase Inductance (Is) of the Motor	30.01 mH
Inertia in kgm^2 of the Motor	2 e-4
Viscous Damping of the Motor	1e-3 N-m-s
Pole Pairs	4

4.2 Selection of Components

The different components utilised, together with their specifications, for the experimental prototype implementation of the recommended work are listed as follows.

4.2.1 BLDC Motor

For the suggested prototype, A2212 BLDC motor is used. It is a brushless outrunner DC motor that offers incredible performance, strength, and efficiency. The specifications of the motor are listed as follows

- Part Number –A2212
- Rating – 15W
- Current Capacity: 12A/60s
- No Load Current @ 10V: 0.5A
- No. Of Cells: 2-3 Li-Poly
- Motor Dimensions: 27.5 x 30mm
- Shaft Diameter: 934;3.17mm
- Shaft diameter: 3.175mm

4.2.2 Electronic Speed Controller (ESC)

An electronic speed control (ESC) is a circuit that modifies the duty cycle or switching frequency of MOSFET to control and regulate the speed of an electric motor.

- CURRENT (A): 30A
- BEC: 3A
- Li-Poly: 2-3
- WEIGHT: 23g
- DIMENSIONS: 45 x 24 x 9 mm (LxWxH)

4.2.3 Regulator (LM7805)

The LM7805 is a three-terminal positive regulator available in the TO-220/D-PAK package used to generate the 5V supply to power the microcontroller.

- Thermal Overload Protection.
- Short Circuit Protection.
- Output Transistor Safe Operating Area Protection.
- Surface mount in TO-220/D-PAK Package.
- Vin = 35V (Absolute Max)
- Operating Temperature: 0 to 125˚C

4.2.4 IR Sensor

The IR sensor is utilized to measure the motor's RPM and transmit that data to the controller.

- Vin: 3-5V
- Detection distance: 2 ~ 30cm
- Detection angle: 35 °
- Comparator chip: LM393
- Size: 3.1CM * 1.5CM

4.2.5 PCF8574

PCF8574 provides the The PCF8574 provides general-purpose remote I/O expansion via the two-wire bidirectional I2C-bus.

- Number Of Pins – 16
- Vin – 2.5V to 6V
- 100 kHz I2C-bus interface
- The device features an 8-bit quasi-bidirectional I/O port.
- SMD with SOIC package

4.2.6 Battery

The Lithium Polymer (LiPo) battery of 2200mAH and 11.1V is used as the DC source in the proposed work to power the BLDC motor.

- Charge Capacity (C): 2200mAh.
- Rated Voltage: 11.1V
- Exact weight: 150 - 160 Grams
- LxWxH: 100*20*30mm Approx.
- Discharge Rate: 25C

4.2.7 Arduino UNO

Arduino Uno is an open-source microcontroller board based on Microchip ATmega328P microcontroller. It is used as the microcontroller to implement the FLC for the proposed work. C/C++ programming language are used to programme Arduino. The Arduino Uno with its pinout is shown in Figure 4.1.

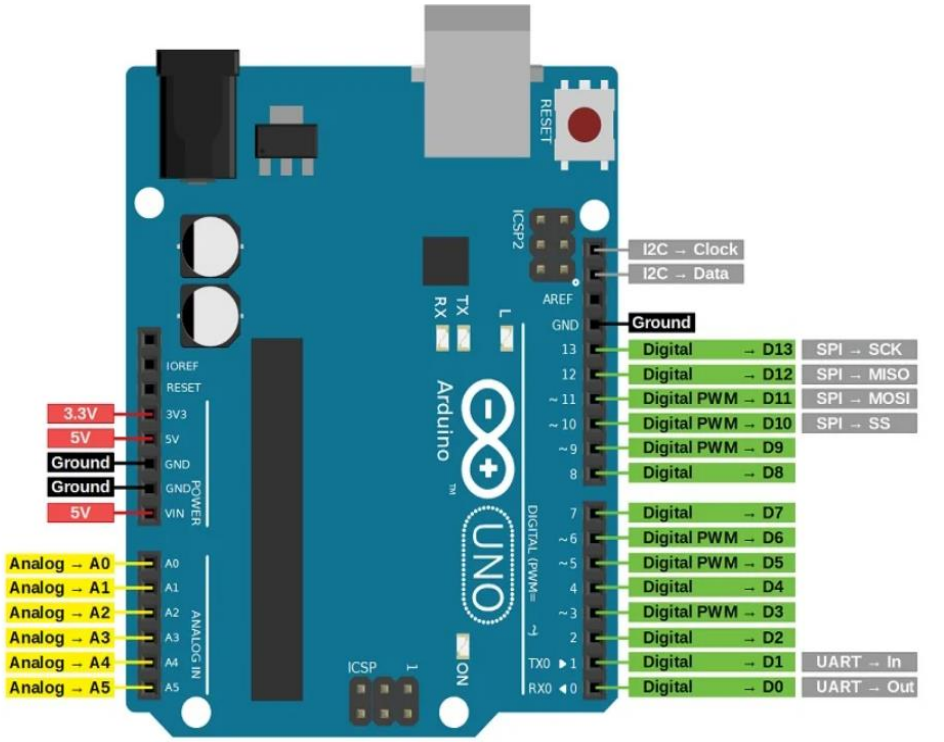

Figure 4.1 Arduino Uno with its Pinout

4.3 FLC Design

The FLC controller for the speed control of BLDC motor is designed using 2 inputs and one output. The two inputs are the error (E) and the change in error (CE) and the output is the controlled output (O). The input variables E and CE are obtained using the equations shown

$$Error\ (E) = Set\ speed - Actual\ Speed \text{ ---------- (4.1)}$$

$$Change\ in\ Error\ (CE) = Previous\ Error - Present\ Error \text{ ---------- (4.2)}$$

Error input is considered to be the triangular membership function consists of the seven linguistic variable, Positive Small (PS), Positive Medium (PM), Positive Big (PB), Zero (Z), Negative Big (NB), Negative Medium (NM), and Negative Small (NS) and ranges between -6.64 to 6.64. The degree of these membership functions is obtained using the triangular rule equation. Table 4.2 shows the linguistic variables of the error inputs and their respective ranges.

Table 4.2 Linguistic Variables of Error input

Error (E)	Range
NB	-6.64 to -3.338
NM	-5 to -1.667
NS	-3.338 to 0
Z	-1.667 to 1.667
PS	0 to 3.338
PM	1.667 to 5
PB	3.338 to 6.64

In the same way the change in error input is also considered to be the triangular membership function with 7 linguistic variables, Positive Small (DPS), Positive Medium (DPM), Positive Big (DPB), Zero (DZ), Negative Big (DNB), Negative Medium (DNM), and Negative Small (DNS) and ranges between -6.64 to 6.64. The degree of these membership functions is obtained using the triangular rule equation. Table 4.3 shows the linguistic variables of the change in error inputs and their respective ranges.

Table 4.3 Linguistic Variables of Change in Error

Error (E)	Range
DNB	-6.64 to -3.338
DNM	-5 to -1.667
DNS	-3.338 to 0
DZ	-1.667 to 1.667
DPS	0 to 3.338
DPM	1.667 to 5
DPB	3.338 to 6.64

The output variable is also considered to be the triangular membership function with 7 linguistic variables, Positive Small (OPS), Positive Medium (OPM), Positive Big (OPB), Zero (OZ), Negative Big (ONB), Negative Medium (ONM), and Negative Small (ONS) and ranges between -1.333 to 1.333. The degree of these membership functions is obtained using the triangular rule equation. Table 4.4 shows the linguistic variables of the output and their respective ranges.

Table 4.4 Linguistic Variable of Output

Output (O)	Range
ONB	-1.333 to -0.6568
ONM	-1 to -0.3432
ONS	-0.6568 to 0
OZ	-0.3432 to 0.3288
OPS	0 to 0.6712
OPM	0.3288 to 1
OPB	0.6712 to 1.333

The fuzzy output is produced by the inference engine by applying the inference rules to the fuzzy input. In particular, the inference rules are used to assess linguistic values and map them to a fuzzy set, that then needs to be defuzzified to become a crisp value. The Mamdani fuzzy inference system is used, and the rule evaluation is done using AND operator. The rules are fired according to the IF-THEN rules combined with the AND operator. The rule base consisting of 49 rules are as shown in the Table 4.5.

Weighted average method of defuzzification is employed to find the de-fuzzified output as shown

$$z = \frac{\sum_{i=1}^{n}(\mu i * ai)}{\sum_{i=1}^{n} \mu i} \quad \text{---------- (4.3)}$$

Here μ is the result of composition rules, a is the value of output.

Table 4.5 The Fuzzy Rule Base

Error/change in error	**DNB (-5)**	**DNM (-3)**	**DNS (-1)**	**Z (0)**	**DPS (1)**	**DPM (3)**	**DPB (5)**
NB (-5)	ONB (-0.892)	ONB (-0.887)	ONB (-0.878)	ONB (-0.892)	ONM (-0.698)	ONS (-0.416)	OZ (-0.0047)
NM (-3)	ONB (-0.887)	ONB (-0.792)	ONB (-0.63)	ONM (-0.584)	ONS (-0.389)	OZ (0.0014)	OPS (0.414)
NS (-1)	ONB (-0.878)	ONB (-0.63)	ONM (-0.374)	ONS (-0.193)	OZ (0.0035)	OPS (0.385)	OPM (0.695)
Z (0)	ONB (-0.892)	ONM (-0.584)	ONS (-0.193)	OZ (-0.0047)	OPS (0.191)	OPM (0.586)	OPB (0.897)
PS (1)	ONM (-0.698)	ONS (-0.389)	OZ (0.0035)	OPS (0.191)	OPM (0.371)	OPB (0.628)	OPB (0.883)
PM (3)	ONS (0.415)	OZ (0.0025)	OPS (0.386)	OPM (0.587)	OPB (0.629)	OPB (0.788)	OPB (0.892)
PB (5)	OZ (-0.0047)	OPS (0.414)	OPM (0.695)	OPB (0.897)	OPB (0.883)	OPB (0.892)	OPB (0.897)

4.4 Summary

In this chapter design of the FLC controller and the specifications of the BLDC motor and the FLC used for the simulation in MATLAB Simulink is discussed in detail.

Chapter 5

SIMULATION AND HARDWARE IMPLEMENTATION

This chapter discusses the simulation of speed control of the BLDC motor using the MATLAB Simulink. The circuit model and the hardware components used are explained in detail.

5.1 Simulation Analysis

The proposed work of speed control of BLDC motor using FLC has been simulated using the MATLAB Simulink Software. The simulation model of BLDC motor by using FLC is shown in Figure 5.1. The Simulink model consists of the BLDC motor model, Decoder, Commutation Logic Block, Inverter, FLC circuit and the reference speed block.

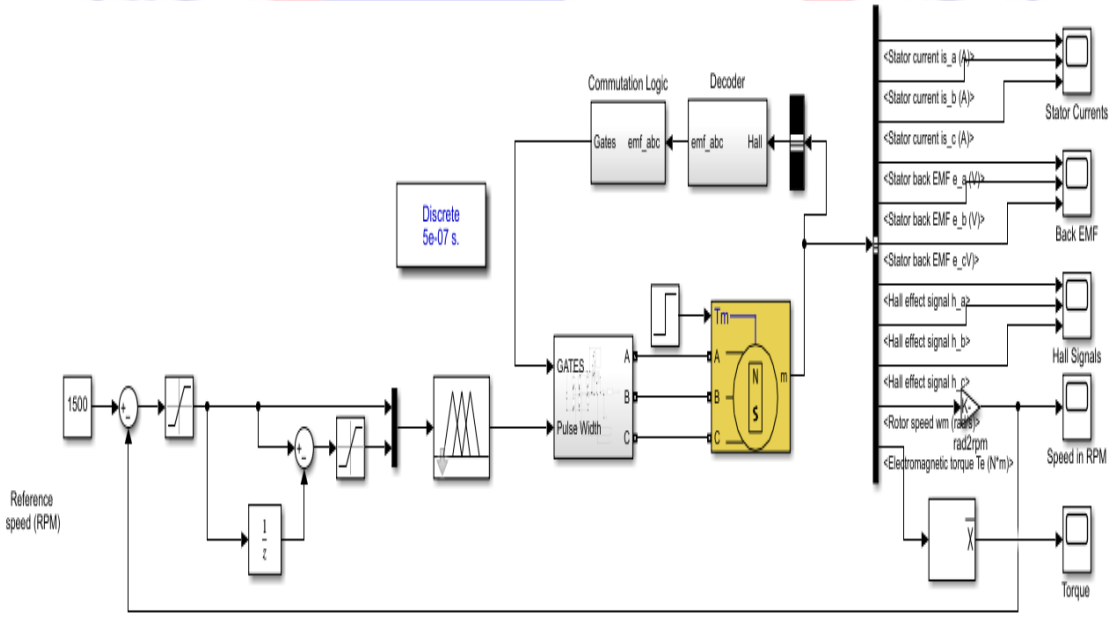

Figure 5.1 Simulation Model of the Proposed Work

5.1.1 BLDC Motor Model

The BLDC motor model used for the simulation to develop FLC for the outer speed and position loops is as shown in the Figure 5.2. The bus selector is used to read the data such as stator currents, back emf, hall sensor signals, speed and torque.

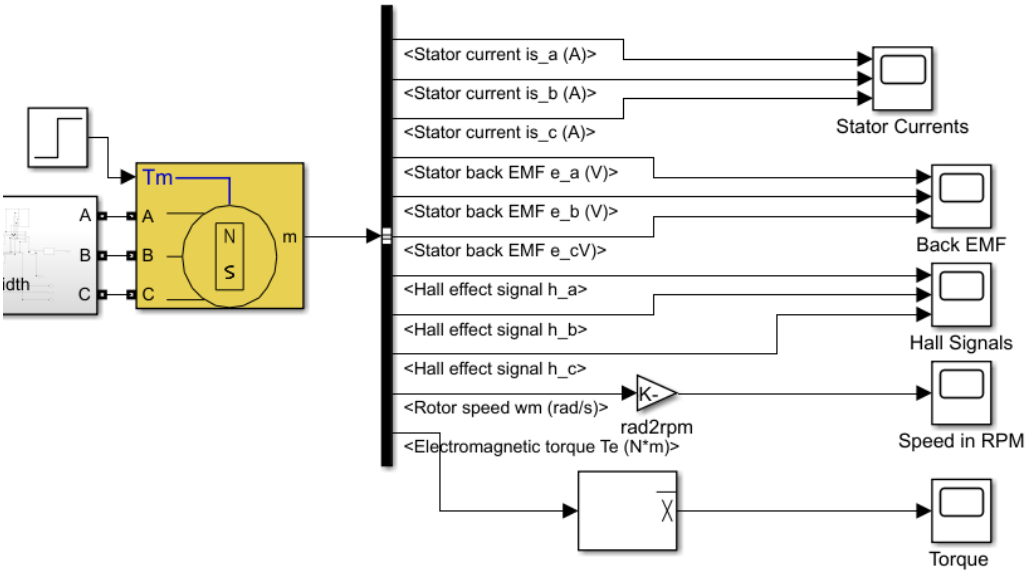

Figure 5.2 BLDC Motor Model

In the simulation of the suggested work, a BLDC motor with trapezoidal back EMF and three phase is chosen. The BLDC motors other specifications are taken as shown in the Figure 5.3

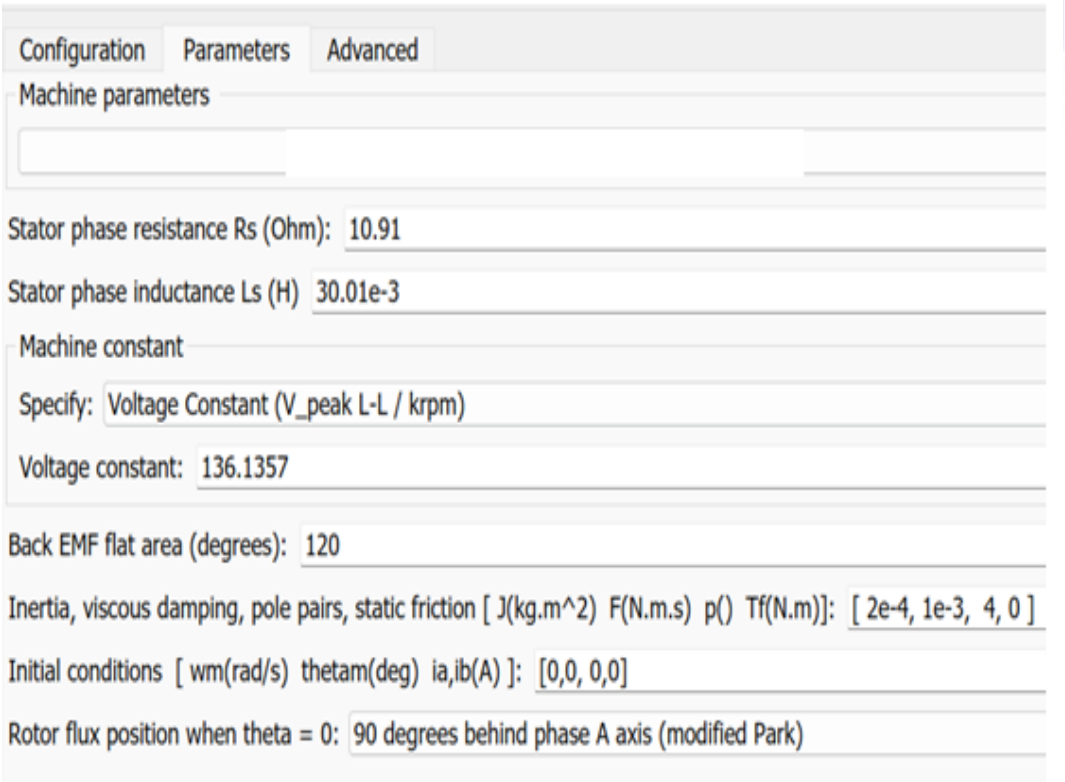

Figure 5.3 Parameters Set for the Motor

5.1.2 Decoder

The hall effect sensor determines the BLDC motors rotor shaft position, and the decoder uses these data as input to produce the EMF (Electromotive Force) signals for the 120˚ conduction by using the combinational logic. Figure 5.4 shows the decoder block of the simulation model.

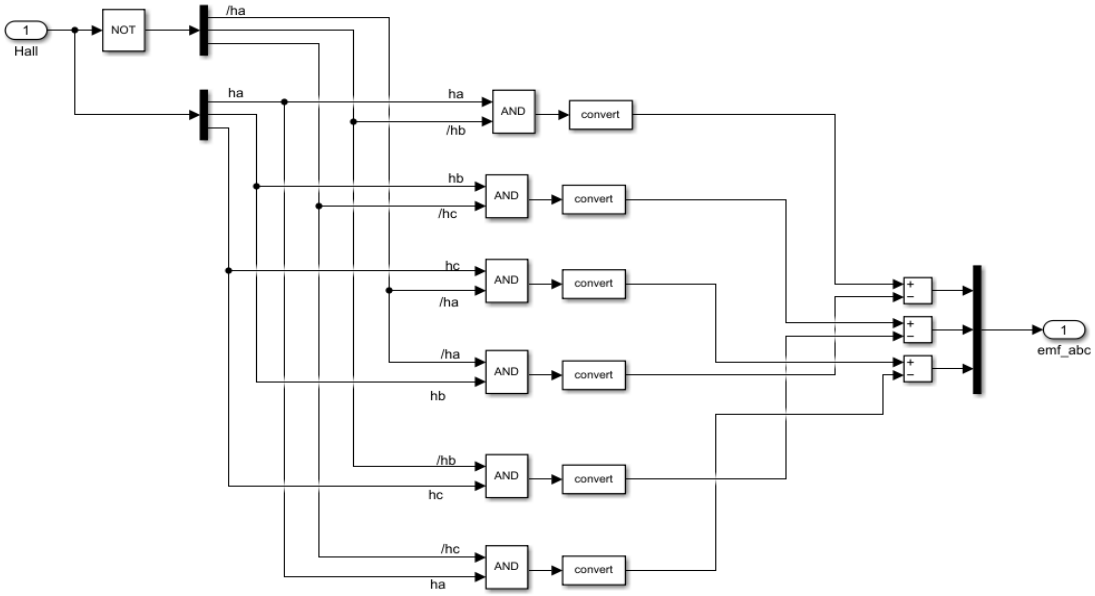

Figure 5.4 Decoder Block of the Simulation Model

The truth table implemented using the decoder module to generate the EMF signals for 120^{o} conduction is as shown in the Table 5.1.

Table 5.1 Truth Table Implemented Using Decoder Module

Ha	Hb	Hc	emf_a	emf_b	emf_c
0	0	0	0	0	0
0	0	1	0	-1	1
0	1	0	-1	1	0
0	1	1	-1	0	1
1	0	0	1	0	-1
1	0	1	1	-1	0
1	1	0	0	1	-1
1	1	1	0	0	0

5.1.3 Commutation Logic Block

This block generates the commutation logic by using the EMF signals that are generated by the decoder block. Figure 5.5 depicts the commutation logic block of the simulation model.

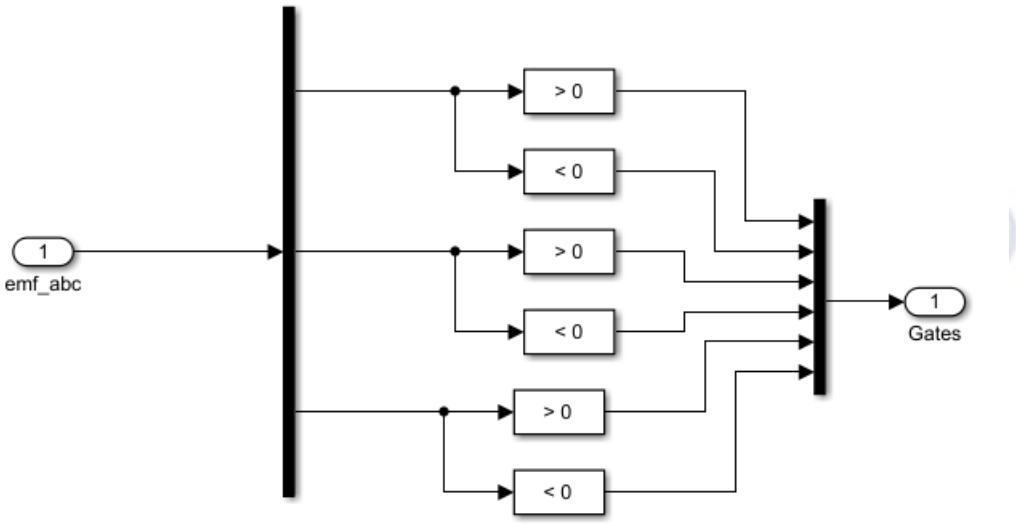

Figure 5.5 Commutation Logic Block of the Simulation Model

The truth table for the commutation logic generated by the commutation logic module is as shown in the Table 5.2.

Table 5.2 Truth Table for Commutation Logic

emf_a	emf_b	emf_c	S1	S2	S3	S4	S5	S6
0	-1	1	0	0	0	1	1	0
-1	1	0	0	1	1	0	0	0
-1	0	1	0	1	0	0	1	0
1	0	-1	1	0	0	0	0	1
1	-1	0	1	0	0	1	0	0
0	1	-1	0	0	1	0	0	1

5.1.4 FLC Block

The predefined block for analysing, creating and simulating systems based on the fuzzy logic is named as fuzzy logic tool box in MATLAB Simulink. This toolkit enables

to apply the fuzzy rules in the Fuzzy Inference system and use them to simulate the behaviour of the complicated system using a few simple logic rules.

The proposed word is executed by utilizing the MATLAB Simulink fuzzy logic tool box by considering two inputs (Error and Change in Error) and one output (Controlled Output). The input and the output are considered to be the triangular membership functions with 7 linguistic variables each as shown in the Figure 5.6 and Figure 5.7 respectively.

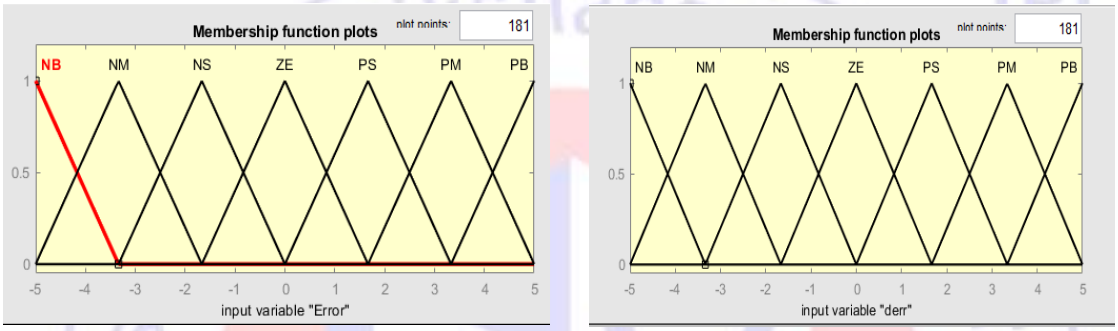

Figure 5.6 Membership Functions for Error Input and Change in Error Input

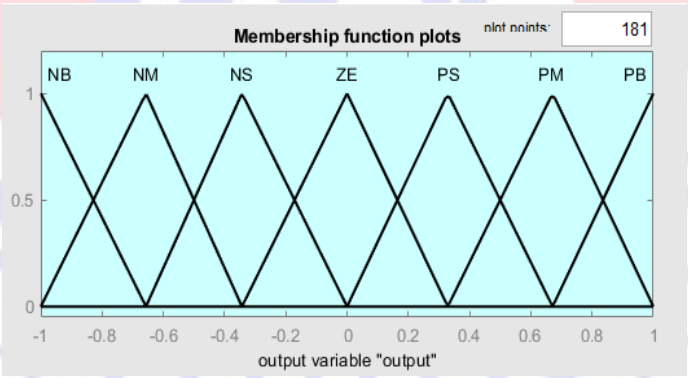

Figure 5.7 Membership Function for Output

The rule base for the proposed work is defined using the rule editor that helps in constructing the rule statements by graphical rule editor interface. It consists of 49 IF – THEN rules connected by the AND operator. The rule editor for proposed work in MATLAB is as shown in the Figure 5.8.

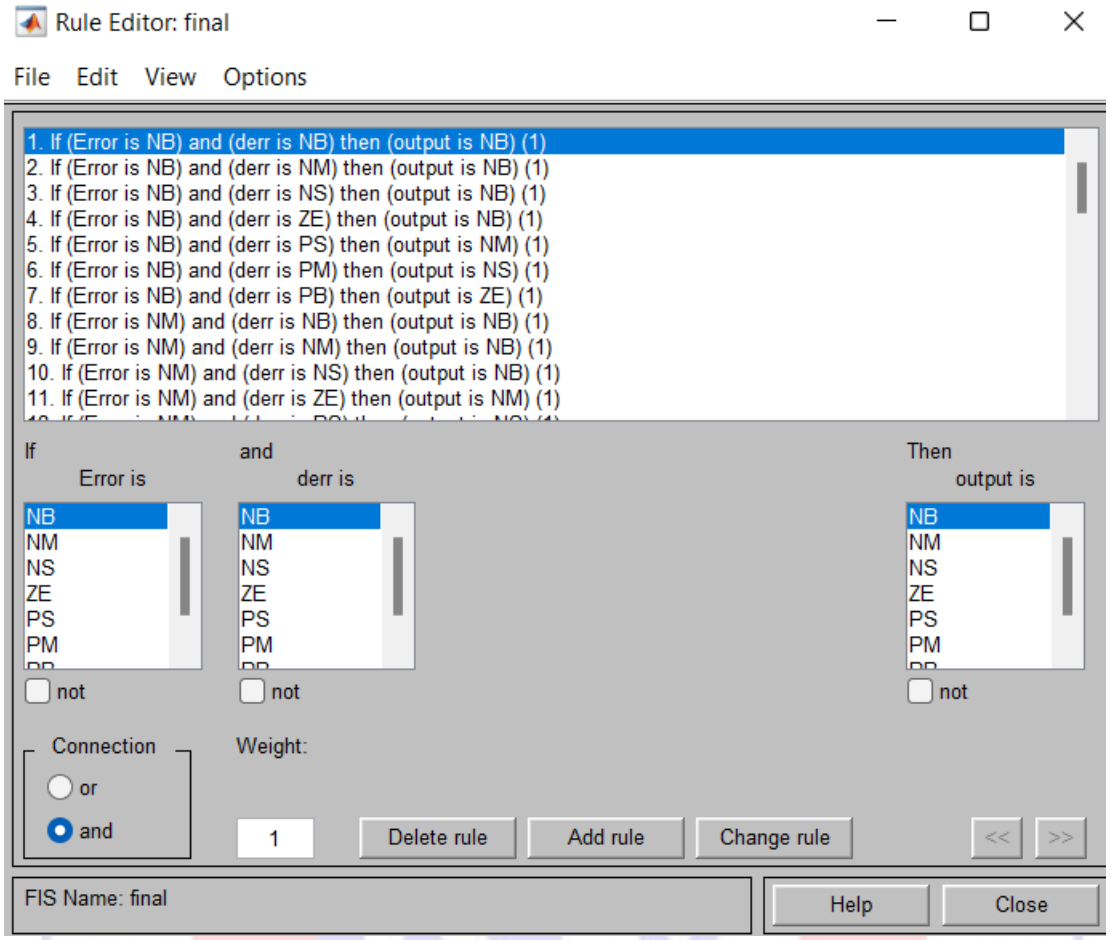

Figure 5.8 Rule Editor for the Proposed Work

The surface viewer generates the three-dimensional output surface of your FIS. The surface viewer corresponding to the present work is as shown in the Figure 5.9.

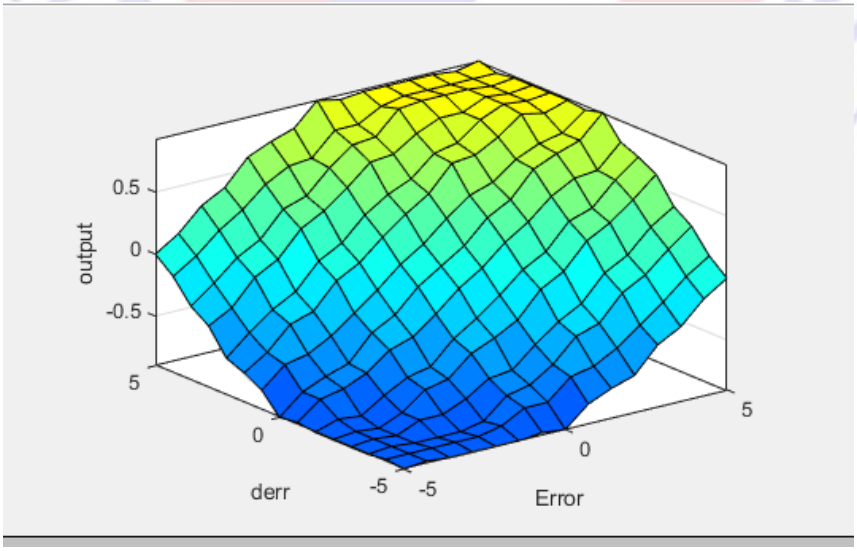

Figure 5.9 Surface Viewer for the Proposed Work

5.1.5 Inverter

The inverter output is used to power the BLDC motor in the proposed work. The duty cycle of the PWM switching signal decides the average supply voltage to the motor in turn the speed. The value of the duty cycle is decided by the controlled output from the FLC. The simulation model of the inverter circuit with the PWM generator is shown in the Figure 5.10. The frequency of the PWM generator is 1KHz with a sample time of 50μ seconds.

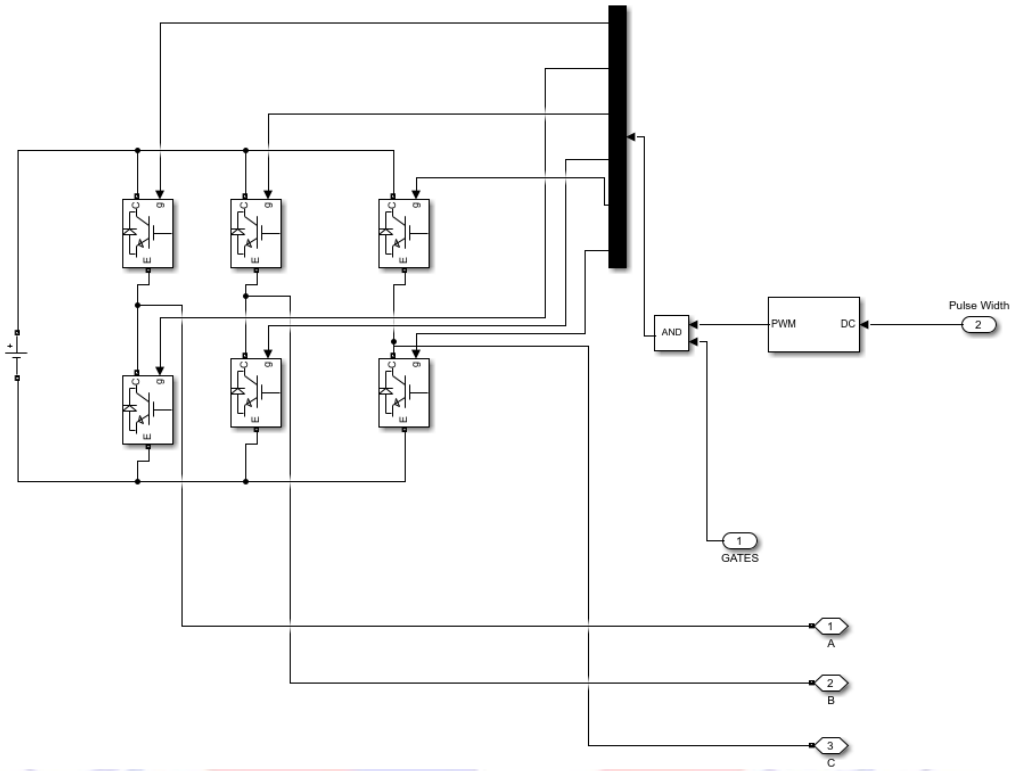

Figure 5.10 Simulation Model of Inverter Circuit

5.2 Implementation

In this section, details of the hardware are presented for experimental validation of the suggested controller technique to regulate the speed of the BLDC motor, schematic and the PCB layout is explained.

The power required by the BLDC motor is supplied by the LiPO battery through the ESC. The required speed of the motor is entered by the user through the keypad that is connected from Pin 15 to 19 of the microcontroller. The IR sensor is used to sense the RPM of the motor and display the current speed on the LED Display. The PCF8574 connected to the SCL and SDL pin of the controller used as the remote input/output expander.

The input from the IR sensor is compared with the reference input speed in the Arduino and the error is generated if the speed is not same. The fuzzy code written on the controller processes the input and generate the PWM output. This PWM output is used to control the supply voltage to the motor by controlling duty cycle or switching frequency of MOSFET present in the ESC and hence the speed is controlled by controlling the average voltage supplied to the BLDC Motor.

The schematic representation and the PCB layout of the proposed work is as shown in the Figure 5.11 and 5.12 respectively.

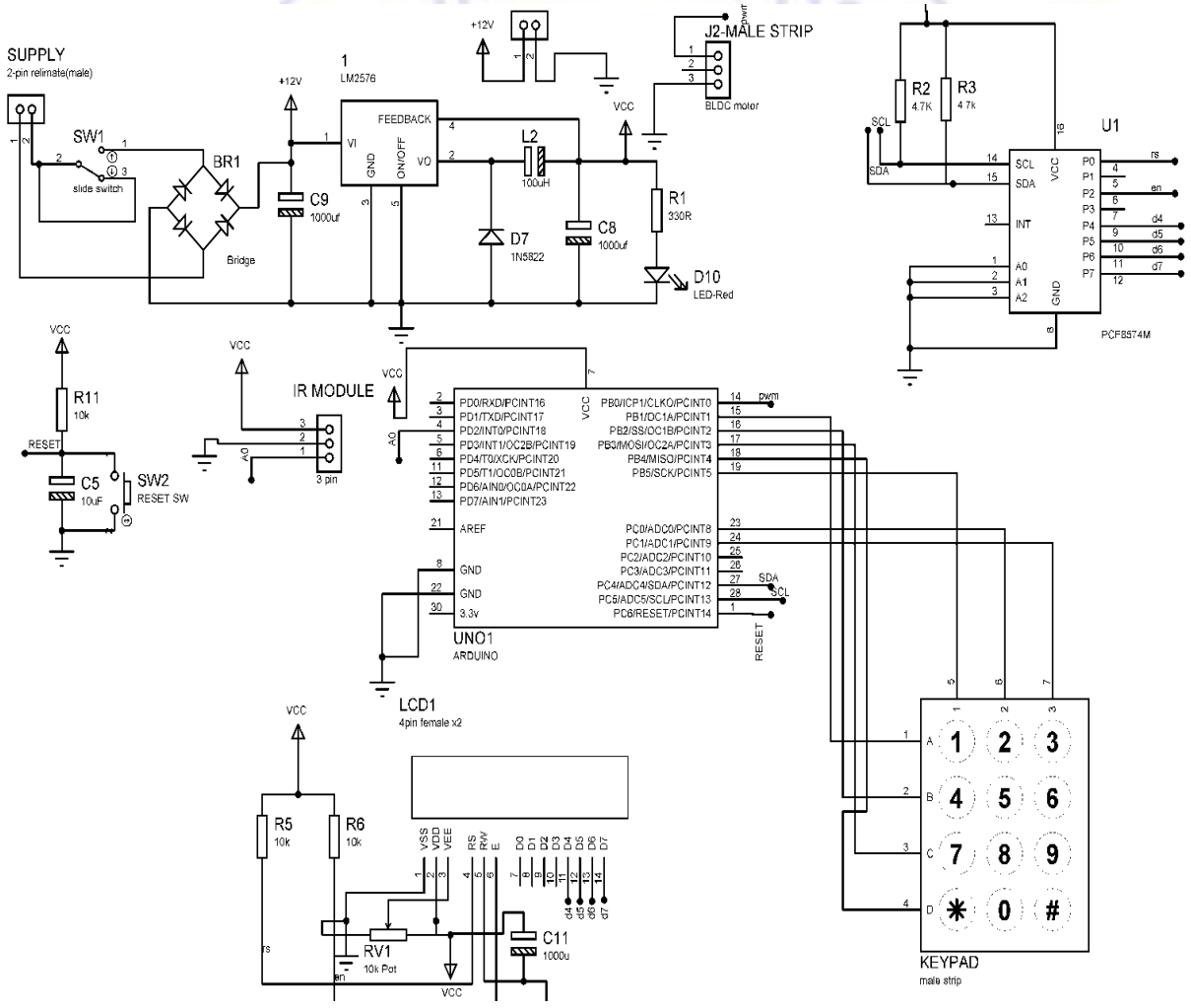

Figure 5.11 Schematic of the Proposed Work.

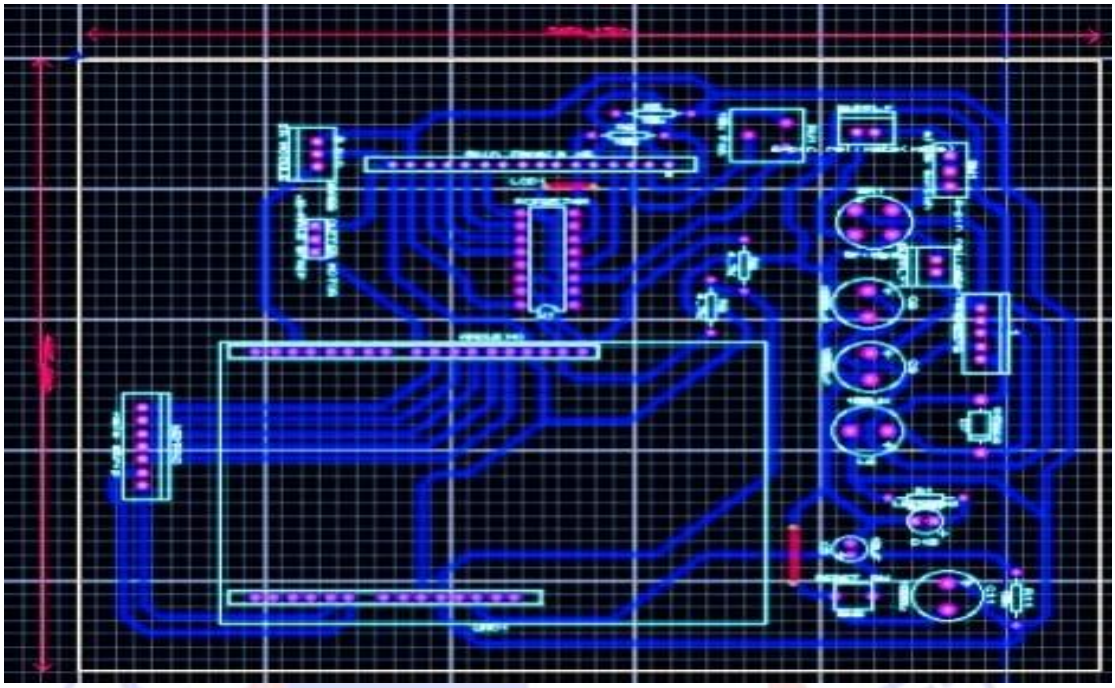

Figure 5.12 PCB Layout of the Proposed Work

The hardware prototype of FLC for speed control of BLDC motor using the Arduino Uno controller, BLDC motor, IR sensor for the closed loop operation, ESC and the Lipo battery to power the motor is as shown in the Figure 5.13

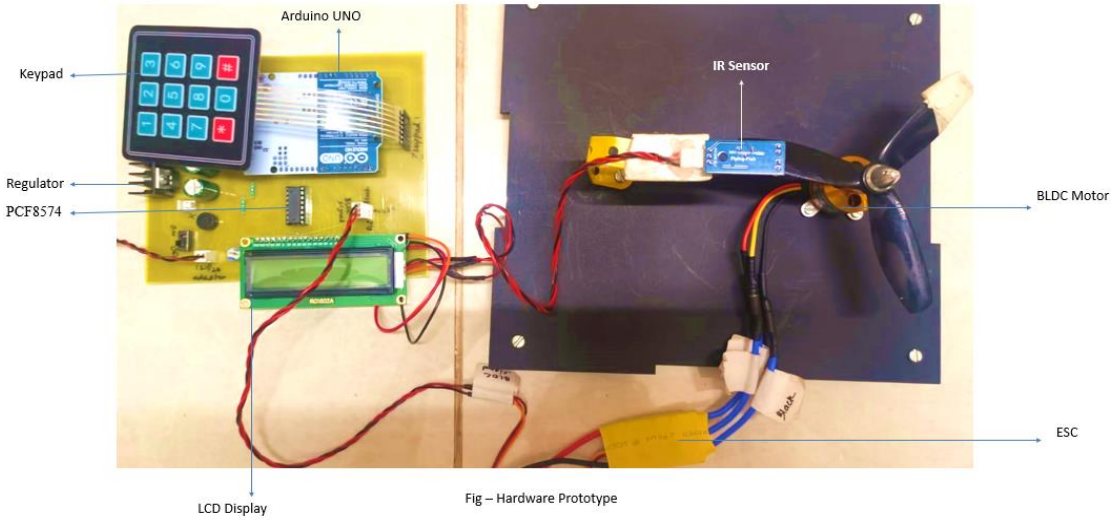

Figure 5.13 Hardware Prototype

5.3 Summary

The simulation of the FLC for speed control of BLDC motor using MATLAB SIMULINK was explained in this chapter. The chapter also describes schematics, PCB layout and the hardware implementation of the work.

Chapter 6

RESULTS AND DISCUSSION

In this chapter the simulation and the hardware results of the BLDC motor speed control using FLC is discussed with its waveforms and results.

6.1 Simulation Results

Chapter 5 presented the simulation circuit of the BLDC motor speed control using FLC with its specifications. The results observed from the circuits are explained. Figure 6.1 shows the speed response of the controller with reference speed 1500rpm the speed response reaches peak value at 3.309ms and reaches a steady state at 2.801ms with the overshoot of 2.577%.

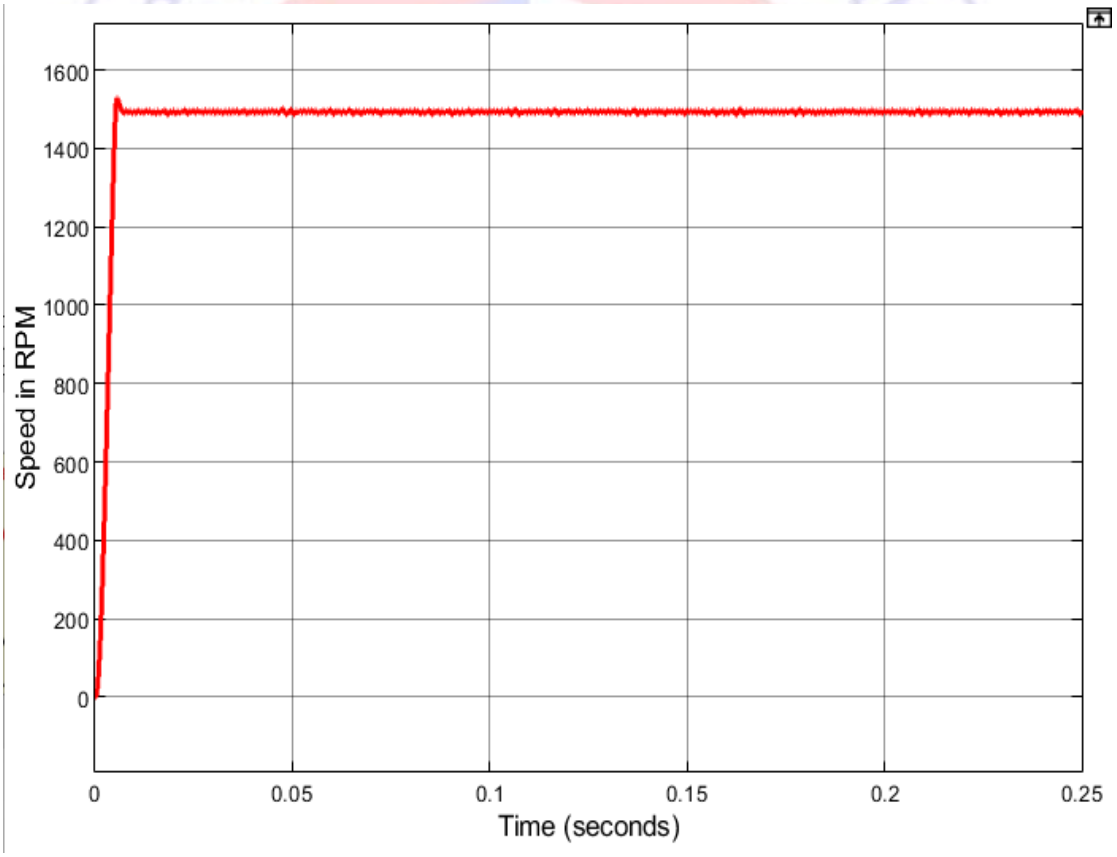

Figure 6.1 Speed Response of the FLC

Figure 6.2 depicts the stator currents, and Figure 6.3 represents the back emf of the motor. It is observed that the stator currents are quasi sinusoidal in nature and are displaced by 120 ° because BLDC motor uses six step commutation. The back emf waveforms confirms that the back emf is trapezoidal and are displaced by 120 °.

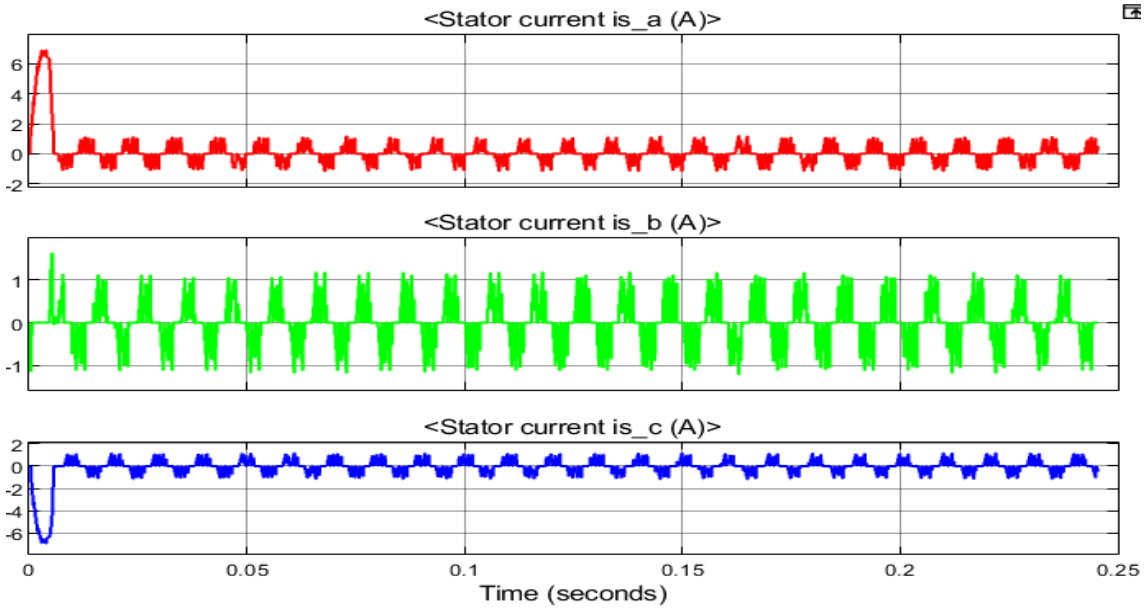

Figure 6.2 Stator Current Waveforms in MATLAB Simulink

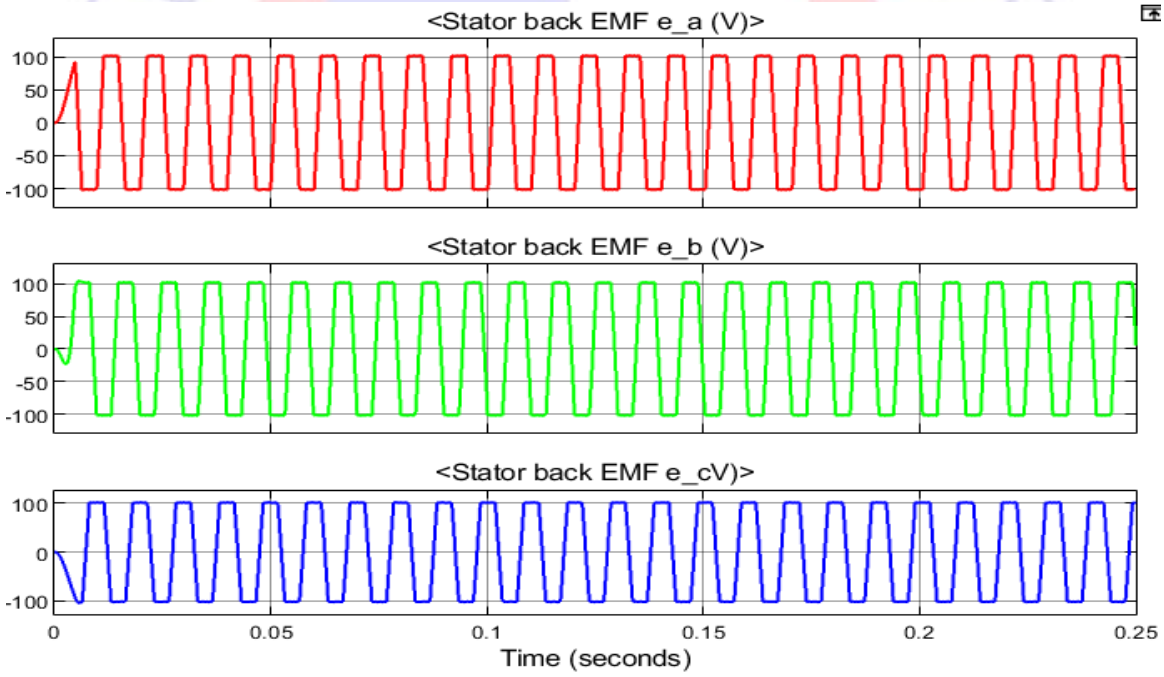

Figure 6.3 Back EMF Waveforms

Figure 6.4 represents the torque response of the BLDC motor with FLC. The torque of the motor reaches to 2.5Nm with a rise time of 292.644 ns with a overshoot of 0.385%. The motor torque reaches to the value of 0.7 Nm and settles at the same torque with the settling time of 0.035s.

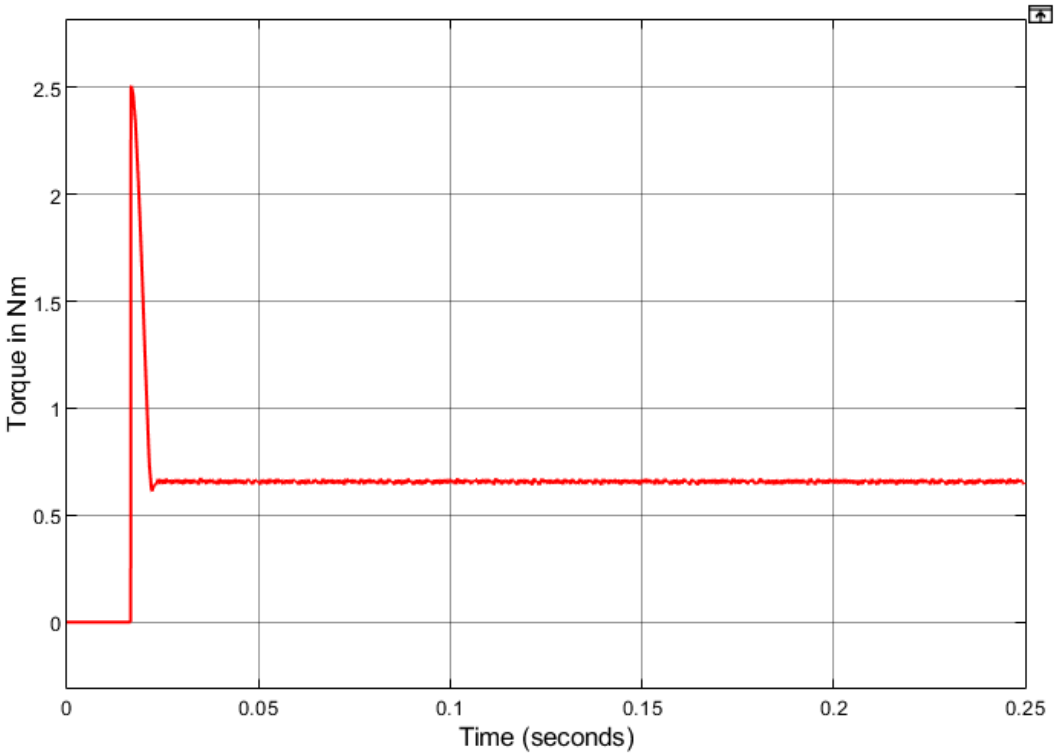

Figure 6.4 Torque Response of BLDC Motor

Figure 6.5 depicts the gating signals given to the inverter circuit obtained using the decoder and the commutation logic circuit. It is observed from the figure that the BLDC motor uses six-step commutation, and the inverter is operating in the 120˚ Conduction mode. From the figure it is observed that at any instant only two devices are conducting because each device conducts at only 120°.

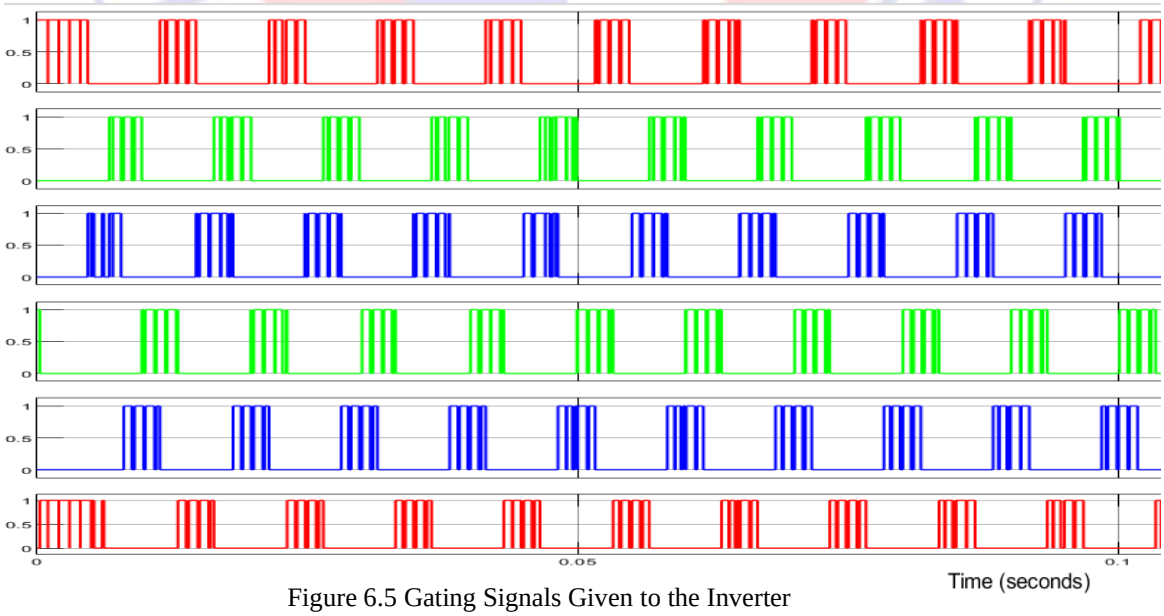

Figure 6.5 Gating Signals Given to the Inverter

To evaluate the performance of the designed controller for the continuous variation in the speed the simulation is done by giving the urban fleet Battery Electric Vehicle (BEV) drive cycle as the input reference speed. A drive cycle is a velocity time profile that reflects a particular type of vehicles driving characteristics in real world driving situation. The information used to create the simulated driving cycle is taken from the project Cross-border Mobility for Electric Vehicles (CROME).

Figure 6.6 represents the speed reference for the drive cycle of the urban fleet BEV for the time duration of 680seconds consisting of 7 micro trips. It is observed from the results shown in Figure 6.7 the speed response of the FLC follows the reference speed with the slight difference of 2 rpm to 15 rpm at different point of time.

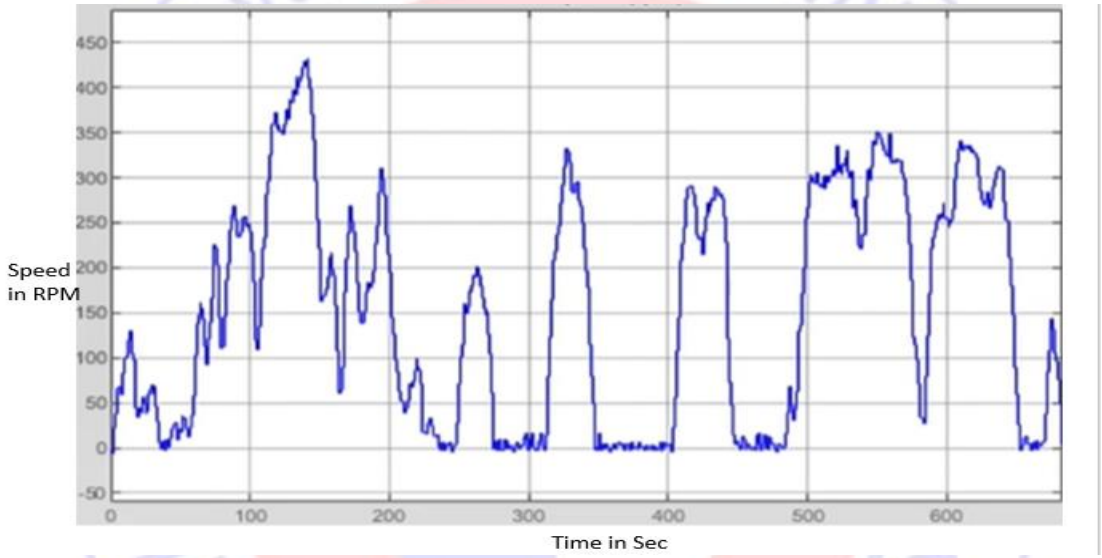

Figure 6.6 Speed Reference to the Controller

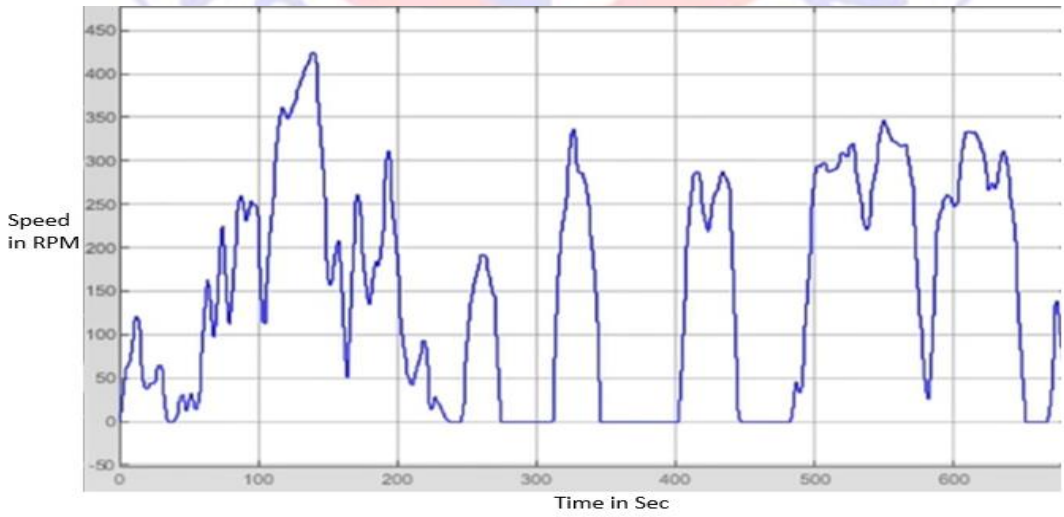

Figure 6.7 Speed Response of the Controller

6.2 Comparative Analysis

The performance of the FLC controller is compared with the conventional PI, PID controller. The speed response BLDC motor with a PI, PID, and FLC controller is shown in Figure 6.8. The PI controller is tuned with K_P =0.8, K_I= 0.02. PID controller gain values are K_P =0.0101, K_I =0.082, K_D =0.00026.

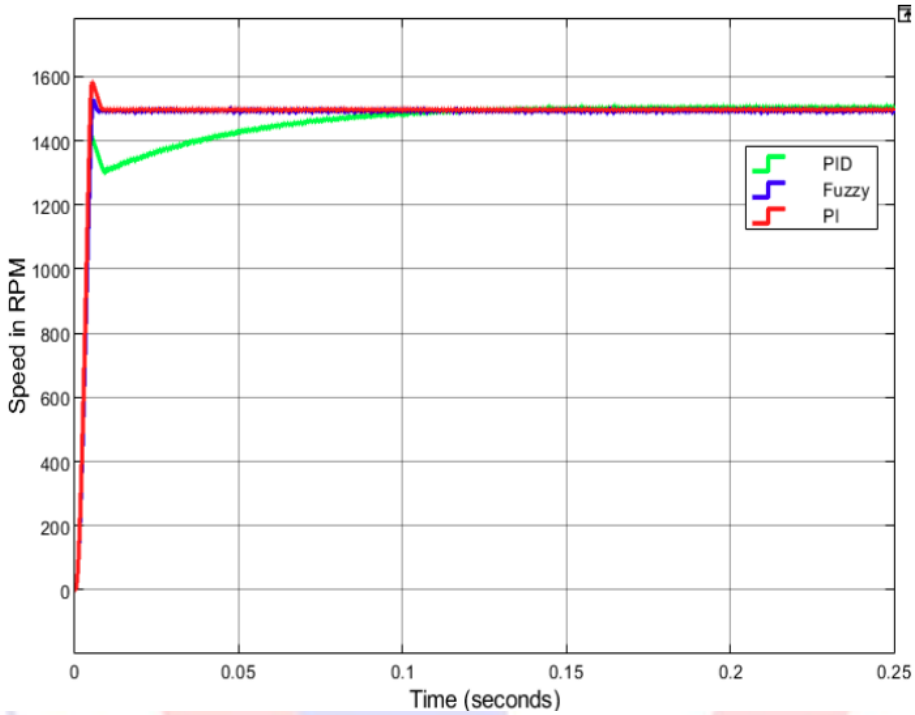

Figure 6.8 Speed Response of PI, PID and FLC

The motor reaches the speed of 1500 rpm in all considered controllers with different rising time, settling time and stability as indicated in Table 6.1.

Table 6.1 Comparison of Operating Conditions

Controller	Preshoot In %	Overshoot in %	Undershoot in %	Settling Time in ms	Rise Time in ms
PI	0.532	5.851	1.998	4.228	3.010
FLC	0.515	2.577	1.997	2.801	3.309
PID	0.505	-1.516	2.595	95.549	3.061

From the Table 6.1 it is observed that the FLC controller is better in terms of the overshoot, undershoot and the settling time but the PI controller gives the better result in terms of the rise time.

6.3 Hardware Results

The prototype of the FLC controller to control the speed of BLDC motor is implemented by using the Arduino UNO and the IR sensor for the closed loop operation. The speed response of the controller for different speed responses are tabulated in the Table 6.2.

Table 6.2 Speed Response of the Hardware Prototype

Reference Speed in RPM	Output Speed in RPM (Experimental)
3000	**3064**
3100	**3121**
3200	**3282**
3300	**3384**

From the Table 6.2 it is observed that the use of the IR sensor and the ESC for the closed loop operation as an alternative to the hall sensors and the inverter circuit resulted in some variation in the speed response of the implemented controller.

6.4 Summary

The simulation of the designed circuit is performed and the waveforms for the same are obtained. The designed component mounted on the PCB and the hardware implementation is carried out. The readings for the circuit are noted.

Chapter 7

CONCLUSION AND FUTURE SCOPE

According to a recent survey globally, the number of EVs sold are increasing gradually, indicating likeliness among people to buy and use EVs daily. The motor and motor controller are the two most crucial parts of electric vehicle power train. For an EV application, it is important to choose the appropriate electric motor and controller. The BLDC motor is used in this work due to the numerous benefits described in the literature.

There are various types of the control techniques available to the motor and these are mainly classified as Classical control techniques and Advance control technique. In classical control techniques, obtaining the solution of mathematical models is tedious and valid for linear systems only. In these systems, variations in setpoint and dynamic load conditions cannot be applied in controlling EVs efficiently, leading to its reduced performance. Therefore, here in this project the advanced control technique like FLC is adopted for the speed control of the BLDC motor to cater for the disadvantages of the classical controllers and to cater for the non-linear situations that arise in the real time.

7.1 Conclusion

- The simulation of the speed control of the BLDC motor using the FLC is simulated using the MATLAB Simulink software by utilising the Fuzzy Logic Toolbox. The simulation results obtained using the FLC is compared with the conventional PI, PID controller.
- The BLDC motor reaches its reference speed with the settling time and rise time of 2.801ms, 3.309ms and overshoot of 2.577% that is 4.228, 3.010 and 5.851% respectively in PI controller. Hence the fuzzy logic controller is better than the PI Controller in terms of overshoot and settling time, but the PI controller seems to be better in terms of the rise time.
- To know the performance of the FLC with the drive cycle the simulation is performed in the MATLAB Simulink by considering the fleet BEV urban drive cycle. From the results it is observed that the output speed follows the reference with a minute variation.

7.2 Future Scope

There is scope for future improvement of the FLC in controlling the speed of the BLDC motor. They are as listed below

- The performance can be further optimised by integrating the FLC and PI controllers or by using the neuro-fuzzy controllers.
- Speed Control using the sensor less technique can be combined with the advance control technique for increasing the performance and economy of the controller.
- The microcontroller can be further studied for controlling speed using DSP based or FPGA based or TI2000 controllers.

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APPENDIX A

BLDC Motor

A2212/13T TECHNICAL DATA

No. of Cells:	2 - 3 Li-Poly 6 - 10 NiCd/NiMH
Kv:	1000 RPM/V
Max Efficiency:	80%
Max Efficiency Current:	4 - 10A (>75%)
No Load Current:	0.5A @10V
Resistance:	0.090 ohms
Max Current:	13A for 60S
Max Watts:	150W
Weight:	52.7 g / 1.86 oz
Size:	28 mm dia x 28 mm bell length

LM7805

FAIRCHILD

September 2014

LM78XX / LM78XXA
3-Terminal 1 A Positive Voltage Regulator

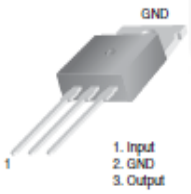
Features

- Output Current up to 1 A
- Output Voltages: 5, 6, 8, 9, 10, 12, 15, 18, 24 V
- Thermal Overload Protection
- Short-Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The LM78XX series of three-terminal positive regulators is available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down, and safe operating area protection. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed-voltage regulators, these devices can be used with external components for adjustable voltages and currents.

TO-220 (Single Gauge)



Ordering Information[1]

Product Number	Output Voltage Tolerance	Package	Operating Temperature	Packing Method
LM7805CT	±4%	TO-220 (Single Gauge)	-40°C to +125°C	Rail
LM7806CT				
LM7808CT				
LM7809CT				
LM7810CT				
LM7812CT				
LM7815CT				
LM7818CT				
LM7824CT				
LM7805ACT	±2%		0°C to +125°C	
LM7809ACT				
LM7810ACT				
LM7812ACT				
LM7815ACT				

Note:

1. Above output voltage tolerance is available at 25°C.

LM78XX / LM78XXA Rev. 1.3.1
www.fairchildsemi.com

Block Diagram

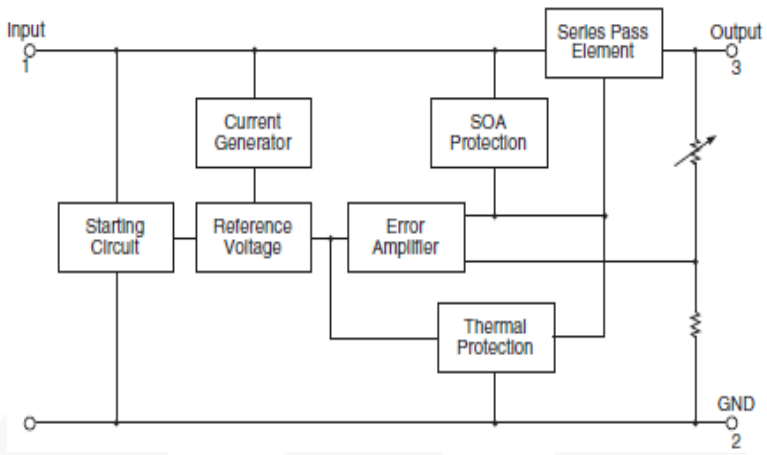


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

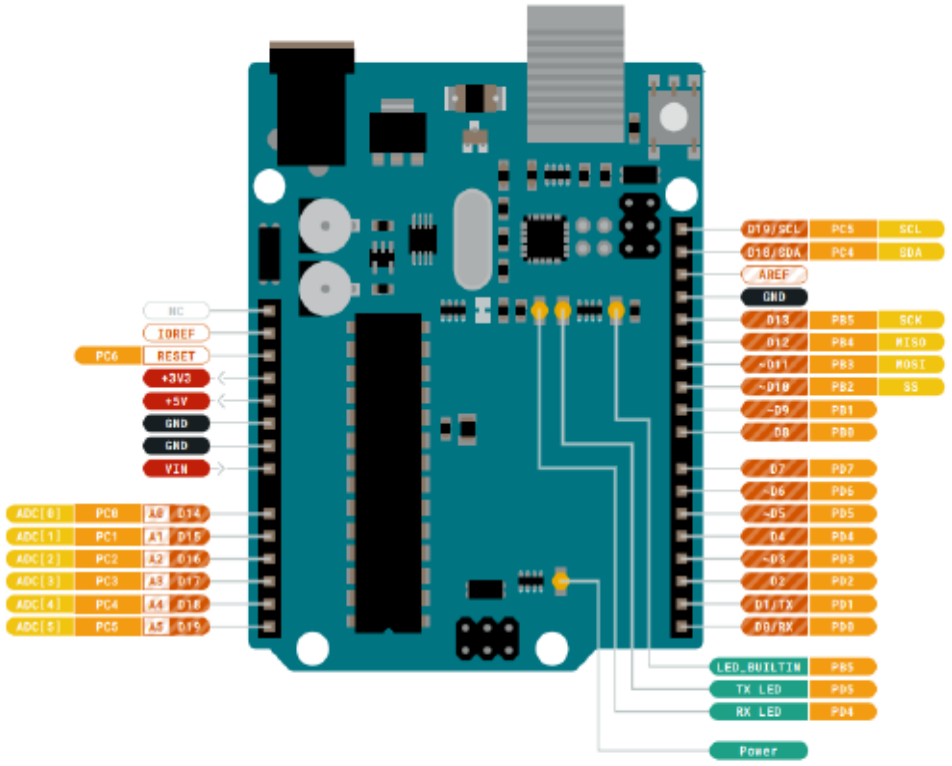
Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5 V to 18 V	35	V
		V_O = 24 V	40	
$R_{\theta JC}$	Thermal Resistance, Junction-Case (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		- 65 to +150	°C

Arduino UNO

4.6 Board Recovery

All Arduino boards have a built-in bootloader which allows flashing the board via USB. In case a sketch locks up the processor and the board is not reachable anymore via USB it is possible to enter bootloader mode by double-tapping the reset button right after power up.

5 Connector Pinouts



Pinout

5.1 JANALOG

Pin	Function	Type	Description
1	NC	NC	Not connected
2	IOREF	IOREF	Reference for digital logic V - connected to 5V
3	Reset	Reset	Reset
4	+3V3	Power	+3V3 Power Rail
5	+5V	Power	+5V Power Rail
6	GND	Power	Ground
7	GND	Power	Ground
8	VIN	Power	Voltage Input
9	A0	Analog/GPIO	Analog input 0 /GPIO
10	A1	Analog/GPIO	Analog input 1 /GPIO
11	A2	Analog/GPIO	Analog input 2 /GPIO
12	A3	Analog/GPIO	Analog input 3 /GPIO
13	A4/SDA	Analog input/I2C	Analog input 4/I2C Data line
14	A5/SCL	Analog input/I2C	Analog input 5/I2C Clock line

5.2 JDIGITAL

Pin	Function	Type	Description
1	D0	Digital/GPIO	Digital pin 0/GPIO
2	D1	Digital/GPIO	Digital pin 1/GPIO
3	D2	Digital/GPIO	Digital pin 2/GPIO
4	D3	Digital/GPIO	Digital pin 3/GPIO
5	D4	Digital/GPIO	Digital pin 4/GPIO
6	D5	Digital/GPIO	Digital pin 5/GPIO
7	D6	Digital/GPIO	Digital pin 6/GPIO
8	D7	Digital/GPIO	Digital pin 7/GPIO
9	D8	Digital/GPIO	Digital pin 8/GPIO
10	D9	Digital/GPIO	Digital pin 9/GPIO
11	SS	Digital	SPI Chip Select
12	MOSI	Digital	SPI1 Main Out Secondary In
13	MISO	Digital	SPI Main In Secondary Out
14	SCK	Digital	SPI serial clock output
15	GND	Power	Ground
16	AREF	Digital	Analog reference voltage
17	A4/SD4	Digital	Analog input 4/I2C Data line (duplicated)
18	A5/SD5	Digital	Analog input 5/I2C Clock line (duplicated)

Design and Implementation of Fuzzy Logic Controller for Speed Control of BLDC Motor
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OBJECTIVE
Project Methodology
Simulation Analysis and Hardware Implementation
Results and Discussion
Simulation Results
Hardware Results
Conclusion
Future Scope
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Closed Loop Control of BLDC Motor Using Fuzzy Logic Controller

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Abstract: The growth of human civilization in the twenty-first century is hampered by two key challenges: energy and the environment. In recent years, energy costs have continued to rise, volatility has become more severe, public opinion on environmental protection has risen, applicable rules and regulations are more stringent, and "energy conservation" and "emission reduction" has become an urgent practical concern. As a result, utilizing new technology to reduce energy consumption and emission has become an important direction of automobile technology development, with pure EVs achieving zero emissions and low energy consumption, there is no doubt that they have become one of the most appealing solutions for energy savings and emission reduction. Hence EVs have been identified as the automobile industry's key trend in recent years. Small size, easier speed control, noiseless operation, high specific power and reduced thermal losses of Brush Less DC(BLDC) motor compared to the induction motor makes it more feasible in automotive industries. Most industrial applications employ conventional controllers to regulate the speed of BLDC motors, although it produces poor results in non-linear situations. To cater for nonlinear situations, that arise in real time, modern control techniques including Artificial Intelligence (AI) and Fuzzy Logic (FL) are gaining importance and lot of research is being conducted. A rule- based FL controller seems to be a better approach for the control of BLDC motors for EV applications as it increases the performance of drive system by using linguistic variables. In this paper, the FLC, PI and PID controllers for BLDC motors are simulated using MATLAB/Simulink and the results obtained from them are being presented in a tabular format.

Index Terms **- Electric Vehicles, Fuzzy Logic Controller, Closed Loop Control, Classical controller, Rule base, Fuzzification, Defuzzification.**

I. INTRODUCTION

The two key issues in recent years are energy and the environment. The reserves of fossil fuels are rapidly depleting, while usage of fossil fuels is rapidly growing. This has resulted in the depletion of fossil fuels as well as an adverse impact on the ecosystem. The growing number of internal-combustion vehicles that utilize exhaustible conventional fuels has resulted in both energy and environmental problems. As a result, several nations have adopted EVs as alternatives to traditional vehicles in order to reduce dependency on oil and air pollution created by conventional automobiles. The selection of the appropriate electric motor is critical for electric vehicles. Various types of electric motors, such as DC motors, permanent magnet motors, induction motors, switched reluctance motors, and so on, have been used in electric vehicles.

Permanent Magnet Synchronous Motors (PMSM) and Permanent Magnet Brushless Direct Current Motors or also called as Brushless Direct Current Motors (BLDCM) are the two types of the Permanent Magnet motors. PMSM are the type of Permanent Magnet Motors with sinusoidal back EMF and the BLDCM are with the trapezoidal back EMF. The rotor of BLDM is made up of Permanent Magnet and the stator comprises of windings. Each phase of this motor is powered by the AC supply from the inverter which is fed from the DC supply. As the name stipulates the BLDC motors neither have brushes nor the commutators. The functionality of the brushes used in DC motors are replaced by the electronic control or a drive circuit to rotate the motor. These motors have various advantages like noiseless operation, longer life, better speed torque characteristics, higher speed range and hence used in many applications like automobile industries, home appliances, Aircraft, computers, robots and many more.

Despite many advantages the development of electronic control algorithm is convoluted as the commutation of the motor is depended on the rotor position. The two ways used to measure the rotor position are sensored and sensor less methods. Position sensors are used in the sensored method and usually the hall effect sensors are used to measure the position of rotors in many applications. In sensor less methods back EMF measurement, high frequency signal injection etc are used to sense the rotor position of the BLDC motor. Despite many advantages of sensor less technique it has many disadvantages like it is more complicated, consumes more computational time and requires processors with large amount of memory. Hence the sensor-based techniques are more preferable in the low speed and variable load conditions.

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The closed loop control techniques are broadly classified into conventional control techniques and advance control techniques. The classical controllers include the Proportional, Proportional Integral, Proportional Integral Derivative Controllers. Fuzzy Logic based Controllers (FLC), Artificial Neural Network based controllers (ANN), Fuzzy-ANN based controllers are few of the examples of advanced control techniques. This paper deals with the comparative study of the classical control techniques (PI, PID) with the advanced fuzzy logic-based control.

II. CLOSED LOOP SPEED CONTROL TECHNIQUES

In general terms control action of the system is depended on the output is known as closed loop control system. In closed loop speed control, the control action is depended on the output speed. In sensor based closed loop speed control, a sensor measures the speed of the motor persistently and is used as the feedback for control action. There are many advantages of closed loop control over the open loop control like robustness, reduces the sensitivity for the disturbances, stable, more accurate.

There are various types of closed loop control techniques available to generate the PWM pulses for inverter circuit to control the speed of the motor. They are broadly classified as Classical Control techniques and advanced control techniques.

2.1 Classical Control Techniques

Classical control techniques are the most fundamental methodology which uses Proportional(P), Proportional Integral (PI), Proportional Integral Derivative (PID) type of controllers. These are considered as the base of the control techniques. These controllers are considered as the industry's most basic controllers for controlling linear systems and are the foundation of control theory.

2.2 Advanced Control Techniques

The advance Control techniques include the category of controllers like intelligent controllers, predictive control, Fuzzy Logic Controllers (FLC) etc. To cater for nonlinear situations, that arise in real time, modern control techniques including Artificial Intelligence (AI) and Fuzzy Logic (FL) are gaining importance and lot of research is being conducted. A rule- based FL controller seems to be a better approach for the control of BLDC motors for EV applications as it increases the performance of drive system by using linguistic variables.

III. FUZZY LOGIC CONTROLLER

Fuzzy logic controller is a control system, suitable for implementation on systems operated with varying values. The advantage of the controller is in the use of linguistic variables so that in design it does not require complicated mathematical equations. Several other reasons are it is easy to use, ready to model nonlinear conditions. Fig.1 shows the structure of Fuzzy Logic Controller, and it consists of fuzzification, inference engine, rule base, and defuzzification processes

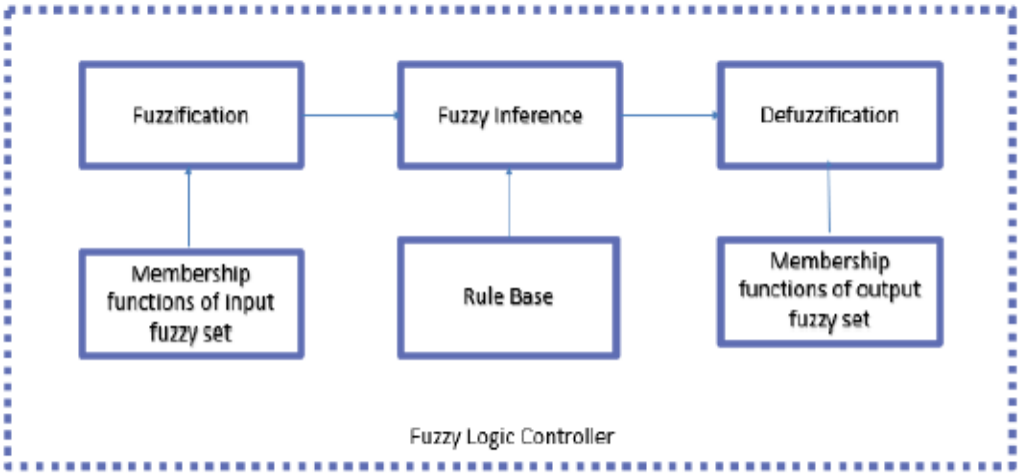

FIGURE1. BLOCK DIAGRAM OF FLC

3.1 Fuzzification

The fuzzification is the process of converting the crisp input values given to the controller into the fuzzy or the linguistic variables based on the membership functions. There are several types of membership functions like triangular, trapezoidal, gaussian etc.

3.2 Rule base

The rule base consists of the set of the rules required for the fuzzification process. The rule base is usually in the IF-THEN format. The rule evaluation is done based on the rule base and it is connected with the AND or OR operator.

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3.3 Inference Engine

The inference engine responsible of generating the fuzzy output by applying the inference rules to the fuzzy input. The inference rules, in particular, are used to evaluate linguistic values and map them to a fuzzy set, which requires defuzzification to be transformed into a crisp value. There are two types namely Mamdani method and Sugeno method. These rules can be based on prior experiences, observations, and expert knowledge. Each fuzzy inference rule is made up of two concepts: if-then statements and linguistic variables. The if-then rules include the antecedents and the consequence, where the antecedent is the verbal input and the consequence is the linguistic output depending on the input.

3.4 Defuzzification

The output of the inference system is in the form of fuzzy variables. To convert the fuzzy output into the defuzzified or the crisp output the defuzzification is required. Some of the types of defuzzification methods are Centroid method, weighted average method, height method etc.

IV. Methodology of Proposed Work

The methodology and flow of the proposed work is as shown in the Figure 2.

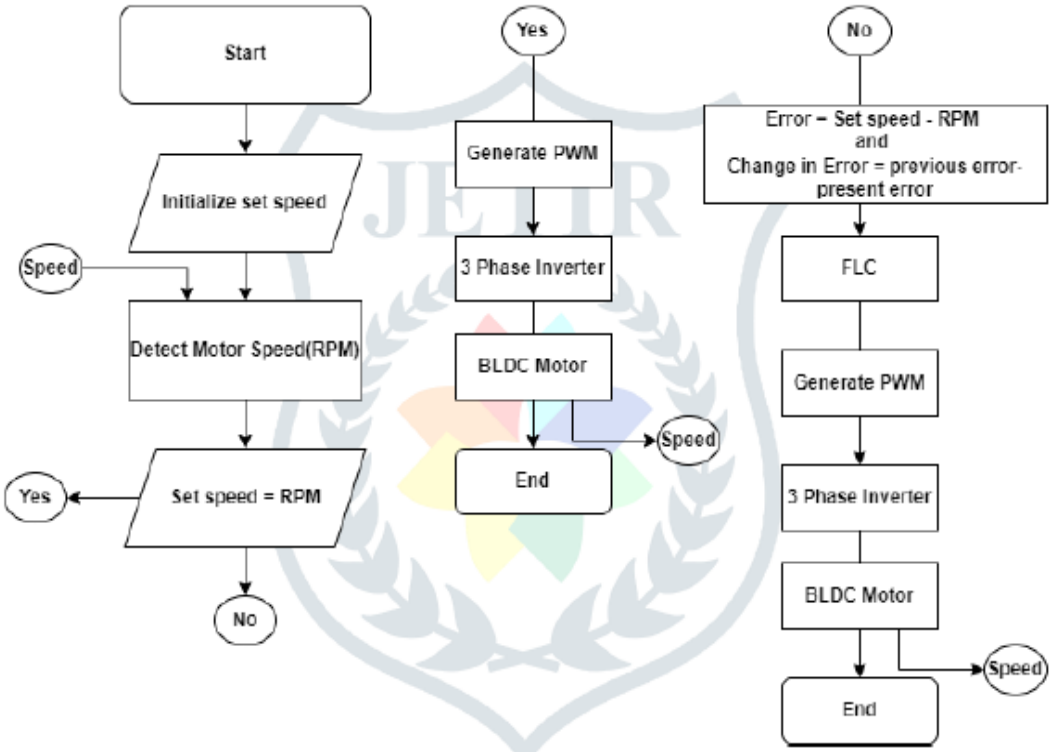

FIGURE 2. FLOW OF THE PROPOSED WORK

The project involves implementing a Fuzzy Logic Controller to regulate the speed of a BLDC motor. The BLDC motor's speed will be regulated by regulating the PWM pulses, which will control the power supplied to the motor. To begin, the required speed will be set. The sensor will determine the actual speed of the BLDC motor. For closed loop speed control, an intelligent fuzzy logic controller is used. If the actual and set speeds of the motor are the same, PWM pulses are generated and supplied to the 3-phase inverter for speed control.

If the actual speed and the motor's set speed differ, the error and change in error of the speed are computed and used as input to the FLC. The two inputs, error input and change in error, are considered to be triangle membership functions, each with seven membership values. In the fuzzification stage, these input values will be converted into linguistic variables or fuzzified values and sent into the inference engine. The values of error and change in error is calculated using the equation (1) and (2) respectively.

$$\text{Error (E)} = \text{Set Speed} - \text{Actual Speed} \quad (1)$$

$$\text{Change in error (CE)} = \text{Current error} - \text{Previous error} \quad (2)$$

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Here the Mamdani fuzzy inference system is used where the rule evaluation is done using AND operator. The rules are fired according to the IF-THEN rules combined with the AND operator. The rule base consisting of 49 rules are as shown in the Table 1.

TABLE 1. RULE BASE

Error/change in error	DNB	DNM	DNS	Z	DPS	DPM	DPB
NB	ONB	ONB	ONB	ONB	ONM	ONS	OZ
NM	ONB	ONB	ONB	ONM	ONS	OZ	OPS
NS	ONB	ONB	ONM	ONS	OZ	OPS	OPM
Z	ONB	ONM	ONS	OZ	OPS	OPM	OPB
PS	ONM	ONS	OZ	OPS	OPM	OPB	OPB
PM	ONS	OZ	OPS	OPM	OPB	OPB	OPB
PB	OZ	OPS	OPM	OPB	OPB	OPB	OPB

Next step after the Inference is Defuzzification. Here the obtained fuzzified value is converted back into the crisp value by using the weighted average method. The weighted average method is formulated using the equation (3).

$$z = \frac{\sum_{i=1}^{n}(\mu i * zi)}{\sum_{i=1}^{n} \mu i} \quad (3)$$

From all these processes the controlled output will be obtained from the fuzzy logic controller. This controlled and defuzzied output will be used for the PWM generation. This PWM will be given to the Inverter in order to obtain the supply voltage required to control the speed of the BLDC Motor.

V. SIMULATION AND RESULTS

Figure 3 shows the simulation model of the speed control of BLDC motor using the Fuzzy Logic Controller. To validate the effectiveness of the controller and to compare its performance with the conventional controllers, the speed control of BLDC motor with PI, PID and FLC controller is simulated using MATLAB SIMULINK. Table.2 shows the components values considered for BLDC motor model.

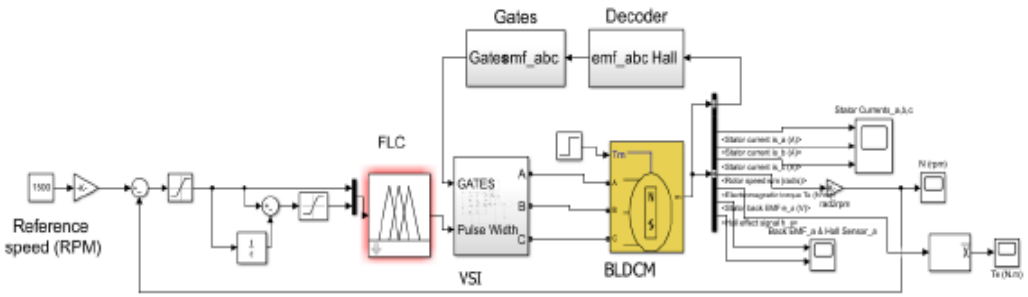

FIGURE 3. SIMULATION MODEL OF FLC

TABLE 2. PARAMETERS OF BLDC MOTOR MODEL

Parameter	Value
Stator Phase Resistance Rs	10.91
Stator Phase Inductance Ls	30.01e-3
Back EMF flat area in degrees	120
Inertia in kgm2	2 e-4
Viscous Damping	1e-3 N-m-s
Pole Pairs	4

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As illustrated in Figure 4, the fuzzy system has two input variables: error, change in error and one output variable with triangle membership function was chosen. Each universe of discourse is divided into seven fuzzy sets such as Negative big (NB), Negative medium (NM), Negative small (NS), Zero (Z), Positive small (PS), Positive medium (PM), Positive big (PB).

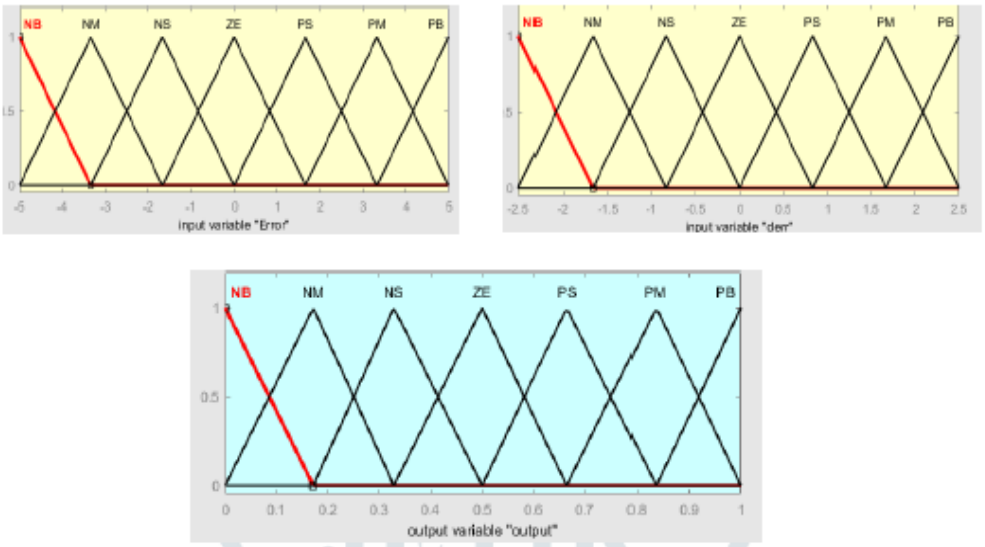

FIGURE 4. INPUT AND OUTPUT TRIANGULAR MEMBERSHIP FUNCTIONS

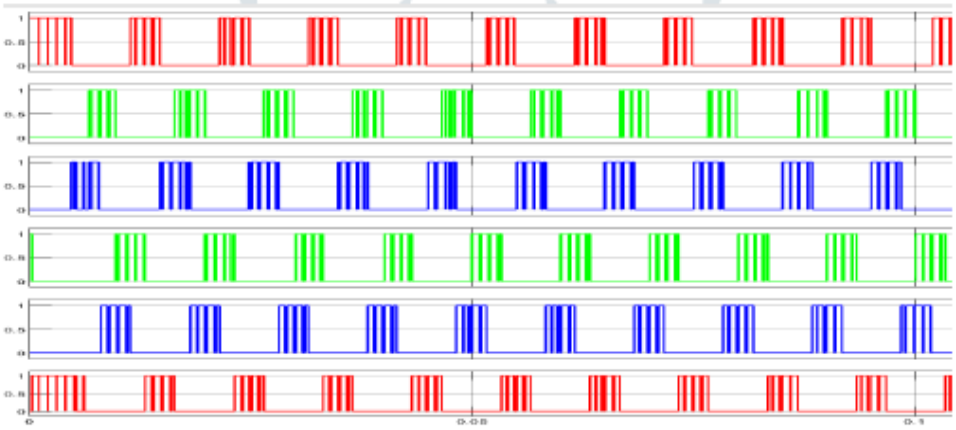

FIGURE 5. GATE SIGNALS

The Fig 7 and Figure 8 shows the stator currents and back emf of the motor. It is observed that the stator currents are quasi sinusoidal in shape and displaced by 120◦. The back EMF waveform depicts that it is displaced by 120◦ and of trapezoidal shape.

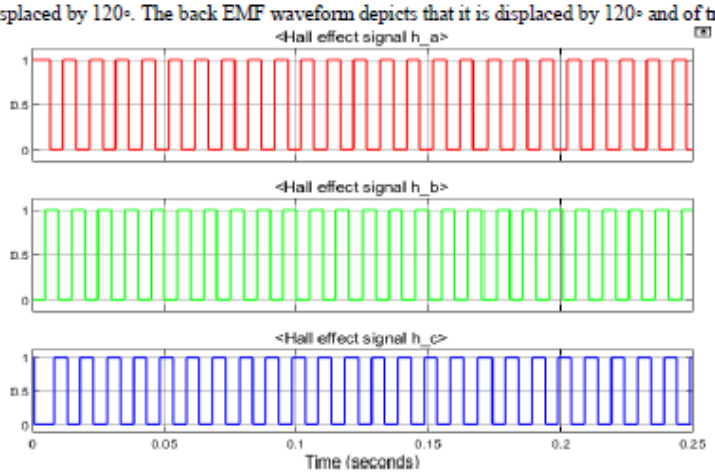

FIGURE 6. HALL EFFECT SENSOR OUTPUT

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The speed BLDC motor with a PI, PID, and FLC controller is shown in Figure 8. The PI controller is tuned with K_P =0.8, K_I= 0.02. PI controller gain values are K_P=0.0101, K_I =0.082, K_D =0.00026. In all circumstances, the motor achieves a speed of 1500 rpm, although with varying rising times, settling times, and stability.

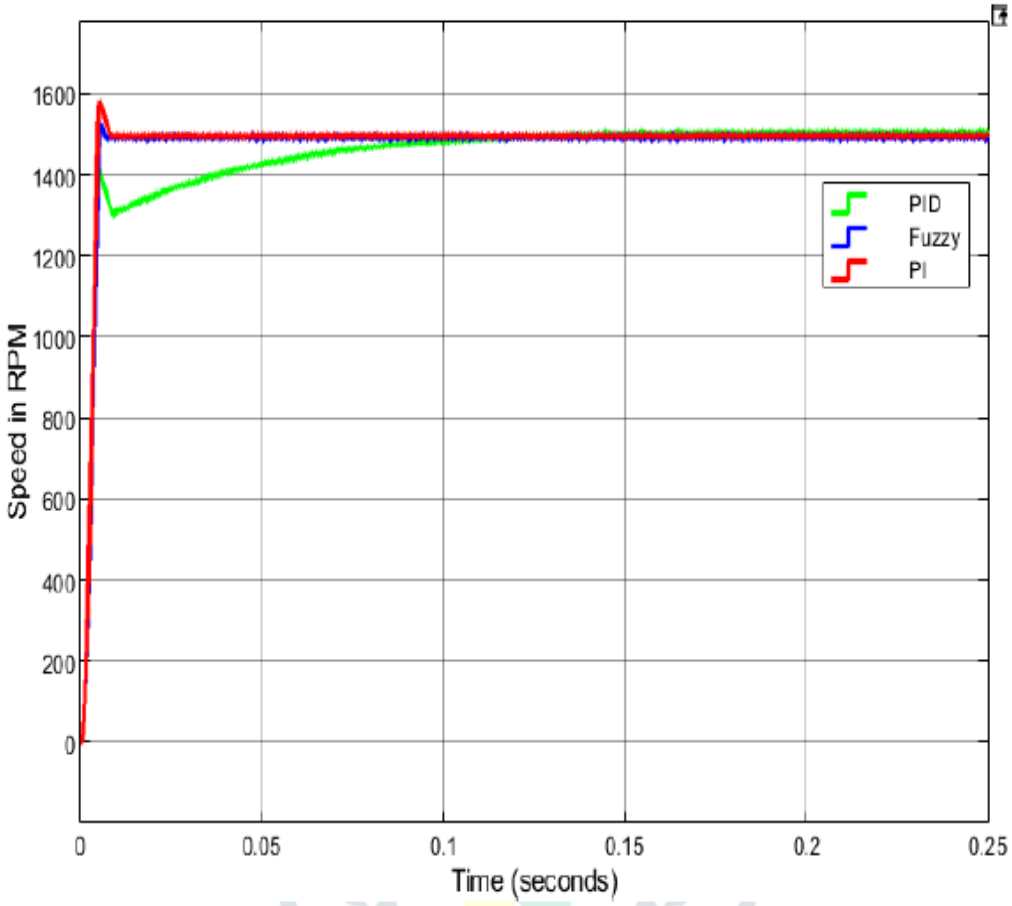

FIGURE 8. SPEED RESPONSE OF DIFFERENT CONTROLLERS

Table 3 shows the comparison of various operating conditions such as rise time, settling time, and overshoot percentage.

TABLE 3. COMPARISON OF VARIOUS OPERATING CONDITIONS OF THE CONTROLLERS

Controller	Preshoot In %	Overshoot in %	Undershoot in %	Settling Time in ms	Rise Time in ms
PI	0.532	5.851	1.998	4.228	3.010
FLC	0.515	2.577	1.997	2.801	3.309
PID	0.505	-1.516	2.595	95.549	3.061

VI. Conclusion

A Fuzzy Logic Controller based speed control of BLDC motor is presented in this paper. The results are compared with the conventional PI, PID controller. From the simulation results the BLDC motor reaches its reference speed with the settling time and rise time of 2.801ms, 3.309ms and a overshoot of 2.577% which is 4.228, 3.010 and 5.851% respectively in PI controller. Hence the fuzzy logic controller is better than the PI Controller in terms of Overshoot and settling time but the PI controller seems to be better in terms of the rise time. The performance in terms of overshoot and the settling time can be further increased by using hybrid PI-Fuzzy Controller.

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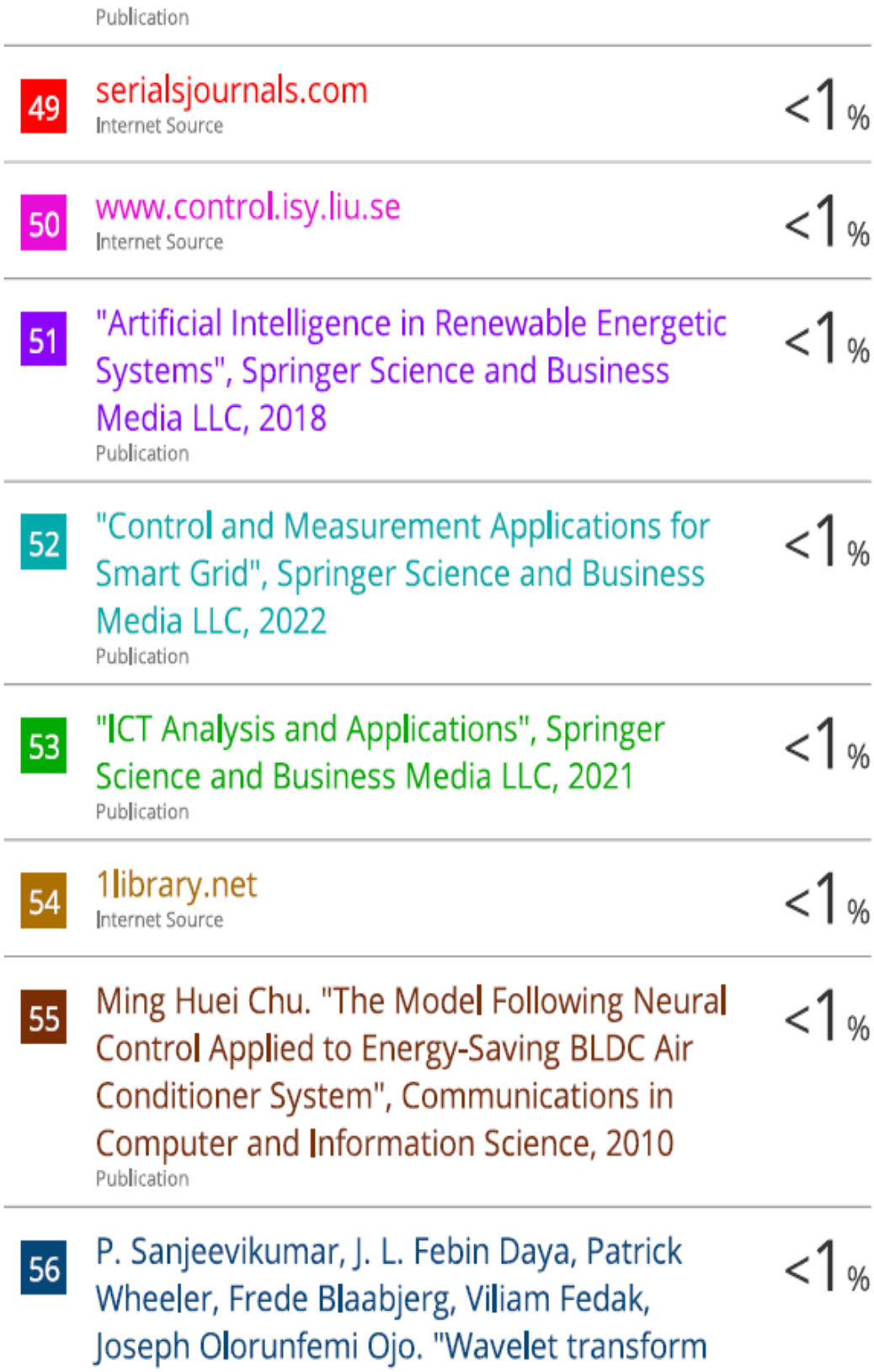
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Bengaluru– 560059

CERTIFICATE

Certified that the project work titled **"Design and Implementation of BLDC Drive for Single Knee Joint Active Exoskeleton"** carried out by **Sanjan P S, USN: 1RV20EPE12** a bonafide student, submitted in partial fulfilment for the award of **Master of Technology** in **Power Electronics** of **RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi,** during the year **2021-22.** It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

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Name of the Examiners	**Signature with Date**
1. _____	_____
2. _____	_____

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DECLARATION

I, Sanjan P S, student of fourth semester M.Tech in Power Electronics, Department of Electrical and Electronics, RV College of Engineering®, Bengaluru, declare that the project titled **Design and Implementation of BLDC Drive for Single Knee Joint Active Exoskeleton,** has been carried out by me. It has been submitted in partial fulfilment for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

Date of Submission: 18/07/2022 **Signature of the Student**

Student Name: Sanjan P S

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TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Mr. Sanjan P S [USN:1RV20EPE12]**, student of R V College of Engineering, Bangalore, has completed the project work entitled "**Design and Implementation of BLDC Drive For Single Knee Joint Active Exoskeleton**" in partial fulfilment for the award of **Master of Technology in Power Electronics** during the time period 2021-2022 under the guidance of **Mr. Udayashankar B K** (Co-founder, CTO – Embedded Systems & Power Electronics)

During the period his conduct was good.

We wish good luck and success in his future endeavours.

For Dvizira Private Limited

Dvizira Private Limited Mysuru

Punithraj R
Executive Director
Dvizira Private Limited

ACKNOWLEDGEMENT

Any achievement, be it scholastic or otherwise does not depend solely on the individual efforts but on the guidance, encouragement and cooperation of intellectuals, elders and friends. A number of personalities, in their own capacities have helped me in carrying out this project titled, "**Design and Implementation of BLDC Drive for Single Knee Joint Active Exoskeleton**". I would like to take this opportunity to thank them all.

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ABSTRACT

Exoskeletons are robotic extensions of a user primarily intended for performance augmentation and aid with human movement. They are complex systems that have to work in sync with the user. Active exoskeletons make use of actuators for power amplification or offsetting the effort of the user to improve endurance. Electric actuators such as BLDC motors are commonly used in this application due to their compactness and high-power density. The overall performance of the exoskeleton that make use of BLDC motors eventually depends on the type of drive scheme used. For high performance applications that demand accurate speed and position control, Field Oriented Control (FOC) scheme is best suited. A robust BLDC drive capable of speed and position control is crucial considering the safety of the user, as inaccuracies are known to cause fatigue, injuries or long-term health issues.

The work was aimed at design and implementation of speed and position control of BLDC motor using FOC scheme. The simulation model is designed using three cascaded control loops. The outer most loop is responsible for maintaining position, followed by speed control loop and finally the current control loop. A scaled down hardware prototype was designed based on open source FOC firmware implemented on a STM32F446RE and based on TI's DRV8323RS smart gate driver IC. An Arduino Uno performs the function of the main controller by sending the speed and position commands to the drive via the Controller Area Network (CAN) protocol. A CAN bus development board is used along with the Arduino for CAN capabilities and a MCP2542 CAN transceiver at the drive end to convert the differential CAN bus to the CAN protocol suitable for microcontroller. A commercially off-the-shelf BLDC motor is used along with 1:6 speed reduction. The whole system was powered by a 12V battery.

Simulation of speed and position control of BLDC motor using FOC was performed using Simulink. The proposed model is able to track the reference positions commanded without overshoots, no steady state error and is capable of reaching the set position within 0.5 seconds. The hardware implementation of the proposed BLDC drive was tested by commanding positions 4π radians and -4π radians as target positions consecutively. The drive was capable of maintaining the positional accuracy as desired by maintaining the error close to 1% at both commanded positions as desired. Motor stall test was conducted to check the behaviour of the controller and validate the functioning of the software based current limiter causing an unexpected failure of the drive due to a malfunction. A detailed root cause analysis revealed an anomaly in the high side gate signal of phase A causing the drive to malfunction.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Sanjan P S, Madhu B R, "Comparative Analysis of Speed and Position Control of BLDC Motor via Field Oriented Control using SPWM and SVPWM Schemes", In International Research Journal of Engineering and Technology (IRJET), pp. 3317-3323 Vol. No. 9, Issue No.6. June 2022

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GLOSSARY

ADC	:	Analog to Digital Converter
BLDC	:	Brushless DC Motor
CAN	:	Controller Area Network
DOF	:	Degree of Freedom
DSP	:	Digital Signal Processor
dq	:	Direct Quadrature
FOC	:	Field Oriented Control
IC	:	Integrated Circuit
PWM	:	Pulse Width Modulation
SPI	:	Serial Peripheral Interface
SVPWM	:	Space Vector Pulse Width Modulation

Chapter 1

INTRODUCTION

Exoskeletons are extensions of human that work in sync with the user to amplify the physical performance and perform tasks such as running, walking, load carrying and other movements with ease. In recent years, the research on exoskeletons is mainly carried out in the medical field for rehabilitation/recovery purposes and in military for performance augmentation. Active exoskeleton makes use of actuators to aid with the movement. The actuator requires a precise controller to be in sync with the user. One of the actuators that are commonly used in compact, lightweight and robust designs are Brushless DC (BLDC) motors that have desirable characteristics such as high power/torque density, high efficiency and low maintenance [1]-[2].

An active exoskeleton primarily consists of two different control loops – the main control loop determines the speed and position required to carry out the next movement and the actuator control loop takes this speed and position commands from the main controller to drive the actuator appropriately to complete the desired movement. Techniques such as Field Oriented Control (FOC) is required for high performance and accurate control of BLDC motor. The FOC scheme is a clever three phase motor control technique that converts the time variant three-phase quantities to time invariant direct quadrature/dq-reference frame that provides a control structure similar to DC motor controller. Also, the time-invariant nature allows for superior dynamic performance (acceleration and deceleration), maximum torque from zero speed and precise speed control through the entire speed range [3]-[4].

Implementation of FOC involves a high-speed Digital Signal Processor (DSP) processor to perform the mathematical transformations and control loop computations, encoder for rotor position feedback, a communication protocol to receive commands and send telemetry information, current sensing to measure phase currents, a three-phase inverter and gate drivers to control the inverter. For speed and position control, the entire motor controller involves three different control loops. The first control loop consists of position control that measures the actual position and reference position to compute the output for the speed control loop. This is finally followed by the current control loop. Space Vector Pulse Width Modulation (SVPWM) technique is used in conjunction with FOC scheme to generate the gate drive signals for the inverter. Advancements in technology have resulted in multifunctional smart Integrated Circuits (ICs) that reduce the load on the DSP and reduce design complexity [5]-[6].

1.1. Overview

An active exoskeleton is a complex system involving various sensors, sophisticated controllers and actuators. This thesis mainly focuses on the controller for the actuator, therefore, for the validation prototype, a single knee joint exoskeleton system is considered. The movement of knee joint is a one Degree of Freedom (DOF) movement, a rotation of one joint against a fixed axis providing a good base for the validation. This actuator system requires speed and position commands to carry out further computation. In robotics, one such communication protocol employed is the Controller Area Network (CAN) protocol. It is also used in automobiles to communicate between various controllers, modules and sensors [7]-[8].

In an active exoskeleton that employs CAN protocol, multiple actuator controllers are connected to the CAN bus. The operation of an actuator controller is as follows – The speed and position parameters are commanded to the motor controller via CAN bus. The microcontroller processes the data to obtain the reference parameters. The DSP runs the FOC algorithm to computes the final torque (in turn current) required to meet the reference commands. The onboard Analog to Digital Converter (ADC) measures the actual phase current via shunt resistors (via appropriate pre-conditioning). The rotor position is measured by an encoder. Appropriate PWM signals are generated and fed to the gate driver IC that controls the MOSFETs in turn driving the BLDC motor. The telemetry is passed on to the CAN bus.

Due to various constraints such as supply chain issues and semiconductor shortage crisis, a scaled down prototype to serve as a validation/proof-of-concept is shown in this study. Modern advancements in gate driver technology as introduced a new era of smart gate driver solutions, reducing the complexity of the design by combining current shunt amplifiers, DC-DC converters and PWM modes in one small package [9].

1.2. Specific Details

The hardware implementation of the FOC based speed and position control of BLDC motor is based on the DRV8323RS Smart Gate Driver IC. In one small package it contains three half-bridge gate drivers, four PWM modes, DC-DC buck converter controller, protection and current shunt amplifiers with configurable gain. The configuration is carried out via SPI. In the prototype, the DRV8323RS Development Board is used with onboard three phase inverter comprising of three CSD88584Q5DC half-bridge power blocks and 7mΩ current shunt resistors.

A commercially available off the shelf DYS D3548-6 BLDC motor rated at 790KV (~790 RPM/V) commonly used in low RPM, large propeller drones is chosen. This BLDC motor offers high power density, the manufacturer claims a maximum output power of 717W with a small form factor of 35mmx48mm frame and weighs 180g.

A STM32F446RE DSP processor is used as the brain of the motor controller, an open source FOC based algorithm with certain modification is implemented in the processor. MA700 absolute angular position sensor provides the DSP with the rotor position via Serial Peripheral Interface (SPI). MCP2542 CAN transceiver interfaces between the differential CAN bus and the DSP. To send speed and positional commands, an ATmega328 microcontroller along with a CAN bus shield comprising of the MCP2551 transceiver and the MCP2515 CAN controller IC is utilized.

1.3. Literature Review

Exoskeletons is a broad area of research, it is classified on the basis of the body part it focuses on, the action (passive or active), the type of technology powering it and purpose. Military and medical are the two most common areas of application. A general characterization of exoskeletons is carried out for a standardized breakdown structure. In recent times, the field of exoskeletons is an expanding area of research [1]-[2]. Electric actuators such as BLDC motors are preferred for exoskeleton application and requires a supporting robust speed and position control scheme for control. FOC scheme is best suited for such high-performance applications [3]-[5].

The design and implementation of low-cost actuators for robotics application using custom made BLDC motors and drivers is presented in [6]. The open-source design promotes the flexibility of the proposed actuators and allows easy extension into various applications. An active exoskeleton is a complex system, knee joint exoskeleton provides a solid foundation for validation studies. Also, the study touches on interesting aspects of human anatomy [7]-[8]. FOC scheme requires high processing power and implementation complexity. Advancements in power electronics technology as resulted in smart gate driver solutions to reduce design complexity [9]. The foundation of FOC scheme relies on Mathematical transformations of Clarke, Park and their respective inverse transforms. The transformation aid in converting the complex three-phase time variant system to DC quantities that are time invariant [10]-[11]. Alongside FOC scheme, SVPWM technique is utilized to extract maximum performance from the motors by controlling the revolving reference vector, the magnitude and frequency of fundamental component is controlled.

The SVPWM is a superior PWM technique providing better utilization of DC bus, low harmonics at output and accurate in reproduction of reference voltage [12]-[18].

Algorithm for reducing the position error of high rotational speed BLDC motors is presented in [19]. The overall improvement in dynamic performance of FOC based speed and position control of BLDC motor and reduction of ripple in torque is carried out using high order sliding mode observer [20]. Novel control schemes are proposed in literature for performance improvement of control technique such as positive current reference generation, hardware in the loop-based simulator for real time control scheme testing, fuzzy logic-based control scheme for improved regenerative braking, variable sampling controller, particle swarm optimization-based PI controller optimization, neural network based indirect position detection [21]-[27]. Apart from control systems, new topologies such as six wire three phase topology and PFC based topologies are proposed [28]-[30]. The design and modelling of FOC scheme-based BLDC drive for various applications is discussed in detail with hardware implementation [31]-[37].

1.4. Problem Definition

The development and implementation of accurate position and speed control of BLDC motor is important for an active exoskeleton as the overall performance is dependent on it. Realization of high performance of motor drive involves FOC control scheme and is a challenge due its complexity, although recent advancements in power electronics technology help reduce the complexity, such as the aforementioned DRV8323RS Smart Gate Driver IC by Texas Instruments.

Using the DRV8323RS development board, the goal is to design and implement an accurate speed and position control of a BLDC motor using sensored FOC scheme for a scaled down mock-up of a single knee joint exoskeleton prototype as a proof of concept/validation model and serve as a foundational development study for upcoming iterations.

1.5. Objectives

The main objectives of the project are -

- To simulate speed and position control of BLDC motor via FOC using Simulink.
- To design and implement small scale prototype of the single knee joint exoskeleton actuator assembly.
- To design and implement the hardware prototype of the BLDC drive using the DRV8323 development board employing the FOC scheme.

- Validate performance of the BLDC drive and conduct behaviour analysis of the controller under motor stall condition by conducting root cause analysis to identify the cause of failure.

1.6. Motivation

The main motivation of the project is to indigenously develop a high-performance drive for an active exoskeleton eventually. Some of the factors that led to this project are listed below –

- **Military Logistics -** Logistics plays a major role in the military, soldiers often have to carry/lift heavy loads and walk/climb over rough terrains. This takes a toll on their performance and health on the long run. Exoskeletons are one of the solutions the Indian armed forces and various other armed forces are actively looking at for their logistics requirement. Overall, it helps improves the strength, endurance, reduce fatigue and avoid the chances of stress and pressure related injuries from occurring.
- **The Market –** The exoskeleton market is currently valued at $499 million and is projected to reach $3340 million by 2026, by indigenously developing components for the exoskeleton and developing an entire exoskeleton at this time is an attractive prospect.
- **Shortcomings with drive system** – An active exoskeleton needs to be in sync with the human wearing it, any delays or errors in actuation can make the exoskeleton feel clumsy, inhibit the wearer's movement, cause injuries or make it uncomfortable for the wearer over continuous long duration usage

1.7. Organization of the Report

The project work is organized in seven chapters.

Chapter-1 consists of literature survey carried out to understand the topic of exoskeletons and high-performance BLDC motor drivers based on FOC scheme. It includes the problem definition, objectives of the project motivation behind carrying out this project and the methodology.

Chapter-2 followed by basics of active exoskeleton, the operation of speed and position control of BLDC motor using FOC scheme, mathematical transformations involved and SVPWM are discussed.

Chapter-3 consists of the proposed converter Block diagram with explanation of working and Methodology.

Chapter-4 presents the design details of the BLDC drive.

Chapter-5 describes simulation of the proposed drive unit and hardware implementation of the circuit.

Chapter-6 discusses the simulation and hardware result of the proposed drive unit

Chapter-7 includes the overall conclusion drawn from the project and the future works that can be carried out.

Chapter 2

ACTIVE EXOSKELETON AND FOC SCHEME OF BLDC DRIVE

This chapter discusses the concepts of active exoskeleton and the working principle of the FOC scheme. The mathematical transformations and the operational flow of the FOC scheme are explained.

2.1. Active Exoskeleton

Exoskeletons is a broad term as shown by the detailed classification represented in Fig. 2.1. An active exoskeleton is a wearable robotic structure that works in sync with the user to augment performance and increase endurance. It uses a system of actuators to aid with movement and there are many types of actuators such as electric motors, hydraulic and pneumatic actuators. Hydraulic and pneumatic solutions are quite bulky as the supporting components and reservoirs take up a large space and usually are heavy. Often multiple conversions are involved, for example, in a pneumatic system, a battery runs the compressor to pressurise the air tanks and via valves, pneumatic cylinders are controlled. Energy is wasted at each conversion from one form of storage to another. As a result, various active exoskeleton implementation uses electric motors, especially BLDC or PMSM motors as they are compact, lightweight, high-power density, high efficiency and high torque [1]-[2].

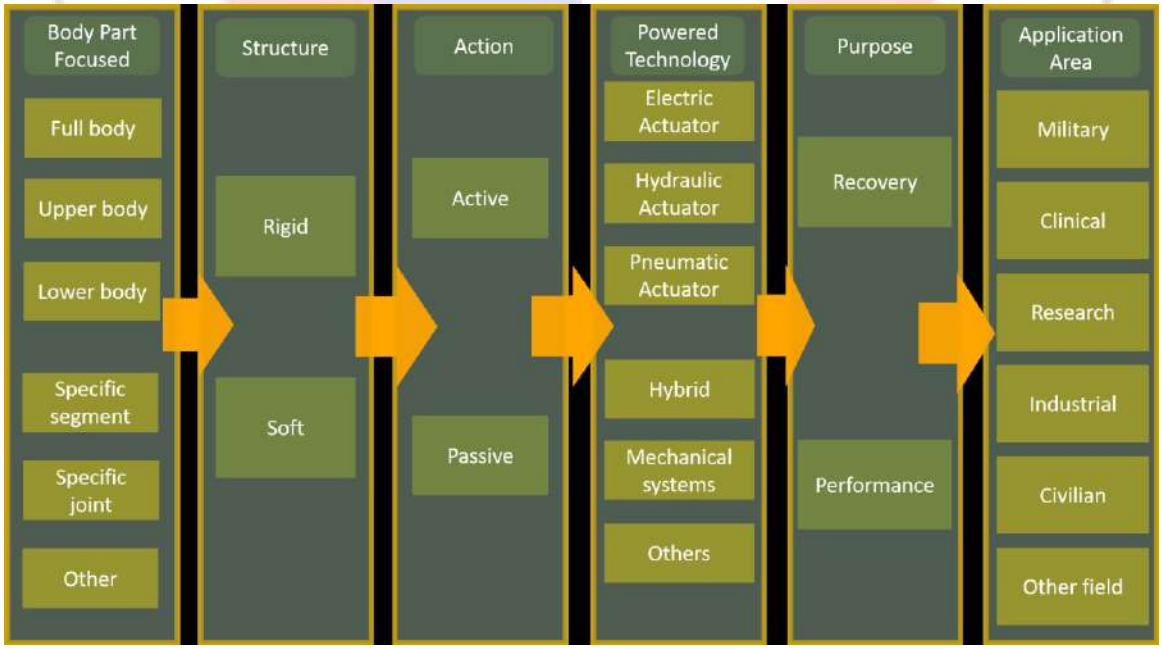

Fig. 2.1. Classification of Exoskeleton [1]

Active exoskeleton contains a suite of sensors that determine the intention of the user, a complex control system that as to determine the user's movement profile, maintain stability of the structure. The thesis focuses on transforming the output of that control system into desired movement by controlling the motor. In a robotic application, such as the active exoskeleton, movement of any joint to a desired position, involves speed and position parameters. An example of a commercial exoskeleton is shown in Fig. 2.2. This is Lockheed's Onyx lower-body exoskeleton designed for military applications. The electric motor-based drive is seen imposed on the knee joint (the circular assembly). The control of this motor plays a crucial role in its performance. A dedicated actuator for Exoskeleton application is seen in Fig. 2.3., a solution developed by Maxon. It is an integrated motor drive with position controller, high resolution encoder and CAN interface. An internal view of this integrated motor drive is seen in Fig. 2.4.

Fig. 2.2. Lockheed Martin's Onyx Exoskeleton (Courtesy – Lockheed Martin)

Fig. 2.3. BLDC Based Actuator for Exoskeleton by Maxon (Courtesy – Maxon)

Fig. 2.4. Inside View of the BLDC Based Actuator for Exoskeleton by Maxon (Courtesy – Motion Control Tips)

2.2. Model of a BLDC Motor

A system of BLDC motor and three-phase inverter powered by DC source as shown in Fig. 2.5 is considered. The three-phase motor is star connected and assuming a balanced three phase system [12], then the phase voltage is given by equations (2.1) - (2.3),

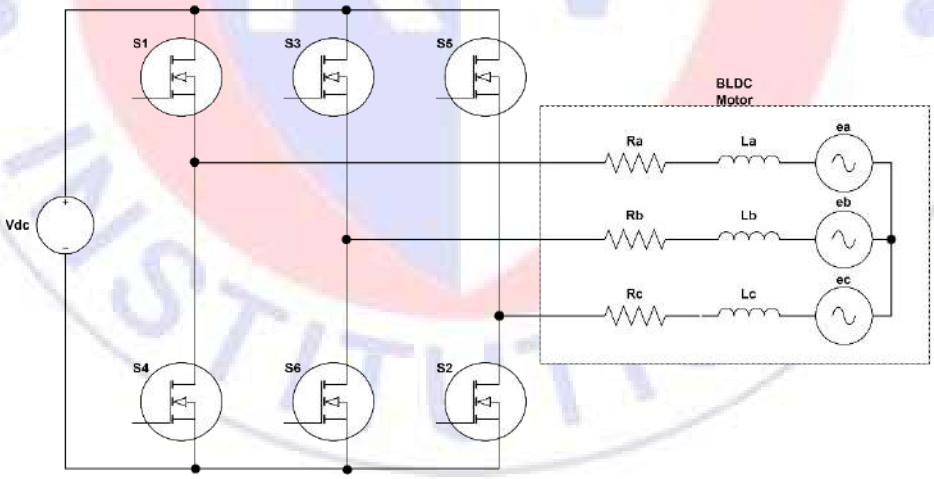

Fig. 2.5. Equivalent Circuit of BLDC Motor

$$V_a = RI_a + (L - M)\frac{dI_a}{dt} + e_a \tag{2.1}$$

$$V_b = RI_b + (L - M)\frac{dI_b}{dt} + e_b \tag{2.2}$$

$$V_c = RI_c + (L - M)\frac{dI_c}{dt} + e_c \tag{2.3}$$

In equation (2.1-2.3),

V_a, V_b, V_c = phase voltages

R = Armature resistance

L = Armature self-inductance

M = Mutual inductance

i_a, i_b, i_c = phase current

e_a, e_b, e_c = motor back emf

The back emf of the motor is written as shown in (2.4) – (2.6)

$$e_a = K_w f(\theta_e)\omega \tag{2.4}$$

$$e_b = K_w f(\theta_e - \frac{2\pi}{3})\omega \tag{2.5}$$

$$e_c = K_w f(\theta_e + \frac{2\pi}{3})\omega \tag{2.6}$$

The electrical angle, $\theta_e = (P/2)\,\theta_m$, where θ_m is the mechanical angle of the rotor and P are the number of pole pairs. The function given by f in (2.7) gives the back emf that is trapezoidal in nature for phase A of the motor. Kw is the back emf constant and ω is the rotor speed.

$$f = \begin{cases} 1 & 0 \le \theta_e \le \frac{2\pi}{3} \\ 1 - \frac{6}{\pi}(\theta_e - \frac{2\pi}{3}) & \frac{2\pi}{3} \le \theta_e \le \pi \\ -1 & \pi \le \theta_e \le \frac{5\pi}{3} \\ -1 - \frac{6}{\pi}(\theta_e - \frac{5\pi}{3}) & \frac{5\pi}{3} \le \theta_e \le 2\pi \end{cases} \tag{2.7}$$

The electromagnetic torque in both electrical form and mechanical form is given in (2.8) and (2.9) respectively.

$$T_{em} = \frac{1}{\omega}(e_a i_a + e_b i_b + e_c i_c) \tag{2.8}$$

$$T_e = J\frac{d\omega}{dt} + B\omega + T_L \tag{2.9}$$

In this,

P = Number of pole pairs

TL = Load Torque

J = Moment of Inertia

B = Friction Constant

2.3. FOC Based BLDC Drive

A BLDC motor consists of stator windings in 3-phase configuration, placed 120 ^{o} apart. The vector sum of force generated by three phases determines the motor rotation. The magnetic field of the rotor generated from the permanent magnets attached to it interacts with the stator magnetic field to generate force. Depending on the sequence the coils are driven, it can either generate rotational torque or not generate rotational torque. There are two different types of forces acting on the rotor, quadrature component running perpendicular to pole axis of rotor responsible for producing the torque and the direct component running in line to the pole axis that does not generate any force. The scheme employs techniques to maximise the quadrature component and reduce the direct component to get maximum useful torque, utilising maximum power only to feed the useful components, as a result high performance with high efficiency is achieved. In order to determine the direction of magnetic field, sensors/encoders are employed to determine the rotor position [16].

A general speed and position control of BLDC motor employing FOC scheme uses three cascaded control loops as shown in Fig. 2.6. The power side of the motor driver involves the DC power supply connected to a three-phase inverter that converts DC to three-phase currents required to drive the BLDC motor. The control side of the motor driver makes use of transformations called Clarke's transformation and Park's transformation. The transformations play a crucial role as describing the behaviour of three-phase machine using their respective current and voltage equations tend to make the mathematical modelling of the system complex as the system is time variant. To describe such complex three-phase machines and perform analysis, mathematical transformations are used to decouple the variables (making them time invariant) by referring the three phase quantities to a common frame of reference. The first control loop is the position control loop, reference position is compared with actual reference to calculate position error and is fed to the position controller. The output of position controller is fed to the speed reference. The speed reference is either user provided or the speed required to reduce the position error. This reference is compared with actual reference.

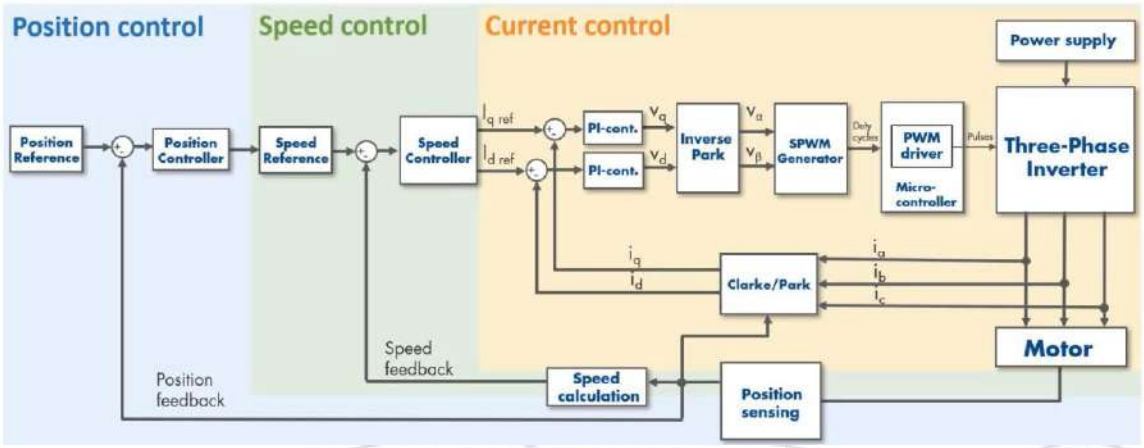

Fig. 2.6. General Speed and Position Control of BLDC Motor Using FOC Scheme (Courtesy – MathWorks)

2.4. Working Principle of FOC Scheme

The three phase stator currents of the BLDC motor are represented by a vector and the main concept of FOC is controlling these currents. The three-phase quantities that are speed and time dependent are subjected to projections that transform the system into a two coordinate dq frame time invariant system, these components are modified as desired using techniques such as PI controller to track the reference. The modified components are converted from the dq reference frame back to three phase quantities to be fed to the PWM modulator to derive the gate signals for the inverter.

2.4.1. Mathematical Transformation

Clarke's Transform

The Clarke's transform is used to convert three-phase quantities to two-phase orthogonal system. The transformation is given by (2.10) – (2.12).

$$i_\alpha = \frac{2}{3} \cdot i_a - \frac{1}{3}(i_b - i_c) \tag{2.10}$$

$$i_\beta = \frac{2}{\sqrt{3}}(i_b - i_c) \tag{2.11}$$

$$i_0 = \frac{2}{3}(i_a + i_b + i_c) \tag{2.12}$$

A particular case i_α is in line with vector i_a, then the particular case of Clarke's transformation is given by (2.13) – (2.15)

$$i_\alpha = i_a \tag{2.13}$$

$$i_\beta = \frac{1}{\sqrt{3}} \cdot i_a + \frac{2}{\sqrt{3}} \cdot i_b \tag{2.14}$$

$$i_a + i_b + i_c = 0 \tag{2.15}$$

Park's Transform

The previously calculated alpha beta quantities calculated via Clarke transform is fed to a vector rotation block to rotate the quantities over an angle theta to follow the dq frame attached to the rotor flux

The rotation over angle theta is carried out as shown in (2.16) – (2.17)

$$i_d = i_\alpha \cdot cos(\theta) + i_\beta \cdot sin(\theta) \tag{2.17}$$

$$i_q = -i_\alpha \cdot sin(\theta) + i_\beta \cdot cos(\theta) \tag{2.18}$$

Inverse Park Transforms

The vectors in dq frame are transformed to two phase alpha beta orthogonal frame representation calculated with a rotation over an angle theta using (2.19) – (2.20)

$$i_\alpha = i_d \cdot cos(\theta) - i_q \cdot sin(\theta) \tag{2.19}$$

$$i_\beta = i_d \cdot sin(\theta) + i_q \cdot cos(\theta) \tag{2.20}$$

Inverse Clarke Transform

The conversion from two phase orthogonal alpha beta frame to three phase quantities using the following equations (2.21) – (2.23)

$$i_a = i_\alpha \tag{2.21}$$

$$i_b = -\frac{1}{2} i_\alpha + \frac{\sqrt{3}}{2} i_\beta \tag{2.22}$$

$$i_c = -\frac{1}{2} i_\alpha - \frac{\sqrt{3}}{2} i_\beta \tag{2.23}$$

Final vector representation of all three coordinate systems – abc, αβ and dq are shown in Fig. 2.7 [10]-[14].

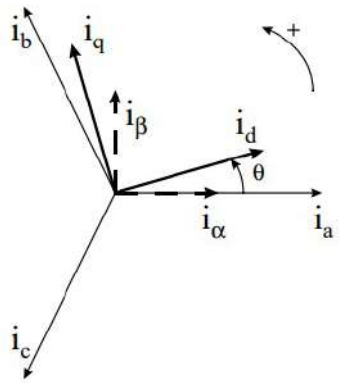

Fig. 2.7. Combined Current Vector Representation [10]

2.4.2. Operational Flow

The instantaneous phase currents are measured using appropriate current sensing techniques. The reference currents required are calculated by the speed and position control loops. Assuming a balanced three phase system, for the conversion from three-phase abc quantities to αβ reference frame, only two instantaneous current vectors are required, for this implementation, only a and b phase currents are considered, phase c current is calculated easily as the sum of all currents at any instant is zero.

Clarke's transformation is carried out using (2.13) – (2.15) followed by Park's transformation using (2.17) – (2.18). By fiddling with the quadrature component of current shown in (2.17), the torque is controlled and direct component controls the rotor flux.

The direct component shown in (2.18) controls the rotor flux. Maximum torque and high efficiency are obtained by maintaining the direct component close to zero using PI controller. Similarly, the quadrature component is maintained close to reference current using another PI controller. The output of the PI controllers results in the required voltage in dq reference frame. This is to be converted to αβ reference frame using inverse park's transformation as shown in (2.19) – (2.20). The voltage in alpha-beta coordinate system is directly used by the SVPWM modulator to obtain the required gate signals [31]-[37].

2.5. SVPWM Generator

Space Vector Pulse Width Modulation is a PWM modulation scheme used to generate the desired voltage vector. The goal of SVPWM is to generate the three-phase waveform required with adjustable amplitude and frequency via a typical three-phase H-bridge inverter. It is a superior PWM technique compared to techniques such as Sinusoidal PWM and offers better utilisation of the DC bus and harmonic content of the output is less. The space vector representation of the inverter system is shown in Fig. 2.8. The power is delivered to the motor via a three-phase inverter as shown in Fig 2.5. containing six switches. Each of the three outputs, either high side or low side is allowed to be ON. This gives 8 total states represented by the 8 spokes in the vector representation. The goal of SVPWM is to generate a mean vector during the PWM time period equal to the desired voltage (V_{out}). The location of V_{out} is determined on the space vector representation, that is determining the sector. The two adjacent base vectors along with one null vector are used to synthesise the desired voltage [12]-[17]. Considering sector 1 shown in Fig. 2.9 the time periods of each vector are given by equations (2.24) – (2.26) and the resulting V_{out} is shown in (2.27).

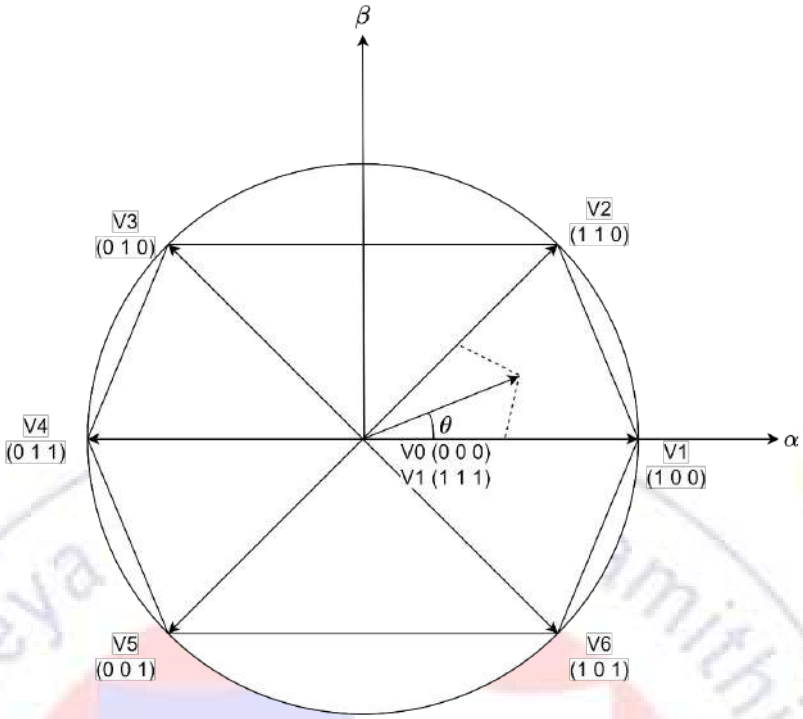

Fig. 2.8. Vector Representation Using SVPWM

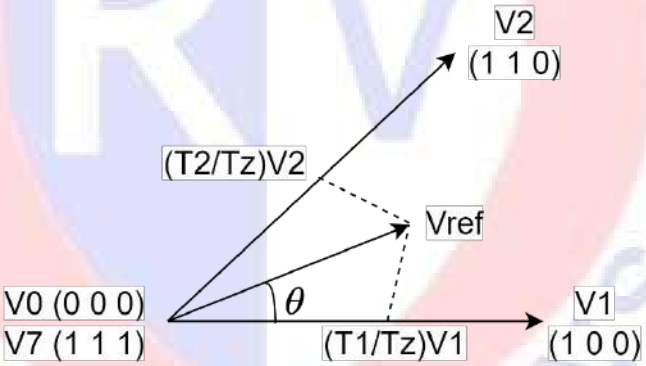

Fig. 2.9. Sector 1 Representation

$$T_1 = \left|\frac{V_{out}}{V_1}\right| \cdot T_{PWM} \tag{2.24}$$

$$T_2 = \left|\frac{V_{out}}{V_2}\right| \cdot T_{PWM} \tag{2.25}$$

$$T_0 = T_{PWM} - (T_1 - T_2) \tag{2.26}$$

$$V_{out} = V_1 T_1 + V_2 T_2 + V_0 T_0 \tag{2.27}$$

2.6. Summary

The basics of active exoskeleton is discussed followed by the control structure of the speed and position control of BLDC motor using FOC scheme are discussed. The transformation involved in the FOC scheme and the SVPWM scheme are briefly dealt with in this chapter.

Chapter 3

METHODOLOGY AND BLOCK DIAGRAM

In this chapter the methodology and the block diagrams used for the study and hardware implementation of the FOC based speed and position control of BLDC motor are discussed.

3.1. Methodology

The methodology followed for the development of the BLDC Drive is shown in Fig. 3.1. Literature survey is carried out to study different speed and position control techniques for BLDC motor to identify a suitable technique for an active exoskeleton application [6]. Next, the electrical and mechanical architecture of the BLDC drive is designed. The mechanical design is the final speed reduction unit to obtain the desired speed. The electrical architecture is designed to be compatible with the open-source firmware. Simulation studies are carried out to validate the proposed design. Hardware implementation is carried out next, followed by performance validation to check the behaviour of the drive and root cause analysis to study the cause of failure. The performance validation is carried out by commanding the drive to move to set positions and measure the positional error after the command as executed. Root cause analysis is the process of discovering the root causes of problems in order to identify appropriate solution. The first goal of root cause analysis is to discover the root cause of a problem or event. The second goal is to identify potential fixes, compensate, or learn from any underlying issues within the root cause. The third goal is to apply learnings from this analysis to systematically prevent future issues or to repeat successes. In this case, waveforms are studied in details to identify the cause of failure.

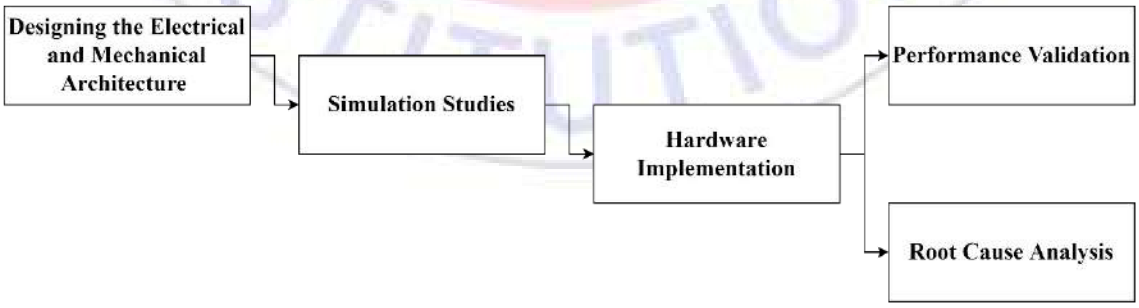

Fig. 3.1. Methodology for BLDC Drive Development

The flowchart of the FOC firmware is shown in Fig. 3.2. The pre-requisite for the FOC loop is the reference current that is calculated by speed and position controllers. The actual and reference speed and positions are used to identify the torque/current required to

obtain the reference commands. The software configurations of different hardware component are carried out at setup. In the current loop, the stator currents are measured using ADCs with appropriate pre-conditioning and transformed from 3 phase quantities to αβ stationary reference frame via Clarke's transformations. The rotor position is sensed using encoders for feedback. Using Park's transformation, the stationary reference frame is converted to rotating reference frame. The quadrature current is maintained close to reference current and direct current is maintained close to zero using PI controller. Inverse Park's transformation is carried out and corresponding gate signals to drive the three-phase inverter are generated using SVPWM. The loop continues at set intervals usually setup with interrupt with highest priority.

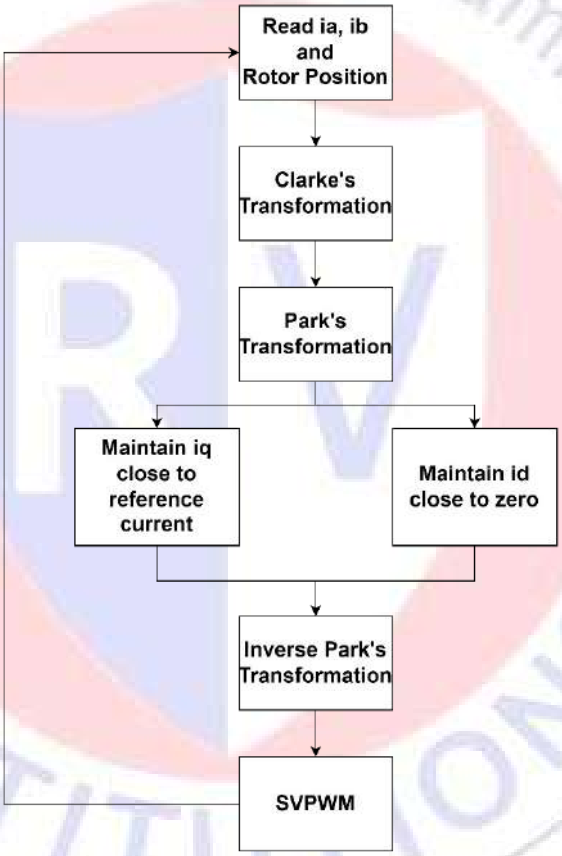

Fig. 3.2. Flowchart of the FOC Firmware

3.2. Block Diagram

The block diagram of the exoskeleton system with BLDC Drive is shown in Fig. 3.3.

- The main controller mimics the function of the main control system of an exoskeleton by commanding the speed and position control to the BLDC drive system and receive telemetry to obtain the status of the drive. Various protocols

are available for communication between main controller and motor controller, although CAN protocol is preferred.

- The Microcontroller (MCU) uses these speed and position commands to calculate the torque/current required. The actual stator currents are measured, transformed and modified according to reference, followed by inverse transformations to obtain reference voltage.
- The reference voltages are converted to gate signals using SVPWM scheme and are fed to the gate driver IC to drive the power switches appropriately.
- Current feedback for the FOC scheme is obtained using current sensors and position feedback is obtained via encoder.

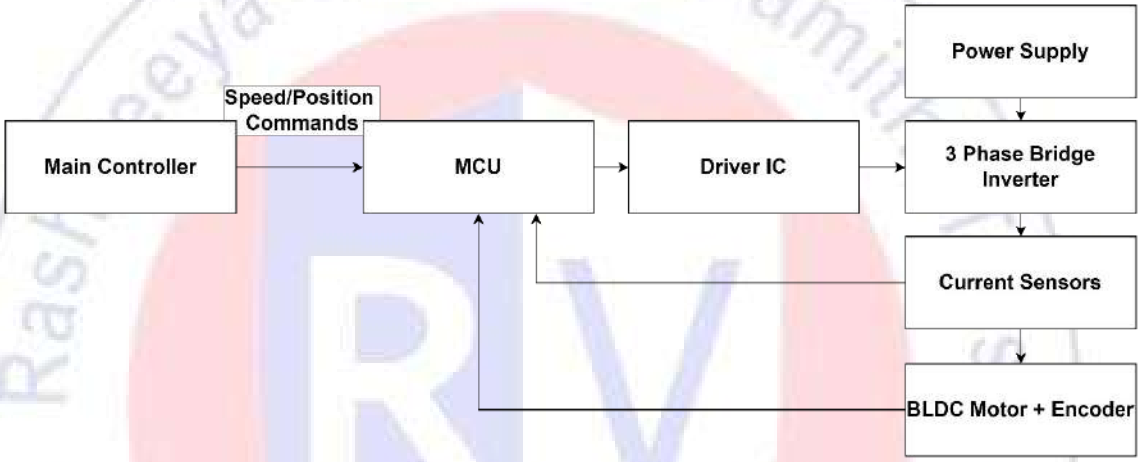

Fig. 3.3. Block Diagram of Exoskeleton System with BLDC Drive

The block diagram of the proposed BLDC drive is shown in Fig. 3.4.

- The main controller function is performed by an Arduino Uno, an ATmega328P based development board. The firmware running on this is responsible for sending reference speed and position commands. Also, it receives telemetry from the motor controller. The ATmega328P does not have CAN capabilities in-built, therefore an external CAN bus controller board is utilised. The external CAN controller board contains Microchip's MCP2515 CAN Controller IC that communicates with the ATmega328P via SPI, it is responsible for converting the digital data stream being sent out by the ATmega328P and vice-versa to signals suitable for the CAN. This is linked with the Microchip's MCP2551 CAN Transceiver IC, it is responsible for taking the digital signals from the CAN controller and convert it to the differential CAN bus signal.

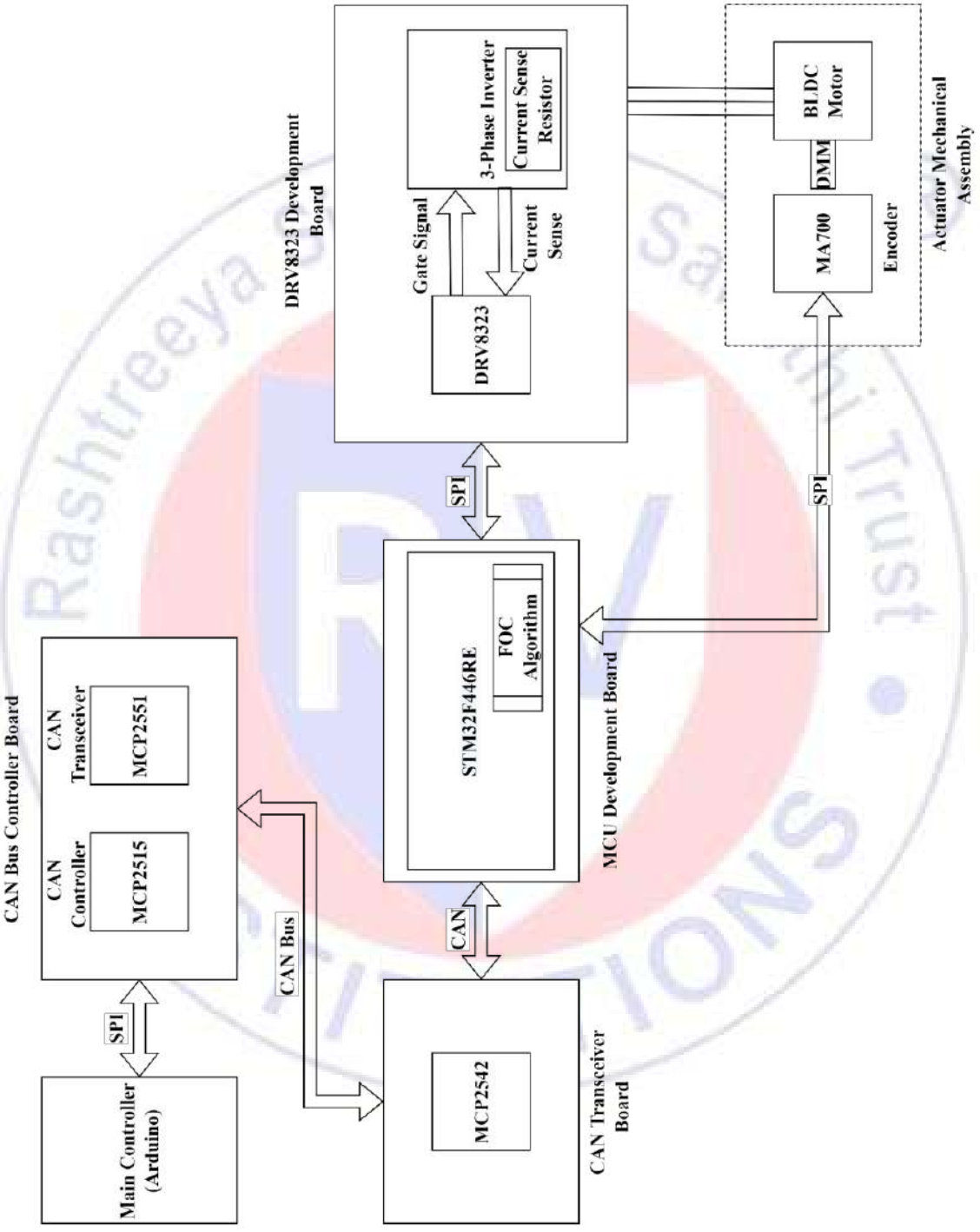

Fig. 3.4. Block Diagram of the Proposed BLDC Drive

- The differential CAN bus signal as to be converted back to a form usable by the motor controller, therefore, Microchip's MCP2542 CAN Transceiver IC is used for this purpose. ST's STM32F446RE MCU is used as the motor controller IC. This DSP as the FOC algorithm running on it, in this case an open-source firmware is adopted for validation. It also as CAN capabilities in built. It receives the reference parameters from the main controller and performs the FOC control loop to generate the gate drive signal. It has inbuilt ADCs to measure the stator currents and the algorithm performs the required transformations and control loop computations to derive the gate control signals.
- Texas Instruments DRV8323RS Smart Gate Driver IC, is employed to drive the inverter. In this project, the DRV8323RS development board is used that as onboard three-phase inverter, current sense resistors and associated current shunt amplifiers and fault indication. This clever driver IC takes care of majority of the burden involved in driving the MOSFETs properly. The configurations are carried out via SPI. The configurations are set accordingly, the current sense amplifiers measure the voltage drop across the current sense resistor, pre-condition it, amplify it by the factor selected by the user and output them directly to the microcontroller via dedicated pins. The gate control signals have dedicated pins and the required processing to drive the gate properly and safely is taken care by the digital core.
- For position feedback, a MagAlpha MA700 Encoder is employed. This is directly placed above the shaft to read the position. The shaft positions are communicated to the drive via SPI. The encoder uses a diametrically magnetised magnet placed in axis with the shaft to identify the rotor position. It is used for both position control loop and the FOC control loop.

3.3. Summary

The methodology used in this study and the hardware implementation are discussed in this chapter, followed by the detailed block diagram of the hardware implementation.

Chapter 4

SPECIFICATION AND DESIGN

Specifications of the final drive, all the hardware components, firmware, schematic and pin mappings are specified. The control loop gains calculation and the mechanical design are also discussed.

4.1. Specification of BLDC Drive

Based on report by Army Research Laboratory (ARL), USA (Appendix C)

- The angular velocity of knee joint is 100°/s that corresponds to 16 RPM
- The maximum angular velocity is 400°/s that corresponds to 66 RPM
- Maximum power required is 1050W
- Maximum torque required is between 50-100Nm

As mentioned in previous section, due to supply chain related issues and semiconductor shortage crisis, the desired full-scale implementation is difficult. Therefore, for the validation prototype, a scaled down version of the BLDC drive with the final specifications are listed in Table. 4.1. The development boards pose several hardware constraints, for example, the inverter on the DRV8323RS development board is limited by the lack of power dissipation capabilities on the board and the maximum current the power switches are capable of handling is less than the maximum rated current of motor. Similarly, the motor is optimized for drone applications, the down draft of the propellers cools the motor. In this case cooling is not available hence short duration tests are carried out to test the firmware. For safe operation, the current is limited in software.

Table 4.1. Proposed Drive Specification

Parameter	**Value**
Input Voltage	12V-18V
Output Current	Upto 15A
Maximum Power	200W
Communication Protocol	CAN, Serial
Speed Reduction Ratio	1:6
Range of Motion	360° Continuous
Desired Position Accuracy	±1° Error

4.2. Hardware Components

The specification and particular details related to hardware components are listed below –

4.2.1. BLDC Motor

A DYS3548-6 motor is selected for this application, a picture of it is shown in Fig 4.1. Specification of the BLDC motor is listed below – A low RPM, high torque and high-power density motor is selected for this application.

- Model Number - DYS D3548-6
- Motor KV (RPM/V) – 790KV
- Resistance – 0.01ohm
- Max Voltage – 18.5V
- Shaft Diameter – 5mm
- Maximum Power – 717W
- Poles - 12/14
- No-Load Current/Max Current – 1.8A/40A
- Dimensions – 35mmx48mm

Fig. 4.1. DYS D3548 BLDC Motor

4.2.2. DRV8323RS Development Board

Specifications of DRV8323RS Development Board (Appendix A) -

- Input Voltage – 6 to 40V
- Max Drive Current – Upto 15A
- MOSFET - CSD88584Q5DC (40V Half-Bridge Power Block, Capable of 50A continuous but limited by power dissipation capabilities on board)
- 0.007Ω current sense resistor between each phase and ground

The DRV8323RS is a smart three-phase gate driver IC by Texas Instruments. It contains a triple half bridge gate driver with three high side and three low side N-channel MOSFET drivers. A charge pump-based topology is used to drive the high side switches. The smart gate drive architecture provides a simple way to configure the deadtime,

adjustable slew rate and fault indication. It has internal current sense amplifier with adjustable amplifier to further simplify pre-conditioning requirements for current sensing. A general block diagram of the DRV8323RS family is shown in Fig. 4.2.

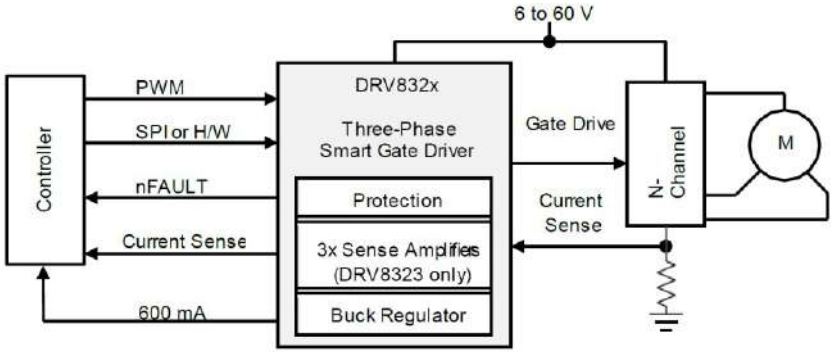

Fig. 4.2. Block Diagram of DRV8323RS

The image of the DRV8323RS development board is shown in Fig. 4.3. The board contains the main driver IC with supporting components, an onboard buck converter severing as the local power supply for the driver IC and the main controller. There are three 7mΩ current sense resistors between each phase and ground. There are three test points corresponding to each phase, six test points connected to gate drive outputs and one common ground point. The schematic of inverter side of the development board as provided by Texas Instruments is shown in Fig. 4.4 Apart from the main gate drive IC, another technological advancement is seen in the MOSFET used. The CSD88584Q5DC Power Block is used, it contains one complete half-bridge in one small package of size 5x6mm, the block diagram is shown in Fig. 4.5.

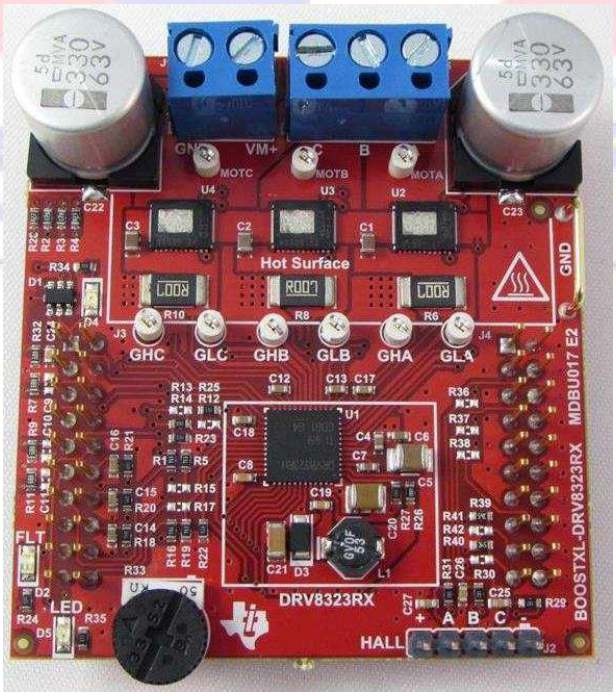

Fig. 4.3. DRV8323RS Development Board

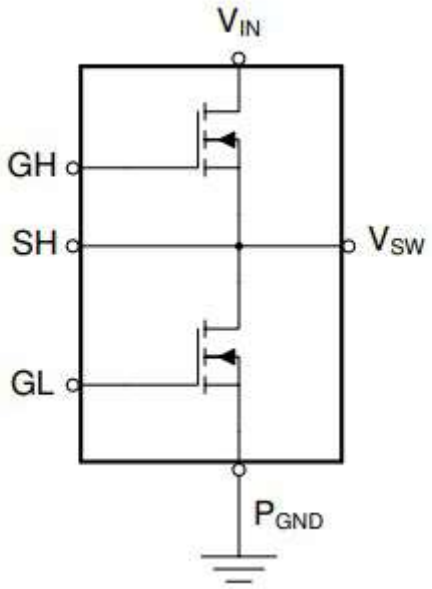

Fig. 4.4. Block Diagram of CSD88584Q5DC

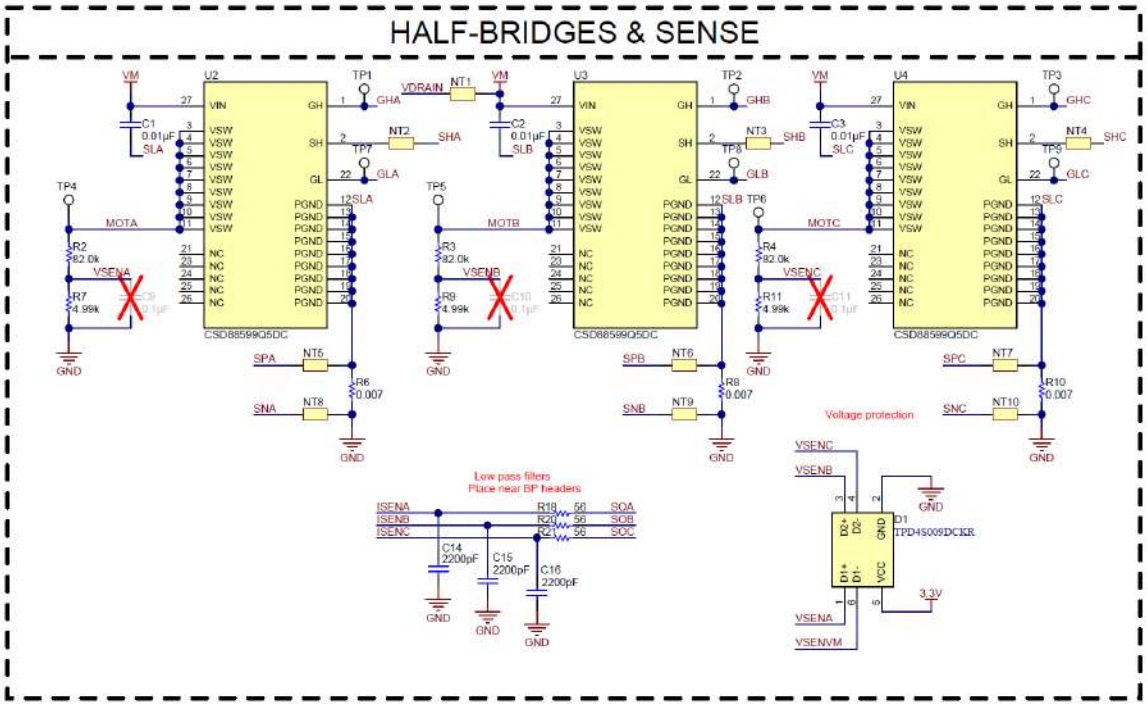

Fig. 4.5. Schematic of the Inverter Side of the DRV8323RS Development Board

4.2.3. Nucleo F446RE

The Nucleo F446RE is a development board based on the STM32F446RE microcontroller by STMicroelectronics. An image of the development board is shown in Fig. 4.6. The main specifications of the microcontroller are listed below (Appendix A) -

- 32-bit Arm Cortex-M4 (upto 180MHz) core with DSP and FPU
- 512 Kbytes of Flash memory
- 128 Kbytes of SRAM

- Up to four SPIs
- 2× CAN (2.0B Active)

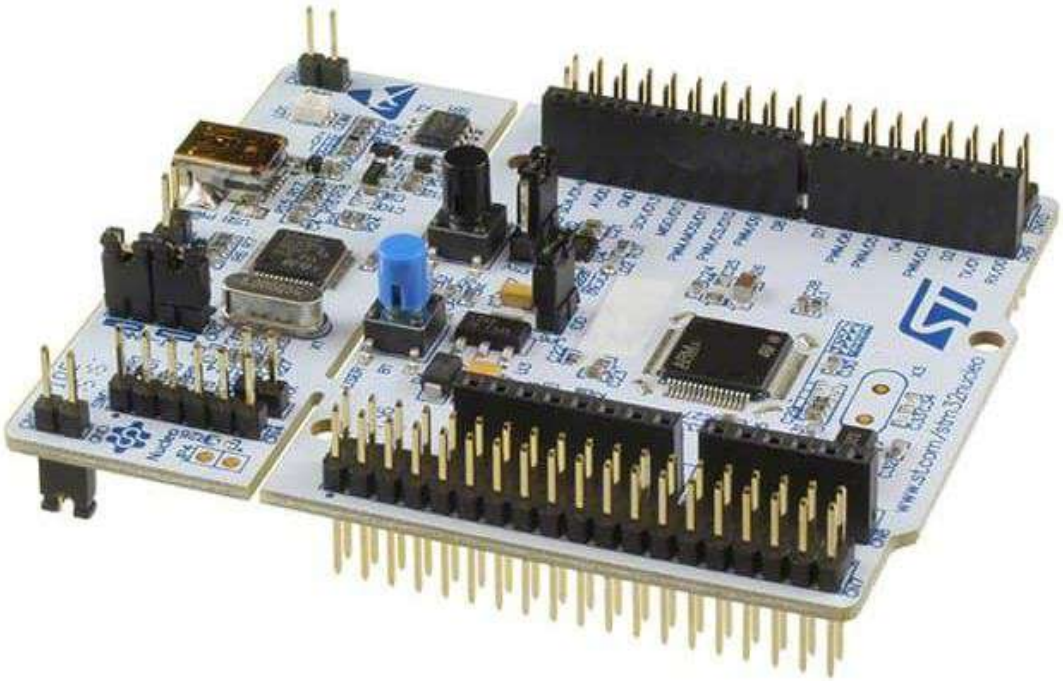

Fig. 4.6. Nucleo F446RE Development Board

4.2.4. Angle 2 Click (MA700 Encoder)

The Angle 2 Click module is development board based on MagAlpha MA700 angle encoder made by Mikroe. It is a robust, contactless angle encoder that detects the angular position of the rotor via diametrically magnetized magnet attached in axis to the rotor. It communicates with the main controller via SPI. The Fig. 4.7. shows an image of the development board. The main specifications of MA700 are (Appendix A) –

- 11-Bit Resolution Absolute Angle Encoder
- 500kHz Refresh Rate
- Ultra-Low Latency: 3µs
- Serial Interface for Data Readout and settings
- Accurate angle measurement at speeds from 0 to 100,000 RPM

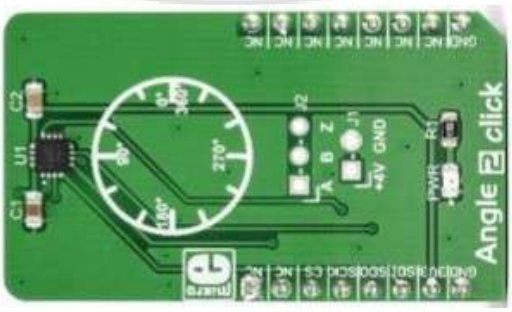

Fig. 4.7. MA700 Angle to Click Module from Mikroe

4.2.5. MCP2542 Click

The MCP2542 Click is a development board based on Microchip's MCP2542 CAN transceiver IC made by Mikroe. Its primary function is to interface between the differential CAN bus and the CAN protocol suitable for the microcontroller. An image of the controller is shown in Fig. 4.8.

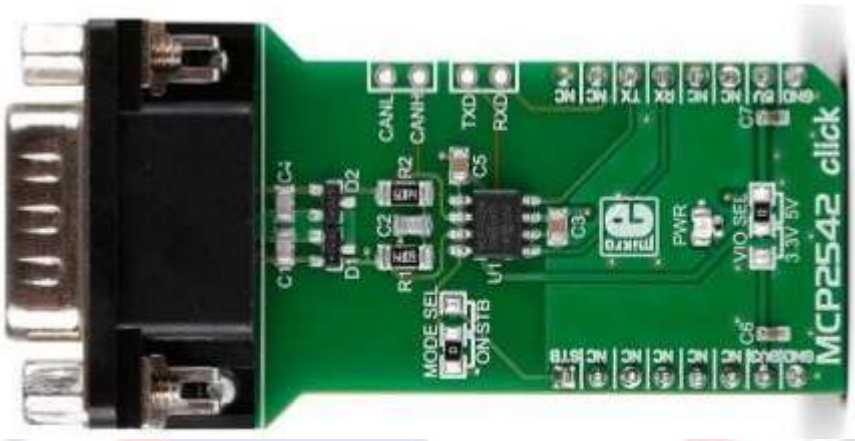

Fig. 4.8. MCP2542 CAN Transceiver by Mikroe

4.2.6. Arduino Uno and CAN Bus Shield

Arduino Uno is a popular open-source development board based on the ATmega328P, shown in Fig 4.9. It is used to perform the function of the main controller to send speed, position commands and receive telemetry information. The CAN Bus Shield is made by Sparkfun shown in Fig. 4.10 and it directly connects with the Arduino Uno to provide it with CAN protocol capabilities. It consists of Microchip's MCP2515 CAN controller that communicates with the ATMega328P via SPI and Microchip's MCP2551 CAN transceiver in turn converts it to the differential CAN bus.

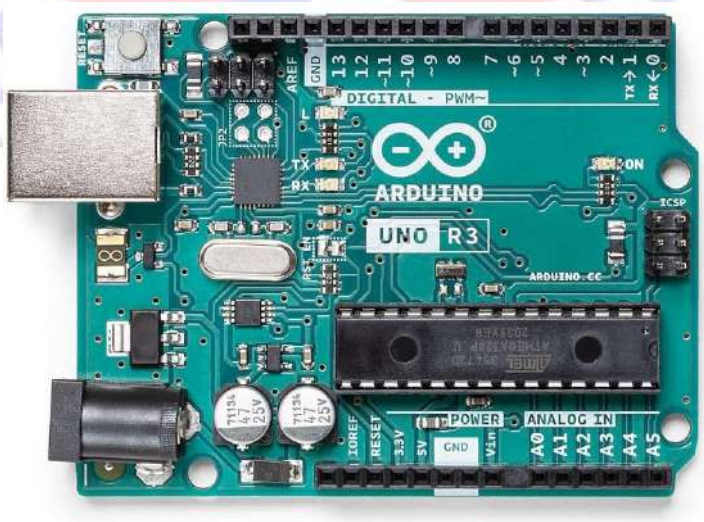

Fig. 4.9. Arduino Uno Development Board

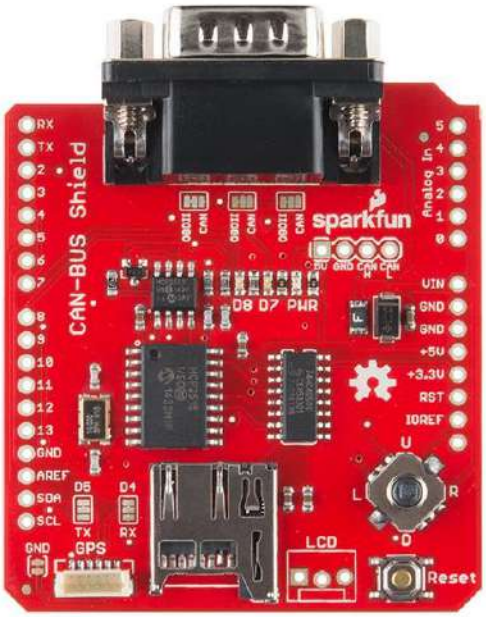

Fig. 4.10. Sparkfun CAN Bus shield

4.3. Firmware

An entirely open-source firmware is employed for both motor control and main controller code.

4.3.1. Motor Control Firmware

Details of the motor control firmware are given below –

- Based on an open source FOC-based motor control firmware
- OS - Mbed RTOS
- IDE - Mbed Online IDE
- Development Board – Nucleo F446RE (based on STM32F446RE)
- Programming Interface – Onboard ST-Link
- CAN Controller – Onboard
- Current Control Loop Frequency – 40kHz

The modified code and the link to the base open-source firmware is given in Appendix B. Important configurations made in the firmware are shown below –

The DRV8323RS as various configurable PWM modes, to lower complexity of design and reduce pin count, “3x PWM Mode” is chosen. Table 4.2. shows the logic table of the inputs and the respective gate outputs, the ‘x’ stands for phase A, B and C, Hi-Z

means high impedance state. In this mode, all the low side gate input pins are tied to logic high, only by controlling the high side gate input pins, both high side and low side switches are controlled complimentary in nature. When the low side input is pulled high and high side input is high, the high side MOSFET is turned on and vice versa.

Table 4.2. Logic Table in PWM3x Mode

INLx	INHx	GLx	GHx	SHx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

The gain of the current sense amplifier is set at 40, the gate driver fault status is enabled, gate fault retry time set to 50us, deadtime set to 100ns and CAN frequency set at 1MHz. The choice of deadtime is higher than the maximum turnoff delay time of CSD88584Q5DC, Appendix A shows a snippet of the datasheet of the turn-on and turn-off times. Table 4.3. shows the software current limits and parameters scaling limits.

Table 4.3. Important Configurations in the Firmware

Parameters	Value
Max Current	5A
Field Weaking Current	1.5A
Max Continuous Current	3A
Position Range	-12.5 to 12.5 (Corresponds to -4xpi and 4xpi)
Velocity Range	-65 to 65 (Corresponds to -30 to +30 rad/s)

The firmware takes a different approach to speed and position control, the final torque reference is calculated as shown in (4.1), this torque command corresponds to the quadrature component.

$$Torque_{reference} = K_p\,(p_{des} - p_{real}) + K_d\,(V_{des} - V_{real}) + T_{in} \quad (4.1)$$

Where,

Kp →*Position Gain*

Kd →*Velocity Gain*

Pdes , Preal →*Desired Position, Real Position*

Vdes, Vreal →Desired Velocity, Real Velocity

Tin →Torque

4.3.2. Main Controller Firmware

Details of the main control firmware are given below –

- Arduino Based Code
- IDE – Arduino IDE
- Development Board – Arduino Uno (ATmega 328P)
- Programming Interface – Onboard
- Communication Interface – External (via Sparkfun CAN Bus Shield - Controller + Transceiver)
- CAN Frequency – 1MHz

The Table 4.4. shows the CAN Data structure. The Main controller firmware code shown in Appendix B, performs the conversion from float to integer and vice-versa.

Table 4.4. CAN Data Structure

Command (Sending)		Measurement (Receiving)	
Parameter	Resolution (Bits)	Parameter	Resolution (Bits)
Position Setpoint	16	Position	16
Velocity Setpoint	12	Velocity	12
Position Setpoint	12	Estimated Torque	12
Velocity Gain	12	CAN ID	8
Torque	12		

4.4. Calculating Loop Gain

Considering the motor control concept, the goal is to control current i(t) through the stator by the control effort v(t) that is generated by the PWM scheme. The dynamics of an electrical system is faster compared to its mechanical dynamics; therefore, it is ignored along with the back-emf for the purpose of current control. The representation of the system of one stator phase is shown in Fig. 4.11.

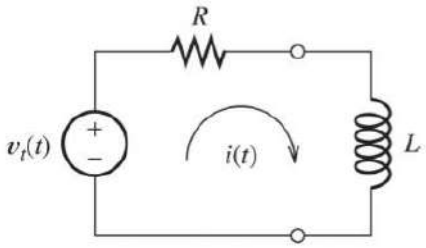

Fig. 4.11. Representation of One Stator Phase of BLDC Motor

The continuous time frequency response has the transfer function shown in. The function is a first order low-pass filter with DC gain given by 1/R and cutoff frequency of R/L. To implement in microcontroller, the continuous time model is converted to discrete time model as shown in (4.2)

$$\frac{I(s)}{V(s)} = \frac{1}{Ls + R} \tag{4.2}$$

Discrete time PI controller is written in the form shown in (4.3)

$$\frac{I(z)}{V(z)} = \frac{\frac{1}{R}(1 - e^{\frac{-RTs}{L}})}{z - e^{\frac{-RTs}{L}}} \tag{4.3}$$

where U is control effort, and E is error, pole at $z = 1$, a zero at $z = 1 - ki$, and a high-frequency gain of k. Changing k only affects the loop gain, and changing ki only affects the zero location, ki is given by (4.4).

$$ki = 1 - e^{\frac{-RTs}{L}} \tag{4.4}$$

The zero of the controllers is set near the pole of the RL system, then the loop return ratio just looks like an integrator. This is carried out by setting k given by (4.5)

$$k = R\left(\frac{\omega_c}{1 - e^{\frac{-RTs}{L}}}\right) \tag{4.5}$$

The above equation is close to discrete time version provided the RL time constant L/R is larger than Ts (preferably 10 times more). Loop gain is calculated by choosing the desired crossover frequency of the current loop keeping in consideration the effects of current sensor noise, otherwise at high gains, the noise gets amplified. A reasonable crossover frequency is around pi/10 radians per sample or faster. A current loop frequency of 40kHz and 1kHz crossover frequency, the loop gain is calculated. The loop gains k required to set the desired crossover frequency is calculated using (4.5). The process of calculating loop gains is carried out using a MATLAB script shown in Appendix B.

The pseudo code of the current control loop in C [6] is given below –

current = sample_current();

```
current_error = current_ref - current;

integral += ki*current_error;

//Saturate the integrator to prevent windup

integral = fmaxf(fminf(integral, integral_max), -integral_max);

voltage = k*current_error + integral;

//Saturate controller output to be within valid range

voltage = fmaxf(fminf(voltage, voltage_max), -voltage_max);

set_voltage();
```

The actual current is first sampled and the error between actual and reference current is calculated. The integral is calculated by accumulating the error and multiplying it with the gain. The integral output is maintained within limits by saturating it to the set limits. Final control voltage is calculated by taking the sum of the product of current error and proportional gain. The voltage is maintained within limits and the output voltage is set.

4.5. Mechanical Design

The mechanical assembly is designed for speed reduction as the motor chosen is of a higher rated RPM than desired. Although low speed direct drive is possible, the motor is not optimized for it and leads to cogging. The top view of the mechanical setup is shown in Fig. 4.12. A 30 teeth pulley is connected to the motor that as a diametrically magnetized magnet mounted on top to interface with the encoder. This pulley drives a 60 teeth pulley to provide 1:2 speed reduction via a rubber belt that in turn rotates a 20 teeth pulley. Final reduction is carried out by a 60 teeth pulley to reduce the speed by 1:3 ratio at the output shaft. This output shaft mimics the knee joint. The side view is shown in Fig. 4.13 and Fig 4.14 shows the magnetization of a diametrically magnetized magnet.

4.6. Schematic

The schematic of the main controller consisting of the Arduino Uno and Sparkfun CAN bus shield is shown in Fig. 4.15. The schematic of the complete drive unit is shown in Fig. 4.16. Pin mappings and functionality of each pin used in STM32F446RE are listed in Table 4.4.

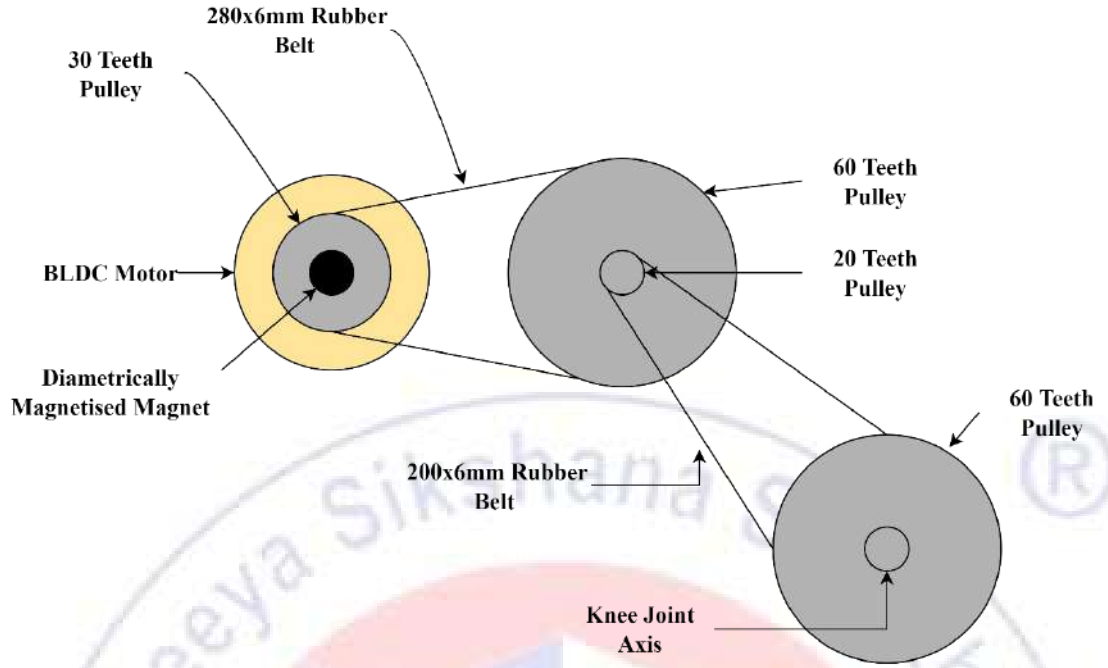

Fig. 4.12. Top View of BLDC Drive's Mechanical Setup

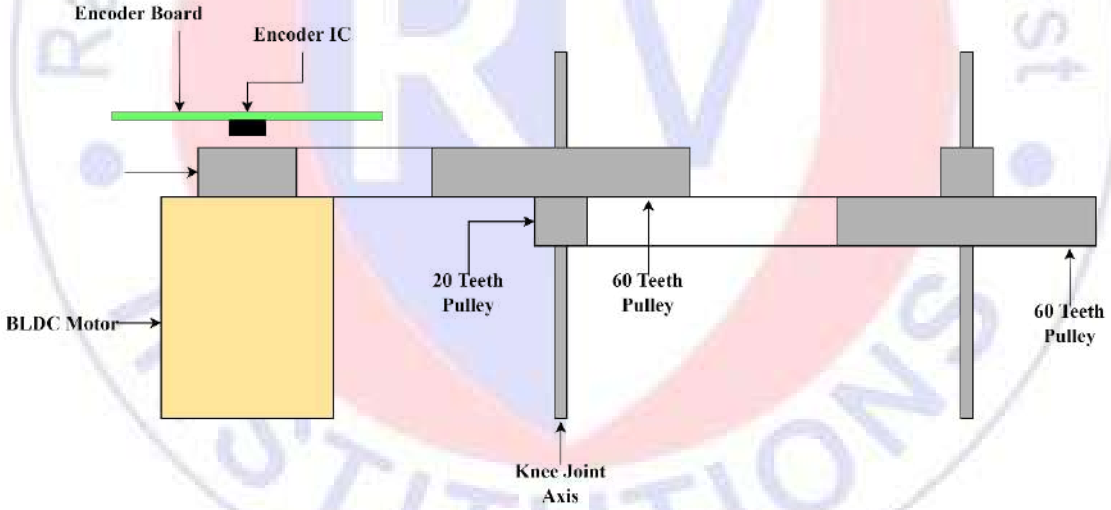

Fig. 4.13. Side View of BLDC Drive's Mechanical Setup

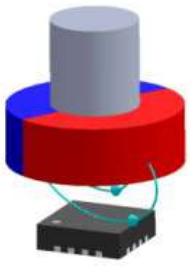

Fig. 4.14. Placement Of Diametrically Magnetized Magnet Over the MA700 Encoder

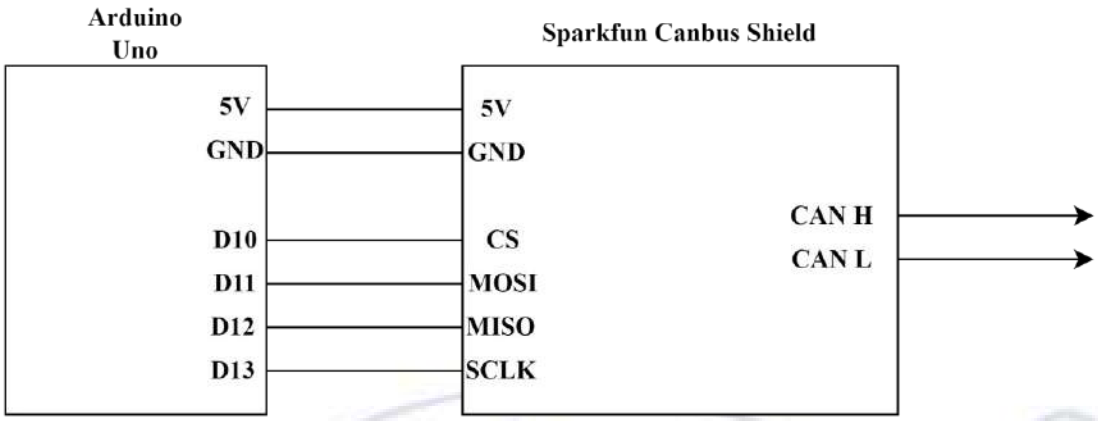

Fig. 4.15. Main Controller Schematic

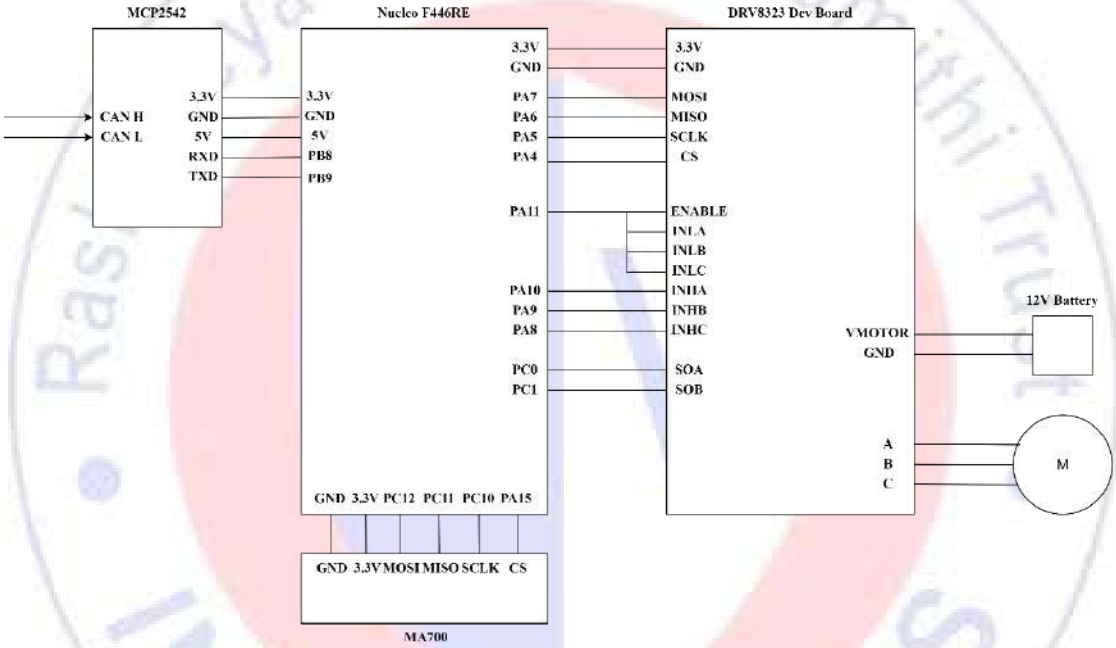

Fig. 4.16. BLDC Drive Schematic

Table 4.5. Pin Mapping of STM32F446RE

STM32F446RE Pin Name	To Module	Module Pin Name	Functionality
PB8	MCP2542	RXD	CAN Controller Receive Data
PB9	MCP2542	TXD	CAN Controller Transmit Data
PA7	DRV8323RS	MOSI	SPI
PA6		MISO	
PA5		SCLK	
PA4		CS	

PA11		ENABLE, INLA, INLB, INLC	Enable DRV8323RS and enabling PWM3x mode (Logic high to enable)
PA10		INHA	Phase A high side switch gate driver control input
PA9		INHB	Phase B high side switch gate driver control input
PA8		INHC	Phase C high side switch gate driver control input
PC0		SOA	Phase A current sense amplifier output
PC1		SOB	Phase B current sense amplifier output
PC12	MA700	MOSI	SPI
PC11		MISO	
PC10		SCLK	
PA15		CS	

4.7. Summary

Specifications of the final drive, all the hardware components, firmware, schematic and pin mappings are specified. The control loop gains calculation and the mechanical design are also discussed in this chapter.

Chapter 5

SIMULATION AND HARDWARE IMPLEMENTATION

The speed and position control of BLDC motor using FOC is designed and implement in Simulink followed by the hardware implementation.

5.1. Simulation Analysis

The speed and position control of BLDC Motor via FOC is carried out in Simulink and the performance is validated. The design parameters are shown in Table 4.1 – The system is modelled as shown in Fig. 5.1. in the lines of the block diagram discussed in section 2.3. The position of the rotor is obtained by integrating the speed of the rotor over time. PI controllers are used for all the control loops. The current control loop gains are calculated using the MATLAB script. The gain values of the speed and position control loop are calculated by trial-and-error method. For the motor, PMBLDC block is used. Transformations are performed by the blocks available in Simscape libraries. SVPWM is directly implemented using the SVPWM block. Position references are generated by the stair generator block. 0.1 seconds, the position is set to 4 radians or 4 revolutions of the rotor shaft. At 2 seconds, the rotor position is set to -4 radians and is set back to 0 radians at 3.5 seconds.

Table 5.1. Parameters Considered for the Simulation Model of BLDC Drive

Parameter	Value
Rs	0.01Ω
Ls	0.00004H
Pole Pairs	7
Vdc	12V
Switching Frequency	8kHz
Position Controller Gains	k = 10, ki = 0.25
Speed Controller Gains	k = 0.5, ki = 1.5
Current Controller Gains	k = 0.5, ki = 0.0062

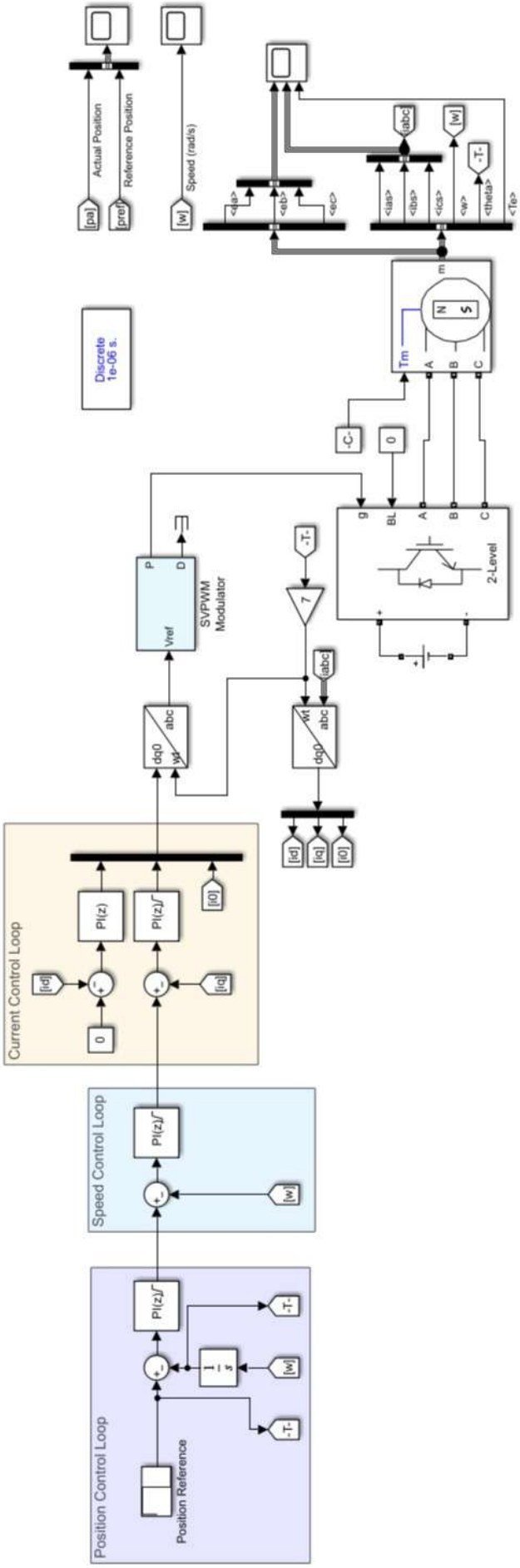

Fig. 5.1. Simulation Model of Speed and Position Control of BLDC Motor Using FOC Scheme

5.2. Hardware Implementation

The entire assembly is constructed using 20x20 T-Slot Aluminum Extrusions for modularity. Different views of mechanical side of the hardware implementation focusing on the two-stage pulley-based speed reduction is shown in Fig. 5.2. and Fig. 5.3. Referring to Fig. 5.2. the components are listed below –

1. Aluminum Extrusion Structure
2. DYS 3548-6 BLDC Motor
3. GT2 Pulley – 30 Teeth, 5mm Bore
4. 10x3mm Diametrically Magnetized Magnet Embedded in 3
5. MA700 Encoder Board
6. 8mm Shaft
7. Bearing Holder
8. GT2 Pulley – 60 Teeth, 8mm Bore
9. GT2 Pulley – 20 Teeth, 8mm Bore
10. GT2 Pulley – 60 Teeth, 5mm Bore
11. Bearing Holder With 5mm Shaft
12. 280x6mm GT2 Belt Between 3 and 8
13. 200x6mm GT2 Belt Between 9 and 10

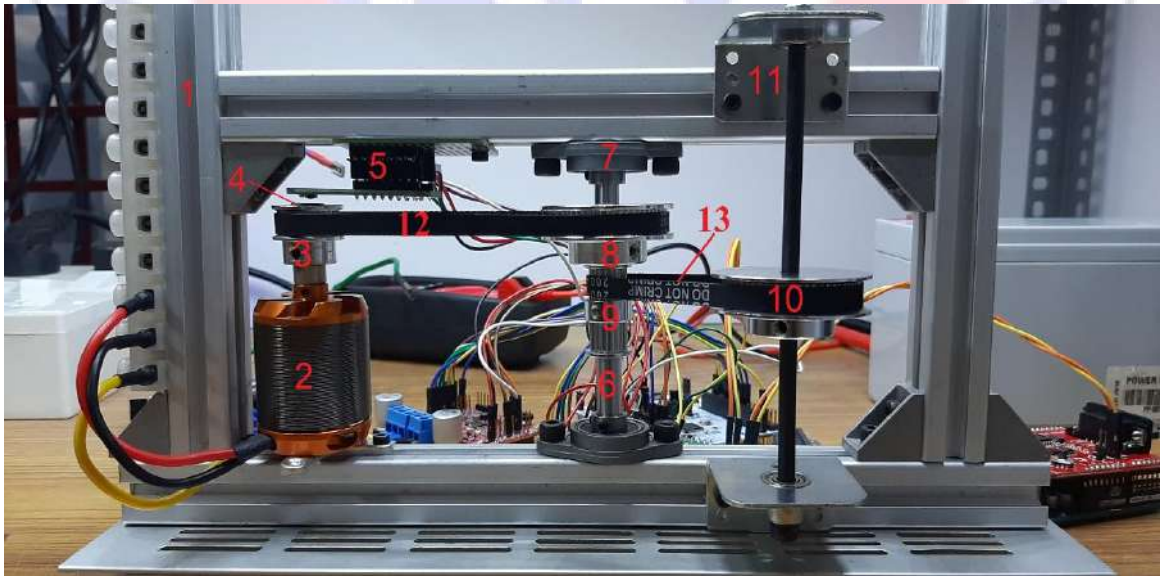

Fig. 5.2. Side View of Hardware Implementation Showing BLDC Motor and The Two-Stage Pulley-Based Speed Reduction Setup

Fig. 5.3. Top View Hardware Implementation Showing BLDC Motor and The Two-Stage Pulley Based Speed Reduction Setup

The placement of the MA700 encoder is shown in Fig. 5.4. and Fig. 5.5. The placement of diametrically magnetized magnet in the pulley is shown in Fig. 5.6. The BLDC motor connections made with the help of a screw terminal strip are shown in Fig. 5.7. The complete setup is shown in Fig. 5.8. The connections are made with standard jumper wires. The name of components is listed below –

1. Arduino Uno With Sparkfun CAN Bus Shield
2. MCP2542 Click CAN Controller Board
3. Nucleo F446RE Board
4. DRV8323RS Development Board
5. Power Connector with Fuse
6. 12V, 7.5 Ah Lead Acid Battery

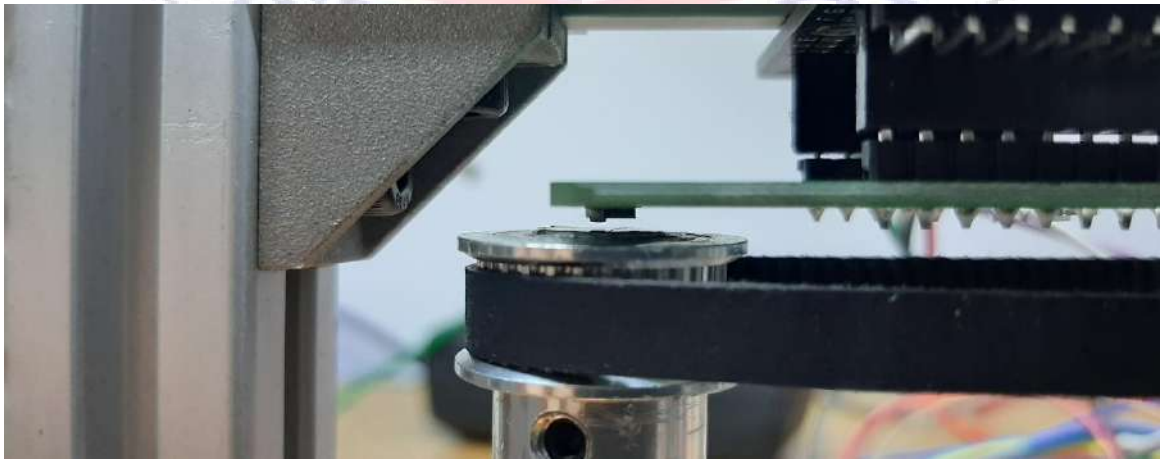

Fig. 5.4. Side View of Encoder Development Board Above Diametrically Magnetised Magnet Attached to Pulley

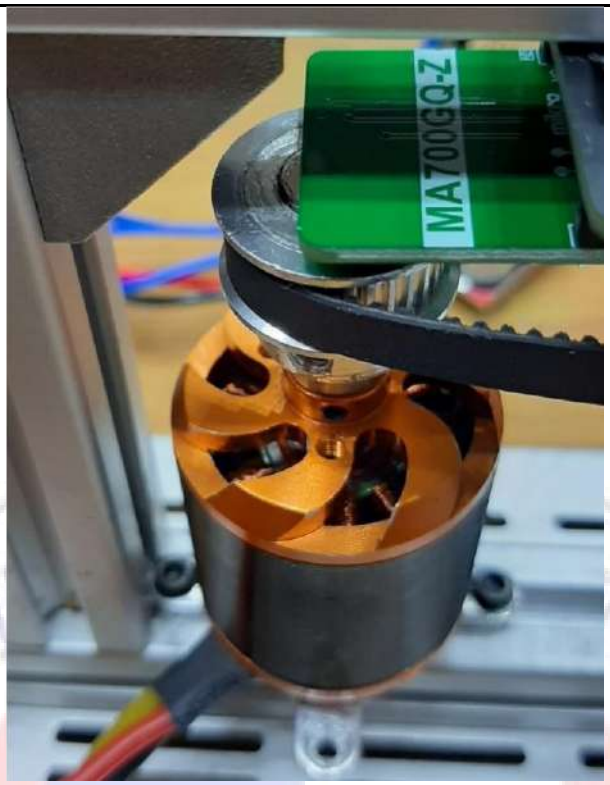

Fig. 5.5. Top View of Encoder Development Board Above Diametrically Magnetised Magnet Attached to Pulley

Fig. 5.6. Diametrically Magnetised Magnet Placed in The Pulley

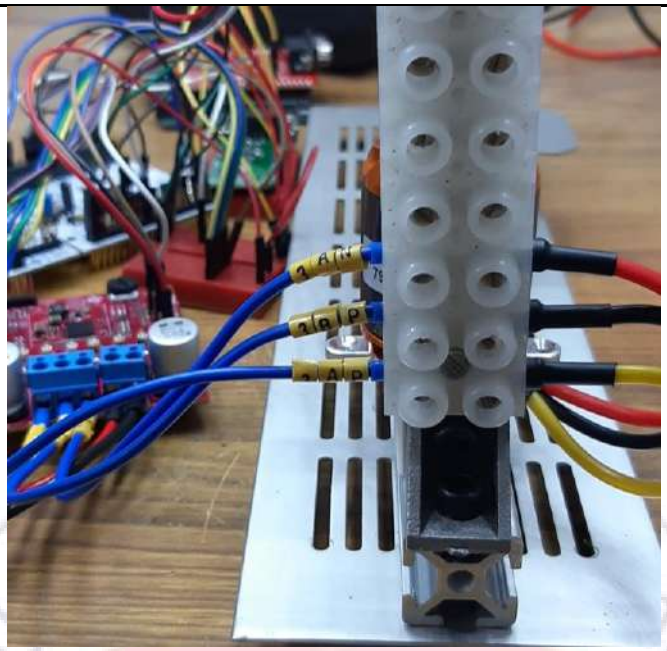

Fig. 5.7. Motor Connection Between DRV8323RS Development Board and BLDC

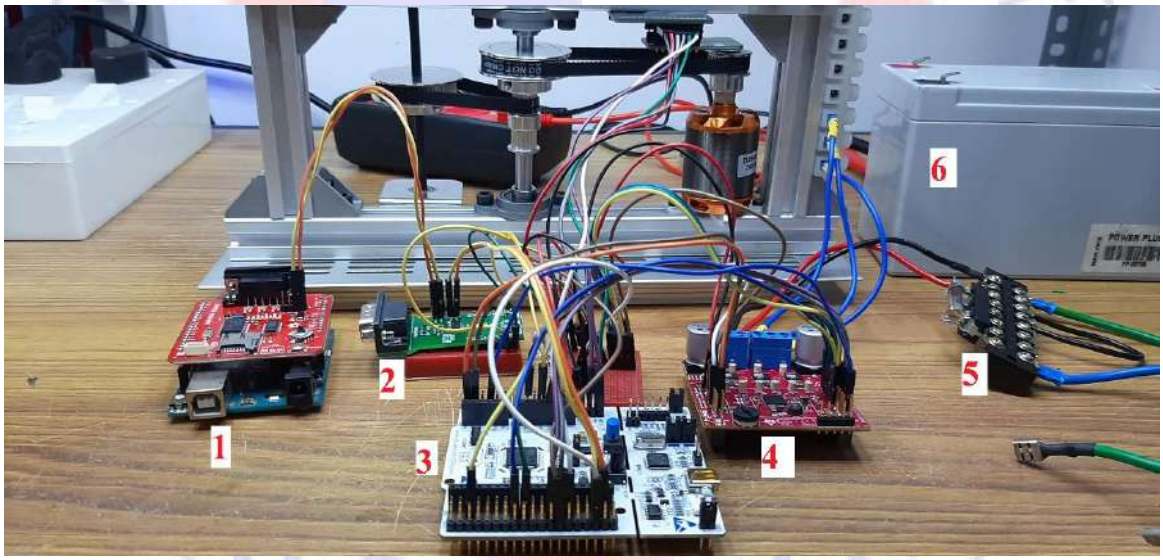

Fig. 5.8. Complete Electronics Setup

5.3. Summary

The implementation of the simulation model of the speed and position control of BLDC motor using FOC is discussed followed by the hardware implementation in detail.

Chapter 6

RESULTS AND DISCUSSION

The output of the control loop gain calculating script followed by simulation results of the BLDC drive are analysed. Results of the hardware along with the root cause analysis of the failure are discussed.

6.1. Output of Loop Gain Calculation

The output of the gain calculating script are k = 0.5 and ki = 0.0062. The Fig. 6.1. is the bode plot of the transfer function. The gain margin is 16.1dB and phase margin of 81 degrees.

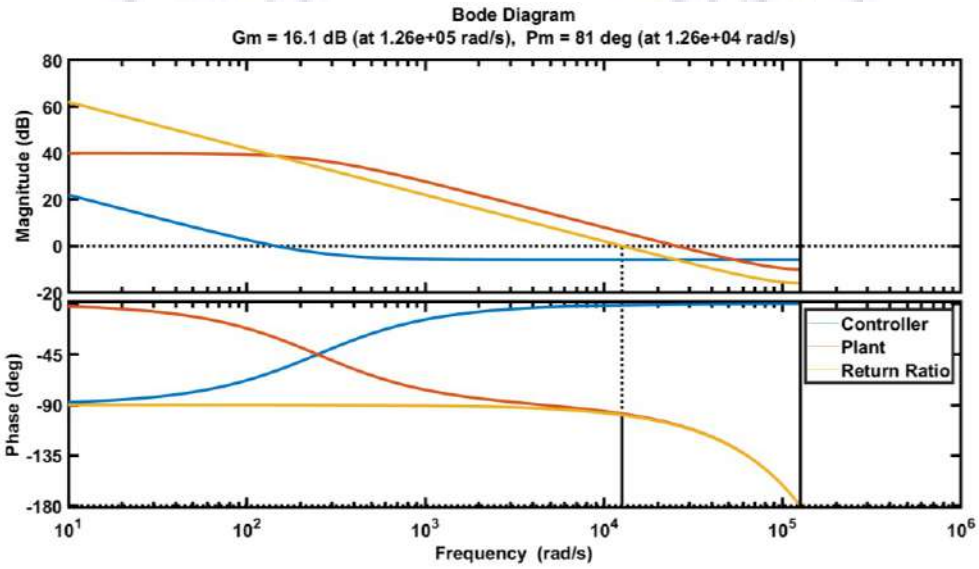

Fig. 6.1. Bode Plot of Current Controller Transfer Function

The step response of this transfer function and loop gain is shown in Fig. 6.2. No overshoots are observed and the response is desirable.

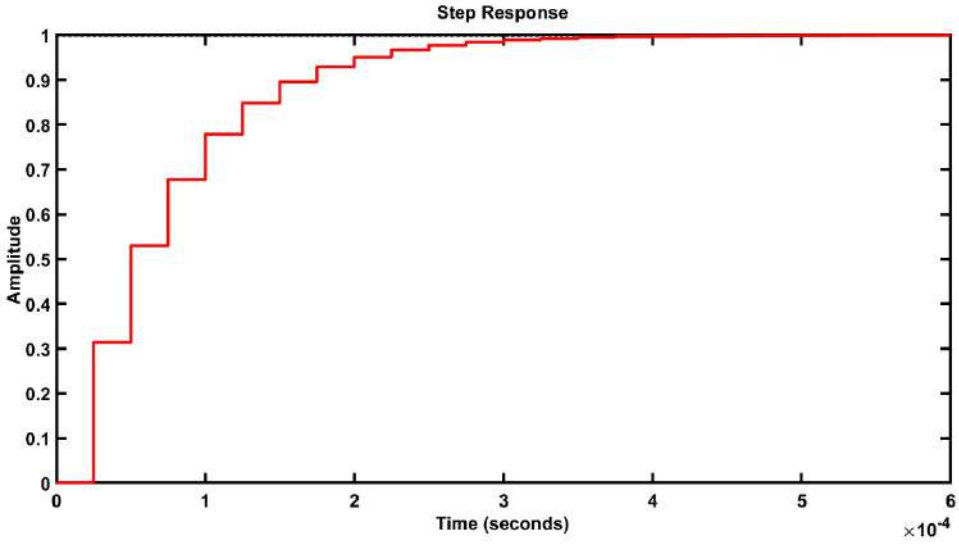

Fig. 6.2. Step Response of Current Controller Transfer Function

6.2. Simulation Output of FOC based BLDC Drive

Section 5.1 presented the simulation model of the speed and position control of BLDC motor using FOC. The comparison between reference position and actual position waveform is shown in Fig. 6.3. A short run-up takes place after the position change, no overshoots occur and the reference position is attained within 0.5 seconds. The position changes are spread across the range from +4 radians to -4 radians.

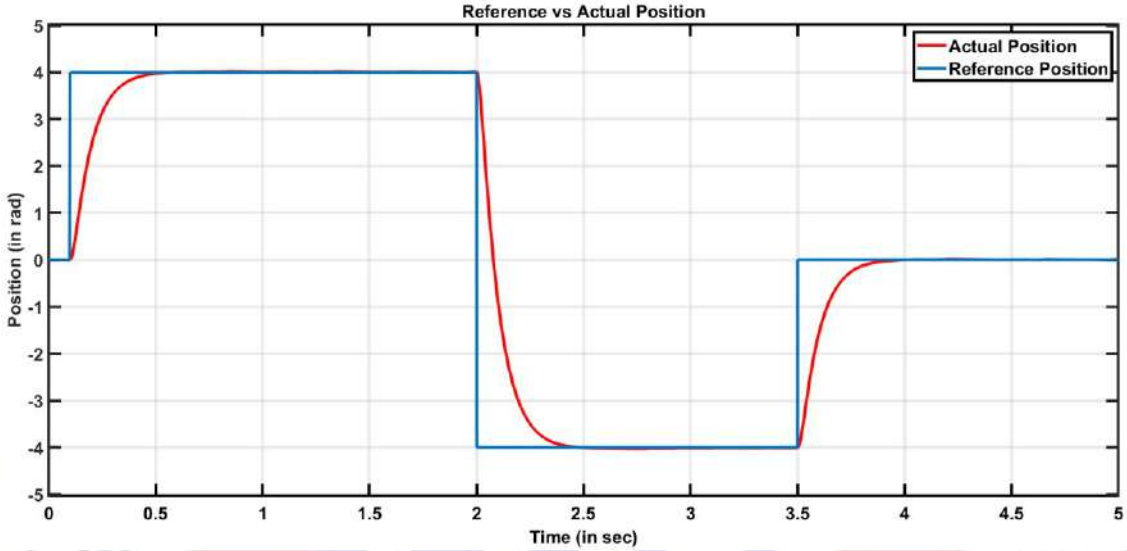

Fig. 6.3. Comparison Between Reference Position and Actual Position

The results of back-emf, phase currents and electromagnetic torque are presented in Fig. 6.4. A spike in all three are seen during position change as torque is required to change from one position to the other. Maximum back-emf lies in the range of 1V peak to peak, Maximum phase currents are 40A peak to peak and 0.38Nm of electromagnetic torque is observed during the position change from +4 radians to -4 radians.

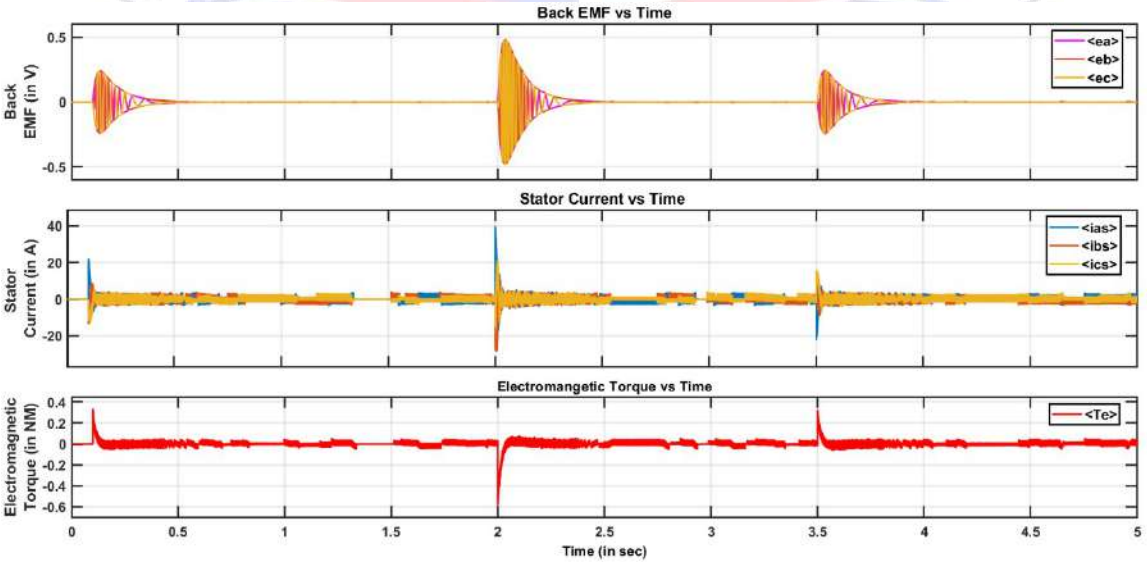

Fig. 6.4. Back EMF, Stator Current and Electromagnetic Waveforms of BLDC Motor

The change in speed during position change is seen in Fig. 6.5. As the reference position changes, the speed increases to attain the reference position and speed starts to drop when the actual position is close to reference and eventually reaches zero after reference position is attained. A maximum of -62 rad/sec speed is reached during position change from +4 radians to -4 radians. The motor as to wind back hence the negative speed.

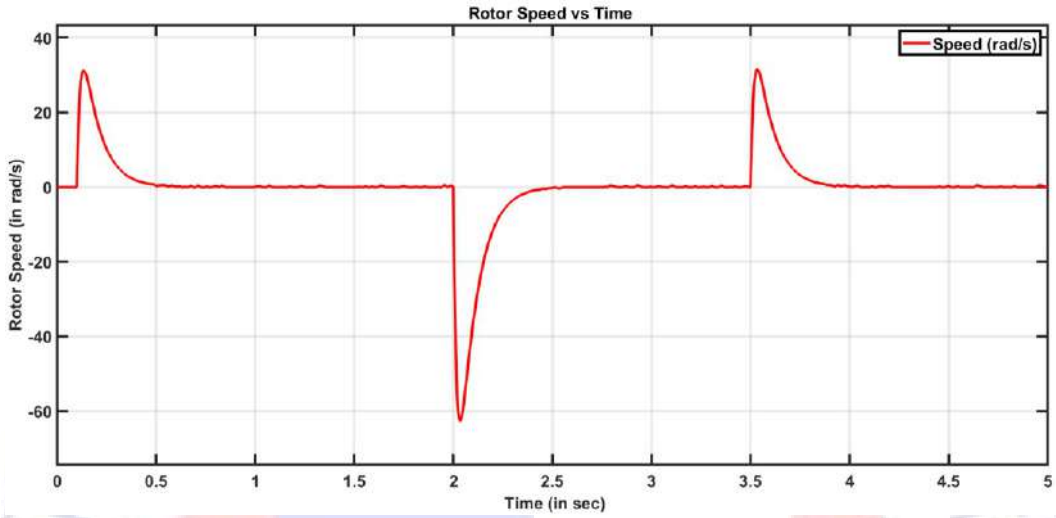

Fig. 6.5. Speed Waveform of Rotor Throughout Simulation

6.3. Hardware Results

First, the drive is configured via serial protocol using Tera Term serial communication tool. Upon connecting to the drive, the user is greeted with commands as shown in Fig. 6.6, a screenshot of the Tera Term tool. Different configurations are available, by clicking on the letter 'm', the drive is put into motor mode. The letter 'c' puts the drive into encoder calibration mode, the motor turns one rotation clockwise and one rotation anti-clockwise to determine encoder offsets. The letter 's' is used to configure software current limits, CAN ID etc. The letter 'e' displays the live encoder position data and the letter 'z' sets the zero position of the drive, any positional change is carried out from these zero positions. A screenshot of the encoder live display is shown in Fig. 6.7.

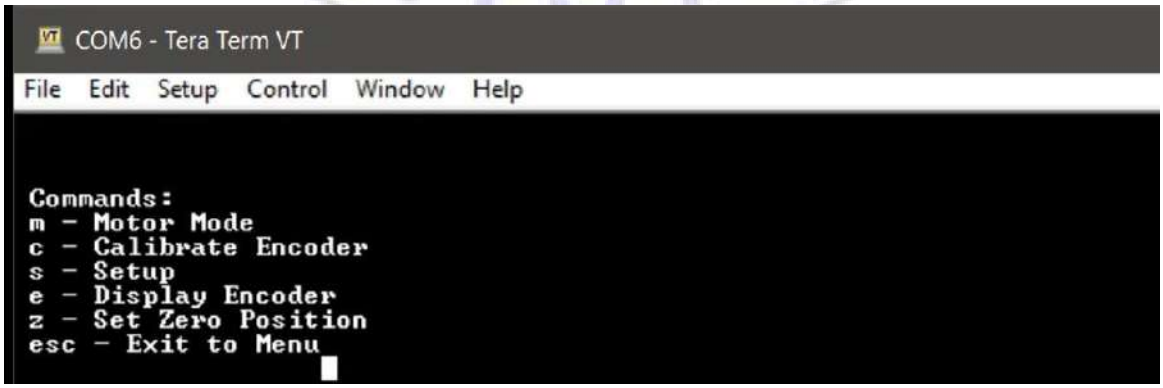

Fig. 6.6. Screenshot of the Welcome Screen of the Controller Connected Via Serial

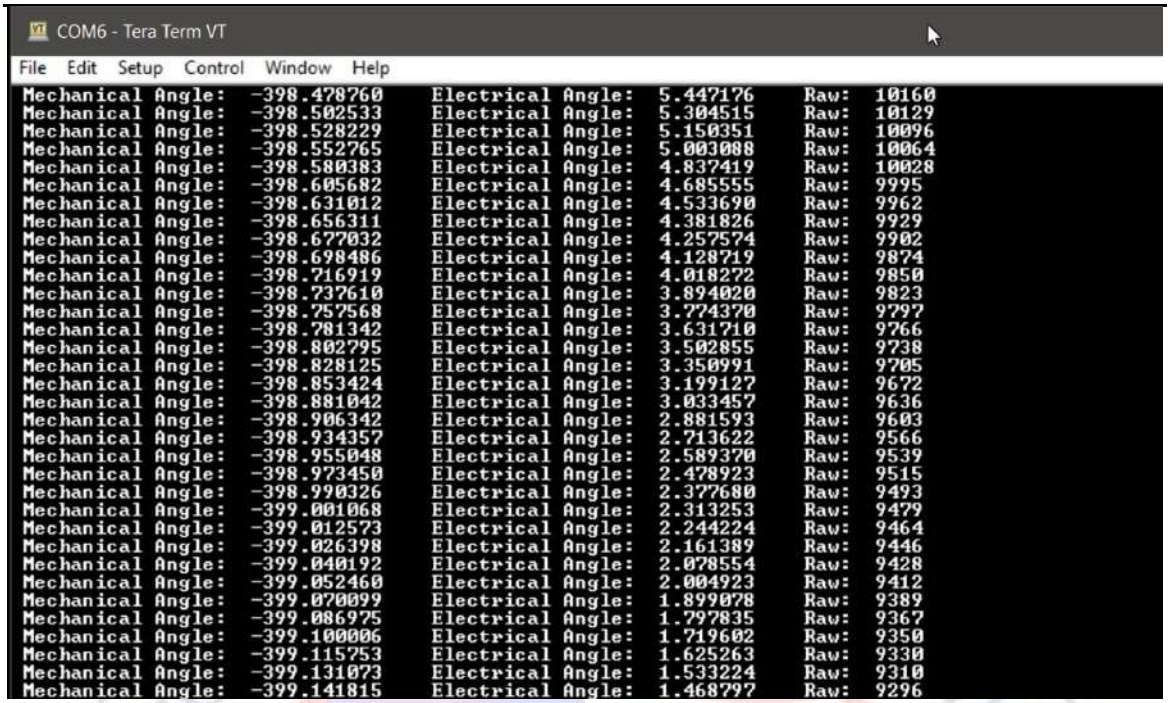

Fig. 6.7. Screenshot of the Encoder Display Mode Showing Live Encoder Readings

The code is modified to accept speed and position commands directly via Serial for initial testing. The onboard button on the Nucleo F446RE development board is configured to set the position at 4π radians when the button is pressed and -4π radians when released. The test is carried out as follows –

1. The drive is put into motor mode by selecting 'm' and is set at 0 position.
2. The onboard button is pressed setting the position to 65535 (16-bit command corresponding to 4π radians) and constant speed set to 500 (12-bit command corresponding to 7.3 rad/sec)
3. The motor responds to the command and position information is tabulated
4. The button is released, the position is set to 1 at the same constant speed and the position information is tabulated
5. Error is calculated as shown in (6.1)

$$\%Error = \frac{Actual\ Position - Set\ Position}{Set\ Position} \times 100 \qquad (6.1)$$

Table 6.1. Results of Position Control Test of the BLDC Drive

Set Position	Actual Position	Error
65535 (4π)	65032 (3.93π)	1.75%
1 (-4π)	153 (-3.98π)	0.5%

The measured percentage error is higher than desired. The hardware constraints mentioned earlier limit the capabilities of the BLDC motor. Also, the motor as a strong indent as the rotor magnet interact with stator due to the low pole-pair count.

6.4. Root Cause Analysis

The behavior of the BLDC drive during motor stall condition is conducted to validate the operation of software current limiter. An unfortunate chain of events led to the partial failure of the drive system. The failure however gave rise to an opportunity to analyze and better understand it. This study is crucial in development phase as results help in improving future iterations of the drive. The events leading to the failure are listed below.

1. To validate software current limiter, the motor is subjected to stall condition
2. The motor in stall condition tends to draw high current
3. In motor mode, due to a controller hiccup and driver IC malfunctioned, causing a direct short via A and B legs of the inverter (ground loop is suspected)
4. This caused the shunt resistors to overheat and desolder itself from the PCB before the fuse opened (localized heating)
5. In the process, either the MOSFET or the driver IC got permanently damaged
6. As a result, the motor is cogging, a characteristic of one phase not working
7. On further testing, the driver IC shows the following fault codes (refer Appendix A for fault codes) -

   OTW – Thermal Warning

   OTSD – Thermal Shutdown

   VDS_OCP – MOSFET Vds Overcurrent Protection

   CPUV – Charge Pump Undervoltage Lockout

Only in the case, both MOSFETs of one leg are driven ON simultaneously, the overheating event of the current sense resistor is justifiable. In the condition both switches are on simultaneously, there is direct short between power and ground via the shunt resistor that is rated at 7mΩ 3W. As the resistance is low, the current is high and extreme amounts of power is dissipated across the resistor. A simple analysis using ohms law is shown (6.2).

$$V = IR \tag{6.2}$$

Here R = ON resistance of the MOSFETs in series + resistance of current shunt

Therefore, R and I are calculated using (6.3) and (6.4) respectively,

$$R = 2 \times 1.5m\Omega + 7m\Omega = 10m\Omega \tag{6.3}$$

$$I = \frac{V}{R} = \frac{12}{10m\Omega} = 1200\text{A} \tag{6.4}$$

Power dissipation is calculated as shown in (6.5)

$$P = I^2R = 1200^2 \times 10m\Omega = 14.4\text{kW} \tag{6.5}$$

V = 12V, therefore I = 1200A, although this is theoretical maximum current, the resistance of wires and internal resistance of the battery limit it. Considering the theoretical case, the power dissipation across the resistor is 14.4kW. Considering losses, assuming current of 50A, as the battery is capable of delivering it for short durations, the power dissipated is 25W as shown in (6.6).

$$P = I^2R = 50^2 \times 10m\Omega = 25\text{W} \tag{6.6}$$

In a small area, this amount of power causes extreme localized heating. Damage caused to the shunt resistor due to overheating is shown in Fig. and a reference image of its position on the board is shown in Fig. Replacement of shunt resistors did not solve the problem as the failure occurred in the driver or MOSFET as discussed in detail in the next section.

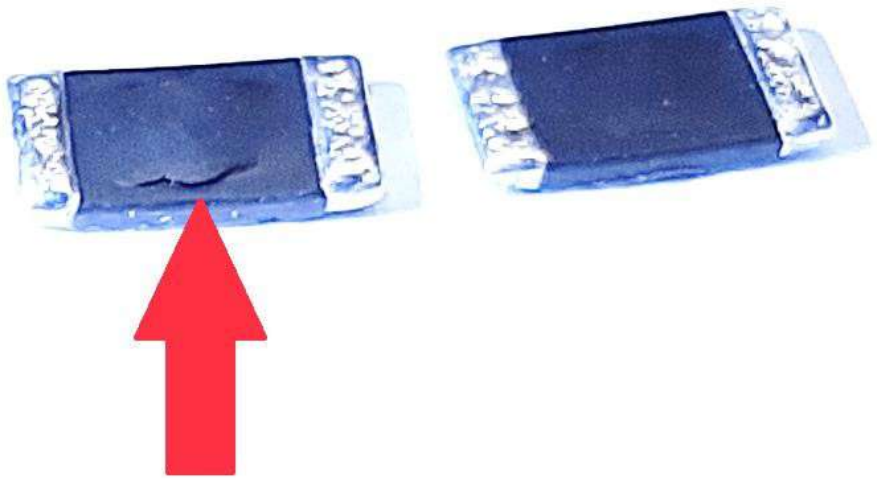

Fig. 6.8. Crack in the Shunt Resistor Due to Overheating

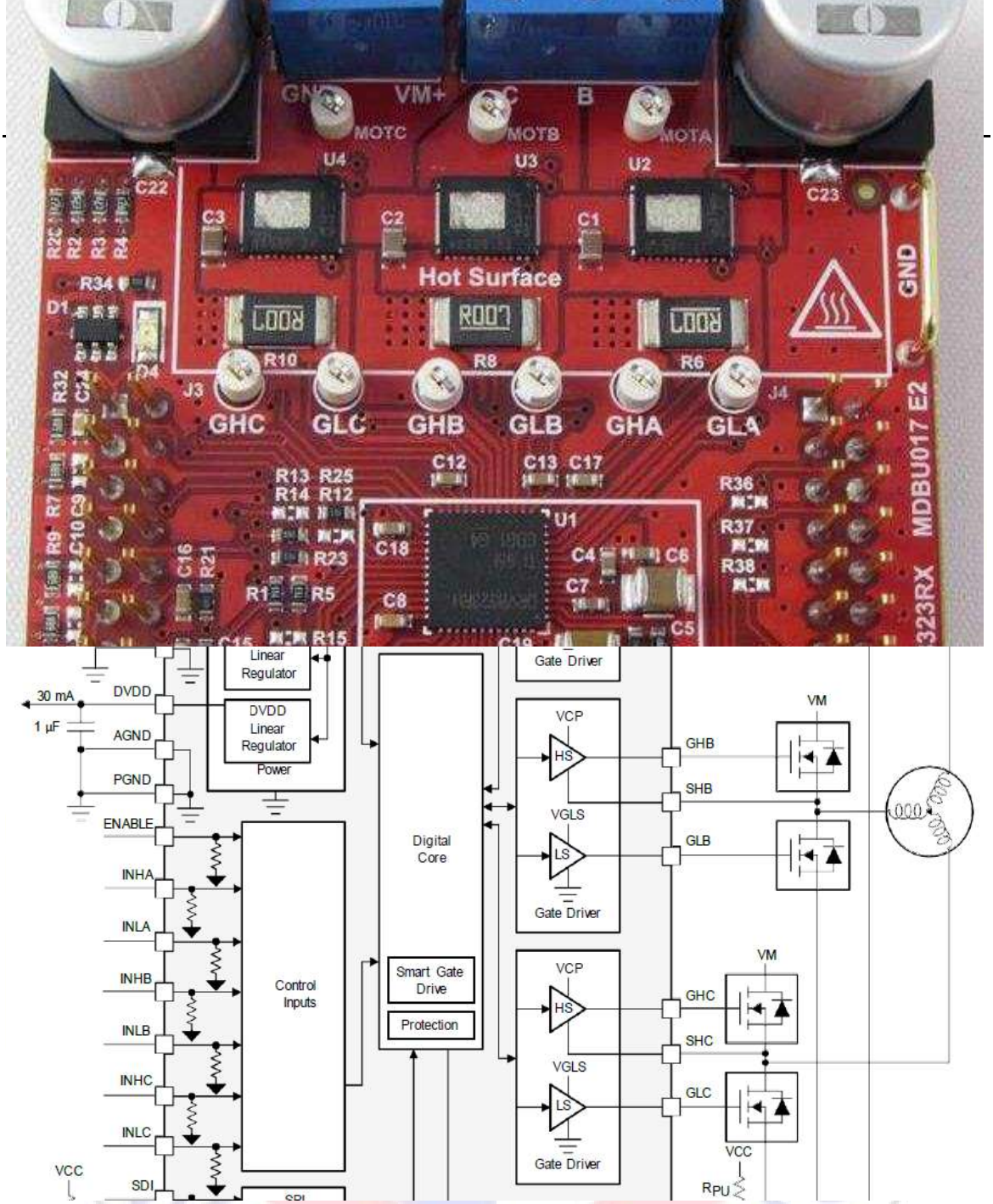

Fig. 6.10. Detailed Block Diagram of the DRV8323RS Showing No Direct Connection Between Input Signals from Microcontroller and Final Gate Driver Unit

6.4.1 Analysis of Waveforms Using Oscilloscope

Further studies are carried out with an oscilloscope to narrow down and visualize the failure. The description of the test points is listed in Table. 6.2. The reason only high side of gate control signal is probed as it makes use of the clever PWM3x mode of the DRV8323RS. The probe setup is shown in Fig. 6.11. and Fig. 6.12. the onboard test points are utilized. As the CAN bus is not utilized, components associated to it are removed and motor commands are sent via serial.

Table 6.2. Description of Test Points Considered in Root Cause Analysis

Test Point	Description	Location
GHA	High side gate drive signal of leg A	DRV8323RS Development Board
GHB	High side gate drive signal of leg B	
GHC	High side gate drive signal of leg C	
GLA	Low side gate drive signal of leg A	
GLB	Low side gate drive signal of leg B	
GLC	Low side gate drive signal of leg C	
PA10 (or INHA)	High side gate control signal of phase A	STM32F446RE
PA9 (or INHB)	High side gate control signal of phase B	
PA8 (or INHC)	High side gate signal control of phase C	

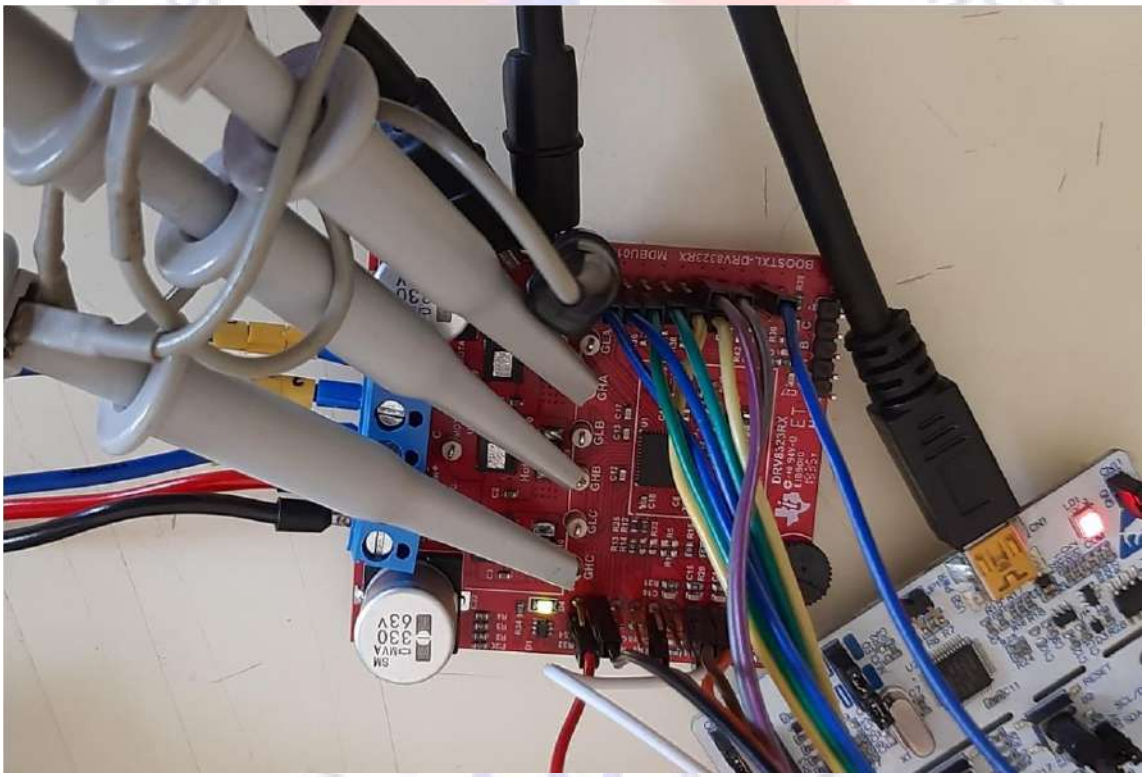

Fig. 6.11. Probing Points of the Gate Signals on DRV8323RS Development Board

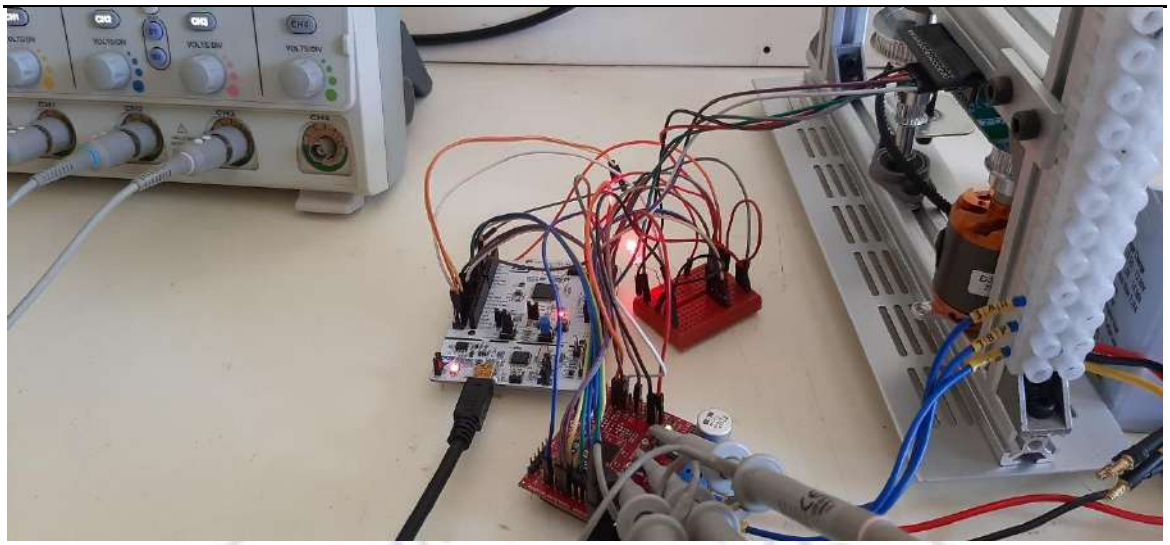

Fig. 6.12. Probing Points Shown Along with the Setup

Fig. 6.13. and Fig. 6.14. show the comparison between the gate drive signals of phases B and C, represented by Red and Green colored waveform respectively, working as desired and phase A waveform, represented by blue waveform, showing an anomality.

Fig. 6.13. High Side Gate Drive Signals Measured at Points GHA (Blue), GHB (Red) And GHC (Green) In Rotor Position Showing Phase C And Phase B Active

Closer inspection of waveforms associated to phase A is shown in Fig. 6.15. probing at high side gate drive signal represented by Red and low side gate drive signal represented by Blue. The low side gate drive signal is as expected and is complimentary to the high side gate drive signal, however, the high side gate drive signal is not able to hold the gate

drive current and is being loaded close to 0 volts, rendering phase A to malfunction. A comparison is carried out with working phase C in Fig. 6.16. that shows both high side and low side gate signal of phase C, both are complimentary as expected.

Fig. 6.14. High Side Gate Drive Signals Measured at Points GHA (Blue), GHB (Red) And GHC (Green) In Rotor Position Showing Phase C And Phase A Active, Area Enclosed in Cyan Showing Anomality at Phase A

Fig. 6.15. Gate Drive Signals Measured at Points GLA (Blue) And GHA (Red) Showing Switches Operating Complementarily with Anomality

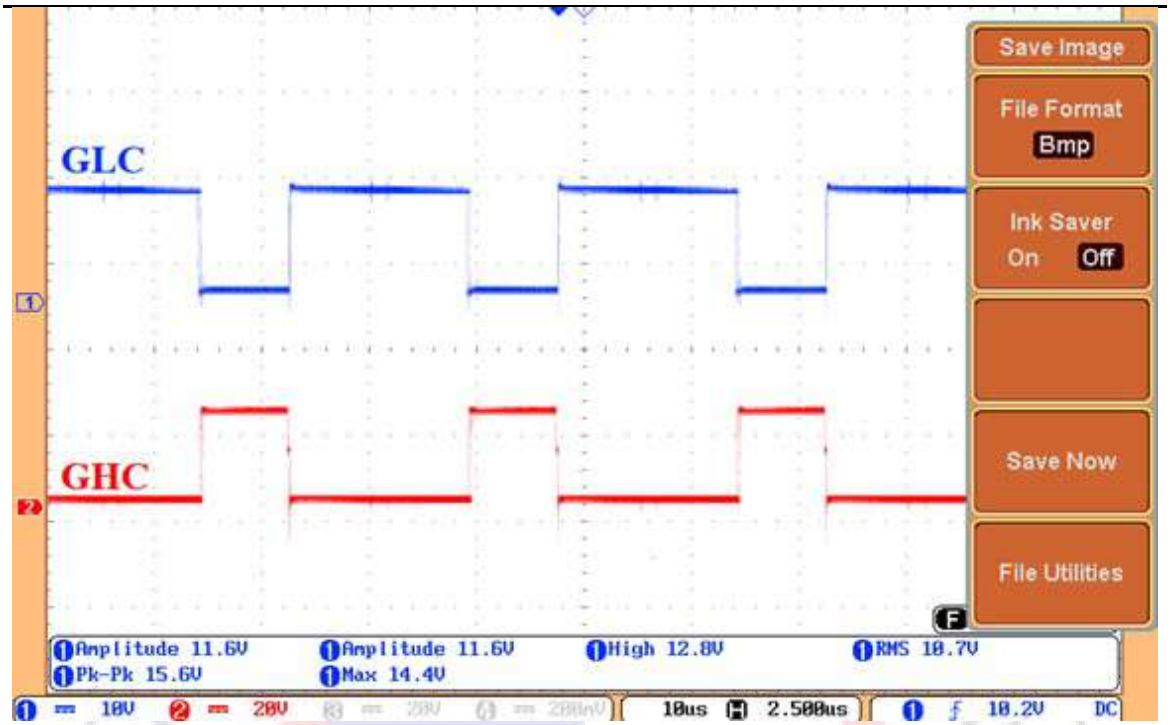

Fig. 6.16. Gate Drive Signals Measured at Points GLC (Blue) And GHC (Red) Showing Switches Operating Complementarily Working as Expected

Further testing is carried out to check behavior of the high side gate drive signals with respect to its input control waveform from the STM32F446RE microcontroller. The working phases B and C are seen in Fig. 6.17 and Fig. 6.18 the high side gate drive signals, represented by Blue, follow the gate drive control inputs represented by Red. Comparison of the working phases and the non-working phase A shown in Fig. 6.19 probed at the same corresponding points show the gate drive signal not able to follow the gate control signal, the gate drive signal is loaded and dropping to zero, although the control signal is high.

Finally, the deadtime at turn ON and turn OFF of the complementary switches of working phase C is measured. Referring to Fig. 6.20. the deadtime is set to 50ns for this test, although upon closer inspection by using the measurement tools available in the oscilloscope, the deadtime is more than 130ns at phase C low side turn ON and phase C high side turn OFF, the step in red waveform is caused by the drive signal slew rate control called “I_Drive” as shown in application waveforms in Appendix A. Referring to Fig. 6.21. the deadtime at phase C low side turn OFF and phase C high side turn ON, the deadtime is 80nS. Finally, Fig. 6.22. shows the gate control signals of phase A represented by Blue and phase C represented by Green working as expected. Due to the failure, testing related to CAN bus is not carried out.

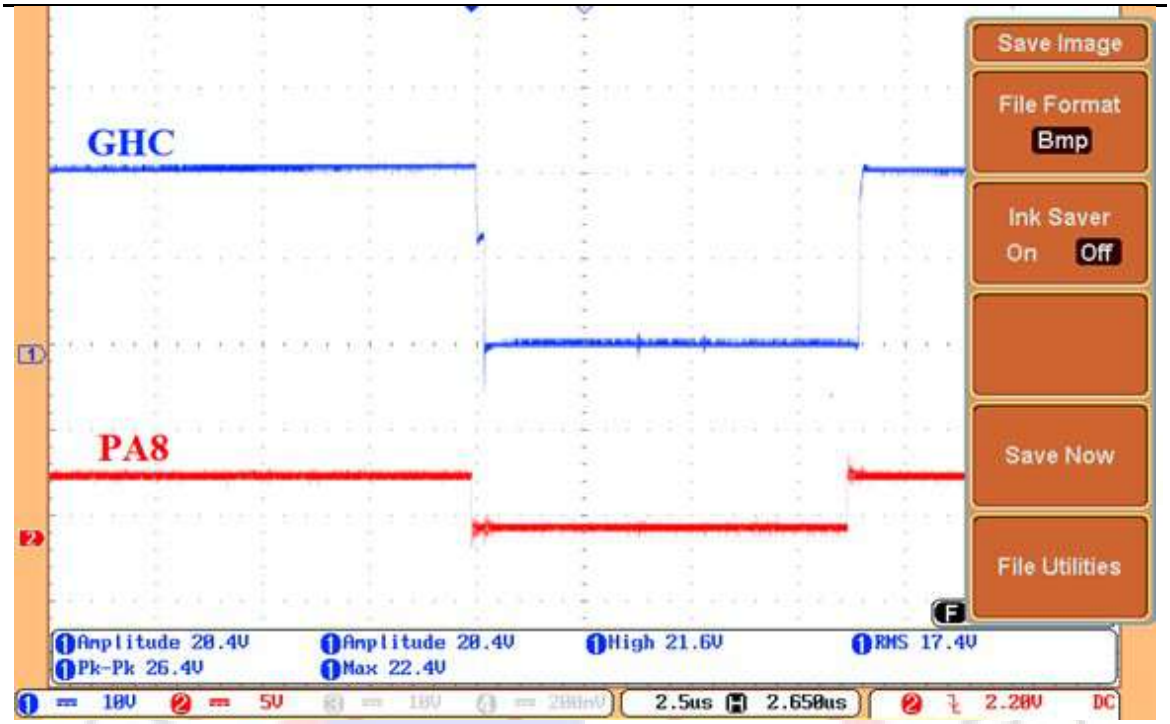

Fig. 6.17. Gate Drive Signals Measured at Points GHC (Blue) And Gate Control Signal Measured at Point PA8 (Red) Working as Expected

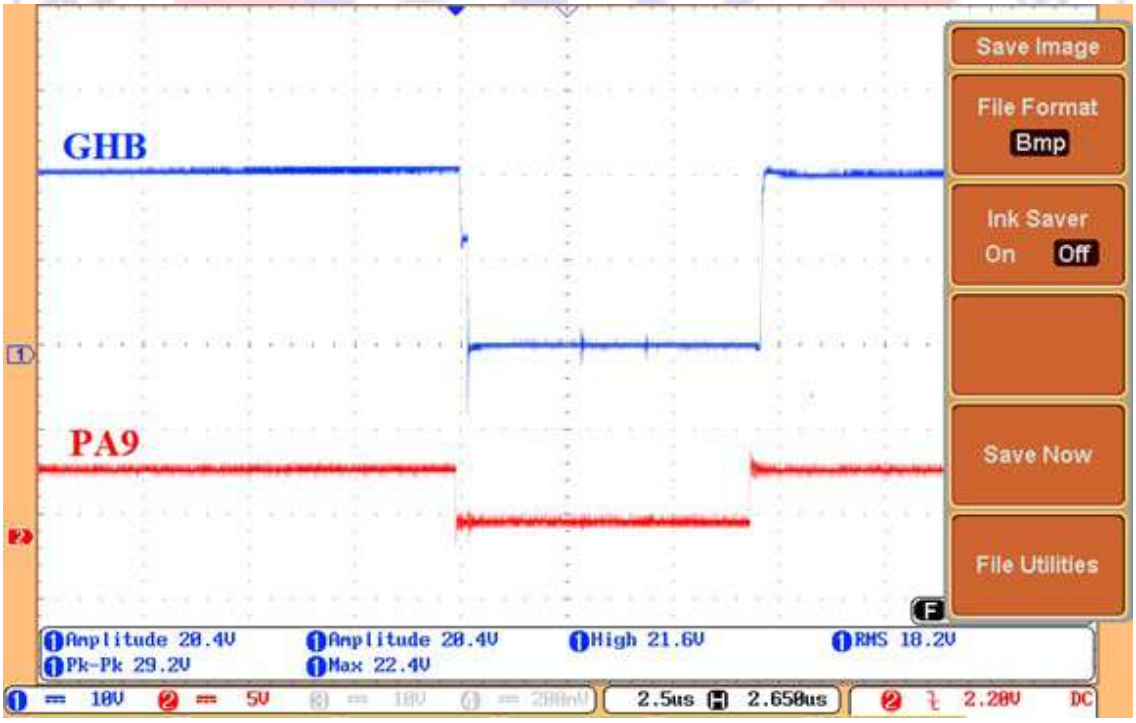

Fig. 6.18. Gate Drive Signals Measured at Points GHB (Blue) And Gate Control Signal Measured at Point PA9 (Red) Working as Expected

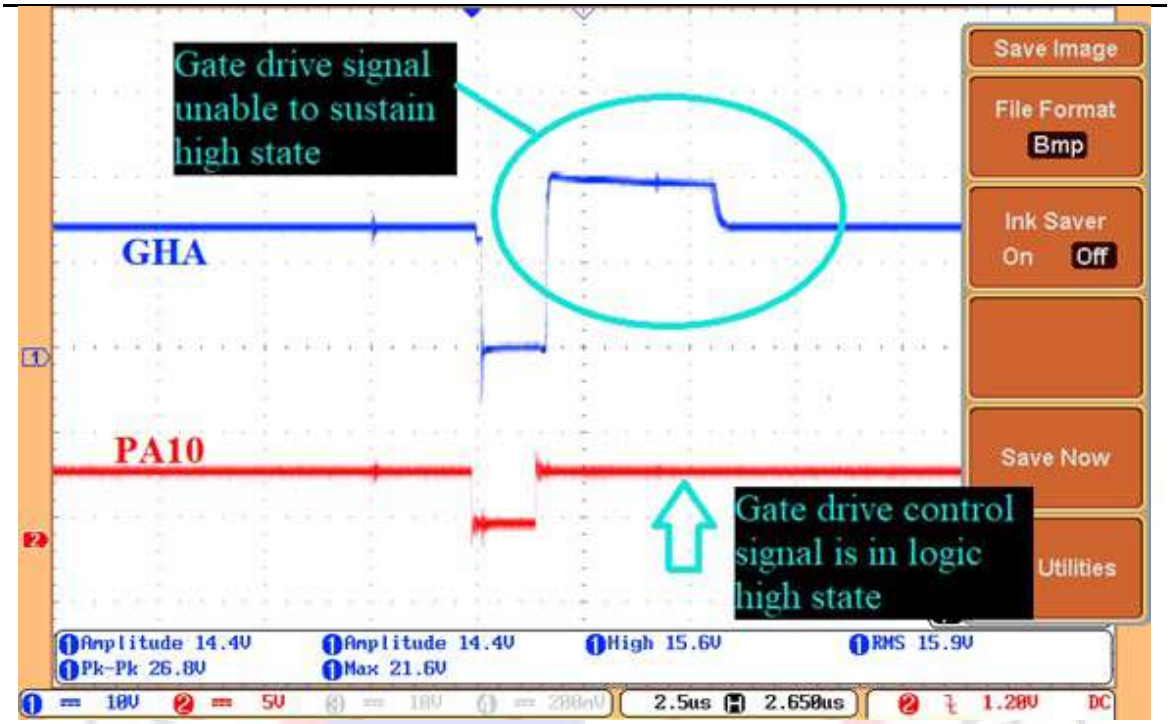

Fig. 6.19. Gate Drive Signals Measured at Points GHA (Blue) And Gate Control Signal Measured at Point PA10 (Red) Showing Anomality Marked in Cyan

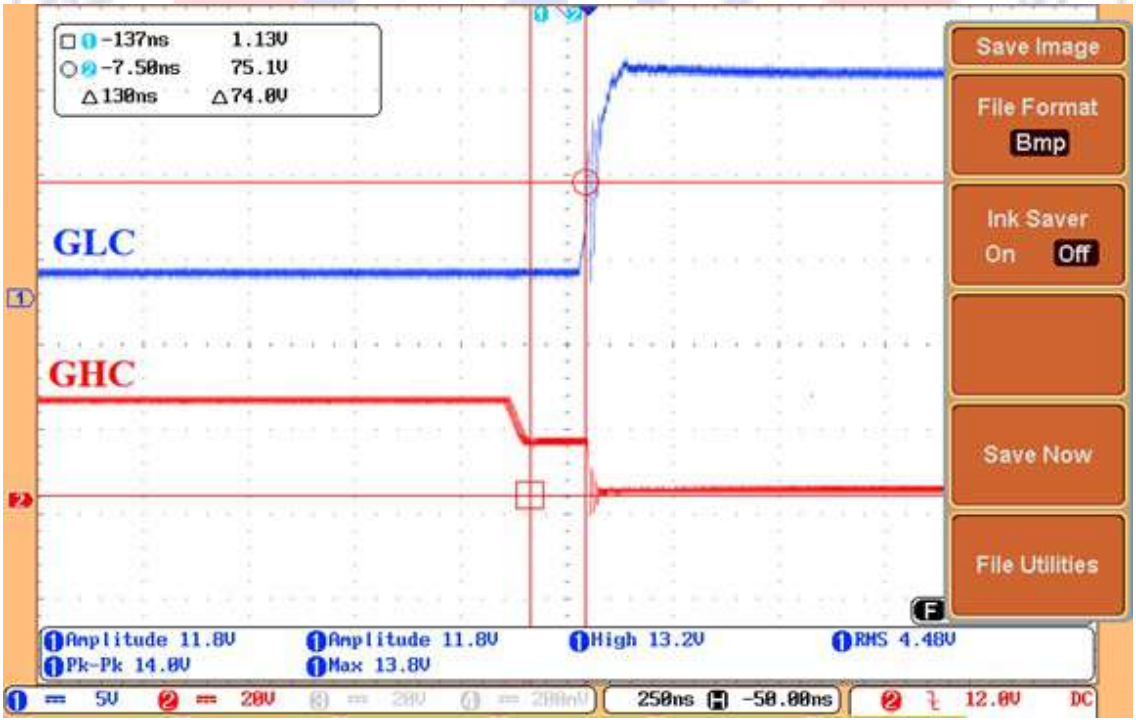

Fig. 6.20. Deadtime Measurement Between Gate Drive Signals at GHC At Turn ON (Blue) And GLC at Turn OFF (Blue) of 130ns

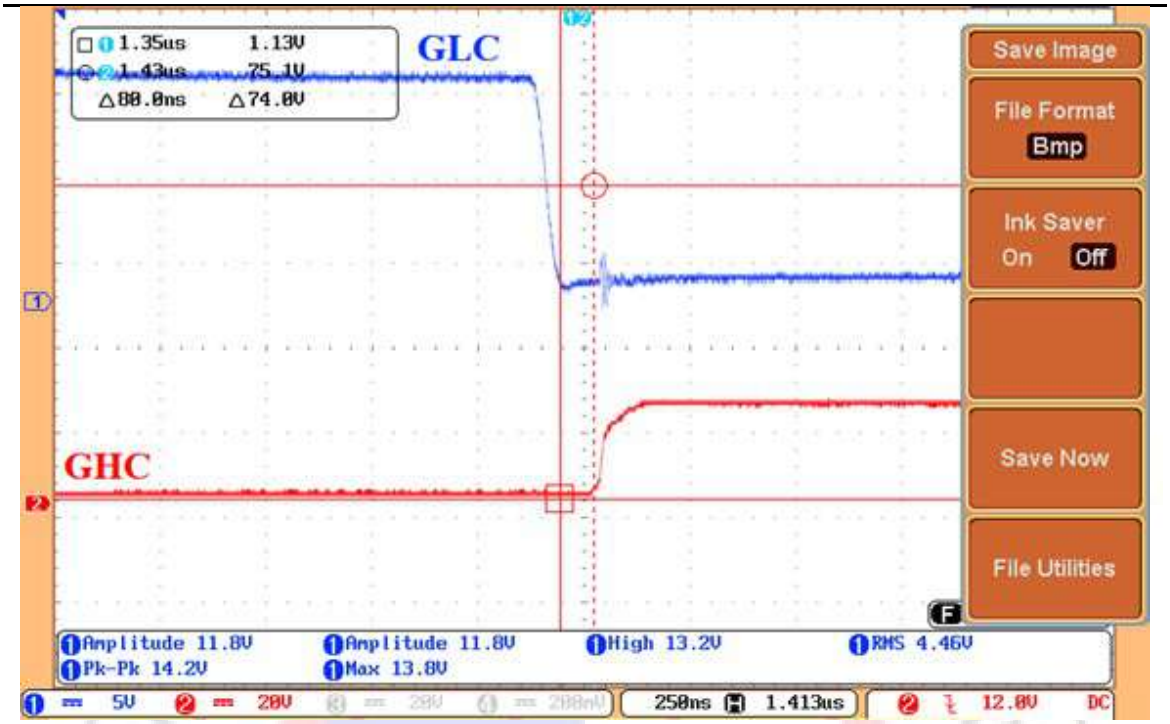

Fig. 6.21. Deadtime Measurement Between Gate Drive Signals at GHC At Turn OFF (Blue) And GLC At Turn ON (Blue) Of 80ns

Fig. 6.22. Gate Control Signals Measured at Points PA10 (Blue), PA9 (Red), PA8 (Green)

6.5. Summary

The output of the control loop gain calculating script followed by simulation results of the BLDC drive are analysed in details. Results of the hardware implementation and the root cause analysis of the failure are studied in detail with the help of waveforms.

Chapter 7

CONCLUSION AND FUTURE SCOPE

Active Exoskeleton is a wearable robotic structure that augments the user performance. The research and the market for the exoskeletons has increased in the recent years as it finds applications mainly in the military, to help soldier and improve their performance and in medical field for rehabilitation purposes. An electrically driven active exoskeleton commonly uses electric motors such as BLDC or PMSM motors and one of the most crucial components is the drive for the motor. Accurate speed and position control capabilities are desired characteristics as the performance of the entire exoskeleton depends on it. A main control system commands the drive by sending speed and position commands, the drive responds by attaining the commands. Improper response can lead to fatigue, injuries or long-term health complications. A preferred high performance BLDC motor control scheme is Field-Oriented Control.

Speed and position control of BLDC Drive using FOC is designed and implemented in this project. Due to constraints, a low power, rudimentary, validation prototype is designed. The drive is based on the Texas Instruments DRV8323RS smart gate driver IC development board containing an onboard inverter. An open-source FOC algorithm is implemented on a STM32F446RE microcontroller. MCP2545 CAN controller is used to interface between differential CAN bus and microcontroller. MA700 angle encoder along with a diametrically magnetised magnet is used for position sensing and an off-the shelf BLDC motor is used along with appropriate speed reduction stages. The whole system is powered by a 12V lead acid battery for testing. The speed and position commands are sent to the drive via an Arduino and a CAN bus interface and receive telemetry. Complementary simulations studies are performed using Simulink and control loop gains are calculated using MATLAB script.

7.1. Conclusion

A BLDC drive with the aim of accurate speed and position control was designed. FOC scheme is utilized for the implementation. Development boards are used for quick validation. The following results are obtained -

- The simulation studies with the proposed control scheme offer desired results, tracking the reference position waveform set at 4 radians at 0.1 seconds, -4 radians at 2 seconds and 0 radians at 3.5 seconds without any overshoots and negligible steady state error.

- The hardware implementation of the proposed BLDC drive was tested by commanding positions 4π radians and -4π radians. The drive was capable of maintaining the positional accuracy as desired by maintaining the error close to 1% at both commanded positions as desired.
- Motor stall test was conducted to check the behaviour of the controller and validate the functioning of the software based current limiter causing an unexpected failure of the drive due to a malfunction. Due to failure of the driver IC or MOSFET during initial phases of testing, hindered the project but an opportunity arose from the failure to conduct a detailed root cause analysis of the failure.
- Upon analysis, it was found that due to a controller/driver hiccup, a direct short led to failure of shunt resistors and in the process damaged the MOSFET/driver IC as the problem persisted after replacing the failed shunt resistors. A closer inspection of associated waveforms with an oscilloscope shows an anomality associated to phase A. The high side gate drive signal is loaded due to the failure and the driver IC is unable to sustain the voltage rendering the phase A to malfunction.

7.2. Future Scope

The future scope of the project is listed below -

- As per end user requirements, the final product intended is an integrated motor drive unit that involves a custom designed motor that directly couples to the joint without any speed reduction unit for more compact design and lower mechanical losses.
- High power density, low form factor, high efficiency, safer and stable motor driver unit with robust firmware optimized for performance is the goal.
- Miniaturization and ruggedization of the entire integrated motor drive unit for military applications.
- Exploration of other motor types such as PMSM for better efficiency and performance.

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Appendix A

Datasheets

TEXAS INSTRUMENTS

DRV8320, DRV8320R
DRV8323, DRV8323R

SLVSDJ3D – FEBRUARY 2017 – REVISED MARCH 2022

DRV832x 6 to 60-V Three-Phase Smart Gate Driver

1 Features

- Triple Half-Bridge Gate Driver
  - Drives 3 High-Side and 3 Low-Side N-Channel MOSFETs (NMOS)
- Smart Gate Drive Architecture
  - Adjustable Slew Rate Control
  - 10-mA to 1-A Peak Source Current
  - 20-mA to 2-A Peak Sink Current
- Integrated Gate Driver Power Supplies
  - Supports 100% PWM Duty Cycle
  - High-Side Charge Pump
  - Low-Side Linear Regulator
- 6 to 60-V Operating Voltage Range
- Optional Integrated Buck Regulator
  - LMR16006X SIMPLE SWITCHER®
  - 4 to 60-V Operating Voltage Range
  - 0.8 to 60-V, 600-mA Output Capability
- Optional Integrated Triple Current Sense Amplifiers (CSAs)
  - Adjustable Gain (5, 10, 20, 40 V/V)
  - Bidirectional or Unidirectional Support
- SPI and Hardware Interface Available
- 6x, 3x, 1x, and Independent PWM Modes
- Supports 1.8-V, 3.3-V, and 5-V Logic Inputs
- Low-Power Sleep Mode (12 µA)
- Linear Voltage Regulator, 3.3 V, 30 mA
- Compact QFN Packages and Footprints
- Efficient System Design With Power Blocks
- Integrated Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - MOSFET Overcurrent Protection (OCP)
  - Gate Driver Fault (GDF)
  - Thermal Warning and Shutdown (OTW/OTSD)
  - Fault Condition Indicator (nFAULT)

2 Applications

- Brushless-DC (BLDC) Motor Modules and PMSM
- Fans, Pumps, and Servo Drives
- E-Bikes, E-Scooters, and E-Mobility
- Cordless Garden and Power Tools, Lawnmowers
- Cordless Vacuum Cleaners
- Drones, Robotics, and RC Toys
- Industrial and Logistics Robots

3 Description

The DRV832x family of devices is an integrated gate driver for three-phase applications. The devices provide three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV832x generates the correct gate drive voltages using an integrated charge pump for the high-side MOSFETs and a linear regulator for the low-side MOSFETs. The Smart Gate Drive architecture supports peak gate drive currents up to 1-A source and 2-A. The DRV832x can operate from a single power supply and supports a wide input supply range of 6 to 60 V for the gate driver and 4 to 60 V for the optional buck regulator.

The 6x, 3x, 1x, and independent input PWM modes allow for simple interfacing to controller circuits. The configuration settings for the gate driver and device are highly configurable through the SPI or hardware (H/W) interface. The DRV8323 and DRV8323R devices integrate three low-side current sense amplifiers that allow bidirectional current sensing on all three phases of the drive stage. The DRV8320R and DRV8323R devices integrate a 600-mA buck regulator.

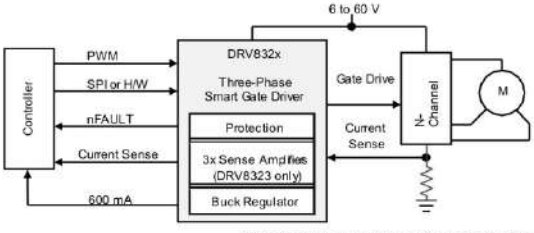
A low-power sleep mode is provided to achieve low quiescent current draw by shutting down most of the internal circuitry. Internal protection functions are provided for undervoltage lockout, charge pump fault, MOSFET overcurrent, MOSFET short circuit, gate driver fault, and overtemperature. Fault conditions are indicated on the nFAULT pin with details through the device registers for SPI device variants.

Device Information(1)

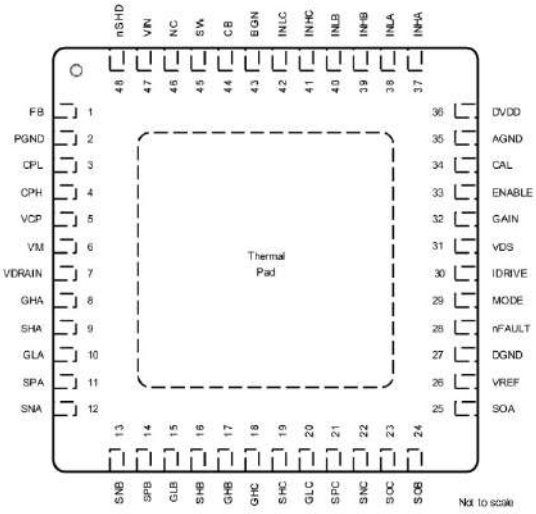
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8320	WQFN (32)	5.00 mm × 5.00 mm
DRV8320R	VQFN (40)	6.00 mm × 6.00 mm
DRV8323	WQFN (40)	6.00 mm × 6.00 mm
DRV8323R	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

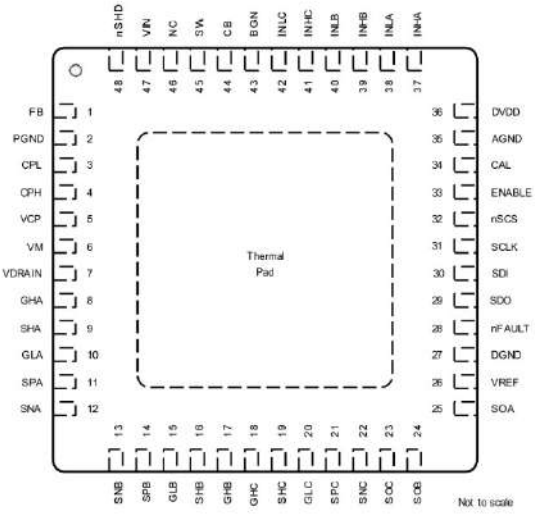
Simplified Schematic



DRV8323RH RGZ Package
48-Pin VQFN With Exposed Thermal Pad
Top View



DRV8323RS RGZ Package
48-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions—48-Pin DRV8323R Devices

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8323RH	DRV8323RS		
AGND	35	35	PWR	Device analog ground. Connect to system ground.
BGND	43	43	PWR	Buck regulator ground. Connect to system ground.
CAL	34	34	I	Amplifier calibration input. Set logic high to internally short amplifier inputs and perform auto offset calibration.
CB	44	44	PWR	Buck regulator bootstrap input. Connect a X5R or X7R, 0.1-µF, 16-V, capacitor between the CB and SW pins.
CPH	4	4	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	3	3	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DGND	27	27	PWR	Device ground. Connect to system ground.
DVDD	36	36	PWR	3.3-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	33	33	I	Gate driver enable. When this pin is logic low the device goes to a low-power sleep mode. An 8 to 40-µs low pulse can be used to reset fault conditions.
FB	1	1	I	Buck feedback input. A resistor divider from the buck post inductor output to this pin sets the buck output voltage.
GAIN	32	—	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GHA	8	8	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	17	17	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	18	18	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	10	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	15	15	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	20	20	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	30	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	37	37	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	39	39	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	41	41	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	38	38	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	40	40	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	42	42	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	29	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
NC	46	46	NC	No internal connection. This pin can be left floating or connected to system ground.
nFAULT	28	28	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain output

Pin Functions—48-Pin DRV8323R Devices (continued)

NAME	PIN NO. DRV8323RH	PIN NO. DRV8323RS	TYPE[1]	DESCRIPTION
nSCS	—	32	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSHDN	48	48	I	Buck shutdown input. Enable and disable input (high voltage tolerant). Internal pullup current source. Pull lower than 1.25 V to disable. Float to enable. Establish input undervoltage lockout with two resistor divider.
PGND	2	2	PWR	Device power ground. Connect to system ground.
SCLK	—	31	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	30	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	29	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor.
SHA	9	9	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	16	16	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	19	19	I	High-side source sense input. Connect to the high-side power MOSFET source.
SNA	12	12	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SNB	13	13	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SNC	22	22	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SOA	25	25	O	Current sense amplifier output.
SOB	24	24	O	Current sense amplifier output.
SOC	23	23	O	Current sense amplifier output.
SPA	11	11	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPB	14	14	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPC	21	21	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SW	45	45	O	Buck switch node. Connect this pin to an inductor, diode, and the CB bootstrap capacitor.
VCP	5	5	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
VDRAIN	7	7	I	High-side MOSFET drain sense input. Connect to the common point of the MOSFET drains.
VDS	31	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VIN	47	47	PWR	Buck regulator power supply input. Place an X5R or X7R, VM-rated ceramic capacitor between the VIN and BGND pins.
VM	6	6	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.
VREF	26	26	PWR	Current sense amplifier power supply input and reference. Connect a X5R or X7R, 0.1-µF, 6.3-V ceramic capacitor between the VREF and AGND pins.
Thermal Pad			PWR	Must be connected to ground

Functional Block Diagram (continued)

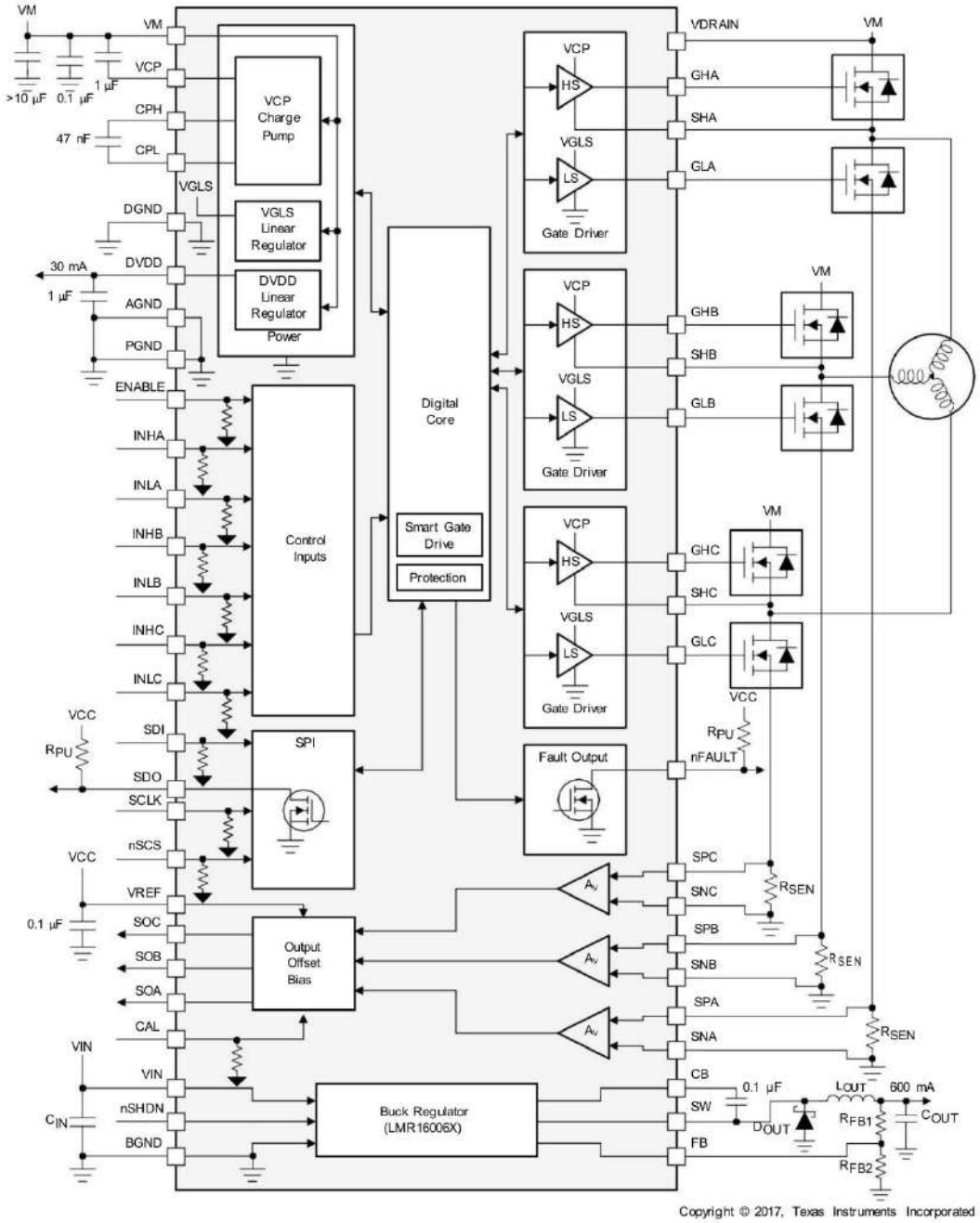


Figure 17. Block Diagram for DRV8323RS

8.3.1.1.1 6x PWM Mode (PWM_MODE = 00b or MODE Pin Tied to AGND)

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in Table 2.

Table 2. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

8.3.1.1.2 3x PWM Mode (PWM_MODE = 01b or MODE Pin = 47 kΩ to AGND)

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in Table 3.

Table 3. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

8.3.1.1.3 1x PWM Mode (PWM_MODE = 10b or MODE Pin = Hi-Z)

In 1x PWM mode, the DRV832x family of devices uses 6-step block commutation tables that are stored internally. This feature allows for a three-phase BLDC motor to be controlled using one PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to the digital outputs of the Hall effect sensor from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation); however, the mode can be configured to use asynchronous rectification (MOSFET body diode freewheeling) on SPI devices. This configuration is set using the 1PWM_COM bit in the SPI registers.

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when Hall effect sensors are directly controlling the state of the INLA, INHB, and INLB inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when the INLC pin is pulled low. This brake is independent of the state of the other input pins. Tie the INLC pin high if this feature is not required.

Table 4. Synchronous 1x PWM Mode

STATE	LOGIC AND HALL INPUTS						GATE DRIVE OUTPUTS(1)						DESCRIPTION
	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

(1) *!PWM* is the inverse of the PWM signal.

8.3.6.4 V_{SENSE} Overcurrent Protection (SEN_OCP)

Half-bridge overcurrent is also monitored by sensing the voltage drop across the external current sense resistor with the SP pin. If at any time the voltage on the SP input of the CSA exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the V_{SENSE} threshold is fixed at 1 V, t_{OCP_DEG} is fixed at 4 µs, and the OCP_MODE for V_{SENSE} is fixed for 4-ms automatic retry. On SPI devices, the V_{SENSE} threshold is set through the SEN_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: V_{SENSE} latched shutdown, V_{SENSE} automatic retry, V_{SENSE} report only, and V_{SENSE} disabled.

8.3.6.4.1 V_{SENSE} Latched Shutdown (OCP_MODE = 00b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and SEN_OCP bits are latched high in the SPI registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the SEN_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.4.2 V_{SENSE} Automatic Retry (OCP_MODE = 01b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, SEN_OCP, and corresponding sense OCP bits are latched high in the SPI registers. Normal operation starts again automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT , SEN_OCP, and sense OCP bits stay latched until the t_{RETRY} period expires.

8.3.6.4.3 V_{SENSE} Report Only (OCP_MODE = 10b)

No protective action occurs after a SEN_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT and SEN_OCP bits high in the SPI registers. The gate drivers continue to operate. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT released) when the SEN_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.4.4 V_{SENSE} Disabled (OCP_MODE = 11b or DIS_SEN = 1b)

No action occurs after a SEN_OCP event in this mode. The SEN_OCP bit can be disabled independently of the VDS_OCP bit by using the DIS_SEN SPI register.

8.3.6.5 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault may be encountered if the GHx or GLx pins are shorted to the PGND, SHx, or VM pins. Additionally, a gate driver fault may be encountered if the selected I_{DRIVE} setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin driven low. In addition, the FAULT, GDF, and corresponding VGS bits are latched high in the SPI registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the gate driver fault condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). On SPI devices, setting the DIS_GDF bit high disables this protection feature.

Gate driver faults can indicate that the selected I_{DRIVE} or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the I_{DRIVE} or t_{DRIVE} setting can resolve gate driver faults in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on.

8.3.6.6 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. When the die temperature falls lower than the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin by setting the OTW_REP bit to 1 through the SPI registers.

8.3.6.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the external MOSFETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and TSD bits are latched high. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the overtemperature condition clears. The TSD bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). This protection feature cannot be disabled.

8.4 Device Functional Modes

8.4.1 Gate Driver Functional Modes

8.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV832x family of devices. When the ENABLE pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, sense amplifiers (if present) are disabled, all external MOSFETs are disabled, the charge pump is disabled, the DVDD regulator is disabled, and the SPI bus is disabled. The LMR16006X buck regulator (if present) is not controlled by the ENABLE pin and can be operated independently of the gate driver. The t_{SLEEP} time must elapse after a falling edge on the ENABLE pin before the device goes into sleep mode.

NOTE

The INHx and INLx pins should be low before t_{RST} (max 40 µs) after ENABLE goes low to prevent the GHx and GLx outputs from entering into Hi-Z state while any of the gates are high.

Figure 43 shows the behavior of the device after ENABLE goes low when the INHx and INLx pins are low prior to the time when the driver outputs ignore the inputs 50 µs after ENABLE goes low. The GHx and GLx pins will remain low as the device begins the process to enter sleep mode. Figure 44 shows the behavior of the device if the input PWMs are not pulled low prior to the driver outputs ignoring the inputs. The GHx and GLx pins will follow the inputs for 50 µs after ENABLE goes low, then will become Hi-Z until nFAULT goes low up to 400 µs after ENABLE is low. To avoid this behavior, the INHx and INLx pins should be low before t_{RST} (max 40 µs) after ENABLE goes low as shown in Figure 43 to avoid the GHx and GLx outputs going into Hi-Z state while any of the gate outputs are high.

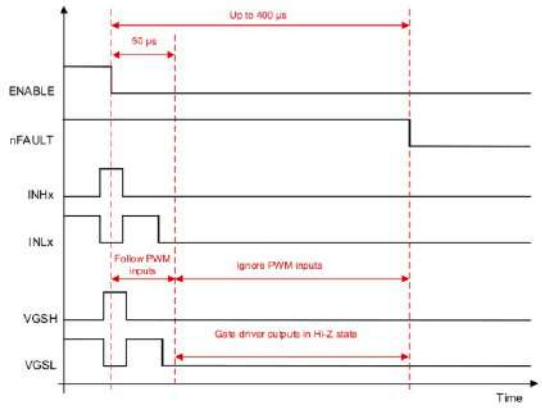


Figure 43. ENABLE Low Timing Diagram: Inputs Low Before PWM Inputs Ignored

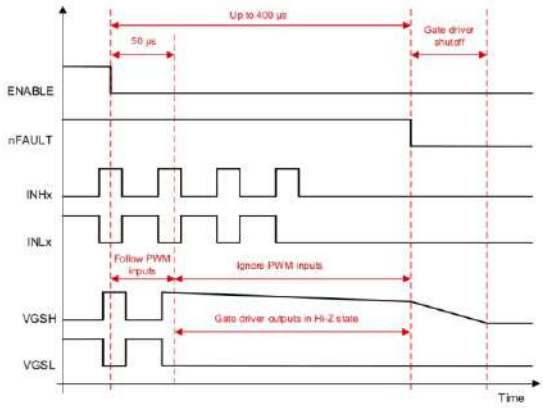


Figure 44. ENABLE Low Timing Diagram: Inputs Continue to Toggle 50 µs After ENABLE Goes Low

The device comes out of sleep mode automatically if the ENABLE pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

$$V_O = (V_{VREF} - 0.25\ V) - \frac{V_{VREF}}{2} \tag{19}$$

Use Equation 20 to calculate the approximate value of the selected sense resistor with V_O calculated using Equation 19,

$$R = \frac{V_O}{A_V \times I} \quad P_{SENSE} > I_{RMS}^2 \times R \tag{20}$$

From Equation 19 and Equation 20, select a target gain setting based on the power rating of the target sense resistor.

9.2.1.2.4.1 Example

In this system example, the value of the VREF voltage is 3.3 V with a sense current from –40 to +40 A. The linear range of the SOx output is 0.25 V to V_{VREF} – 0.25 V (from the V_{LINEAR} specification). The differential range of the sense amplifier input is –0.3 to +0.3 V (V_{DIFF}).

$$V_O = (3.3\ V - 0.25\ V) - \frac{3.3\ V}{2} = 1.4\ V \tag{21}$$

$$R = \frac{1.4\ V}{A_V \times 40\ A} \quad 2\ W > 28.3^2 \times R \rightarrow R < 2.5\ m\Omega \tag{22}$$

$$2.5\ m\Omega > \frac{1.4\ V}{A_V \times 40\ A} \rightarrow A_V > 14 \tag{23}$$

Therefore, the gain setting must be selected as 20 V/V or 40 V/V and the value of the sense resistor must be less than 2.5 mΩ to meet the power rating for the sense resistor. For this example, the gain setting was selected as 20 V/V. The value of the resistor and worst case current can be verified that R < 2.5 mΩ and I_{max} = 40 A does not violate the differential range specification of the sense amplifier input (V_{SPxD}).

9.2.1.2.5 Buck Regulator Configuration (DRV8320R and DRV8323R)

For a detailed design procedure and information on selecting the correct buck regulator external components, refer to the *LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency Eco-mode* data sheet.

9.2.1.3 Application Curves

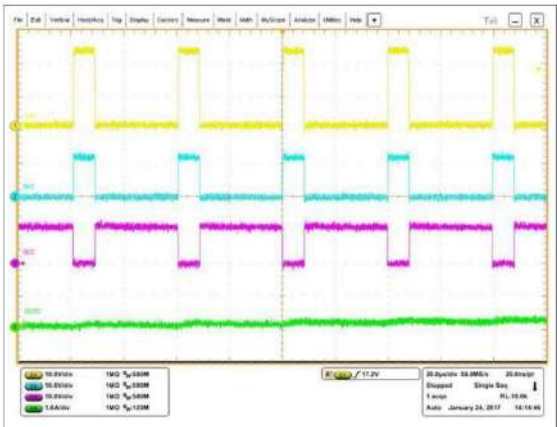


Figure 54. Gate Drive at 20% Duty Cycle

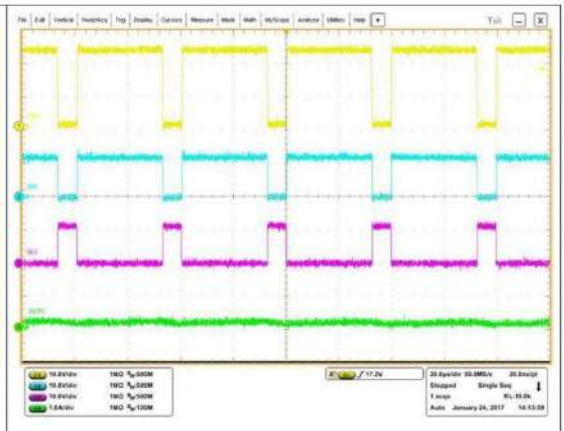


Figure 55. Gate Drive at 80% Duty Cycle

Figure 56. BLDC Motor Commutation 1000 RPM

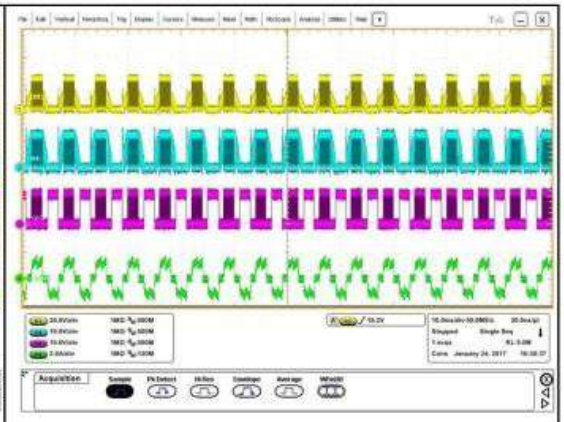


Figure 57. BLDC Motor Commutation 2000 RPM

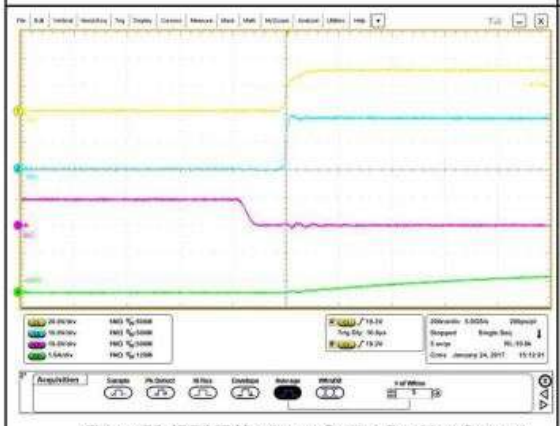


Figure 58. IDRIVE Maximum Setting Positive Current

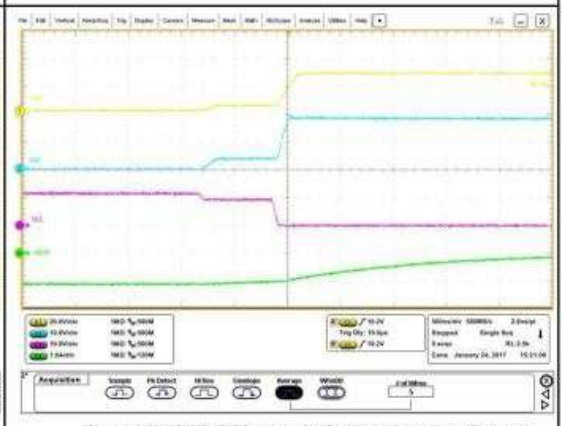


Figure 59. IDRIVE Maximum Setting Negative Current

Figure 60. IDRIVE Minimum Setting Positive Current

Figure 61. IDRIVE Minimum Setting Negative Current

Figure 62. IDRIVE 260 to 520-mA Setting Negative Current

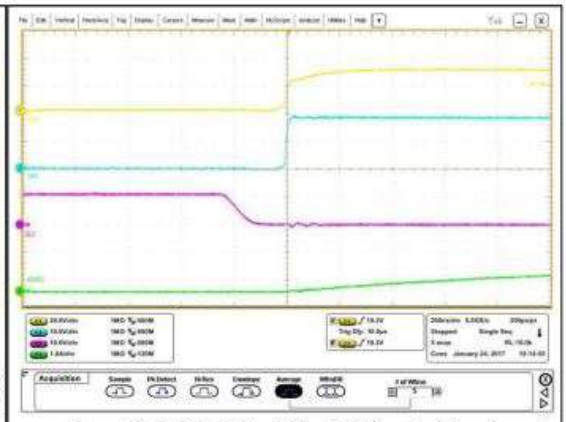


Figure 63. IDRIVE 260 to 520-mA Setting Positive Current

Ordering & quality | Technical documentation | Design & development | Support & training

TEXAS INSTRUMENTS

CSD88584Q5DC

SLPS598D – MAY 2017 – REVISED DECEMBER 2018

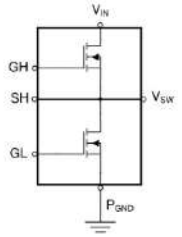
CSD88584Q5DC 40-V Half-Bridge NexFET™ Power Block

1 Features

- Half-bridge power block
- High-density SON 5-mm × 6-mm footprint
- Low $R_{DS(ON)}$ for minimized conduction losses
  - 2.4-W P_{Loss} at 35 A
- DualCool™ thermally enhanced package
- Ultra-Low-inductance package
- RoHS compliant
- Halogen free
- Lead-free terminal plating

2 Applications

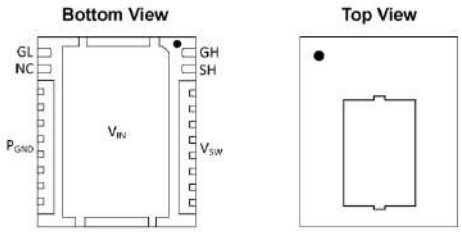
- Three-Phase Bridge for Brushless DC Motor Control
- Up to 8s Battery Power Tools
- Other Half and Full Bridge Topologies



Power Block Schematic

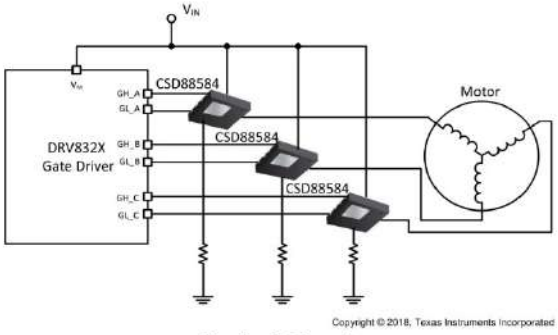
3 Description

The CSD88584Q5DC 40-V power block is an optimized design for high-current motor control applications, such as handheld, cordless garden and power tools. This device utilizes TI's patented stacked die technology in order to minimize parasitic inductances while offering a complete half bridge in a space saving thermally enhanced DualCool™ 5-mm × 6-mm package. With an exposed metal top, this power block device allows for simple heat sink application to draw heat out through the top of the package and away from the PCB, for superior thermal performance at the higher currents demanded by many motor control applications.

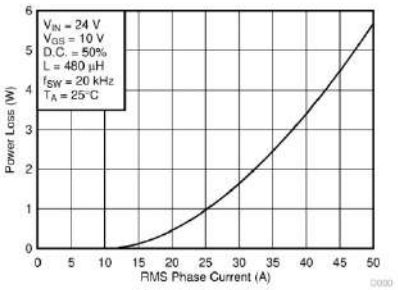


Device Information

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD88584Q5DC	2500	13-Inch Reel	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel
CSD88584Q5DCT	250	7-Inch Reel		



Typical Circuit



Power Loss vs Output Current

The Future of Analog IC Technology

MagAlpha MA700

Angular Sensor for Position Control with Side-Shaft Positioning Capability

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MagAlpha MA700 is a robust, contactless, angle encoder. The IC detects the absolute angular position of a permanent magnet, typically a diametrically magnetized cylinder attached to the rotor. The data acquisition and processing is extremely fast, allowing accurate angle measurement at speeds from 0 to 100,000 RPM

The MA700 supports a wide range of magnetic field strengths and spatial configurations, which help to relax mechanical tolerances and simplify system design. Both end-of-shaft magnet and off axis magnet positioning (side-shaft mounting) topologies are supported.

Please See Position Sensor Design Support for All Supporting Software

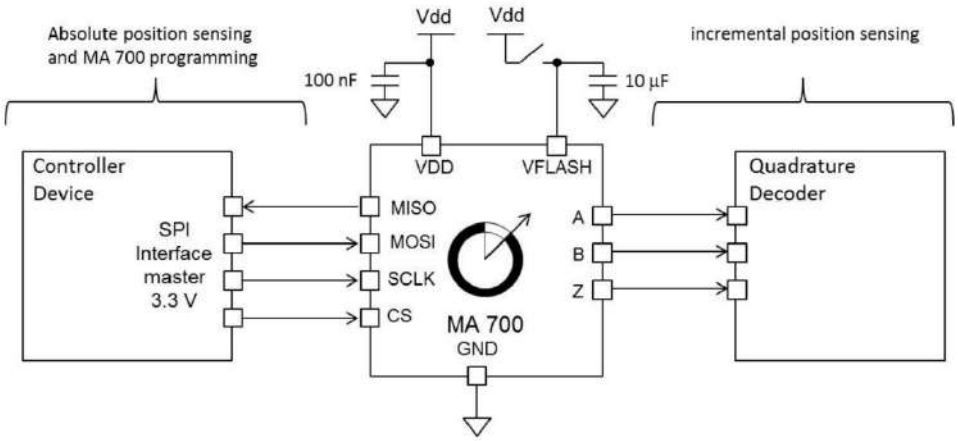
FEATURES

- 11-Bit Resolution Absolute Angle Encoder
- 500kHz Refresh Rate
- Ultra-Low Latency: 3µs
- Serial Interface for Data Readout and settings
- 10-Bit Incremental Output (A, B, Z)
- Built-In Linearization for Side-Shaft Mounting
- 3.3V, 7.7mA Supply
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Servo Drives
- Robotics
- Automotive
- PSM/BLDC Motors
- Encoders

TYPICAL APPLICATION



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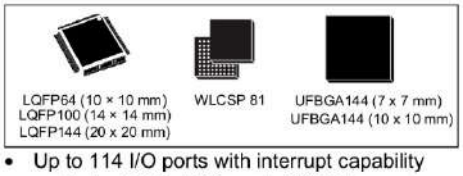
STM32F446xC/E

Arm® Cortex®-M4 32-bit MCU+FPU, 225 DMIPS, up to 512 KB Flash/128+4 KB RAM, USB OTG HS/FS, seventeen TIMs, three ADCs and twenty communication interfaces

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator) allowing 0-wait state execution from Flash memory, frequency up to 180 MHz, MPU, 225 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - 512 Kbytes of Flash memory
  - 128 Kbytes of SRAM
  - Flexible external memory controller with up to 16-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND Flash memories
  - Dual mode QuadSPI interface
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4 to 26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20×32 bit backup registers plus optional 4 KB backup SRAM
- 3× 12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2× 12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: 2x watchdog, 1x SysTick timer and up to twelve 16-bit and two 32-bit timers up to 180 MHz, each with up to four IC/OC/PWM or pulse counter
- Debug mode
  - SWD and JTAG interfaces
  - Cortex®-M4 Trace Macrocell™



LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)
LQFP144 (20 x 20 mm)

WLCSP 81

UFBGA144 (7 x 7 mm)
UFBGA144 (10 x 10 mm)

- Up to 114 I/O ports with interrupt capability
  - Up to 111 fast I/Os up to 90 MHz
  - Up to 112 5 V-tolerant I/Os
- Up to 20 communication interfaces
  - SPDIF-Rx
  - Up to 4× I^2C interfaces (SMBus/PMBus)
  - Up to four USARTs and two UARTs (11.25 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to four SPIs (45 Mbits/s), three with muxed I^2S for audio class accuracy via internal audio PLL or external clock
  - 2x SAI (serial audio interface)
  - 2× CAN (2.0B Active)
  - SDIO interface
  - Consumer electronics control (CEC) I/F
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - Dedicated USB power rail enabling on-chip PHYs operation throughout the entire MCU power supply range
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part numbers
STM32F446xC/E	STM32F446MC, STM32F446ME, STM32F446RC, STM32F446RE, STM32F446VC, STM32F446VE, STM32F446ZC, STM32F446ZE.

January 2021 DS10693 Rev 10 1/198

This is information on a product in full production. www.st.com

Appendix B

Code

AB.1. Motor Controller Code

Open-Source Code Details -

Author – Ben Katz

Link - https://os.mbed.com/users/benkatz/code/HKC_MiniCheetah/

IDE – Mbed Online IDE

Only the modified sections of the code are included –

1. CAN_com.cpp

```
#include "CAN_com.h"
 #define P_MIN -12.5f
 #define P_MAX 12.5f
 #define V_MIN -65.0f
 #define V_MAX 65.0f
 #define KP_MIN 0.0f
 #define KP_MAX 50.0f
 #define KD_MIN 0.0f
 #define KD_MAX 0.6f
 #define T_MIN -0.5f
 #define T_MAX 0.5f
void pack_reply(CANMessage *msg, float p, float v, float t){
    int p_int = float_to_uint(p, P_MIN, P_MAX, 16);
    int v_int = float_to_uint(v, V_MIN, V_MAX, 12);
    int t_int = float_to_uint(t, -T_MAX, T_MAX, 12);
    msg->data[0] = CAN_ID;
    msg->data[1] = p_int>>8;
    msg->data[2] = p_int&0xFF;
    msg->data[3] = v_int>>4;
    msg->data[4] = ((v_int&0xF)<<4) + (t_int>>8);
    msg->data[5] = t_int&0xFF;
    printf(" Commands:\n\r");
void unpack_cmd(CANMessage msg, ControllerStruct * controller){
        int p_int = (msg.data[0]<<8)|msg.data[1];
        int v_int = (msg.data[2]<<4)|(msg.data[3]>>4);
```

```
    int kp_int = ((msg.data[3]&0xF)<<8)|msg.data[4];
    int kd_int = (msg.data[5]<<4)|(msg.data[6]>>4);
    int t_int = ((msg.data[6]&0xF)<<8)|msg.data[7];
    controller->p_des = uint_to_float(p_int, P_MIN, P_MAX, 16);
    controller->v_des = uint_to_float(v_int, V_MIN, V_MAX, 12);
    controller->kp = uint_to_float(kp_int, KP_MIN, KP_MAX, 12);
    controller->kd = uint_to_float(kd_int, KD_MIN, KD_MAX, 12);
    controller->t_ff = uint_to_float(t_int, T_MIN, T_MAX, 12);
  //printf("Received   ");
  //printf("%.3f  %.3f  %.3f  %.3f  %.3f   %.3f", controller->p_des, controller->v_des, controller->kp, controller->kd, controller->t_ff, controller->i_q_ref);
  //printf("\n\r");
  }
```

2. current_controller_config.h

```
#ifndef CURRENT_CONTROLLER_CONFIG_H
#define CURRENT_CONTROLLER_CONFIG_H
// Current controller///
#define K_D .05f                // Loop gain,  Volts/Amp
#define K_Q .05f                // Loop gain,  Volts/Amp
#define K_SCALE 0.0001f         // K_loop/Loop BW (Hz) 0.0042
#define KI_D 0.0455f            // PI zero, in radians per sample
#define KI_Q 0.0455f            // PI zero, in radians per sample
#define V_BUS 12.0f             // Volts
#define OVERMODULATION 1.15f    // 1.0 = no overmodulation
#define D_INT_LIM V_BUS/(K_D*KI_D)  // Amps*samples
#define Q_INT_LIM V_BUS/(K_Q*KI_Q)  // Amps*samples
//Observer//
#define DT 0.000025f
```

3. hw_config.h

```
#ifndef HW_CONFIG_H
#define HW_CONFIG_H
#define PIN_U PA_10
#define PIN_V PA_9
#define PIN_W PA_8
#define ENABLE_PIN PA_11        // Enable gate drive pin
```

```
#define LED         PC_5        // LED Pin
#define I_SCALE 0.1007080075f    //0.00287737165f  // Amps per A/D Count
#define V_SCALE 0.012890625f     // Bus volts per A/D Count
#define DTC_MAX 0.94f          // Max phase duty cycle
#define DTC_MIN 0.0f          // Min phase duty cycle
#define PWM_ARR 0x8CA           /// timer autoreload value
#define DTC_COMP .000f          /// deadtime compensation (100 ns / 25 us)
#endif
```

4. motor_config.h

```
#ifndef MOTOR_CONFIG_H
#define MOTOR_CONFIG_H
#define R_PHASE 0.1f          //Ohms
#define L_D 0.00004f          //Henries
#define L_Q 0.00004f          //Henries
#define KT .012f              //N-m per peak phase amp, = WB*NPP*3/2
#define NPP 12                //Number of pole pairs
#define GR 6.0f               //Gear ratio
#define KT_OUT 0.07f          //KT*GR
#define WB 0.0011f            //Flux linkage, Webers.
#define R_TH 1.25f            //Kelvin per watt
#define INV_M_TH 0.02825f     //Kelvin per joule
#define T_AMBIENT 25.0f       // ambient temperature during temp calibration
```

5. main.cpp

```
  if(isnan(E_OFFSET)){E_OFFSET = 0.0f;}
  if(isnan(M_OFFSET)){M_OFFSET = 0.0f;}
  if(isnan(I_BW) || I_BW==-1){I_BW = 1000;}
  if(isnan(I_MAX) || I_MAX ==-1){I_MAX=5;}
  if(isnan(I_FW_MAX) || I_FW_MAX ==-1){I_FW_MAX=1.5f;}
  if(isnan(CAN_ID) || CAN_ID==-1){CAN_ID = 1;}
  if(isnan(CAN_MASTER) || CAN_MASTER==-1){CAN_MASTER = 0;}
  if(isnan(CAN_TIMEOUT) || CAN_TIMEOUT==-1){CAN_TIMEOUT = 1000;}
  if(isnan(R_NOMINAL) || R_NOMINAL==-1){R_NOMINAL = 0.0f;}
  if(isnan(TEMP_MAX) || TEMP_MAX==-1){TEMP_MAX = 125.0f;}
  if(isnan(I_MAX_CONT) || I_MAX_CONT==-1){I_MAX_CONT = 1.7f;}
```

```
    if((state == MOTOR_MODE))
    {
      int p_int = 1;
      if (!enable) {
        p_int = 65535;
        }
      else {
        p_int = 1;
        }
      int v_int = 500;
      int kp_int = 2000;
      int kd_int = 2000;
      int t_int = 500;
      controller.p_des = uint_to_float(p_int, -12.5f, 12.5f, 16);
      controller.v_des = uint_to_float(v_int, -65.0f, 65.0f, 12);
      controller.kp = uint_to_float(kp_int, 0.0f, 50.0f, 12);
      controller.kd = uint_to_float(kd_int, 0.0f, 0.6f, 12);
      controller.t_ff = uint_to_float(t_int, -0.5f, 0.5f, 12);
      pc.printf("%f \t %f \t %f \t \n\r" ,controller.theta_mech, controller.dtheta_mech,
controller.i_q_filt*KT_OUT);
}
```

AB.2. Main Controller Code

Open-Source Code Details –

IDE – Arduino IDE

```
void pack_cmd() {
  byte buf[8];
  ///limit data to within bounds///
  float p_des = constrain(p_in, P_MIN, P_MAX);
  float v_des = constrain(v_in, V_MIN, V_MAX);
  float kp = constrain(kp_in, KP_MIN, KP_MAX);
  float kd = constrain(kd_in, KD_MIN, KD_MAX);
  float t_ff = constrain(t_in, T_MIN, T_MAX);
  /// convert floats to unsugned ints///
  unsigned int p_int = float_to_uint(p_des, P_MIN, P_MAX, 16);
  unsigned int v_int = float_to_uint(v_des, V_MIN, V_MAX, 12);
  unsigned int kp_int = float_to_uint(kp, KP_MIN, KP_MAX, 12);
```

```
  unsigned int kd_int = float_to_uint(kd, KD_MIN, KD_MAX, 12);
  unsigned int t_int = float_to_uint(t_ff, T_MIN, T_MAX, 12);
  /// pack ints into the CAN buffer///
  buf[0] = p_int >> 8;
  buf[1] = p_int & 0xFF;
  buf[2] = v_int >> 4;
  buf[3] = ((v_int & 0xF) << 4) | (kp_int >> 8);
  buf[4] = kp_int & 0xFF;
  buf[5] = kd_int >> 4;
  buf[6] = ((kd_int & 0xF) << 4) | (t_int >> 8);
  buf[7] = t_int & 0xFF;
  CAN.sendMsgBuf(0x01, 0, 8, buf);
}

void unpack_reply() {
  byte len = 0;
  byte buf[8];
  CAN.readMsgBuf(&len, buf);
  unsigned long canID = CAN.getCanId();
  ///unpack ints from can buffer///
  unsigned int id = buf[0];
  unsigned int p_int = (buf[1] << 8) | buf[2];
  unsigned int v_int = (buf[3] << 4) | (buf[4] >> 4);
  unsigned int i_int = ((buf[4] & 0xF) << 8) | buf[5];
  ///convert uints to floats///
  p_out = uint_to_float(p_int, P_MIN, P_MAX, 16);
  v_out = uint_to_float(v_int, V_MIN, V_MAX, 12);
  t_out = uint_to_float(i_int, -T_MAX, T_MAX, 12);
}

unsigned int float_to_uint(float x, float x_min, float x_max, int bits) {
  ///converts a float to an unsigned int, given range and number of bits///
  float span = x_max - x_min;
  float offset = x_min;
  unsigned int pgg = 0;
  if (bits == 12) {
    pgg = (unsigned int)((x - offset) * 4095.0 / span);
```

```
  }
  if (bits == 16) {
    pgg = (unsigned int) ((x - offset) * 65535.0 / span);
  }
  return pgg;
}

float uint_to_float(unsigned int x_int, float x_min, float x_max, int bits) {
  float span = x_max - x_min;
  float offset = x_min;
  float pgg = 0;
  if (bits == 12) {
    pgg = ((float)x_int) * span / 4095.0 + offset;
  }
  if (bits == 16) {
    pgg = ((float)x_int) * span / 65535.0 + offset;
  }
  return pgg;
}
```

AB.3. MATLAB Gain Calculating Code

```
clear()
%%% System Parameters %%%
R = .01; % Resistance in Ohms
L = 0.00004; % Inductance in Henries
Ts = .000025; % Sample period
wc = pi/10; % Crossover frequency, in Radians per sample
%%%
s = tf('s');
sys = 1/(L*s + R); % Continuous time transfer function
z = tf('z', Ts);
sys_d = c2d(sys, Ts); % Zero order hold equivalent
ki = 1-exp(-R*Ts/L) % Calculate Ki
k = R*((wc)/(1-exp(-R*Ts/L))) % Calculate loop gain
controller = k*(1 + ki/((z-1))); % PI controller transfer function
```

```
fp = series(controller, sys_d); % Forward Path

cl = feedback(fp, 1); % Unity feedback

%%% Plot open-loop, return ratio, and controller bode plots %%%

figure;

hold all

bode(controller);

bode(sys_d);

margin(fp);

legend('Controller', 'Plant', 'Return Ratio')

%%% Plot closed-loop step response %%%

figure;step(cl);
```

Appendix C

Exoskeleton Power and Torque Requirements Based on Human Biomechanics - Army Research Laboratory, USA

muscle mechanics, energy transfer, and neural factors. Therefore, actuator and power supply design criteria should be based on data from locomotion studies, not isokinetic studies.

Table 2. Maximum joint moments during walking, running, and concentric isokinetic testing

Joint	Muscle Group	Walking	Running	Isokinetic
Hip	Extensors	15-140 [100]	40-80	300
	Flexors	40-120 [70]		170
Knee	Extensors	5-140 [80]	125-273	235 (50°/s), 166 (60°/s), 154 (180°/s), 120 (400°/s)
	Flexors	15-50 [30]		93 (60°/s), 70 (180°/s)
Ankle	Plantarflexors	85-165 [130]	180-240	89 (30°/s), 50 (90°/s), 21 (180°/s)

Note: Moments given in newton meters; average peak values in brackets; angular velocities in parentheses. For walking, knee angular velocity is ≈ 100°/s, and ankle angular velocity is ≈ 50°/s at the time when peak moment occurs.

Table 3. Maximum joint powers generated during walking, running, and concentric isokinetic testing

Joint	Muscle Group	Walking	Running	Isokinetic
Hip	Extensors	0-175	160-660	200 (100°/s)
Knee	Extensors	10-235	210-1050	205 (50°/s), 840 (400°/s)
	Flexors	10-50		97 (60°/s), 220 (180°/s)
Ankle	Plantarflexors	180-790	550-1580	47 (30°/s), 79 (90°/s), 66 (180°/s)

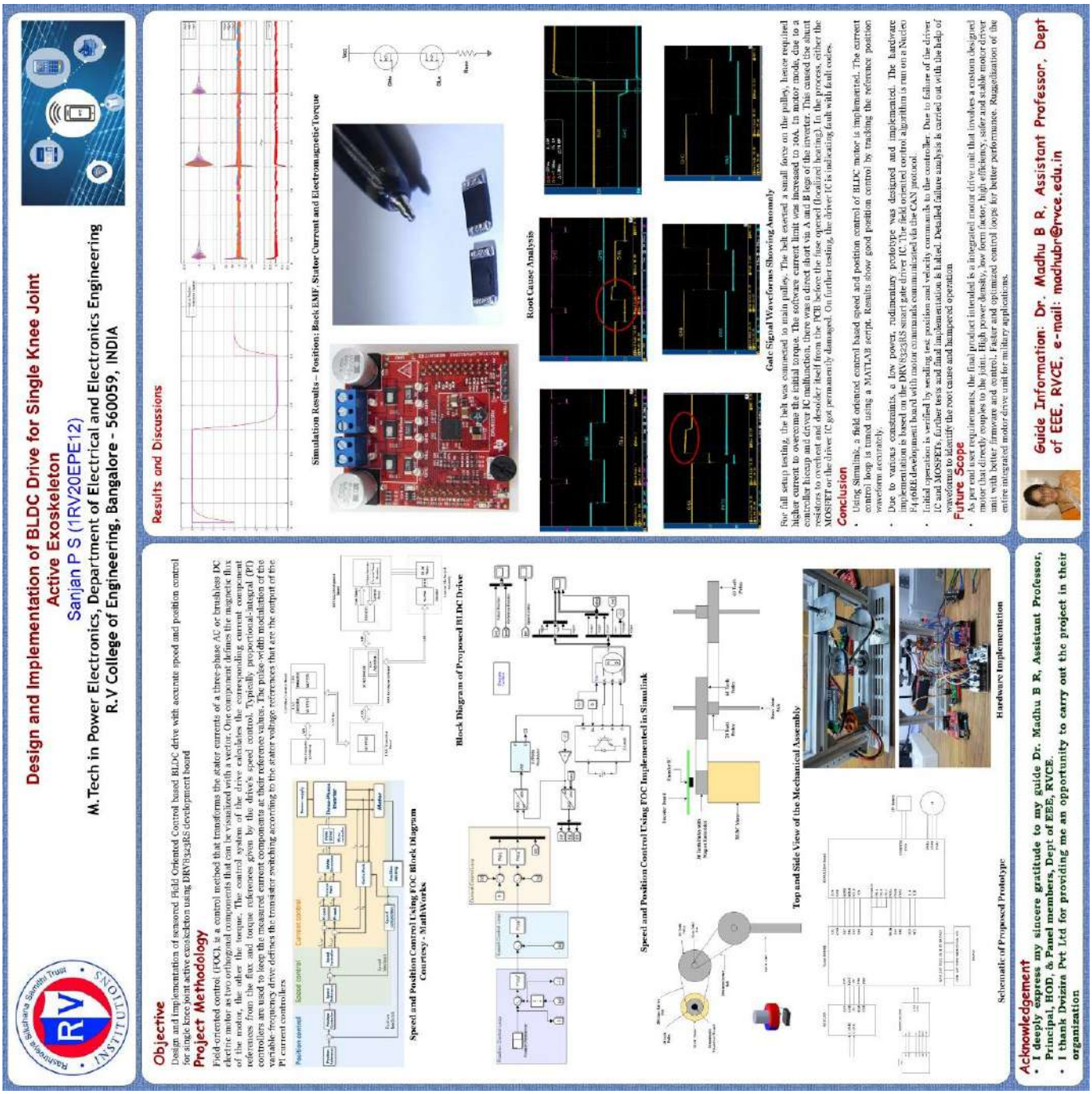
Note: Powers given in watts; angular velocities in parentheses. For walking, ankle angular velocity is ≈ 200°/s at the time when peak power occurs.

6. Lower Limb Kinematics and Kinetics for Various Activities

6.1 Walking

6.1.1 Walking at a Normal Speed

The biomechanics of "normal" walking at a natural pace are well established. Kinematic (Kadaba, Ramakrishnan, & Wootten, 1990) and normalized (to body mass) kinetic (Eng & Winter, 1995) data for all three planes of motion are given in Appendix A (Figures A-1, A-2, and A-3 for the hip, knee, and ankle, respectively). Examining the joint angle data, one finds that the


Design and Implementation of BLDC Drive for Single Knee Joint
Active Exoskeleton
Sanjan P S (1RV20EPE12)
M.Tech in Power Electronics, Department of Electrical and Electronics Engineering
R.V College of Engineering, Bangalore - 560059, INDIA
Objective
Design and implementation of sensored Field Oriented Control based BLDC drive with accurate speed and position control for single knee joint active exoskeleton using DRV8323RS development board
Project Methodology
Field-oriented control (FOC), is a control method that transforms the stator currents of a three-phase AC or brushless DC electric motor as two orthogonal components that can be visualized with a vector. One component defines the magnetic flux of the motor, the other the torque. The control system of the drive calculates the corresponding current component references from the flux and torque references given by the drive's speed control. Typically proportional-integral (PI) controllers are used to keep the measured current components at their reference values. The pulse-width modulation of the variable-frequency drive defines the transistor switching according to the stator voltage references that are the output of the PI current controllers
Speed and Position Control Using FOC Block Diagram
Courtesy - MathWorks
Block Diagram of Proposed BLDC Drive
Speed and Position Control Using FOC Implemented in Simulink
Top and Side View of the Mechanical Assembly
Schematic of Proposed Prototype
Hardware Implementation
Results and Discussions
Simulation Results – Position; Back EMF, Stator Current and Electromagnetic Torque
Root Cause Analysis
Gate Signal Waveforms Showing Anomaly
For full setup testing, the belt was connected to main pulley. The belt exerted a small force on the pulley, hence required higher current to overcome the initial torque. The software current limit was increased to 50A. In motor mode, due to a controller hiccup and driver IC malfunction, there was a direct short via A and B legs of the inverter. This caused the shunt resistors to overheat and desolder itself from the PCB before the fuse opened (localized heating). In the process, either the MOSFET or the driver IC got permanently damaged. On further testing, the driver IC is indicating fault with fault codes.
Conclusion
Using Simulink, a field oriented control based speed and position control of BLDC motor is implemented. The current control loop is tuned using a MATLAB script. Results show good position control by tracking the reference position waveform accurately.
Due to various constraints, a low power, rudimentary prototype was designed and implemented. The hardware implementation is based on the DRV8323RS smart gate driver IC. The field oriented control algorithm is run on a Nucleo F446RE development board with motor commands communicated via the CAN protocol.
Initial operation is verified by sending test position and velocity commands to the controller. Due to failure of the driver IC and MOSFETs, further tests and final implementation is halted. Detailed failure analysis is carried out with the help of waveforms to identify the root causes and hampered operation
Future Scope
As per end user requirements, the final product intended is a integrated motor drive unit that involves a custom designed motor that directly couples to the joint. High power density, low form factor, high efficiency, safer and stable motor driver unit with better firmware and control. Faster and optimized control loops for better performance. Ruggedization of the entire integrated motor drive unit for military applications.
Acknowledgement
I deeply express my sincere gratitude to my guide Dr. Madhu B R, Assistant Professor, Principal, HOD, & Panel members, Dept of EEE, RVCE.
I thank Dvizira Pvt Ltd for providing me an opportunity to carry out the project in their organization
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Comparitive Analysis of Speed and Position Control of BLDC Motor via Field Oriented Control Using SPWM and SVPWM Schemes

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***Abstract*— In this paper, a comparative analysis is carried out on the performance of a Field Oriented Controlled (FOC) based speed and position control of BLDC motor using Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) schemes. FOC is commonly used in high performance motor driver/controller for its superior performance such as high efficiency and lower torque ripple content, especially in applications such as robotics, electric vehicles, power tools, etc. Advancements in Digital Signal Processors and lower costs have allowed this technique to be used in more high-performance applications. The overall performance also depends on PWM control scheme used. SPWM and SVPWM techniques are two most commonly used techniques in motor control and inverter control applications. Hence a comparison study is carried out with the two schemes using Simulink. In light loading conditions, the results show that the performance is quite similar, but on closer inspection, SVPWM based FOC offers better performance compared to SPWM based FOC.**

Keywords—FOC; BLDC; SVPWM; SPWM; Clarke Transformation; Park Transformation;

I. INTRODUCTION

Over the years, Brushless DC Motors (BLDC), a type of permanent magnet synchronous motor has gained wide spread popularity. Now, it is commonly used in electric vehicles, precision motor control applications such as CNCs and robotic arms, power tools, aerospace applications, drones etc. This is due to its high-power density, high efficiency, more robust and reliable compared to a typical brushed DC motor, also, high rotor speeds can be achieved and quieter operation. Typical construction of a BLDC motor uses an armature that is stationery with the three phase coils arranged 120° electrical apart and permanent magnets are attached on the rotor. Due to this type of construction, the commutation needs to be done electronically unlike a brushed DC motor that commutates mechanically. In order to control a BLDC motor, the current flowing through each coil needs to be controlled, by doing so, the net magnetic field vector can be controlled (i.e., both direction of rotation and magnitude). The rotor magnetic field catches up with the net stator magnetic field vector to produce torque, since the strength of magnetic field is directly dependent on the current flowing in the coils, the torque can be controlled [1-3].

Various BLDC control techniques have been defined in literature, these include, trapezoidal control that involves controlling the current through any two pair of coils simultaneously, the sequence of firing is decided by a lookup table and feedback from the hall effect sensors that measure rotor position. Although this technique is simple to implement, it does not provide smooth and precise motor control. Sinusoidal control involves controlling the three phase currents though the coils sinusoidally as the motor rotates. This results in a smoothly rotating magnetic field vector; therefore, it eliminates the torque ripples and commutation spikes. One of the drawbacks with this technique is that its performance degrades at higher speeds because of the time variant nature of the control scheme that causes the breakdown due to limited bandwidth of PI (Proportional Integral) Controller. Field-oriented control, also called as vector control is a scheme that offers great performance and efficiency. In this technique, the stator currents of the motor are represented in dq reference frame. One vector corresponds to the magnetic flux of the rotor and the other vector represents the torque. By manipulating these vectors based on the desired output required, the motor is controlled. A detailed explanation of this scheme is provided in section. Although this scheme requires high processing requirements, recent advancements and reduction of cost in microprocessor and power electronics technology have led to wide spread usage of this scheme in AC motor drives [2-3].

For field-oriented control and various other industrial application, two of the most commonly used PWM (Pulse Width Modulation) schemes to control the inverter are SPWM (Sinusoidal PWM) and SVPWM (Space Vector PWM). In SPWM technique, two different signal types are used – sinusoidal reference waveforms and a high frequency triangular waveform (i.e., carrier waveform) for comparison to generate pulses. In SVPWM, the rotating space vector of either the reference voltage or current is recomposed by taking the vector sum of available base vectors [5-8].

Position control requires feedback of the rotor position, usually encoders are used to sense the rotor position. There are various types of encoders such as magnetic and optical encoders, in this there are incremental and absolute types. Depending on the application and accuracy it demands an appropriate encoder is selected. An encoder can provide information on direction of rotation, speed, amount of rotation and position. The sensitivity of an encoder is defined by its resolution. In general, a typical FOC based speed and position control is shown in Fig. 1. It consists of three control loops. Position control loop feeds the speed control loop, this inturn feeds the current control loop [9-12].

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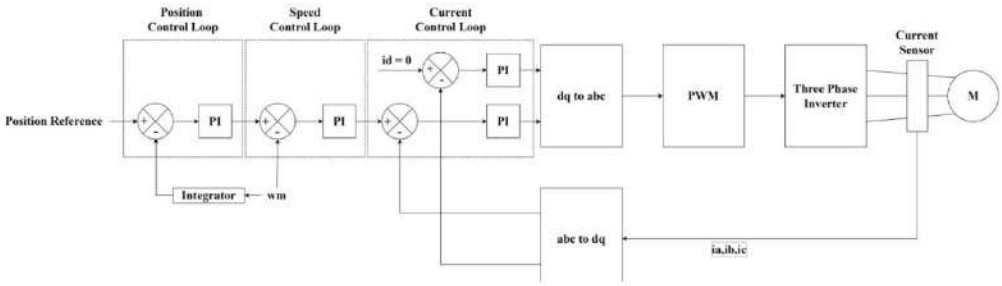

Fig. 1. General Block Diagram of Position and Speed Control of BLDC Motor Using FOC

II. MODELLING OF THE BLDC MOTOR

Let's assume a system of BLDC motor connected via a three-phase inverter and powered by a DC source as shown in Fig.2. To model the motor, consider a star connected configuration for the BLDC motor [2] and assuming a balanced three phase system, then, R = Ra + Rb + Rc.

$$V_a = RI_a + (L - M)\frac{dI_a}{dt} + e_a \quad (1)$$

$$V_b = RI_b + (L - M)\frac{dI_b}{dt} + e_b \quad (2)$$

$$V_c = RI_c + (L - M)\frac{dI_c}{dt} + e_c \quad (3)$$

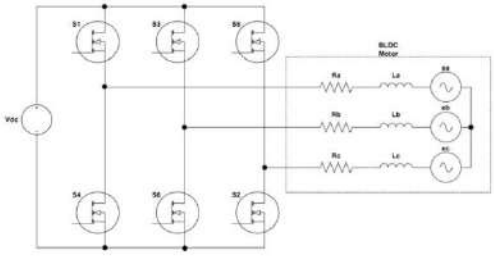

Fig. 2. Equivalent Circuit of BLDC Motor

In equation (1-3),

Va, Vb, Vc = phase voltages

R = Armature resistance

L = Armature self-inductance

M = Mutual inductance

Ia, ib, ic = phase current

Ea, eb, ec = motor back emf

The back emf of the motor is written as shown in (4-7)–

$$e_a = K_w f(\theta_e)\omega \quad (4)$$

$$e_b = K_w f(\theta_e - \frac{2\pi}{3})\omega \quad (5)$$

$$e_c = K_w f(\theta_e + \frac{2\pi}{3})\omega \quad (6)$$

$$f = \begin{cases} 1 & 0 \le \theta_e \le \frac{2\pi}{3} \\ 1 - \frac{6}{\pi}(\theta_e - \frac{2\pi}{3}) & \frac{2\pi}{3} \le \theta_e \le \pi \\ -1 & \pi \le \theta_e \le \frac{5\pi}{3} \\ -1 - \frac{6}{\pi}(\theta_e - \frac{5\pi}{3}) & \frac{5\pi}{3} \le \theta_e \le 2\pi \end{cases} \quad (7)$$

The electrical angle, θe = (P/2)θm, where θm is the mechanical angle of the rotor and P are the number of pole pairs. The function given by f in (7) gives the back emf that is trapezoidal in nature for phase A of the motor. Kw is the back emf constant and ω is the rotor speed.

The electromagnetic torque in both electrical form and mechanical form is given in (8) and (9) respectively.

$$T_{em} = \frac{1}{\omega}(e_a i_a + e_b i_b + e_c i_c) \quad (8)$$

$$T_e = J\frac{d\omega}{dt} + B\omega + T_L \quad (9)$$

In this,

P = Number of pole pairs

TL = Load Torque

J = Moment of Inertia

B = Friction Constant

III. FIELD ORIENTED CONTROL

Fig.3 shows the vector representation of the stator current in abc, alpha-beta and dq reference frames. For conversion from abc to alpha-beta reference frame, only two instantaneous current vectors are sufficient, in this case phase currents of a and b. Phase c current can be computed using the current relation shown in (10).

$$i_a + i_b + i_c = 0 \quad (10)$$

Using Clarke's transformation, the phase vectors are converted to alpha-beta orthogonal reference frame (11-12).

$$i_\alpha = i_a \quad (11)$$

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$$i_\beta = \frac{1}{\sqrt{3}} i_a + \frac{2}{\sqrt{3}} i_b \quad (12)$$

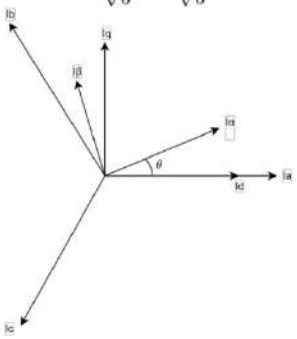

Fig. 3. Current Vector Representation Combined

Using Park's transformation, the vectors are converted from alpha-beta coordinate system to dq coordinate system (13-14).

$$i_d = i_\alpha cos(\theta) + i_\beta cos(\theta) \quad (13)$$

$$i_q = -i_\alpha cos(\theta) + i_\beta cos(\theta) \quad (14)$$

Here, θ is the instantaneous rotor position angle, also in the dq reference frame, the quantities are time invariant. By controlling/modifying the quadrature component of the current, the torque can be controlled. By controlling the direct component, the rotor flux can be controlled.

In order to maximize torque and overall efficiency, the direct component must be ideally maintained at zero and quadrature component is generated based on torque and speed requirements. The reference values are compared with actual values and via a PI controller, the corresponding voltage is calculated. The voltage in dq reference frame is converted back to alpha-beta coordinate system using Inverse Park's transformation as shown (15-16). This is typically used to generate the gate pulses using SVPWM.

$$V_\alpha = V_d cos(\theta) - V_q sin(\theta) \quad (15)$$

$$V_\beta = V_d sin(\theta) + V_q cos(\theta) \quad (16)$$

In order to convert from alpha-beta coordinate system to abc, Inverse Clarke's transformation is used as shown (17-19). This is used to generate the SPWM for the inverter.

$$V_a = V_\alpha \quad (17)$$

$$V_b = -\frac{1}{2} V_\alpha + \frac{\sqrt{3}}{2} V_\beta \quad (18)$$

$$V_c = -\frac{1}{2} V_\alpha - \frac{\sqrt{3}}{2} V_\beta \quad (19)$$

IV. SINUSOIDAL PULSE WIDTH MODULATION

Sinusoidal Pulse Width Modulation, is one of the most commonly used technique for motor control and inverter applications. Implementation of this technique is simple and processing requirements are less. The sinusoidal reference waveforms are compared with a high frequency triangular carrier waveform to obtain the switching pulses for the respective switches.

V. SPACE VECTOR PULSE WIDTH MODULATION

Space Vector Pulse Width Modulation is a more advanced technique compared to the SPWM technique. The added complexity offers many advantages such as better utilization of DC bus voltage, lower harmonics and better flexibility. Fig.4 shows a space vector representation of the inverter system with six sectors. The reference vector rotates with an angular velocity against the stationary alpha-beta reference frame. By controlling the frequency and magnitude of vref, the magnitude and frequency of the corresponding fundamental component is varied [6-8]. The required output voltage of each phase is shown in (20-22).

$$V_b = V_m cos(\omega t - 120°) \quad (20)$$

$$V_a = V_m cos(\omega t) \quad (21)$$

$$V_c = V_m cos(\omega t + 120°) \quad (22)$$

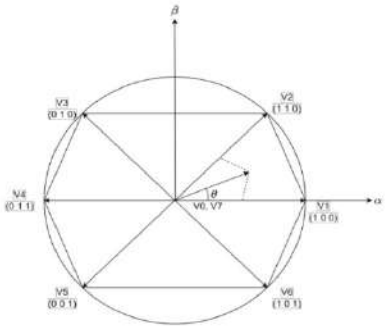

Fig. 4. Vector Representation of SVPWM

Vref is calculated using (23) and the Fig.5 visualizes the representation of sector 1.

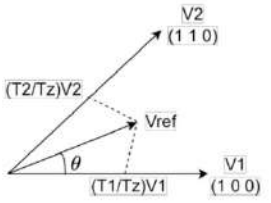

Fig. 5. Sector 1 Representation

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$$V_{ref} = \sqrt{\frac{3}{2}} V_m e^{j\theta} \quad (23)$$

In this $\theta = \omega t = 2\pi ft$

$$\overrightarrow{V_{ref}} T_Z = \vec{V_1} T_1 + \vec{V_2} T_2 \quad (24)$$

In this Tz is the time period of the PWM signal or the reciprocal of the switching frequency fs (i.e., Tz = 1/fs). The angle between the sectors is given by ϕ with range between 0° to 60°.

$$\phi = \theta - (N-1)60 \quad (25)$$

(26-28) is used to determine the switching period.

$$T_0 = T_Z - (T_1 + T_2) \quad (26)$$

$$T_1 = T_Z \frac{2}{\sqrt{3}} \frac{V_{ref}}{V_1} sin(60 - \phi) \quad (27)$$

$$T_2 = T_Z \frac{2}{\sqrt{3}} \frac{V_{ref}}{V_2} sin(\phi) \quad (28)$$

VI. Simulation and Results

A. Simulation Setup

The simulation studies are carried out using Simulink. In accordance to fig, the models for the comparison studies using the SPWM and SVPWM based speed and position control of BLDC motor is shown in Fig.6. The Simulink model consists of PMBLDC motor configured for trapezoidal back emf, stator resistance of 0.01ohms and inductance of 40uH. For the inverter, a two-level inverter block is used, powered by a DC source of 12V. The transformations are directly performed using the conversion blocks available in Simulink. The PWM scheme is directly implemented using the PWM modulator block that offers both SVPWM and SPWM capabilities. The PWM scheme is changed between studies to perform the comparison study. The switching frequency is set at 8kHz. There are three control loops, one current control loop, speed control loop and position control loop connected in cascaded configuration. In order to keep track of the position, the integral of speed is taken. A constant torque of 0.008Nm is applied on the motor with a total simulation time of 5 seconds. Using a stair generator block, the reference position is generated. From 0, at 0.1 seconds, the position is set to 4 radians or 4 revolutions of the rotor shaft. At 2 seconds, the rotor position is set to -4 radians and is set back to 0 radians at 3.5 seconds. The PI controller of the current control loop is tuned using a separate MATLAB script. The speed and position control loop are tuned by trial-and-error method. The model is run at constant speed next to obtain the back emf and electromagnetic torque waveforms.

B. Results

Fig.7 shows the waveforms related to the motor. In order, the first waveform shows the back emf, the phase currents and the electromagnetic torque. At the commanded positions, the waveforms using both SPWM and SVPWM look similar, upon closer inspection, the electromagnetic torque ripple is relatively less in SVPWM scheme. During position change, the current draw increases to reach the desired position, the current starts dropping once the positional error start reducing. Spikes in electromagnetic torque is seen during position changes. Fig. 8 and Fig.9 shows the comparison between speed and position waveforms respectively. The rotor speed waveforms show the speed increasing during position changes and reducing when positional error reduces. The position waveforms show the actual position and reference position waveforms. The control system is able to track the reference positions accurately and no overshoots occur. A similar conclusion is drawn by comparison of these waveforms. This similar performance is due to the light loading conditions. Fig.10 shows a comparison of the motor parameters at constant speed of 100 rad/sec with increased loading of 0.08Nm compared to the 0.008Nm previously. In this case, only a small difference is seen in the electromagnetic torque. The back-emf at this loading is at 0.7V and the current draw is close to 10A(peak). The overall torque ripple is less in SVPWM compared to SPWM. This is verified by taking a moving average of the electromagnetic torque to reduce the noise caused by switching as shown in Fig.11. There are a lot less variations in the SVPWM based FOC compared to

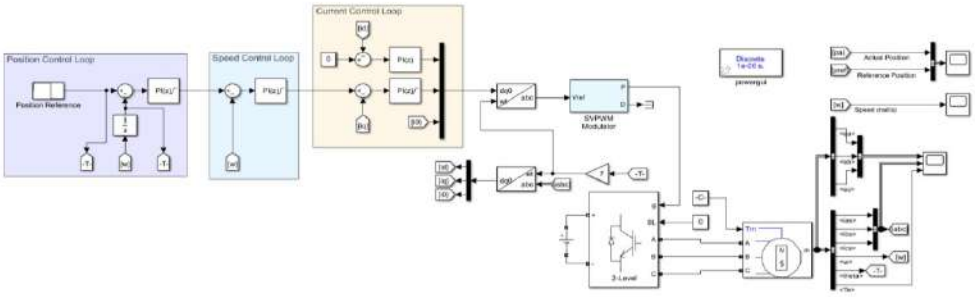

Fig. 6. Simulation Model of the FOC Based Speed and Positon Control of BLDC Motor Using SPWM and SVPWM

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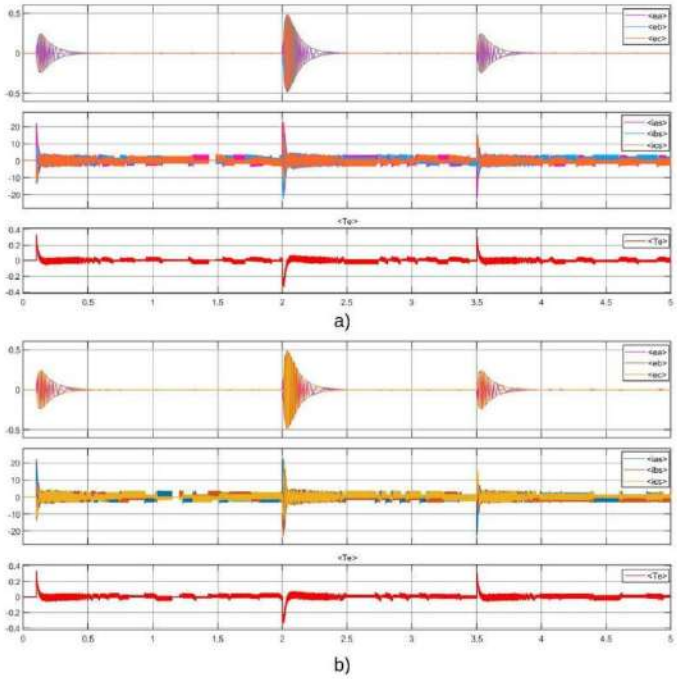

Fig. 7. Back EMF, Stator Current, Electromagnetic Torque Waveforms of the BLDC Motor a) SVPWM b) SPWM

SPWM based FOC.

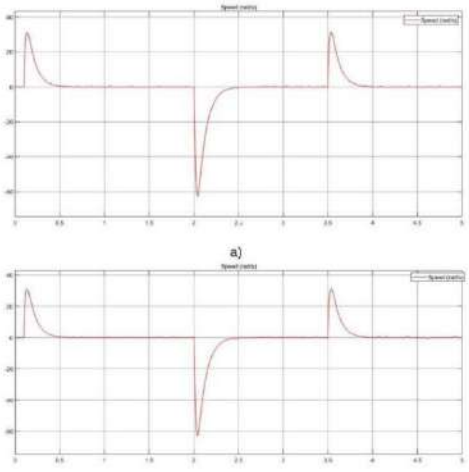

Fig. 8. Speed Waveform in rad/sec a) SVPWM b) SPWM

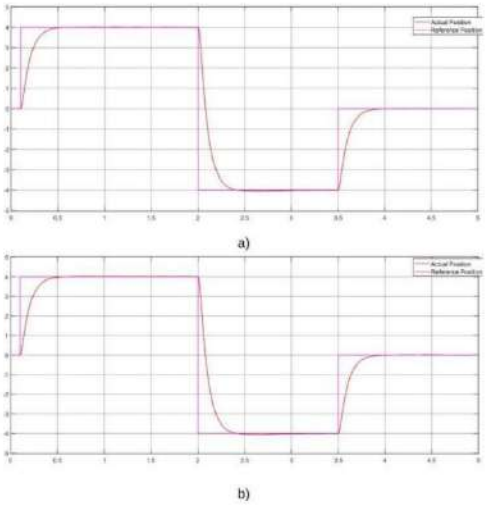

Fig. 9. Actual Position (Red) and Reference Position (Purple) Waveform a) SVPWM b) SPWM

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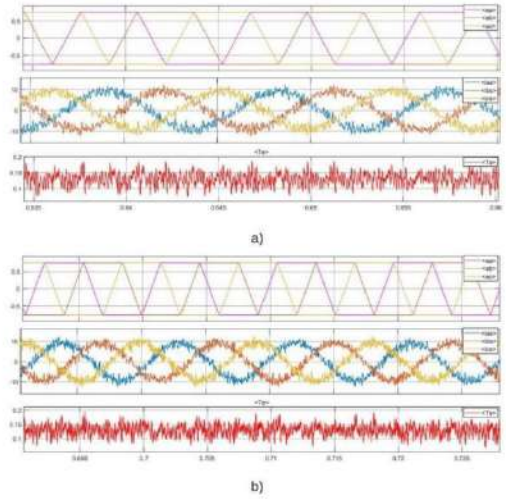

Fig. 10. Back EMF, Stator Current, Electromagnetic Torque Waveforms of the BLDC Motor at Constant Speed a) SVPWM b) SPWM

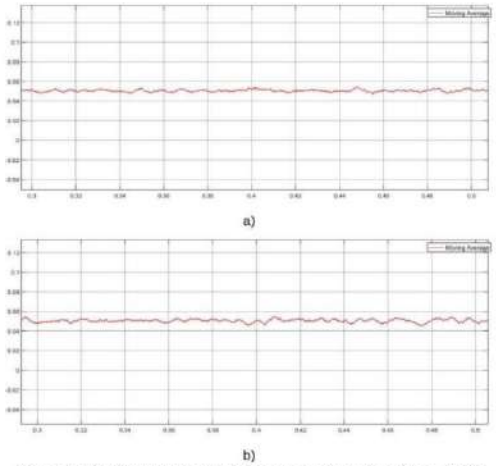

Fig. 11. Electromagnetic Torque at Constant Speed a) SVPWM b) SPWM

VII. CONCLUSIONS

The comparison study of position and speed control of BLDC motor via FOC using SPWM and SVPWM has been carried out using Simulink and the corresponding output waveforms of comparison is presented. In this study, due to light loading conditions, the performance of the FOC based algorithm using both SPWM and SVPWM scheme are quite similar. Small variations can be seen in the waveforms especially comparing the electromagnetic torque, the SVPWM performs slightly better with less torque ripple compared to SPWM technique. The averaged torque waveform of SVPWM is relatively smoother compared to SPWM.

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on

DESIGN AND IMPLEMENTATION OF FOC AND GUI FOR EV TEST BENCH IN LABVIEW

18MPE41

Submitted by

PRADEEP KUMAR S

USN: 1RV20EPE09

Under the Guidance of

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Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY
in
POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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His conduct during the period of internship was found to be good

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Pradeep Kumar S

Power Electronics

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RV College of Engineering

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ABSTRACT

Electric vehicles have grown in popularity and demand in recent years. The EV motor before being installed in an electric vehicle needs to be examined and calibrated in a dyno test bench under real-time load circumstances. The EV motor under test – Device Under Test (DUT) is required to operate in an error-free control system for the performance analysis. The Field Oriented Control (FOC) algorithm suits the required motor control criteria to operate the motor with torque control and field weakening control. The existing motor controllers lack to operate the motor in wide ranges of speed. To test the DUT motors at higher speed, a motor controller module with increased speed range needs to be developed.

The FOC algorithm was developed in LabVIEW using National Instruments cRIO-9046, FPGA modules NI-9223 (Analog input module – 1MS/s) and NI-9401 (Digital IO – 10MHz) as motor controller to control the DUT motor in an EV test bench, processing at 47us to control the motor in real-time at wide range of speed up to 25000 rpm. The interior Permanent Magnet Synchronous Motors (PMSM) was considered as drive motor in the electric vehicle. Performance analysis on the selected motor – device under test (DUT) is performed in a 350kW Dyne Test Bench. The control of PMSM-DUT motor was achieved in torque mode and field weakening mode to test the DUT motor in all four-quadrant operation of motor. The GUI developed allows to set the speed based on the torque measured, the I_q reference value was set and the motor was operated in toque control mode up to base speed of the motor. The I_d reference control was set using the look-up table that provides speed control up to the peak speed of the DUT motor with reduced torque on load conditions operating the DUT motor in Flux weakening control mode.

The DUT motor tested was an 8 pole PMSM motor with peak power of 60kW and peak speed of 4000rpm. The motor was operated at a speed of 2050 rpm with a load of 10Nm for a set speed of 2000rpm. The reference current was set at I_q ref = 50A with input DC voltage of 120V, 60A. On increasing the load for same DC voltage and I_q reference value the change in speed was observed to be -100rpm. The speed of the motor was further increased beyond base speed up to motor's peak speed by modulating the I_d reference and with deteriorated torque of the DUT motor. The motor achieved the set speed from standstill in 3 seconds under no-load condition and achieved the set speed in 6 seconds under on-load condition at speed set at 800rpm and with load torque of 10Nm.

LIST OF PUBLICATIONS

Publication Type	Publication Details
International Journal	Pradeep Kumar S, Dr. Dinesh M N "Design and Implementation of FOC and GUI for EV Test Bench in LabVIEW", *International Research Journal of Emerging Technologies and Innovative Research (JETIR)*, ISSN: 2349-5162, Volume: 09, Issue: 6, June 2022 pp J418-J430

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GLOSSARY

LabVIEW	: Laboratory Virtual Instrumentation Engineering Workbench
PMSM	: Permanent Magnet Synchronous Motor
FOC	: Field Oriented Control
EV	: Electric Vehicle
IPM	: Interior Permanent Magnet
DUT	: Device Under Test
BLDC	: Brushless Direct Current
FPGA	: Field Programmable Gate array
AC	: Alternating Current
DC	: Direct Current
SPWM	: Sinusoidal Pulse Width Modulation
NI	: National Instruments
DMA	: Direct Memory Access
cRIO	: Compact Real Time Input Output
HIL	: Hardware In Loop
SAE	: Society of Automotive Engineers
AIS	: Automotive Industry Standards
GUI	: Graphical User Interface
θ_m	: Mechanical Angular Displacement
θ_e	: Electrical Angular Displacement
rad	: radians
PI	: Proportional Integral
RT-FIFO	: Real-Time First In First Out
Dyno	: Dynamometer motor
VI	: Virtual Instruments

Chapter 1

INTRODUCTION

The rising popularity and demand for electric vehicles have been increasing rapidly in recent years. The conventional drive system uses the three types of motors that have become popular in electric drive applications: 1. PMSM Motor. 2. Brushless DC Motor. 3. Three - Phase Induction motors. The PMSM motors and Three phase Induction motors requires sinusoidal voltage whereas the BLDC motors require trapezoidal voltage to control [1]. The EV motors need to be analyzed and calibrated before being installed in a vehicle by emulating the real-time load conditions in a dyne test bench. The loading capacity of the vehicle, maximum driving speed, acceleration rate, deceleration rate, maximum power, torque on wheels etc. can be analyzed based on the load driving capacity of the motor. The EV motor under test– Device Under Test (DUT) is required to operate in an error-free control system for calibration and performance analysis. The EV test benches are currently using the customized pre-built controllers to control the DUT motors to operate only up to limited speed ranges. The design and development of the reliable motor control modules at higher speed ranges is required.

The PMSM motor is considered for driving the electric vehicle as it is more reliable, less noisy, has higher efficiency, delivers high torque and has better performance in both low and high-speed operations than BLDC motors. The 3-phase induction motor has poor starting torque due to low resistance of rotor windings. The PMSM motors are preferred over induction motors in the electric vehicle applications [2]-[3]. Compared to the six-step commutation control and hysteresis current control the field- oriented control (FOC) delivers fast acceleration and deceleration of motor giving more accurate smoother operation with less torque ripple and fast torque response using maximum torque per ampere [4].

The Field Oriented Control is the vector control method such that the three-phase time varying stator currents I_a, I_b and I_c of the PMSM motors are transformed to equivalent two-phase time invariant orthogonal components I_d and I_q visualized as vectors by performing forward Clarke's and forward Park's transforms. One of the vector components - I_d provides control over the magnetic flux of the motor and the other vector component - I_q

provides control over the torque of the motor [5]-[7]. The drive control system modulates the correction values of flux and torque based on the error generated by the feedback and command reference signals. The PI controllers are employed to modulate the measured vector components tuned to the reference values. The modulated orthogonal voltage vectors V_d and V_q are obtained from the PI controllers. The inverse Park and inverse Clarke's transforms are performed to obtain the time varying voltage signals [8]-[10]. The voltage signals obtained is compared with high frequency triangular wave to generate sinusoidal pulse width modulation signals (SPWM) to operate the motor in forward motoring, forward braking, reverse motoring and reverse braking operations. The National Instruments - LabVIEW graphical development platform is used to program the FOC algorithm, to develop a user interface for monitoring and logging the results. The LabVIEW based FOC controller algorithm provides the custom range of speed operation but limited only by the range of the FPGA modules used.[11]-[13]

1.1 Overview

The EV dyne motor test bench is a platform that evaluates the measure of torque, rotational speed, and indicates the power of the motor. The EV motors need to be analyzed and calibrated before being installed in a vehicle by emulating the real-time load conditions in a dyne test bench. The tests are performed to determine the loading capacity of the vehicle, maximum speed achieved, acceleration and deceleration rate, maximum power, maximum torque and efficiency [14]-[15]. The EV motor under test is required to operate in an error-free controlsystem for calibration and performance analysis.

Field-Oriented Control (FOC) provides faster motor acceleration and deceleration, resulting in more precise control with less torque ripple and faster torque response. It is the vector control method in which the three-phase time varying signals are transformed to two-phase time invariant orthogonal vectors, which are modulated to achieve desired control[16]-[18]. The modulated two-phase time invariant signal is transformed back to three-phasetime varying voltage signals, which are sampled with high frequency carrier to generate sinusoidal PWM signals. The generated SPWM signals drives the motor through the inverter in all four quadrant operations to verify the performance of the test motor in the EV Dyno test bench [19].

1.2 Specific Details

The specifications of the devices considered in the implementation of the FOC algorithm and development of the hardware module is explained in brief. The position of the rotor is sensed using the resolver mounted on the rotor shaft. The three phase currents are sensed using the current sensors embedded in Semikron inverter are considered as feedback for processing of FOC algorithm. The signals sensed are fed to the FPGA modules embedded in cRIO chassis. The FPGA program is designed to acquire jitter free signals using RT-FIFO [20]-[24]. The analog input is fed to analog to digital converter, NI-9223 FPGA module. The LabVIEW program is optimized to acquire and process data in real-time[25]-[28]. The Sinusoidal PWM waveforms obtained are read through digital output pins of NI-9401. The dead time is implemented between top and bottom switches of the generated SPWM signals that drives the PMSM motor through the inverter in all four quadrant operations to verify the performance of the test motor in the EV Dyno test bench [29]-[31]. The Hardware in loop (HIL) test of the developed LabVIEW program is performed to validate the software and verify the performance of the motor.[32]-[34]. The Table 1.1 represents the specific hardware devices used in the development of the hardware module.

Table-1.1 Specific details of Hardware module

Device	Specification detail
Motor	8-pole,41kW,150 V, 450A IPMSM motor,
Inverter	Semikron Inverter- IGBT module - V_{max} = 800V, I_{nom} = 300A, Switching frequency = 12kHz
Resolver	8-pole hollow shaft type resolver
Resolver Decoder	PGA411-Q1 development board
FPGA Modules	Analog Input - NI-9223, Digital output - NI9401
Chassis	cRIO-9046

1.3 Literature survey

Permanent Magnet Synchronous motor (PMSM) has advantages such as high efficiency, high power factor, high power density and maintenance free operation. PMSM is more reliable than the DC motor as there is no commutator and brushes, PMSM produces the rotor magnetic flux with permanent magnets and it offers higher efficiency compared

to Induction motor. Moreover, the availability of low-cost power electronic devices and the improvement of PM characteristics enables the use of PMSM in high performance and high efficiency applications [1]-[2].

Fast acceleration and deceleration and smooth rotation over the entire speed range enhances the motor control performance. Using Field oriented control technique in PMSM, high performance and superior dynamic response is achieved because of independent control of torque and flux. Motor currents (I_a, I_b, I_c) are transformed into d-axis and q-axis currents based on projections. The q-axis component of stator current is used to control the torque and the d-axis component of stator current is used to control the rotor flux. In PMSM motor since the rotor is a permanent magnet, the d-axis component of the stator current can be kept zero.[3]-[5].

PI controllers are used to control the speed, torque and flux of the motor The proposed system continuously injects the q-axis and d-axis currents to generate the voltages of q-axis and d-axis. Integral anti windup is used to prevent the saturation of integral accumulator of PI controllers. The d-axis and q-axis voltage components from the controller are transformed to Va, Vb, Vc, on performing inverse Park and Clarke's transform. The three phase voltages signals are compared with the high frequency triangular reference waveform to generate Sinusoidal pulse width modulated (SPWM) signals for the inverter operation based on Carrier signal frequency [6]-[8].

The acquisition of real time data in LabVIEW hysteresis data loss due to delay in data acquisition and processing of the FOC algorithm. A high-speed data acquisition and processing framework is proposed by combining state machine and production-consumer system using the real-time buffer in LabVIEW. The synchronous data acquisition of four channels data such as position and three phase currents data are processed and displayed in front panel in real time [9]-[11].

The PMSM motor, before being installed in the electric vehicle is emulated on the EV test bench to analyze the performance of the motor verifying the rated maximum speed, maximum torque and efficiency of the motor. The EV test benches are currently using the customized pre-built controllers to operate motors only up to limited speed ranges. The EV motors are tested in forward motoring, forward braking, reverse motoring and reverse re-generative braking operations in both speed and torque mode operations to analyze rate continuous loading capacity, peak loading and maximum speed of DUT motor [12]-[15].

The FOC algorithm developed using NI-FPGA modules consists of jitters, due to asynchronous sampling and data acquisition The real-time data sampling and time synchronization of the analog and digital signals is processed using LabVIEW scan engine data acquisition method cRIO to obtain jitter free data. The timed-loop structure is considered in deterministic data acquisition. The direct memory access (DMA) buffer architecture from FPGA target to host system is considered in reducing the jitters and avoid data loss in read and write processes of the LabVIEW real-time execution [16]-[19].

The LabVIEW program to operate in real-time, the sampling clock frequency of the target FPGA is synchronized with the host computer and cRIO clock frequencies. The program architecture is designed with time critical priority for data acquisition, The program i s further optimized by considering the mega-hertz absolute timed loop structure in cRIO along with the while loop structure in target FPGA program. The optimization of the program to process with 50us or 10kHz is possible in cRIO [20]-[23].

The LabVIEW program optimization is further achieved by programming the FOC algorithm in the target FPGA memory to operate the motors with higher switching frequencies. The creation of Sub-VI is avoided as individual loops may add on delay in processing the algorithm [24]. In high frequency operations the additional dead-time is provided between the top to bottom switching of the inverter using time delay operations provided only for the bottom switches in SPWM signal generation. The FOC algorithm in target FPGA processes at 6us or at 166kHz.[25]-[28]

The EV motor mounted on the dyno-test bench is loaded with variety of torque loads emulating the real -time load circumstances of the vehicle on road. The EV motors are tested along with the inverters for their durability, efficiency and load handling capacities in the hardware in loop (HIL) tests, testing the software as well as the motor and inverter hardware modules [29]-[30]. The standards and procedures to be followed in EV motor testing is obtained by the Society of Automotive Engineers (SAE) and Automotive Industry Standards (AIS). The simulation of the HIL test and the dyno test is considered for the realization and testing of the EV motors in hardware module. [31]-[32]. The Control strategies for controlling the braking forces on front and rear wheels, regenerative braking and mechanical braking energy that can be potentially recovered in typical driving cycle calculated is discussed [33]-[34].

1.4 Motivation

EV motors require testing and calibration emulating in real-time load circumstances on EV test bench. The existing motor controllers are incapable of drivingthe motors at high-speed ranges. To analyze the performance of motors, an error free controller needs to be developed. The conventional motor control methods like six-step commutation control and hysteresis current control, though are very effective in controlling the speed but suffer from issues like generation of torque ripples at low speed, problem of continuous PWM signal generation during constant frequency operation to drive the motor. The Field Oriented Control of PMSM motor is proposed to deliver faster acceleration and deceleration of motor giving more accurate control to test the performance of the motor with less torque ripple and smoother operation on the EV motor Test Bench.

1.5 Problem definition

To develop the FOC algorithm in LabView graphical software using the real time interface; National Instruments CompactRIO 9046 with FPGA modules NI9223 – High speed analog input (1MS/s) and NI9401 – High Speed Digital IO modules (100ns) or (10MHz) and to control the operation of motor in all four quadrants – forward motoring, forward braking, reverse motoring and reverse braking emulating real time load conditions on motor, thereby testing the performance and determining the efficiency of the PMSM motor.

1.6 Objectives

The main objective of the project is to design and implement the Field Oriented Control of PMSM motors using LabVIEW software for the EV test Bench:

- To develop FOC algorithm using LabVIEW software.
- To optimize the algorithm such that the program runs at <50us.
- To develop GUI for speed setting.
- To generate Sinusoidal PWM signals to control the operation of motor in all four quadrants and thereby to achieve the speed of 25000 rpm.

1.7 Organization of Report

The complete report presents the review of the work carried out, concepts, design and its verification. It is organized in seven chapters.

Chapter 1: Introduction briefs the introduction of the project, that includes the overview of the project, specific details, literature survey of the project that gives the consof the project and motivation to take up the project, problem definition, and objectives and scope of the project. It also includes the organization of the report.

Chapter 2: Theory and Concepts gives the basics of the field-oriented control algorithm, the modes of control achieved, brief explanation of constant torque control and field weakening control, brief explanation of EV test bench and the torque mode control and speed mode control.

Chapter 3: Methodology and Block Diagram presents the methodology used in the execution of the FOC algorithm in LabVIEW. It also consists of flow chart and block diagram, that gives the step-by-step process in the implementation of FOC algorithm in LabVIEW for EV test bench.

Chapter 4: Specifications and Design explains in detail the software design specifications, hardware device specifications and the hardware wiring block diagram.

Chapter 5: Simulations provides the simulation of FOC algorithm simulated in MATLAB-Simulink for the PMSM motor. The forward Clarke and Park transforms, PI controllers tuning, inverse Park and Clarke transforms and Sinusoidal PWM generation logic is explained.

Chapter 6: Results and Discussion discusses about the simulation results of the FOC algorithm simulated in MATLAB-Simulink. The GUI developed in LabVIEW is discussed. The results of the HIL testing of the hardware implementation of the FOC in LabVIEW for various load conditions and set speed is explained for all operations of the test motor.

Chapter 7: Conclusion and Future Scope includes the overall conclusion drawn from the project and the future works that can be carried out.

References includes the list of references referred in the successful completion of the project.

Chapter 2

FIELD ORIENTED CONTROL and EV DYNO - TEST BENCH

The chapter explains the overarching basic principles necessary to complete the project work. The chapter covers the fundamentals of field-oriented control, the implementation of torque and flux weakening control of a PMSM motor, and the fundamentals of an EV Dyno-test bench, including operation methods and test settings.

The control techniques involved in the controlling of the PMSM motor are:

- Six-step commutation control
- Hysteresis control
- Direct sinusoidal voltage control
- Field Oriented Control

2.1 Field Oriented Control

The polyphase PMSM control is rendered equivalent to that of the DC machine by a decoupling control known as vector control. The vector control separates the torque and flux channels in the machine through its stator – excitation inputs. The Field Oriented Control or the vector control of the PMSM motors is derived from its dynamic model, considering the three phase currents as inputs, the three phase currents are as shown in equation 2.1.

$$\begin{aligned} i_{as} &= i_s \sin(\omega_r t + \delta) \\ i_{bs} &= i_s \sin\left(\omega_r t + \delta - \frac{2\pi}{3}\right) \\ i_{cs} &= i_s \sin\left(\omega_r t + \delta + \frac{2\pi}{3}\right) \end{aligned} \quad (2.1)$$

Where, ω_r is the electrical rotor speed and δ is the angle between rotor field and stator current phasor known as the torque angle. The stator current space vector can be defined in a (d,q) coordinate system with orthogonal components along d (direct) and q (quadrature) axes such thatfield flux linkage component of current is aligned along the d axis and torque component of current is aligned along the q axis. Using the equation 2.2.

$$\begin{bmatrix} i_{qs}^{r} \\ i_{ds}^{r} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \omega_r t & \cos\left(\omega_r t - \frac{2\pi}{3}\right) & \cos\left(\omega_r t + \frac{2\pi}{3}\right) \\ \sin \omega_r t & \sin\left(\omega_r t - \frac{2\pi}{3}\right) & \sin\left(\omega_r t + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} \quad (2.2)$$

Where,

i_{qs}^{r} = Torque-producing component of stator current = i_T

i_{ds}^{r} = Flux-producing component of stator current = i_f

The torque – angle control provides a wide variety of control choices in the PMSM drive systemsuch as:

- Constant torque angle control or zero – direct axis – current control.
- Unity power factor control
- Constant mutual air gap flux – linkages control
- Field-weakening control.

The constant torque control and field-weakening control modes are considered in EV test bench application. In torque mode, the motor operates at constant torque up to base speed and in field-weakening mode, the motor is operated up to maximum speed beyond base speed with reduced torque response.

2.1.1 Constant (δ = 90°) Torque-Angle Control

In torque control mode, the torque angle δ is maintained at 90 degrees between the quadrature axis and direct axis currents. The direct- axis current is set to zero, leaving only the torque or quadrature-axis current in place. In torque mode of operation, constant torque is delivered for speeds up to the base speed for the given speed and torque load acting on the motor shaft. The torque delivered in torque mode is calculated using equation 2.3.

$$T_e = \frac{3}{2} \cdot \frac{p}{2} \lambda_{af} \cdot i_{qs}^{r} = \frac{3}{2} \cdot \frac{P}{2} \cdot \lambda_{af} Is \quad (2.3)$$

and torque per unit current is a constant, given by equation 2.4.

$$\frac{T_e}{I_s} = \frac{3}{2} \cdot \frac{P}{2} \cdot \lambda_{af} \quad (2.4)$$

and normalized electromagnetic torque is expressed as equation 2.5.

$$T_{em} = \frac{T_e}{T_l} = \frac{\frac{3}{2}.\frac{p}{2}\lambda_{af} I_s}{\frac{3}{2}.\frac{p}{2}\lambda_{af} I_q} = I_S \tag{2.5}$$

indicating that torque equivalent stator current, that gives the simplest control for torque control mode of the PMSM drives. Note that I_s, is the normalized stator current phasor magnitude. Relevant equations to determine the steady-state performance of the PMSM drive with this control strategy are derived in the following. After the modulation of correction voltages in the PI controllers, the q and d axes voltages, in steady state is given as in equation 2.6. (2.6)

$$V_{qs}^r = \left(R_s + L_d \Psi_{qS}\right) I_s + \omega_r \lambda_{af} = R_s I_s + \omega_r \lambda_{af}$$

$$V_{ds}^r = -\omega_r \lambda_{af} I_s L_q$$

The rate of change of currents is zero in the rotor reference frames as the currents are constant in steady state. The magnitude of the voltage phasor is given by equation 2.7.

$$V_s = \sqrt{\left(V_{qs}^r\right)^2 + \left(V_{ds}^r\right)^2} \tag{2.7}$$

The peak threshold voltage setting of PI controller for tuning of d-axis and q-axis voltage components - V_d and V_q is calculated using equation 2.7. The maximum voltage set is $\frac{+V_s}{2}$ and the minimum voltage set is $\frac{-V_s}{2}$. In torque mode, the torque vector component V_q is varied between 0 to $\frac{+V_s}{2}$ to provide proper control of motor to drive the load torque.

2.1.2 Field-Weakening Control

Assuming that the motor is in a steady state and ignoring its winding voltage drop, the motor d–q axis flux linkage is show in equation 2.8. (2.8)

$$\Psi_q = L_q i_q$$

$$\Psi_d = L_d i_d + \phi_f$$

By combining equation 2.8, with the motor torque equation 2.3, the motor d–q axis composite flux linkage can be regarded as a function of the d-axis current as shown in equation 2.9.

$$\left(\Psi_{dq}\right)^2 = \left(L_q i_q\right)^2 + \left(\Psi_f + L_d i_d\right)^2 \tag{2.9}$$

$$(\Psi_{dq})^2 = \left(\frac{L_q T_e}{\Psi_f - L_q i_d + L_d i_d}\right)^2 + (\psi_f + L_d i_d)$$

From Equation (2.9), it can be found that the motor flux linkage increases as the d-axis current increases.

The injection of negative Id current weakens the flux linkage in the airgap for the saturated voltage of the PMSM motor running at the base speed. The negative current injected at Id increases the shaft speed of the motor beyond the base speed up to peak speed for the constant voltage. The torque though is reduced but increasing the shaft speed of the rotor maintains the constant shaft power, driving the motor in maximum speed mode.

2.2 EV Dyno Test Bench

The EV dyno motor test bench is a platform that evaluates the measure of torque, rotational speed and indicates the power of the motor. Dynamometer test bench is used to provide simulated road loading of either the engine using an engine dynamometer or full power train using a chassis dynamometer. In dyno load test, the DUT motor is initially operated at no-load condition, then load is gradually increased to operate at its peak power assuring safe operating conditions.

The dynamometer initially loads the DUT motor with initial load torque emulating the electric vehicle with full load capacity. The motor operation in driving the electric vehicle in flat surface road, up-hill road, slide road and braking of DUT motor are tested to calibrate and verify the ratings of the DUT motor. Two typical test conditions of the DUT motor in torque mode and speed mode are discussed. Fig 2.1. shows the typical schematic diagram of an EV Dyno Test Bench with a test motor, device under test-DUT.

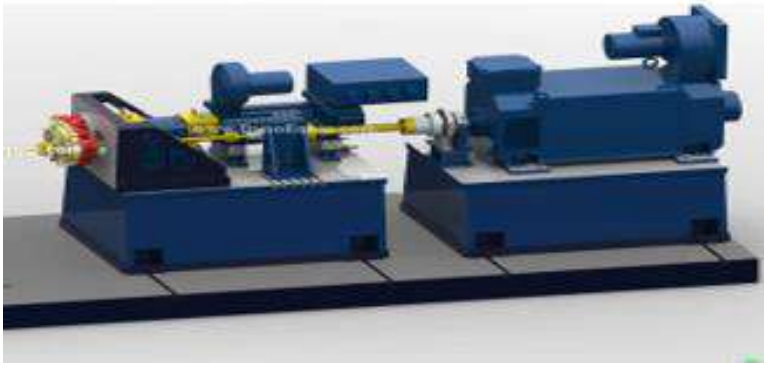


Fig. 2.1 Typical schematic diagram of EV Dyno test bench with DUT motor

2.2.1 Torque mode test

The load handling capacity of the DUT motor is analyzed in torque mode test. The dynamometer is set at zero rpm speed and the torque command to the dynamometer motor is set to a value equivalent to the starting torque of the electric vehicle on a flat surface. The dynamometer motor behaves like a brake drum applying load on test motor. The DUT motor in torque mode runs from stand still and tries to achieve the set speed. The load on DUT motor is increased gradually up to rated torque at speeds under the base speed, considering the real time load circumstances and the motor torque and speed response are recorded for the analysis. The test motor's maximum torque ratings could be identified from torque mode test.

2.2.2 Speed Mode Test

The maximum speed achieved by the test motor under nominal load conditions is analyzed in speed mode test. The DUT motor is initialized first at rated speed and next the dyno motor is set at very low speed equivalent to $1/10^{th}$ speed of DUT motor operating in opposite direction with nominal load torque. The test motor is now injected with the negative I_d reference currents providing field-weakening control to set speed beyond rated speed. The test is repeated until the peak speed is achieved and the maximum nominal load driven by the motor is determined.

2.3 Summary

The chapter includes the theoretical knowledge of the Field Oriented Control algorithm in torque mode and field weakening mode for thePMSM motor. Two typical test were performed on the EV dyno test bench for verifying the maximum torque and peak operating speed of the test motor was discussed.

Chapter 3

METHODOLOGY AND BLOCK DIAGRAM

The chapter includes brief explanation of methodology of Field Oriented Control of PMSM motor. It briefly explains the working of the motor controller in torque mode and field weakening mode. It describes the in-detail structure of the proposed block diagram of the FOC algorithm in LabVIEW.

3.1 Methodology

The methodology involved in developing the Field Oriented Control of PMSM motor is as shown in Fig.3.1.

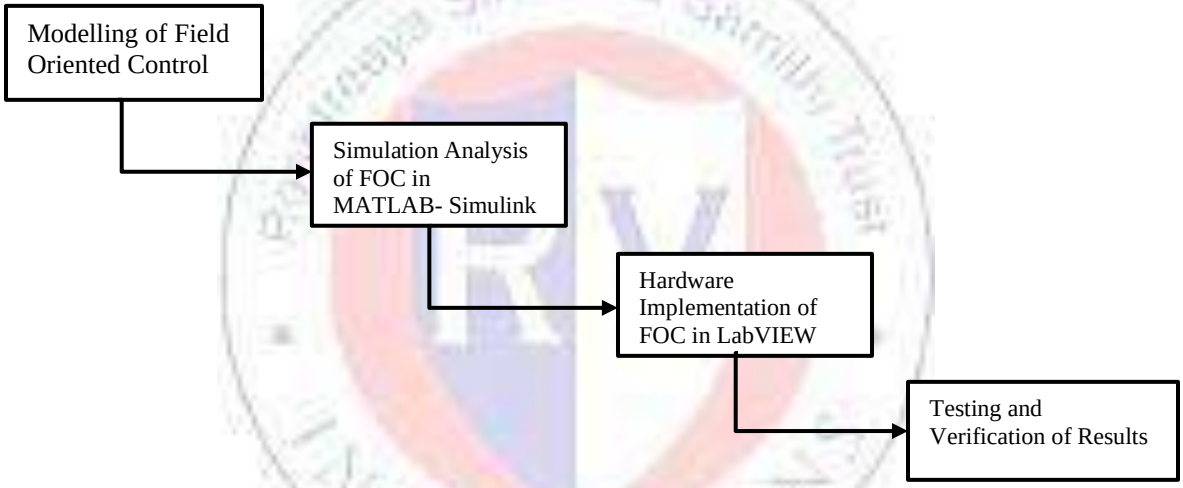


Fig 3.1: Methodology in general

3.1.1 Modelling of Field Oriented Control

The field-oriented control is a vector control method that transforms the three phase time varying components – I_a,I_b and I_c to equivalent two phase time invariant d-q components – I_d and I_q in forward Clarke's and Park's transform. The corrections are modulated to obtain two phase d-q voltage components – V_d and V_q in PI controllers. The d-q voltage components – V_d and V_q are transformed to three phase voltage components V_a, V_b and V_c using inverse Park's and Clarke's transform. The three phase voltages V_a,V_b and V_c are compared with high frequency triangular waveform to generate sinusoidal pulse width modulation signals to drive the motor.

3.1.2 Simulation Analysis

The simulation of the Field Oriented Control algorithm is carried out using MATLAB – Simulink for the mathematic model of PMSM motor in torque control mode and Field weakening mode. The simulation results are used to verify the results obtained in LabVIEW.

3.1.3 Hardware Implementation

The Hardware implementation of the FOC algorithm is realized using Semikron inverter, DUT motor and the NI- cRIO-9046 chassis embedded with FPGA modules NI-9223 (analog input – 1M Samples/s) and NI-9401 (Digital Input-Output – 10MHz). The Hardware wiring connections with EMI and EMC regulations for reducing the noise in system is followed by multi-point grounding and shielding all conductors.

3.1.4 Testing & Verification

The simulation results of FOC algorithm obtained in MATLAB- Simulink is considered as reference for the realization of hardware module. The motor controller module developed is tested to operate the DUT motor in torque loop and speed loop. The speed and torque response of the motor is compared with simulation results and verified with Society of Automotive Engineers standards and Automotive Industry Standards (AIS).

3.2 Flow Chart – FOC in LabVIEW

The steps involved in one complete iteration of the FOC algorithm is explained. Fig. 3.2 shows the flow chart of the proposed FOC algorithm with various modules: 1) Read Analog Inputs; 2) Process Theta Mechanical and Theta Electrical values; 3) Run Forward Clarke's and Park's transform; 4) Check for command signals; 5) Compute modulation of error signals; 6) Run reverse Park and reverse Crake's Transform and 7) Generate the sinusoidal PWM signals. The operation of these modules and the overall proposed method is described.

Fig. 3.2 Methodology of Field Oriented Control in LabVIEW

The proposed technique requires the per phase current and the actual rotor position and speed data to generate the control signals using the FOC algorithm.

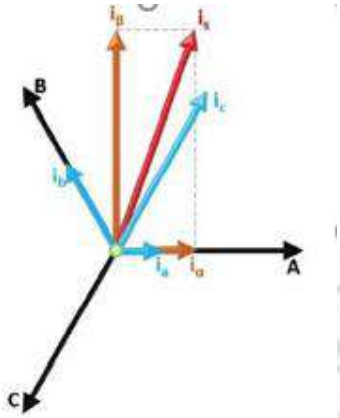
In Module – 1 (read analog inputs), the speed and position of the rotor is identified using the resolver inputs, the resolver data is normalized using the resolver decoder to obtain the mechanical angular displacement values. (θ_m). The currents in each phase are sensed using the integrated current sensors in Semikron inverter and is used to process the FOC algorithm.

In Module - 2 (θ_m to θ_r), the mechanical angular displacement values are normalized to vary from 0 to 2π radians using equation 3.1. The equivalent electrical angular displacement is obtained by the conversion of mechanical angular displacement to equivalent electrical angular displacement using the equation3.2,

$$\theta_m = \frac{ResVoltage - V_{min}}{V_{max} - V_{min}} \times 2\pi[rad] \tag{3.1}$$

$$\theta_e = \frac{P}{2}\theta_m \text{ [rad]} \tag{3.2}$$

In Module-3 (Forward Clarke's Transform) The three phase currents I_a, I_b and I_c are transformed in to two phase equivalent orthogonal currents I_α and I_β using equations 3.3 and 3.4. The three - phase stationary reference phasors are transformed to equivalent two phase orthogonal stationary reference currents in forward Clarke transform as shown in Fig.3.3

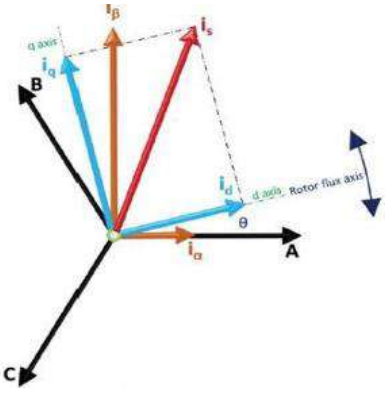


$$I_\alpha = \frac{2}{3}(Ia) - \frac{1}{3}(I_b + I_c) \quad (3.3)$$

$$I_\beta = \frac{1}{\sqrt{3}}(I_b - I_c) \quad (3.4)$$

Fig 3.3 Vector Representation of Clarke's Transform

In Module-4 (Forward Park's Transform), The two-phase orthogonal stationary reference frame currents I_α and I_β are transformed into two phase equivalent orthogonal rotating reference frame current vectors I_d and I_q using equations 3.5 and 3.6. I_d is the direct axis current component that is considered at rotor pole's maximum flux interaction with stator poles, the I_d component is also considered as flux controlling component. I_q current component is in quadrature to I_d at the quadrature axis, the I_q component is considered as the torque controlling component. Fig3.4 shows the vector representation of Forward Park's transform.



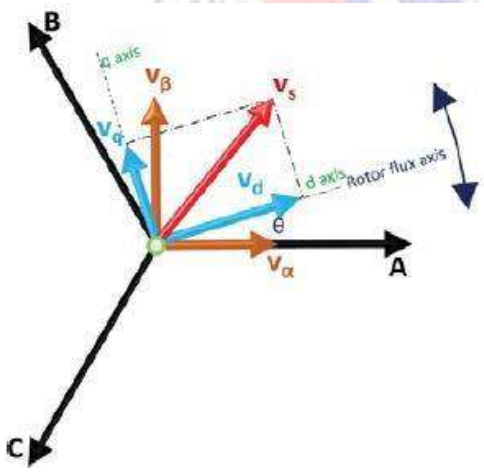
$$I_d = I_\alpha \cos(\theta_r) + I_\beta \sin(\theta_r) \quad (3.5)$$

$$I_q = I_\beta \cos(\theta_r) - I_\alpha \sin(\theta_r) \quad (3.6)$$

Fig 3.4 Vector Representation of Park's transform

In Module 5 (PI Controllers), on performing the forward Clarke and Park transforms, the three phase AC quantities are now considered in Synchronous rotating reference frame eliminating the time varying frequency components, the time invariant current components I_d and I_q values obtained are equivalent DC components of three phase AC current components I_a, I_b and I_c. The I_q reference value corresponding to the speed set is fed to the PI controller, the error associated with measured I_q current and set I_q reference current is modulated as correction signals in PI controllers generating the modulated voltage signals V_d and V_q.

In module-6 (Inverse Park's Transform), The inverse Park transformation, transforms the time invariant d-q-0 voltage signals -V_d and V_q in the rotating reference frame to the equivalent two-phase stationary reference frame components V_α and V_β.using equations 3.7 and 3.8. The two orthogonal time invariant DC components are now considered as two-phase orthogonal time-varying AC equivalent components V_α and V_β. The vector representation of reverse Park's transform is shown in Fig. 3.5.

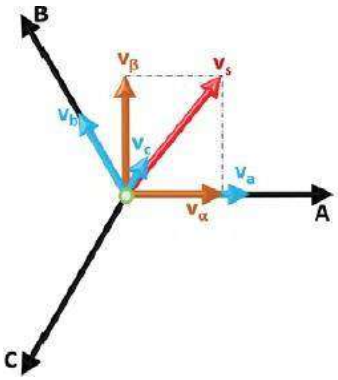


$$V_\alpha = V_q\, cos(\theta_r) - V_d\, sin(\theta_r) \quad (3.7)$$

$$V_\beta = V_d\, sin(\theta_r) + V_q\, sin(\theta_r) \quad (3.8)$$

Fig 3.5 Vector representation of Inverse Park's Transform

In Module-7 (Inverse Clarke's Transform), The two-phase orthogonal AC components are transformed to the three phase equivalent voltages V_a, V_b and V_c. The following equations 3.9, 3.10 and 3.11 are used. The vector representation of reverse Clarke's transform is shown in fig 3.6.



$$V_a = V_\alpha \tag{3.9}$$

$$V_b = -\frac{1}{2}(V_\alpha) + \frac{\sqrt{3}}{2}(V_\beta) \tag{3.10}$$

$$V_C = -\frac{1}{2}(V_\alpha) - \frac{\sqrt{3}}{2}(V_\beta) \tag{3.11}$$

Fig 3.6 Vector representation of reverse Clarke's transformation

In Module 8, (SPWM Generator), The triangular wave is generated at high frequencies equivalent to the switching frequency of 5 kHz. The three-phase Sine waves V_a, V_b and V_c obtained is normalized and then is compared with the high frequency triangular wave to generate the SPWM pulses. Sinusoidal Pulse Width Modulation (SPWM) pulses as shown in Fig 3.7. The Sinusoidal PWM is then fed to the inverter to drive the PMSM motor.

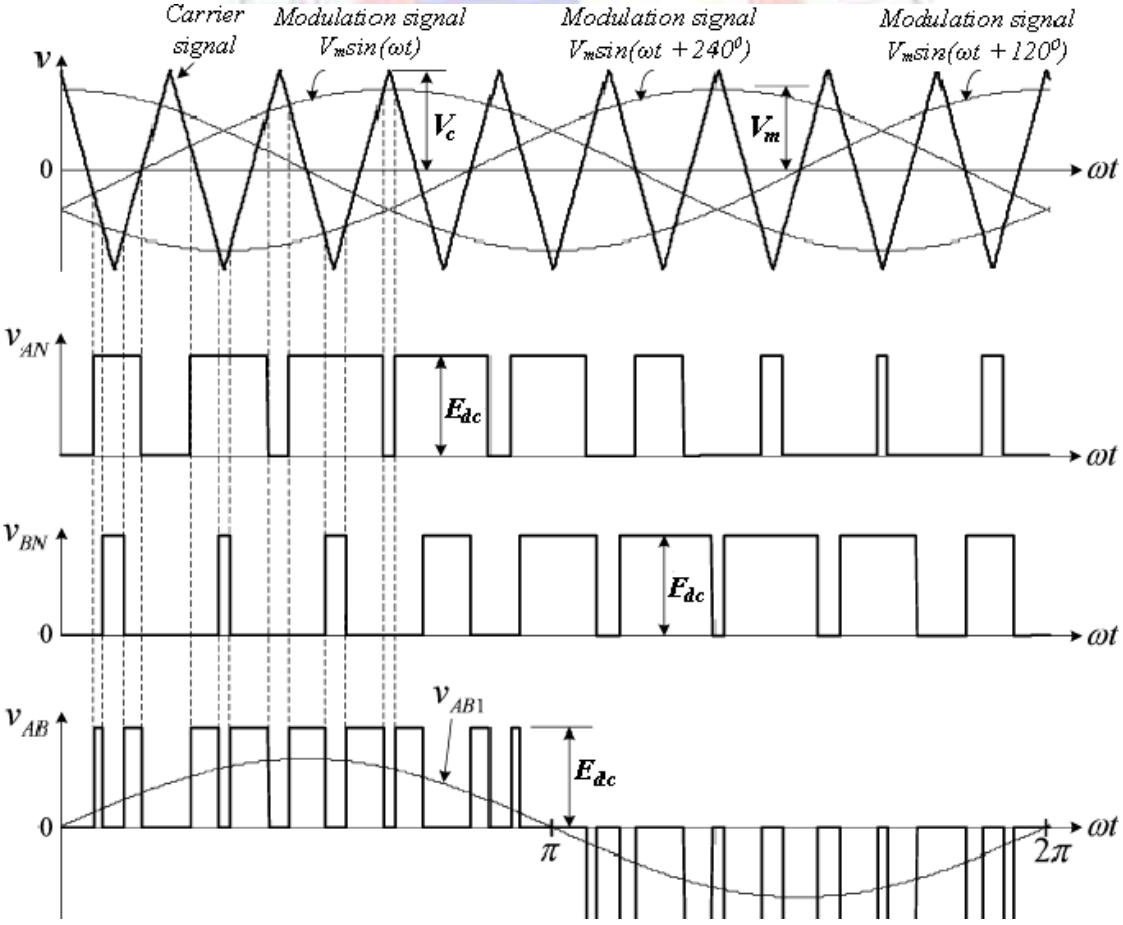


Fig 3.7 Sinusoidal PWM generation

3.3 Block Diagram of FOC algorithm

Fig.3.8 shows the block diagram of the FOC algorithm developed in LabVIEW. The speed and torque control of the PMSM motor is controlled using the feedback signals processed in the FOC algorithm to generate the Sinusoidal PWM signals fed to the inverter to drive the motor.

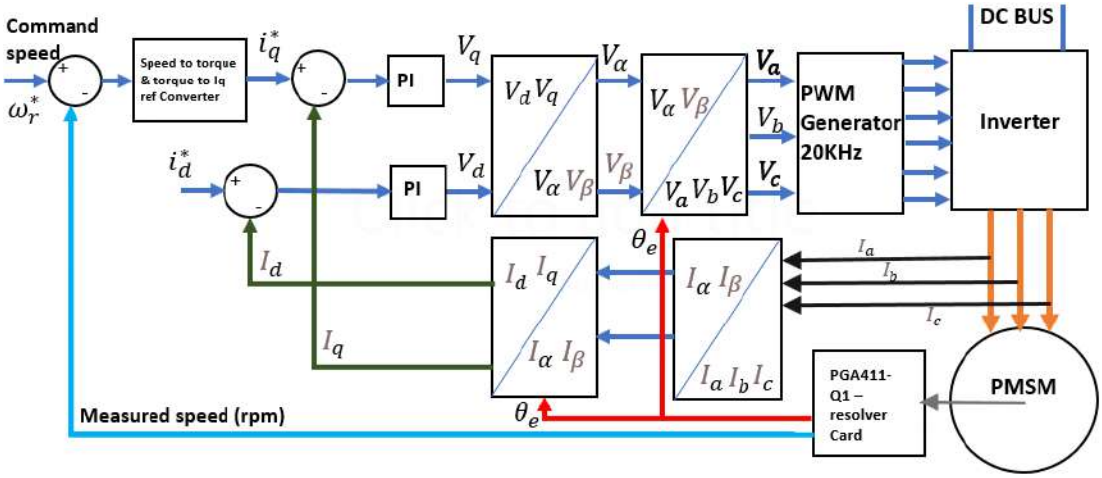


Fig. 3.8 Block Diagram of FOC in LabVIEW

In the Field Oriented Control, the three-phase time varying stator currents I_a, I_b and I_c of the PMSM motors are transformed to equivalent two-phase time invariant orthogonal components I_d and I_q visualized as vectors by performing forward Clarke's and forward Park's transforms. One of the vector components - I_d provides control over the magnetic flux of the motor and the other vector component - I_q provides control over the torque of the motor. The drive control system modulates the correction values of flux and torque based on the error generated by the feedback and command reference signals. The PI controllers are employed to modulate the measured vector components tuned to the reference values. The modulated orthogonal voltage vectors V_d and V_q are obtained from the PI controllers. The inverse Park and inverse Clarke's transforms are performed to obtain the time varying voltage signals. The voltage signals obtained is compared with high frequency triangular wave to generate sinusoidal pulse width modulation signals (SPWM) to operate the motor in forward motoring, forward braking, reverse motoring and reverse braking operations. The summary of the Field Oriented Control for torque control and field-weakening control is shown in Fig.3.9.

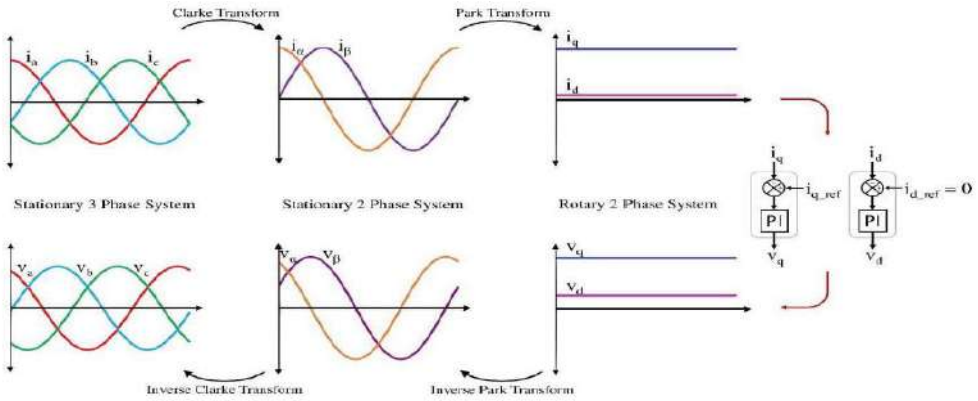


Fig. 3.9 Summary of Field Oriented Control (FOC) algorithm

The position of the rotor is sensed using the resolver embedded to the shaft of the PMSM motor. In resolver decoder block, the resolver decoder – PGA411Q1 module is used to obtain the mechanical angular displacement θ_m. The electrical angular displacement θ_e is calculated for processing of Clarke and Park transforms.

In Clarke and Park transform blocks, the three-phase time varying currents I_a,I_b and I_c are transformed to two phase time invariant current vectors I_d and I_q. The error in measured speed and command speed is used to identify the command currents I_d* and I_q*. The current vectors are modulated to equivalent voltage control vectors V_d and V_q in PI controllers' block.

In inverse Park and Clarke's transform blocks, the two phase time invariant voltage vectors are transformed to equivalent three phase voltages V_a,V_b and V_c. The three phase voltage signals are compared with high frequency triangular waveform to generate the sinusoidal PWM signals at 180-degree conduction mode in PWM generation block.

The sinusoidal PWM signals generated is provided with dead time of 4us for switching between top to bottom switches. The SPWM signals are fed to the Semikron inverter to obtain three phase sinusoidal voltages using the DC bus voltage to drive the PMSM motor.

3.4 Summary

The Field Oriented Control algorithm, methodology followed in realizing the project, block diagram for the proposed methodology to control the motor in torque mode and field-weakening mode to achieve maximum torque and maximum speed were explained.

Chapter 4

SPECIFICATIONS AND DESIGN

The LabVIEW software design requirements and hardware specifications of the devices used in the realization of the proposed FOC algorithm with wire harnessing in reducing noise etc. is discussed in this chapter.

4.1 Software Design Specifications

The LabVIEW graphical software is considered for the implementation of the FOC algorithm for the control of the DUT motor in the real-time. The program is designed to control the motor in all 4 quadrants - forward motoring, forward braking, reverse motoring and reverse braking. The internal buffer of the cRIO and FPGA is in volatile memory and the processing of the signals must be in real time to avoid loss of data. The software expectations are to acquire and process the data at the shortest possible time in order of micro seconds and also generate the desired sinusoidal PWM signals that suits the frequency of the motor inputs. The real-time buffers with producer/consumer design is considered for data acquisition and processing in real time. The data needs to be processed before the buffer memory is overwritten in RT-FIFO. The creation of Sub-Vi and usage of control input are avoided to decrease the process time. The program is designed to execute in a series such that the high priority functions are executed first followed by the normal priority functions. Optimization of the program at each level for individual functions is achieved to process the FOC algorithm under 50us.

The FPGA-target program is designed to read and write functions to read the analog input data through FPGA modules NI-9223 (Analog Input-1MS/s) and write digital data through NI-9401(Digital Output-10Mhz). The FOC algorithm is designed in timed-loop structure in cRIO following the methodology discussed in Chapter – 3. The software design is considered to generate these Sinusoidal PWM signals at – least at minimum of 5kHz.

The front panel of LabVIEW is designed to provide control signals such as speed setting, PI controllers gain setting with record and stop command. The I_q reference and the I_d reference are provided using the look-up table. The real time data such as speed,

torque values are displayed along with position, current and voltage waveforms in the graphical user interface (GUI) to control the DUT motor.

4.2 Hardware Specifications

The specifications of the devices considered in the implementation of the FOC algorithm and development of the hardware module is as follows.

- **Selection of Motor**

  The Electric vehicle chassis considered is the Honda Amaze SUV – petrol variant, the motor rating equivalent to the ICE engine is considered. The motor considered is an 8 pole IPM - PMSM motor with 41 KW – continuous power and 60KW peak power. The base speed of the motor is 2800 rpm and the peak speed is 4000 rpm. The voltage rating of the DUT motor is V_{rms}=150 volts, with current rating of 450 I_{rms} = 450 A.

- **Selection of Resolver**

  The Resolver mounted on the motor shaft is the 8-pole hollow shaft type resolver – 2367254-1 is used to match the motor pole pairs.

- **Selection of Inverter**

  The inverter is chosen based on the maximum switching frequency required to operate the motor at the top most speed. The maximum switching frequency considered for motor control is 12 kHz and the minimum optimal switching frequency is 5kHz. The Semikron Inverter SKAI 45 A2 GD12-WDI module with input voltage rating of DC-V_{max} = 800V and input current rating of DC - I_{nom} = 300A with 12kHz switching frequency IGBT module is employed.

- **Resolver Decoder module**

  The resolver's sine and cosine signals are converted to the real time analog voltage signals observed as an up-ramp signal varying from 0.4V to 4.5 V, using Texas Instruments PGA411-Q1 development board is used as resolver decoder.

- **Selection of Real time interface**

The National Instruments cRIO-9046, FPGA interface cubicle embedded with FPGA modules NI-9223 - the high-speed analog input module with sampling rate of 1 Mega Samples/second and NI-9401 - the high-speed digital output, processing digital signals at frequency of 10Mhz is used.

4.3 Hardware – Wiring Block Diagram

The Fig 4.1 shows the block diagram of the hardware wiring and connection diagram.

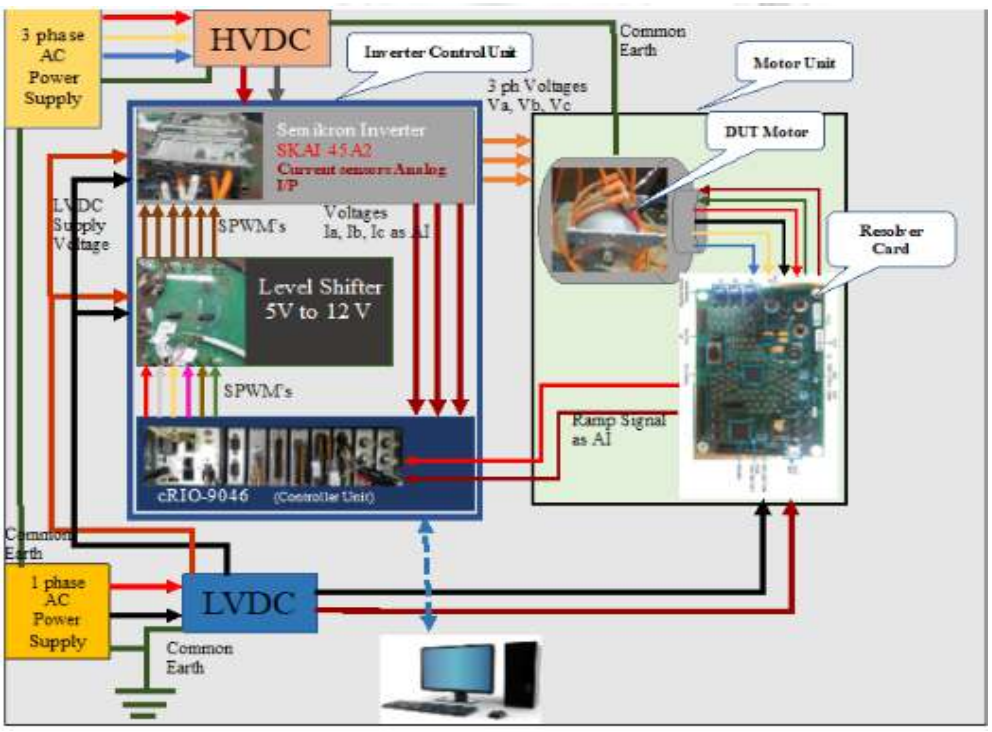


Fig 4.1 Connection block diagram of FOC Hardware module

The EMC and EMI regulations and the necessary measures to reduce noise in the system is followed. The noise in the data transferred is reduced by multi point grounding and shielding all conductors with aluminum foils. The earthing of all equipment to the body ground and the main panel ground is strictly followed. The shielded twisted pair wires are considered for data transmission from current sensors and resolver decoder to NI-cRIO. EtherCAT network at 12 Mbps is established between cRIO, computer, dyno test bench and power sources for remote access of all devices through LabVIEW using MODBUS protocol.

4.4 Summary

The design specifications of the software, steps to be considered in developing the FOC algorithm in LabVIEW, GUI requirements to provide control settings of motor and the hardware requirements with specifications were explained in this chapter.

Chapter 5

SIMULATION AND IMPLEMENTATION

The FOC algorithm developed in LabVIEW software is simulated using MATLAB – Simulink. The steps involved in designing of individual blocks, functions of the block and the results obtained in each block is explained in this chapter.

5.1 MATLAB model of the FOC algorithm

The vector control algorithm – FOC for the torque control and the flux weakening control of the DUT motor is designed using the mathematical model of PMSM motor and the simulation results are verified with mathematical values obtained. The Mathematical model of the motor is considered based on the desired torque and speed response to be achieved by the motor using the following equations 5.1,5.2,5.3 and 5.4.

$$\frac{di_d}{dt} = \frac{1}{L_s}[V_d - Ri_d + wL_s i_q] \tag{5.1}$$

$$\frac{di_q}{dt} = \frac{1}{L_s}[V_q - Ri_q - wL_s i_d - w\psi] \tag{5.2}$$

$$T_e = 1.5p[\lambda i_q + (L_d - L_q) I_d I_q] \tag{5.3}$$

$$\frac{dw}{dt} = \frac{1}{J} T_e \tag{5.4}$$

The inductance, resistance of the windings of the motor, air gap flux, torque and inertia of the motor are known from the equations 5.1,5.2,5.3 and 5.4. The mathematical model of the PMSM motor is developed as shown in Fig 5.1.

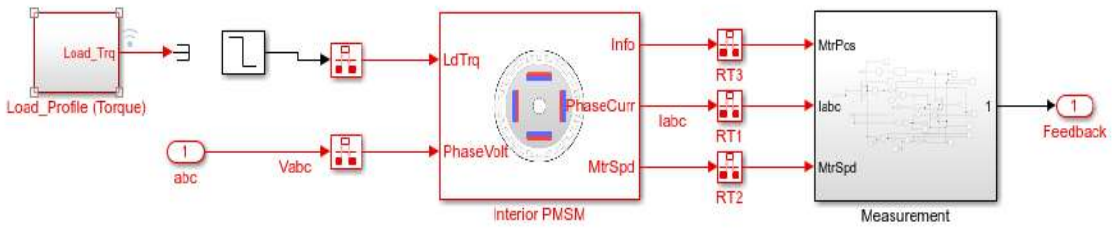


Fig.5.1 MATLAB model of PMSM DUT motor

The Interior PMSM motor is simulated with a constant light load torque of 80mNm. The position of rotor and speed is sensed using the resolver to get the mechanical angular displacement (θ_m). The currents – I_a, I_b and I_c are measured as feedback from motor terminals along with rotor position.

The resolver decoder obtains the rotor position as an up-ramp signal for rotor rotating in clockwise direction. The ramp signal is as a variable analog voltage ranging from 0.4 V to 4.5 V. The measured ramp voltage signal is normalized to vary from 0 to 2π radians representing the mechanical angular displacement (θ_m) using equation 5.5. One complete ramp signal corresponds to one complete rotor shaft rotation.

$$\theta_m = \frac{ResVoltage - V_{min}}{V_{max} - V_{min}} \times 2\pi \ [rad] \tag{5.5}$$

The electrical angular displacement (θ_e) required to achieve one full mechanical rotation depends on the number of rotor poles of PMSM motor. The electrical angular displacement is calculated using equation 5.6.

$$\theta_e = \frac{P}{2}\theta_m \ [rad] \tag{5.6}$$

Where, P – number of poles

The simulation of extraction of rotor position as a ramp, normalizing the ramp to obtain the mechanical angular displacement and calculating the equivalent electrical angular displacement is executed in MATLAB-Simulink. Fig 5.2 represents the measuring and computational blocks of θ_m and θ_e.

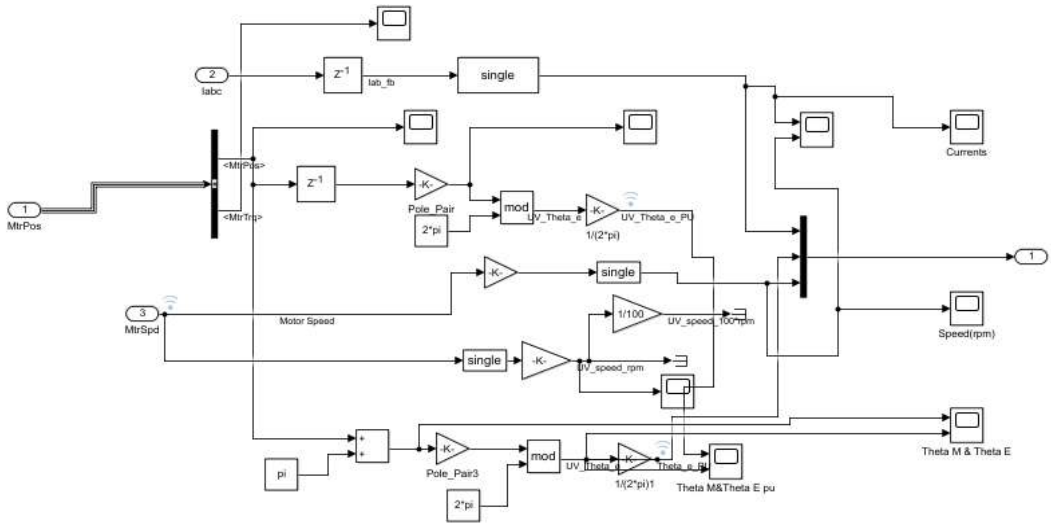


Fig.5.2 Measuring and Computational blocks of θ_m and θ_e

The motor considered for test is an eight pole PMSM motor. For each mechanical rotation represented by ramp θ_m, four electrical ramps θ_e are observed. The θ_m and θ_e values plotted with respect to time is shown in Fig 5.3

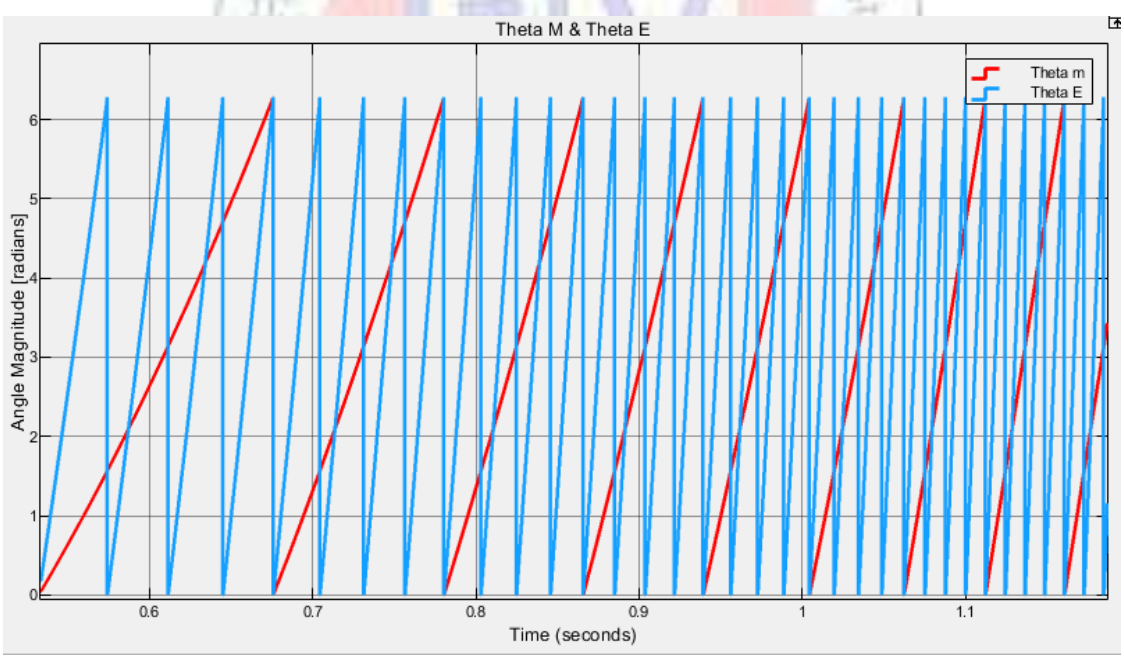


Fig 5.3 θ_m and θ_e values plotted with respect to time

The currents from each phase are considered as the feedback for the processing of forward Clarke's and Park's transformations The three-phase time varying currents I_a, I_b and I_c are shown in Fig 5.4.

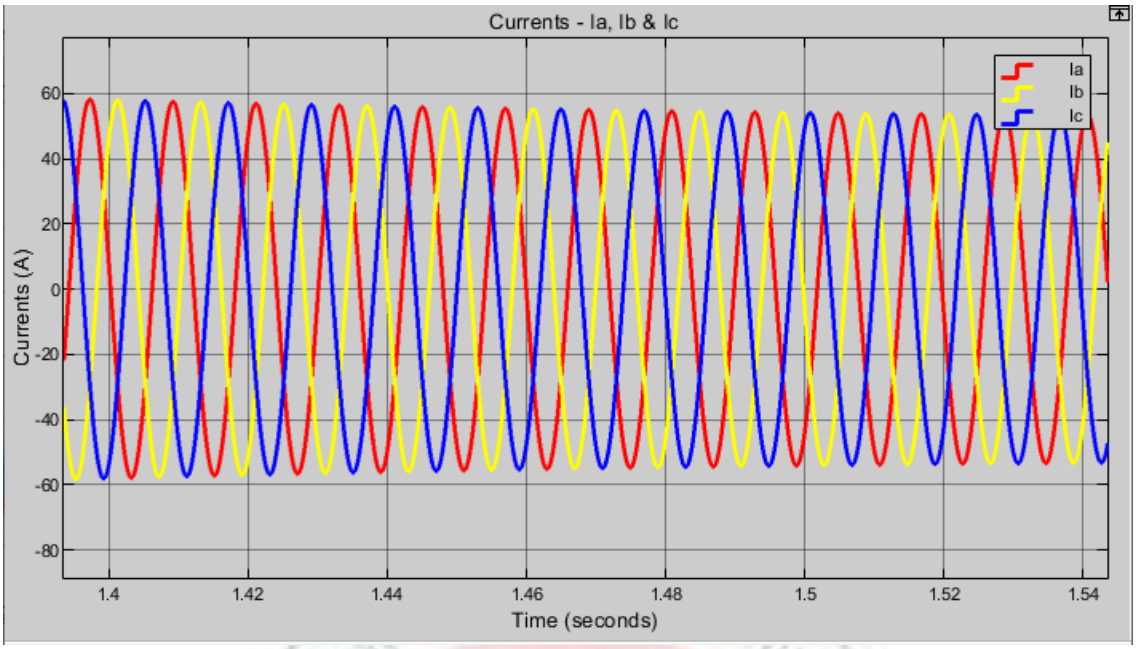


Fig 5.4 Currents I_a, I_b and I_c. measured for forward Clarke's and Park's transforms

The three-phase sinusoidal currents I_a, I_b and I_c are measured from the current sensors embedded in the Semikron inverter on the motor input terminals for the processing of Clarke's and Park's transform. The control blocks of the FOC algorithm – forward Clarke's transform, forward Park's transform, reverse Park's transform and reverse Clarke's transformations is shown in Fig 5.5.

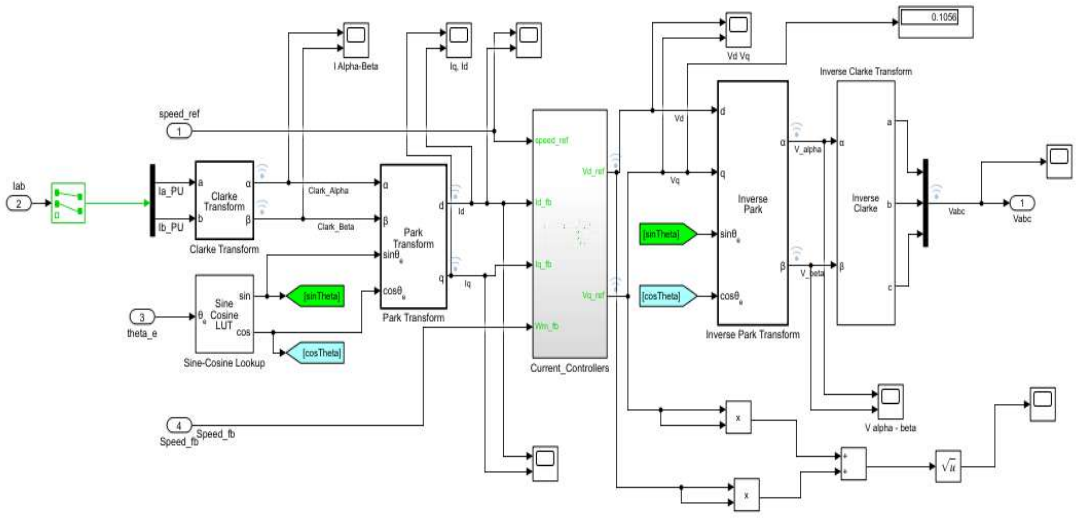


Fig 5.5 Forward and Reverse transformations blocks

- **Forward Clarke's Transform**

The three phase currents I_a, I_b and I_c aretransformed in to two phase equivalent orthogonal currents I_α and I_β. The three - phase stationary reference phasors are transformed to equivalent two phase orthogonal stationary reference currents in forward Clarke transform using equations 5.7 and 5.8.

$$I_\alpha = \frac{2}{3}(Ia) - \frac{1}{3}(I_b + I_c) \tag{5.7}$$

$$I_\beta = \frac{1}{\sqrt{3}}(I_b - I_c) \tag{5.8}$$

The three-phase stationary reference frame currents are transformed to equivalent two-phase orthogonal stationary reference currents I_α and I_β, in forward Clarke's Transform. The orthogonal currents I_α and I_β are plotted in MATLAB-Simulink, shown in Fig.5.6.

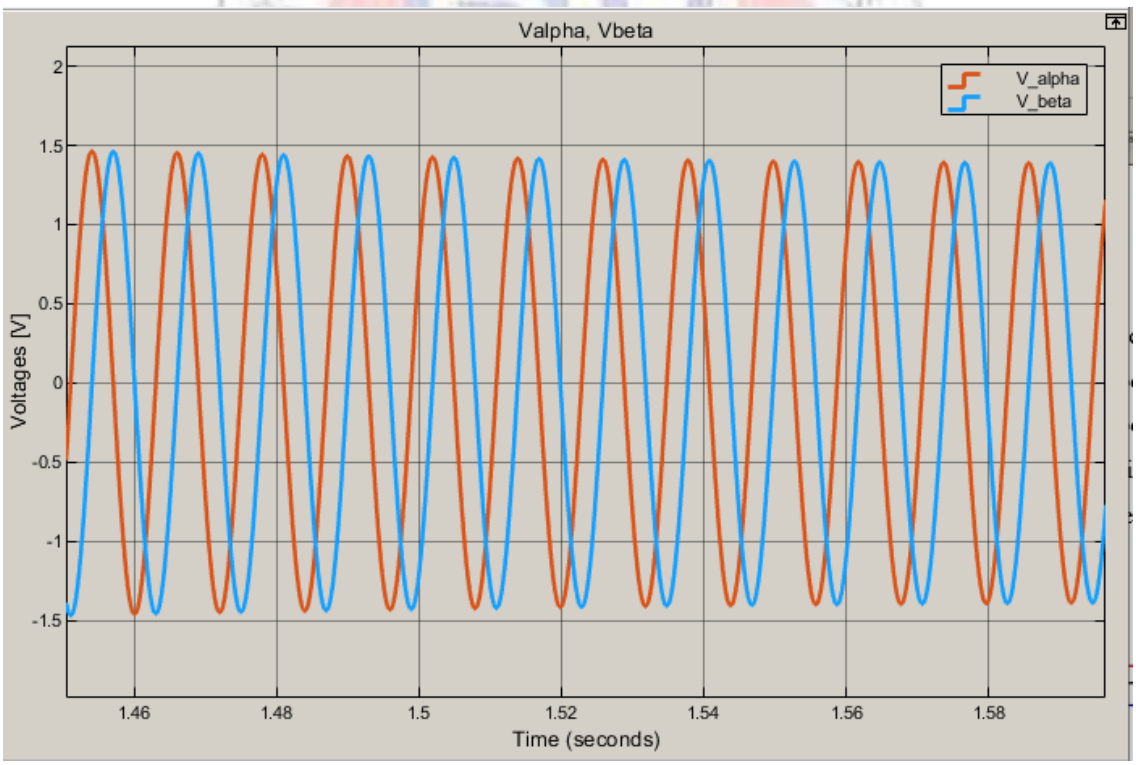


Fig.5.6 I_α and I_β two-phase orthogonal stationary reference currents

The currents I_α and I_β are two-phase orthogonal current components equivalent of the three-phase currents I_a, I_b and I_c.

- **Forward Park Transform**

The two-phase equivalent orthogonal stationary reference frame currents I_α and I_β are transformed into two phase equivalent orthogonal rotating reference current vectors I_d and I_q, using equations 5.9 and 5.10. I_d is the direct axis component considered at maximum flux interaction point of rotor poles with stator poles so I_d component is considered as flux controlling component and I_q current component is in quadrature to I_d at the quadrature axis, the I_q component is the torque controlling component. The two-phase equivalent orthogonal current vectors I_d and I_q in rotating reference frame is shown in Fig.5.7.

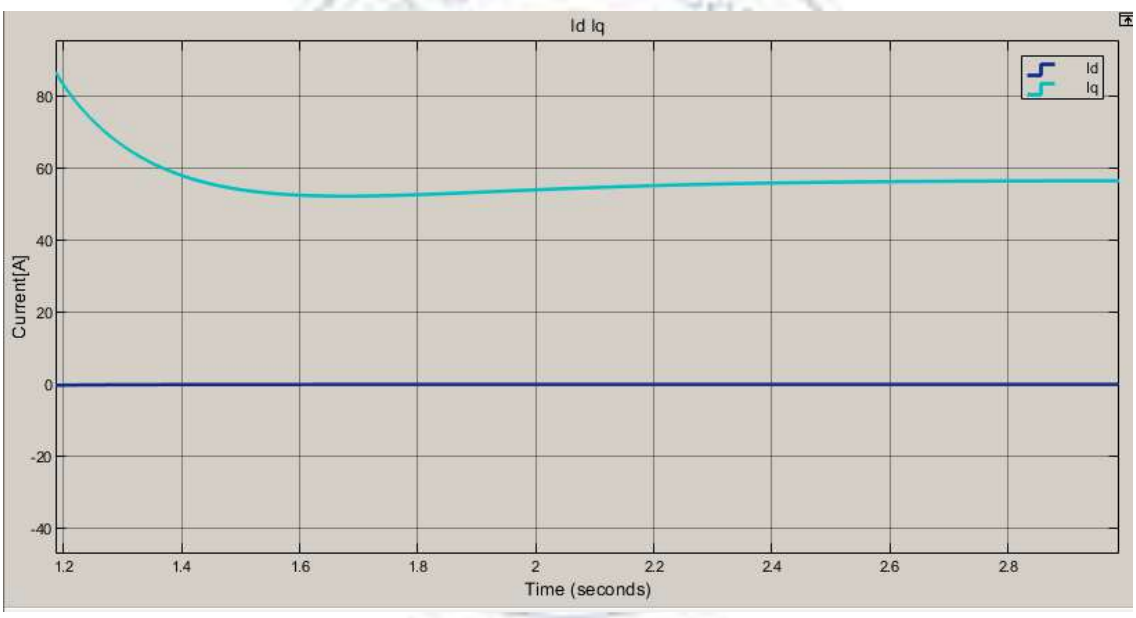


Fig 5.7 The two-phase orthogonal current vectors I_d and I_q in rotating reference frame

The current I_d refers direct axis (d-axis) component – flux control component set zero in torque control mode. The current Iq refers the quadrature axis (q-axis) component – Torque control component modulated to control the torque of motor.

- **PI Controllers Block**

On performing the forward Clarke and Park transforms, the three phase AC quantities are now considered in Synchronous rotating reference frame eliminating the time varying frequency components, the time invariant current components I_d and I_q

values obtained are equivalent DC components of three phase AC current components I_a, I_b and I_c. The I_d and I_q reference values corresponding to the speed set is fed to the PI controller, the error associated with measured I_d, I_q currents and set I_d, I_q reference currents is modulated as correction signals in PI controllers. The proportional gain K_p and integral gain K_i values of the PI controllers are calculated using the equations 5.9 and 5.10.

$$K_P = L_s \omega_0 \tag{5.9}$$

$$K_i = \frac{R\omega_0}{2\pi} \tag{5.10}$$

Where:

L_s is the Line inductance between RY phases

R is the Line resistance between RY phases

ω_0 is the current bandwidth

Fig 5.8 represents the PI controller blocks simulated in MATLAB – Simulink. The Kp gain is tuned with proper current bandwidth to avoid overshoots and to achieve quick response. Ki gain values are tuned to regulate the steady state error vales close to set value. The corrections modulated in PI controller generates the correction modulated voltage signals V_d and V_q.

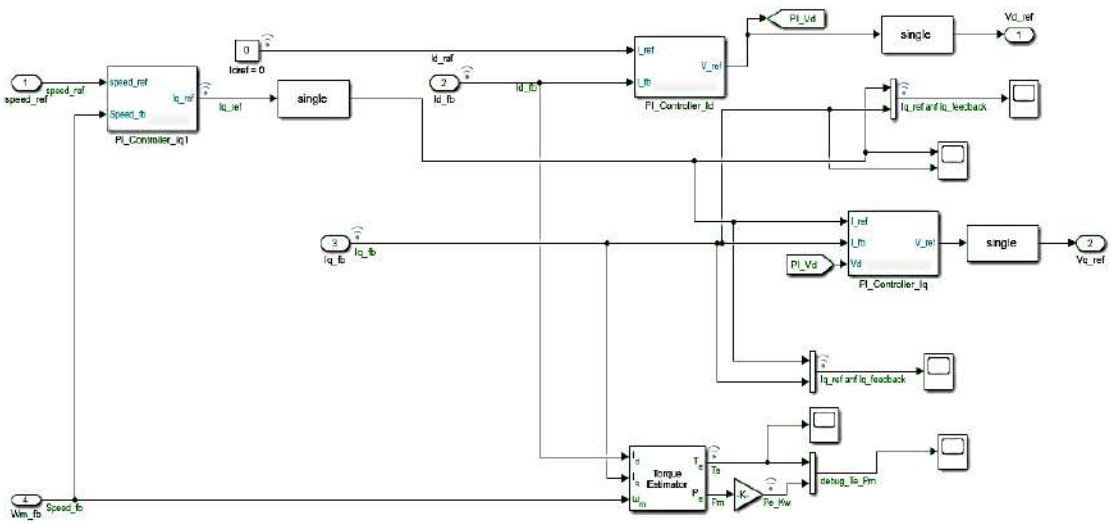


Fig 5.8 PI controller block simulated in MATLAB – Simulink

The injection of I_d and I_q reference currents causes the change in orientation of the d-axis and q-axis current vectors based on the error computed with measured values. The d-axis and q-axis angles are modulated and the voltage signals with modulated d-axis and q-axis angles are obtained as V_d and V_q. Fig 5.9 represents the correction modulated voltage signals V_d and V_q simulated in MATLAB – Simulink.

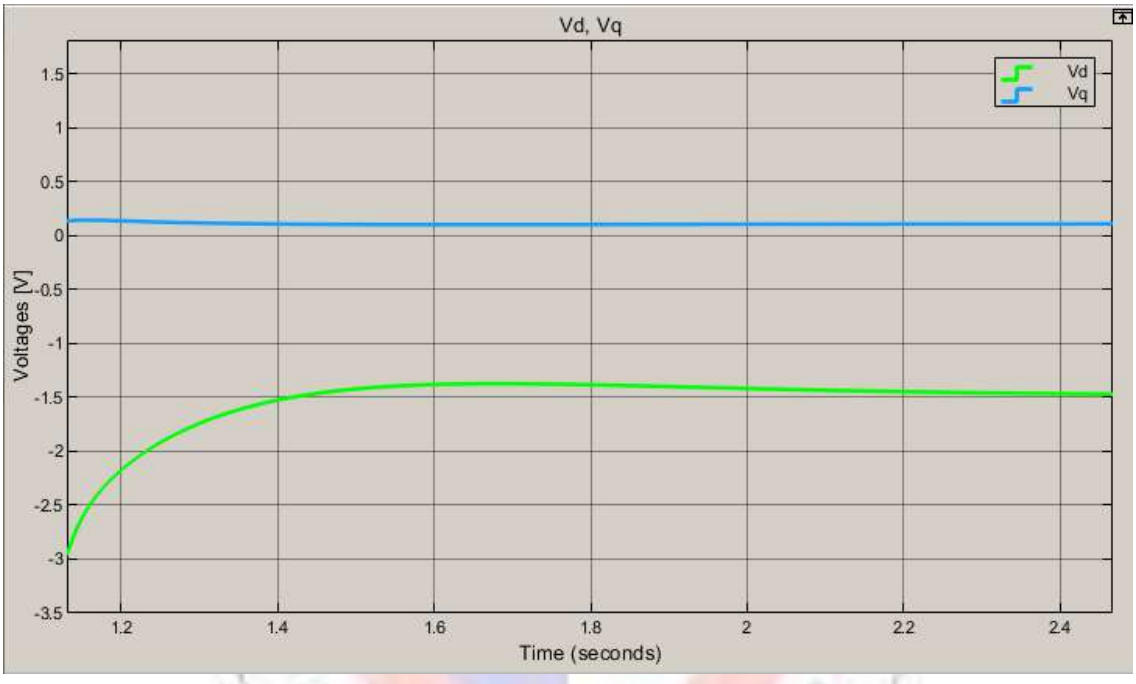


Fig. 5.9 Correction modulated voltage signals V_d and V_q from PI controllers

The d-axis and q-axis voltage vectors Vd and Vq are modulated in the PI controllers based on the error between set speed and measured speed. The direct-axis component Vd is tuned to a constant negative value and the quadrature -axis component Vq tuned to a constant positive value.

- **Inverse Park Transform**

The two-phase time invariant voltage vectors V_d and V_q in rotating reference frame are transformed in to two phase time varying voltages V_α and V_β in stationary reference frame using the equations 5.11 and 5.12.

$$V_\alpha = V_q \cos(\theta_r) - V_d \sin(\theta_r) \quad (5.11)$$

$$V_\beta = V_d\, sin(\theta_r) + V_q\, sin(\theta_r) \tag{5.12}$$

Fig.5.10 represents the two-phase time varying orthogonal voltages V_α and V_β.

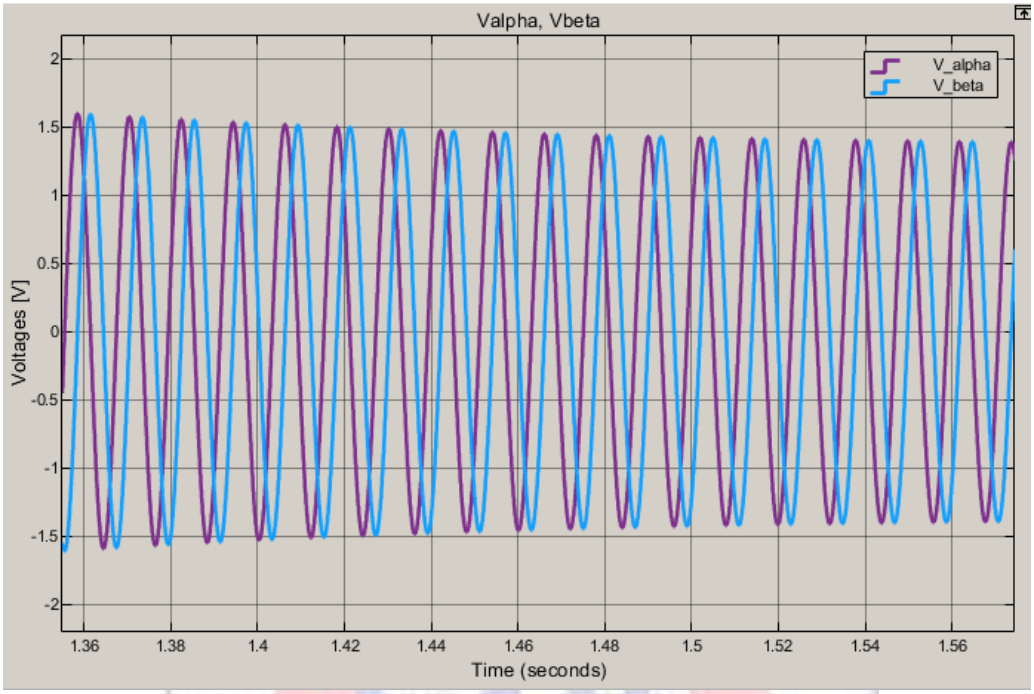


Fig 5.10 V_α and V_β two-phase orthogonal stationary reference frame Voltages

The DC equivalent orthogonal voltage vectors V_d & V_q are transformed to 2 phase AC equivalent sinusoidal voltages V_α and V_β in reverse Park Transform.

- **Inverse Clarke's transform**

The two-phase time varying sinusoidal voltages V_α and V_β are transformed to equivalent three-phase sinusoidal voltages V_a, V_b and V_c using the equations 5.13, 5.14 and 5.15.

$$V_a = V_\alpha \tag{5.13}$$

$$V_b = -\frac{1}{2}(V_\alpha) + \frac{\sqrt{3}}{2}(V_\beta) \tag{5.14}$$

$$V_C = -\tfrac{1}{2}(V_\alpha) - \tfrac{\sqrt{3}}{2}(V_\beta) \tag{5.15}$$

Fig.5.11 represents the simulation of inverse Clarke's transform in MATLAB – Simulink, the two-phase time varying voltage is transformed to three-phase time varying sinusoidal voltage V_a, V_b and V_c.

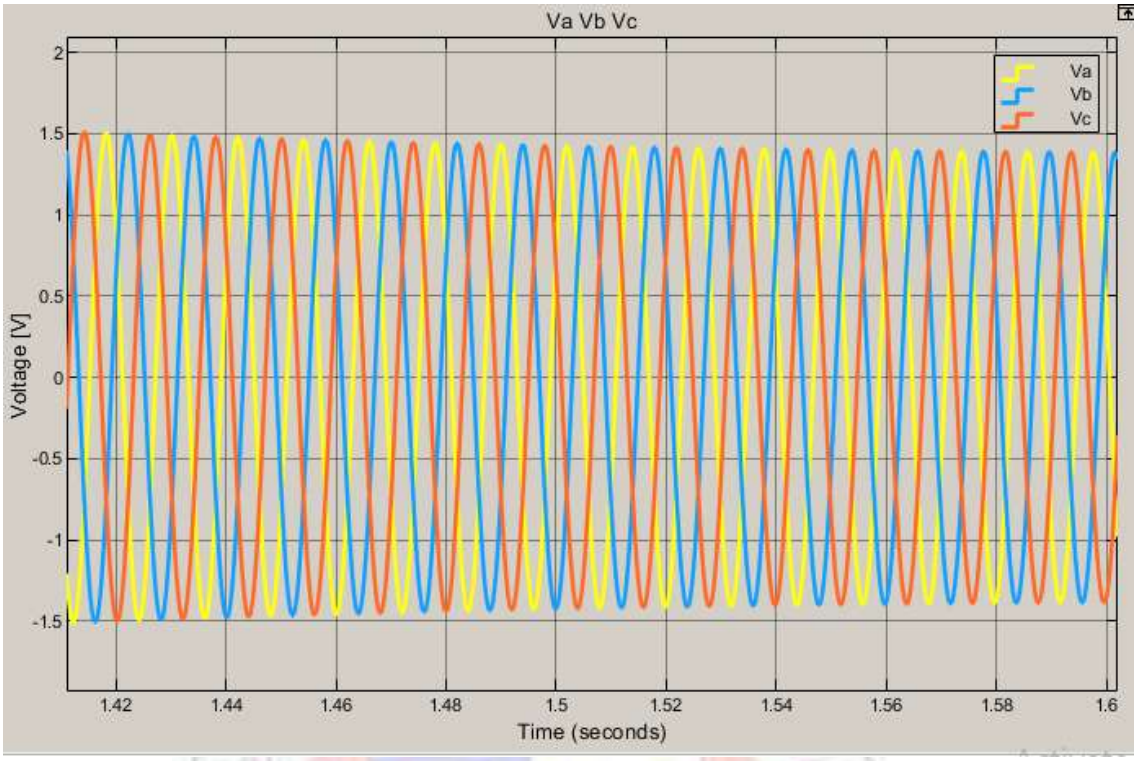


Fig 5.11 – Three-phase time varying sinusoidal voltage V_a, V_b and V_c

The two-phase sinusoidal voltages V_α and V_β are transformed to equivalent three-phase sinusoidal voltages V_a, V_b and V_c at 120-degree phase shift between the phases in inverse Clarke's Transform.

- **Sinusoidal Pulse Width Modulation (SPWM) Signal generation Logic**

A triangular wave is generated at frequency of 5 kHz using the triangle wave generator function in MATLAB/LabVIEW. The three-phase Sinusoidal voltages V_a, V_b and V_c obtained is normalized to amplitude equivalent to the amplitude of three-phase sinusoidal voltages and is compared with the high frequency triangle waveform to generate the Sinusoidal PWM pulses at 180-degree conduction mode. The Sinusoidal PWM generated is then fed to the inverter to drive the PMSM motor. The dead time between switching of the top-to-bottom switches is implemented by providing time delay of 4 micro seconds only for the bottom switches of all three phase. Fig.5.12 represents the simulation of SPWM logic in MATLAB-Simulink.

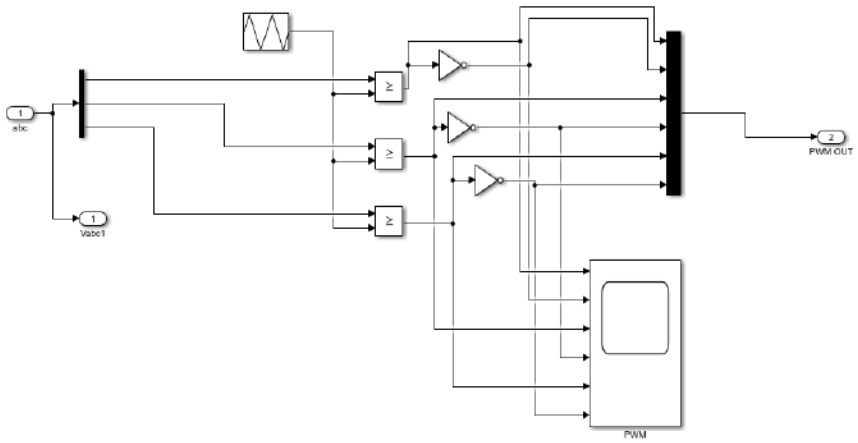


Fig 5.12 Sinusoidal PWM Logic for 180-degree conduction mode

The Sinusoidal PWM signals obtained in MATLAB-Simulink is as shown in Fig 5.13.

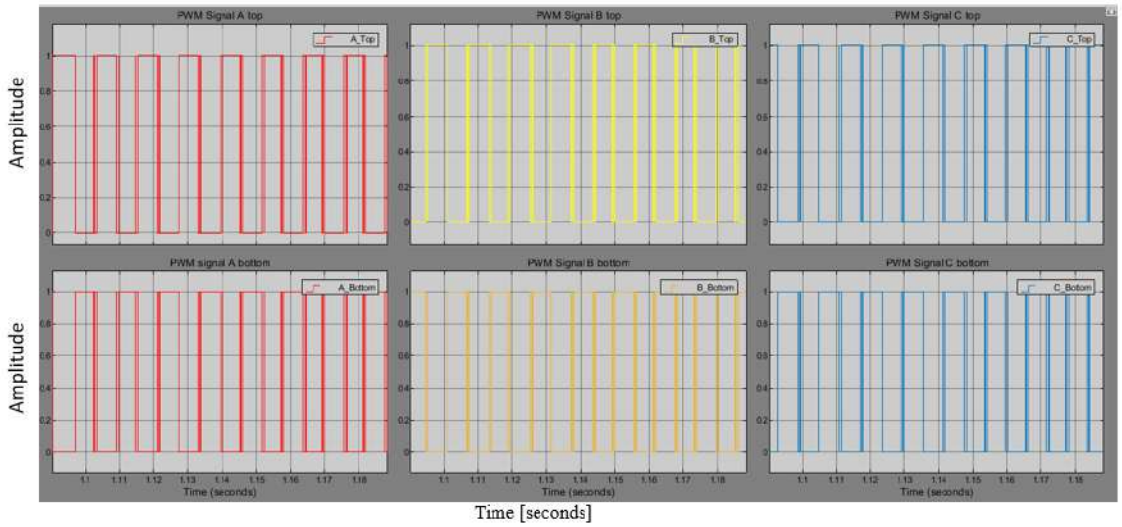


Fig.5.13 Sinusoidal PWM signals generated in MATLAB-Simulink

The Sinusoidal PWM signals are generated at 180-degree conduction mode with 4 micro seconds dead time between the switching of top to bottom switches. The SPWM signal has a 180-degree phase shift between the top and bottom switch of same phase.

5.2 Summary

The FOC algorithm implemented in LabVIEW for the PMSM motor was simulated in MATLAB-Simulink. The forward Clarke and Park transformations, PI controllers tuning, inverse Park and Clarke transformations and Sinusoidal PWM generation logic were explained.

Chapter 6

RESULTS & DISCUSSION

This chapter discusses about the simulation and hardware results of the Field Oriented Control algorithm on PMSM – test motor. The simulation results for speed control and torque response of PMSM motor is shown along with the graphical user interface (GUI) developed in LabVIEW is presented. The Sinusoidal PWM signals, phase and line voltages measured in the developed hardware module is shown, the chapter also discusses a typical torque mode test conducted on the test motor with varying load in forward motoring, forward braking, reverse motoring and reverse braking on a 350kW Dyno test bench.

6.1 Simulation Results

The results of simulation of FOC algorithm carried out in MATLAB-Simulink, presented in chapter 5 are included in this section. The speed and torque response of the motor at speed set under the base speed and speed set beyond base speed of the motor is explained. The test motor's base speed is specified as 2800rpm.

6.1.1 Motor speed set under base speed

The speed of the motor is set to 1000 rpm in the simulation of FOC algorithm. The minimum load torque of 80mNm is set on the motor shaft representing the no-load condition. The I_q reference value is set for the command speed specified using the look-up table shown in Fig 6.1.

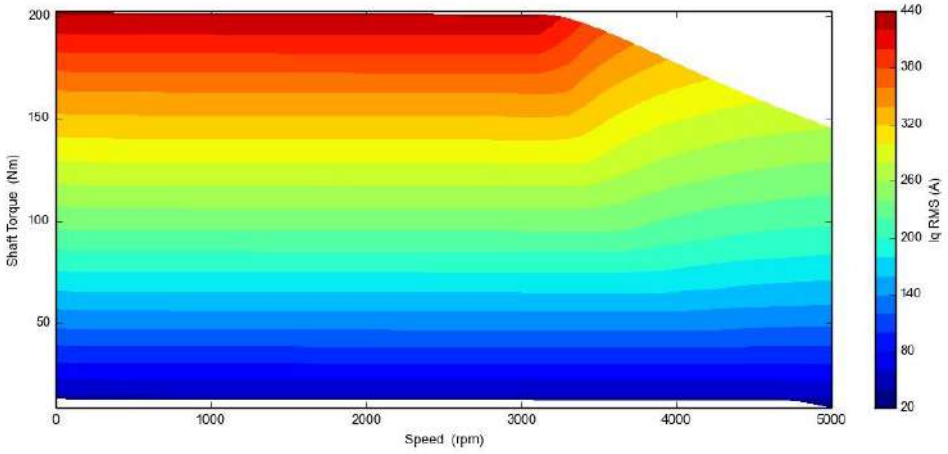


Fig.6.1 I_q reference look-up table for speed command for specified load torque

For command speed of 1000 rpm, at no load condition the I_q reference value of 20 A is set. The motor achieves the set speed in 1.5 seconds. Fig 6.2 represents the speed waveform at 1000 rpm and Fig 6.3 represents the torque response at 80mNm light load at 1000 rpm.

Fig.6.2 The Speed response of the test motor at 1000rpm at 80mNm light load

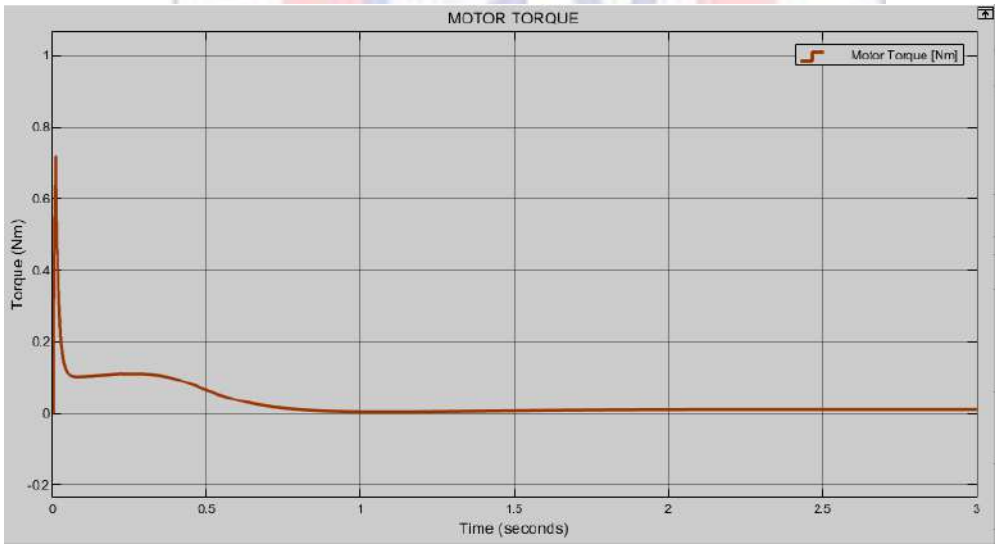


Fig.6.3 The torque response of the motor at 80mNm load at 1000 rpm

The torque increases initially to a peak value to drive the motor from stand still overcoming the cogging torque and to drive to the motor to set rpm value. The torque then reduces gradually and settles to the value equivalent to the load torque on the shaft. The speed of the motor oscillates due to cogging torque then increases gradually and settles at the value equivalent to the set speed.

6.1.2 Motor speed set beyond base speed

The speed of the motor is set to 4000 rpm in the simulation of FOC algorithm. The minimum load torque of 80mNm is set on the motor shaft representing the no-load condition. The I_d reference value is set for the command speed specified using the look-up table shown in Fig 6.4.

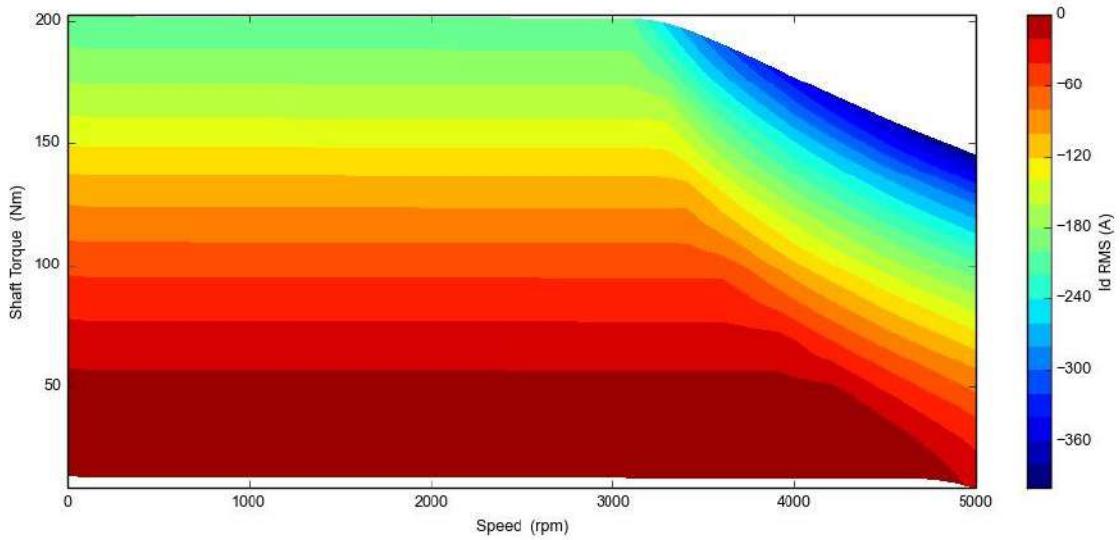


Fig.6.4 I_d reference look-up table for speed command for specified load torque

For command speed of 4000 rpm, at no load condition the I_d reference value of 30 A is set . The motor achieves the set speed in 1 second. Fig 6.5 represents the speed waveform at 4000 rpm and Fig 6.6 represents the torque response at 80mNm light load at 4000 rpm.

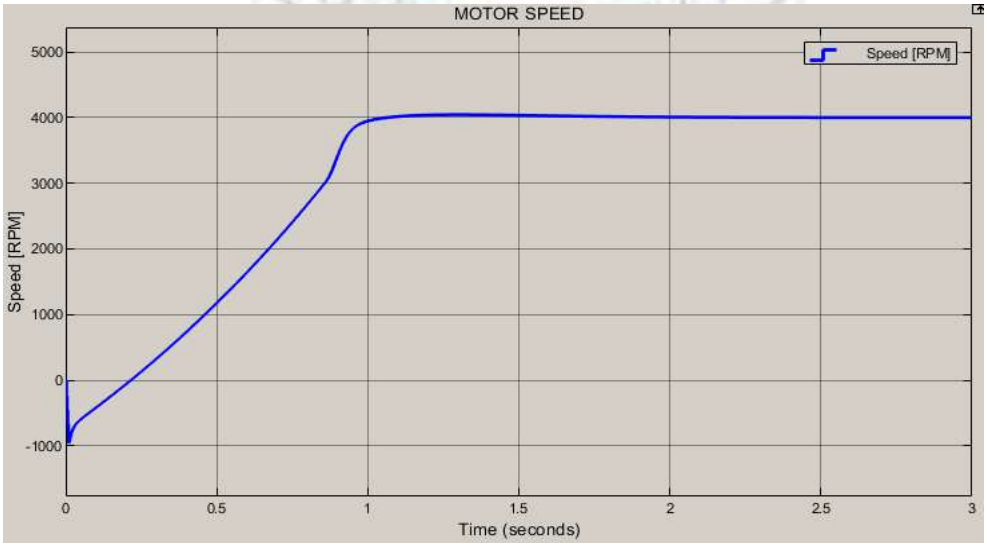


Fig.6.5 The Speed response of the test motor at 4000rpm at 80mNm light load

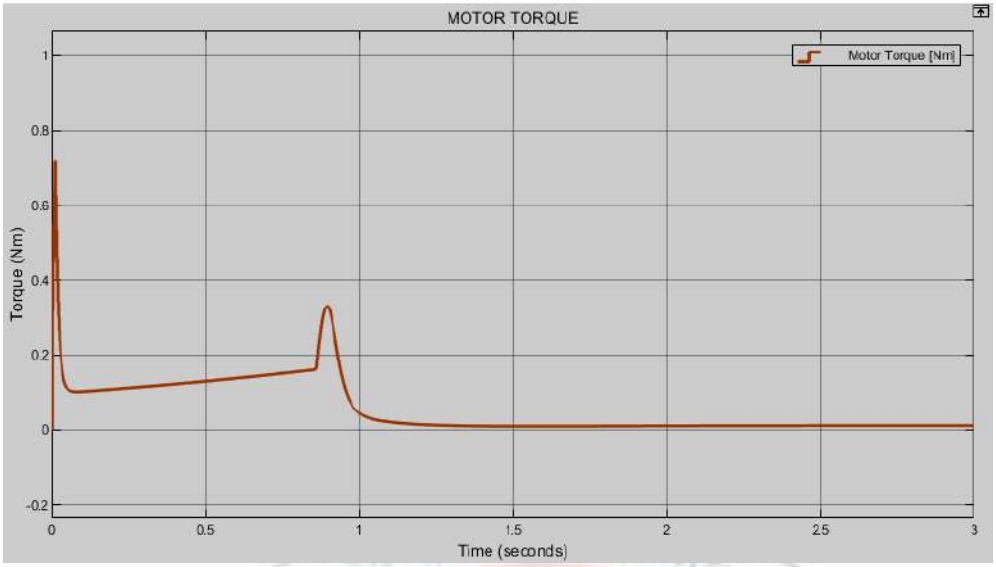


Fig 6.6 The torque response of the motor at 80mNm load at 4000 rpm

The torque rises to its peak initially driving the motor from stand still, the torque drops abruptly on overcoming the cogging torque then increases gradually until the set speed is achieved, the torque gradually decreases and settles at a value equivalent to the load torque. The speed curve initially oscillates showing the cogging effect and then rises gradually and settles at the set speed.

6.2 Graphical User Interface (GUI) in LabVIEW

The graphical user interface (GUI) for the developed FOC algorithm in LabVIEW is as shown in Fig 6.7.

Fig 6.7 The GUI designed in LabVIEW for FOC motor controller algorithm

The Graphical User Interface (GUI) is designed on the front panel of cRIO vi of the FOC algorithm in LabVIEW. The control input for the speed setting, motor parameters settings such as number of rotor poles, DC bus voltage, PI controller gain values settings etc. are provided. The real-time parameters measured in the processing of FOC algorithm such as rotor position - θ_m, θ_e, speed, currents waveforms- I_a, I_b, I_c, I_α, I_β, I_d, I_q, and voltage waveforms - V_α, V_β, V_d, V_q, V_a, V_b and V_c are displayed with their corresponding numeric value. The values displayed in the GUI are also recorded with time stamping in excel spreadsheet.

6.3 Hardware Results of FOC in LabVIEW

The hardware module is developed as discussed in Chapter -4. The Sinusoidal PWM signals generated, the line voltage and the phase voltage measured on no-load condition are explained in brief.

6.3.1 Sinusoidal PWM pulses generated

The sinusoidal pulse width modulation (SPWM) pulses generated is discussed in chapter-5. The SPWM signals in 180-degree conduction mode is measured using the Tektronix-digital storage oscilloscope (DSO), is shown in Fig. 6.8

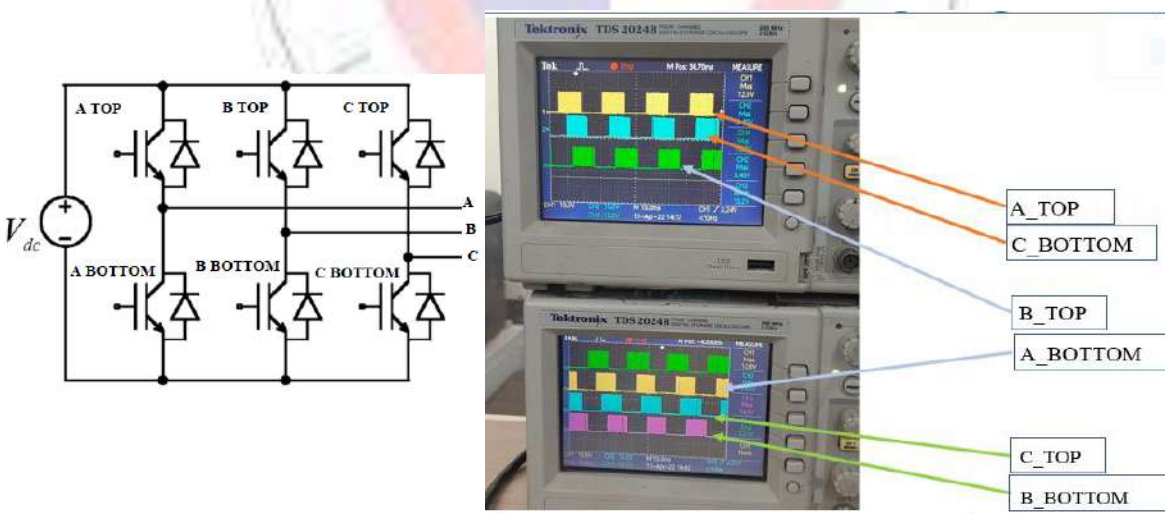


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Fig.6.8. Sinusoidal PWM pulse for inverter at 180-degree conduction mode

The 180-degree conduction mode SPWM signals generated from the developed FOC algorithm is obtained at the DIO pins – 0 to 5 of NI-9401 ultra-high speed digital output FPGA module.

6.3.2. Line Voltages measured across the phases of DUT-PMSM Motor

The Sinusoidal PWM signals generated from the NI-9401 FPGA module is amplified from 5V to 12 V using the level shifter IC – CD40109BE. The line Voltages are measured across RY, YB and BR phases of motor using the differential probe on no-load condition is shown in Fig 6.9.

Fig.6.9. Line Voltages across RY, YB and BR terminals of the DUT motor on no-load

Table-6.1 shows the measured values of the line voltages of DUT-PMSM motor in no-load condition

Table-6.1 Measured values of line voltages across RY, YB and BR phases of DUT motor

.

Phase	V_{max}[V]	V_{min} [V]	V_{rms} [V]	V_{pk-pk} [V]
R-Y	49.6	-51.2	25.3	101
Y-B	52.2	-49.5	25.4	102
B-R	49.5	-52.0	25.2	101

The line voltages measured across the terminals of the DUT motor is balanced with line rms voltage of 25.3 V associated with error of +/-1V. The peak line voltage is observed to be 101V.

6.3.3 Phase Voltages measured across DUT motor terminals:

The phase voltage across each phase of the motor terminals is measured with respect to the dedicated neutral wire in the PMSM test motor considered. Fig.6.10 shows the phase voltages measured across the terminals of DUT motor on no-load condition.

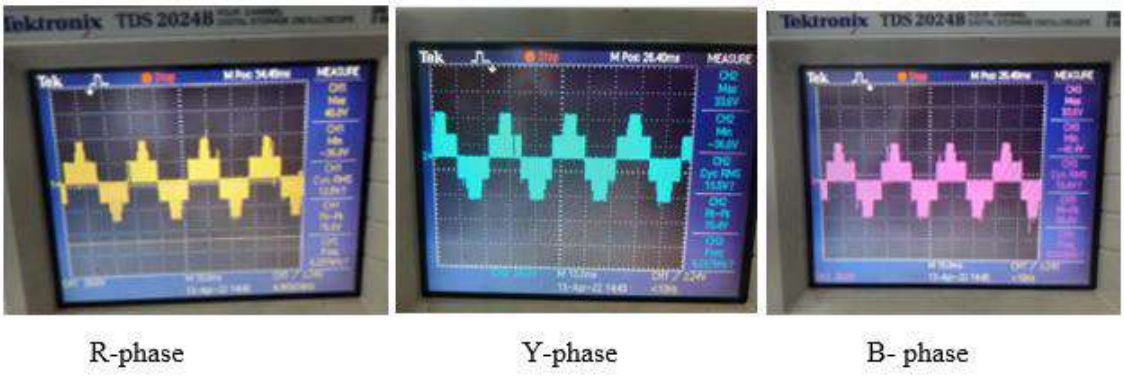

Fig.6.10- Phase voltage measured at each phase of the PMSM-DUT motor

Table-6.2 shows the measured phase voltages across each phase and dedicated neutral wire of the DUT motor

Table-6.2 Phase voltages measured across each phase terminals of the DUT motor

Phase	V_{max}[V]	V_{min} [V]	V_{rms} [V]	V_{pk-pk} [V]	Frequency [kHz]
R	33.3	-36	12	70	6.26
Y	33.6	-36.8	11.5	70.4	6.28
B	33.6	-36.4	13.4	70	6.3

The phase voltage measured across the terminals of each phase and neutral. The rms voltage measured at each phase is 11.5 V with associated error of +/-1V. The peak voltage at each phase is observed to be 70V with switching frequency of PWM pulses at 6.3kHz.

6.3.4 Phase Currents measured at each Phase of the DUT Motor

The phase currents at each phase is measured using the current clamp meter. The phase currents measured at each phase is equal and currents are balanced. Fig. 6.11 shows the phase currents measured at each phase of the DUT motor.

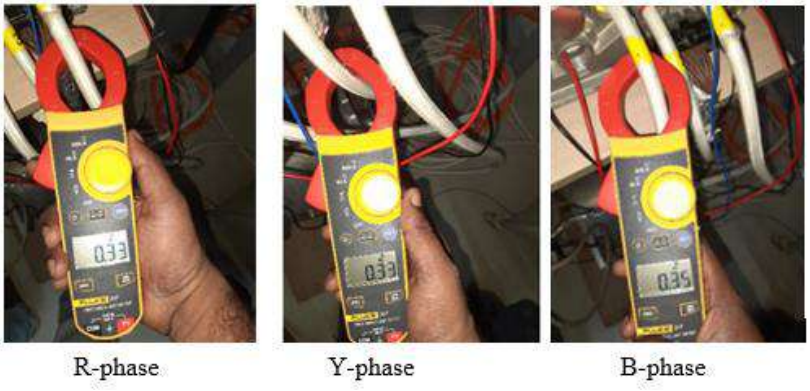

Fig.6.11 – Phase currents measured at each phase of DUT motor

The phase currents measured at each phase is observed to be almost equal. The phase currents at R – Phase is 33A, Y – Phase is 35A and B – Phase is 33A.

6.4 Testing of PMSM motor on EV Dyno Test Bench

The PMSM test motor – device under test (DUT), is mounted on a 350kW dyno test bench. The real time loads acting on the motor shaft installed in the electric vehicle is emulated in the dyno test bench to analyse the performance and verify the ratings of the test motor and also the hardware in loop (HIL) testing is performed on the developed FOC motor controller in LabVIEW to determine the capacity of the developed software to run the motor at various speed driving the loads acting on the motor.

The test motor is subjected to various load circumstances emulating real-time loads on motor shaft during the motor operations in forward motoring, forward braking, reverse motoring, and reverse breaking operations by applying varying loads on the DUT motor by dyno motor. Typical test procedures to determine the maximum torque driven by the test motor and the maximum speed achieved by the test motor at nominal load is discussed in chapter 2.

The FOC motor controller in LabVIEW drives the test motor. The K_p and K_i values of the test motor is determined using the motor parameters and using the equations 6.1 and 6.2.

$$K_P = L_s \omega_0 \tag{6.1}$$

$$K_i = \frac{R}{L_S} \times T_i \quad , \quad T_i = \frac{\omega_0}{2\pi} \times L_S$$

$$K_i = \frac{R\omega_0}{2\pi} \tag{6.2}$$

Where:

L_s is the Line inductance between RY phases
R is the Line resistance between RY phases
ω_0 is the current bandwidth

The inductance and resistance measurements of the test motor is determined using the LCR meter. Table-6.3 represents the inductance and resistance measured across the terminals of the test motor.

Table-6.3 Inductance and Resistance measured across terminal of PMSM motor

	R-Y	Y-B	B-R
Inductance (max) [uH]	182.316	183.642	191.985
Inductance (min) [uH]	95.588	92.584	98.7808
Resistance m.ohms	10.44	10.6	9.6

The average inductance of L_{avg} = 185.981uH , average resistance of R_{avg} = 10.2133 ohms and the current bandwidth $\omega_0 = 500A$ is considered in calculating the K_p and K_i values.

$$K_p = (185.981*500)*10^{-6}\ ,\ \underline{K_p = 0.0925}$$

$$K_i = \frac{R\omega_0}{2\pi}*10^{-3}, Ki = \frac{10.2133*500}{2\pi}*10^{-3},\ \underline{Ki = 0.0812}$$

The high voltage DC source is set at 120V with current limit set to 60 A. The DUT motor is run on no-load initially at the dyno test bench for 10 minutes at 1000 rpm, to determine the system is error free. The DUT motor is now operated in torque mode driving the load torque from dynamometer motor.

- **Forward Motoring and Forward braking**

The test on DUT motor to determine torque driving capacity of motor in forward motoring and forward braking is performed for set speed and set load torque. Table-6.4 represents the variation of speed for load conditions on DUT motor in forward motoring and forward braking.

Table-6.4 Variation of speed for load conditions on DUT motor.

Set Speed [rpm]	Iq ref [A]	R- Phase Current [A]	Actual Speed [rpm]	Load [Nm]
800	50	40-50	830	10
2000	60	50-60	2050	12
2000	70	60-70	1900	14
2000	75	60-75	1890	18
2000	80	70-80	1850	22

- **Reverse Motoring and Reverse braking**

The test on DUT motor to determine torque driving capacity of motor in Reverse motoring and reverse braking is performed for set speed and set load torque. Table-6.5 represents the variation of speed for load conditions on DUT motor in reverse motoring and reverse braking.

Table-6.5 Variation of speed for load conditions on DUT motor in reverse motoring braking

Set Speed [rpm]	Iq ref [A]	R- Phase Current [A]	Actual Speed [rpm]	Load [Nm]
-800	50	40-50	-800	10
-2000	60	50-60	-1950	12
-2000	70	60-70	-1900	14
-2000	75	60-75	-1890	18
-2000	80	70-80	-1850	22

The motor controlled using the developed FOC algorithm in LabVIEW is capable of driving the load at set speed. It is observed that the speed of the DUT motor reduces slightly on increasing the load and the controller has significant delay in tuning back the motor to set speed. The tuning of PI controller's gains needs to be set such that the speed of the motor gets stabilized at shortest possible time.

6.5 Summary

The FOC algorithm implemented in LabVIEW was simulated in MATLAB - Simulink, the results of the simulation carried out was explained. The GUI developed in LabVIEW was discussed. The results of the HIL testing for hardware implementation of FOC algorithm in LabVIEW for various load conditions and set speed were explained for all four quadrant operations of the test motor.

Chapter 7

CONCLUSION and FUTURE SCOPE

This chapter discusses about the conclusions made from the work carried out and also discusses about the future scope of the proposed work.

7.1 Conclusion

The speed control of the IPM- PMSM Motor in closed loop is designed, simulated and implemented using the Field Oriented Control algorithm in torque mode and field weakening mode using the National Instruments – LabVIEW, cRIO-9046 and FPGA modules NI-9223 and NI 9401 for the EV dyno test bench. The conventional motor control methods like six-step commutation control and hysteresis current control, though are very effective in controlling the motor but suffer from issues like torque ripples at low speed, problem of continuous PWM signal generation during steady-state operation to drive the motor. Field-oriented control (FOC) provides faster precise control with less torque ripple and faster torque response. The existing motor controller is not capable to operate the motor in wide ranges of speed. To test the DUT motors at higher speed up to 25000 rpm in a dyno test bench, the operational range of the existing DUT motor controller needs to be increased and is expensive. The proposed FOC algorithm developed in LabVIEW was designed to run the motor up to 25000 rpm, it is less expensive than the equivalent range commercial motor controllers.

- The developed program in LabVIEW software offered robust control of the PMSM motor in torque mode and field weakening mode processing at 47us thereby operating in real-time.
- The DUT motor reached the set speed under no-load condition in 3 seconds. The motor reached the set speed of 800 rpm in 6 seconds driving the load torque of 10Nm.
- The GUI developed provided the access to set the speed of the motor driving the load torque and the real-time waveforms were displayed.
- The error associated with the actual speed measured to the set speed was less than 5%.
- The error associated with the set reference current and measured current was observed to be less than +/-10%.
- The developed module provided the control of DUT motor in all four quadrant

operations and performance analysis was conducted on 350kW Dyno test bench.

7.2 Future Works & Scope

- The PI controllers used in the developed program is parallel PI controller, though it operates in real time and responds fast yet it consists overshoots of 5% and has observable settling time of 6 seconds. For higher speed and precise control, the series PI controller could be designed and considered.
- The FOC algorithm could be developed using the FUZZY LOGIC library in LabVIEW to obtain higher accurate and precise control on speed and torque.
- The automation of the electric drives and test bench could be possible by introducing the Artificial Neural Network based controllers in the FOC algorithm and Dyno test bench by using supervised learning method.

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APPENDIX A
MATLAB- MOTOR PARAMETERS

The Parameters of PMSM Motor model considered for simulation is written in MATLAB

```
%% PWM Switching frequency
PWM_frequency       = 12e3;
T_pwm           = 1/PWM_frequency;

%% Sampling Tim
Ts            = T_pwm;
Ts_simulink     = T_pwm/12;
Ts_motor        = T_pwm/12;
Ts_inverter     = T_pwm/12;
Ts_speed        = 10*Ts;

%% Data Type
dataType = 'single';

%% Motor Parameters
pmsm.model  = 'Teknic-2310P';   % Motor
pmsm.p      = 4;                % Pole Pairs
pmsm.Rs     = 2e-03;             % Stator Resistance (ohms)
pmsm.Ld     = 30e-6;           % D-axis inductance (H)
pmsm.Lq     = 50e-6;           % Q-axis inductance (H)
pmsm.J      = 10.061551833333e-4;% Inertia (Kg-m2)
pmsm.B      = 2.636875217824e-6;% Kg-m2/s
pmsm.Ke     = 0.021             % Bemf Const
pmsm.Kt     = 0.274;            % Nm/A
pmsm.I_rated= 900;              % Max Current Is (A)
pmsm.N_max  = 6000;             % Max Speed (RPM)
pmsm.FluxPM     = (pmsm.Ke)/(sqrt(3)*2*pi*1000*pmsm.p/60); % (Wb)
pmsm.T_rated    = (3/2)*pmsm.p*pmsm.FluxPM*pmsm.I_rated; % Max Torque (Nm)

%% Inverter Parameters

inverter.V_dc           = 58; % (V)
inverter.Rds_on         = 2e-3;     % (Ohms)
inverter.Rshunt         = 1e-6;   % (Ohms)

%% ControllerGains PI

% Reference:
https://e2e.ti.com/blogs_/b/industrial_strength/archive/2015/07/20/teaching-
your-pi-controller-to-behave-part-i
BW_hz = 3200; % in Hz
Kp_id = 2*pi*BW_hz*pmsm.Ld;
Ki_id = 2*pi*BW_hz*pmsm.Rs*Ts;
Kp_iq = 2*pi*BW_hz*pmsm.Lq;
Ki_iq = 2*pi*BW_hz*pmsm.Rs*Ts;
% BW_hz = 3200; % in Hz
% Kp_id = (2*pi*(PWM_frequency/20)*pmsm.Ld);
% Ki_id = (pmsm.Rs/pmsm.Ld)*Ts;
% Kp_iq = (2*pi*(PWM_frequency/20)*pmsm.Lq);
% Ki_iq = (pmsm.Rs/pmsm.Ld)*Ts;
 Kp_spd = 0.9211;
 Ki_spd = 0.0001;
```

Design and Implementation of FOC and GUI for EV Test Bench in LabVIEW

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M.Tech in Power Electronics, Department of Electrical and Electronics Engineering

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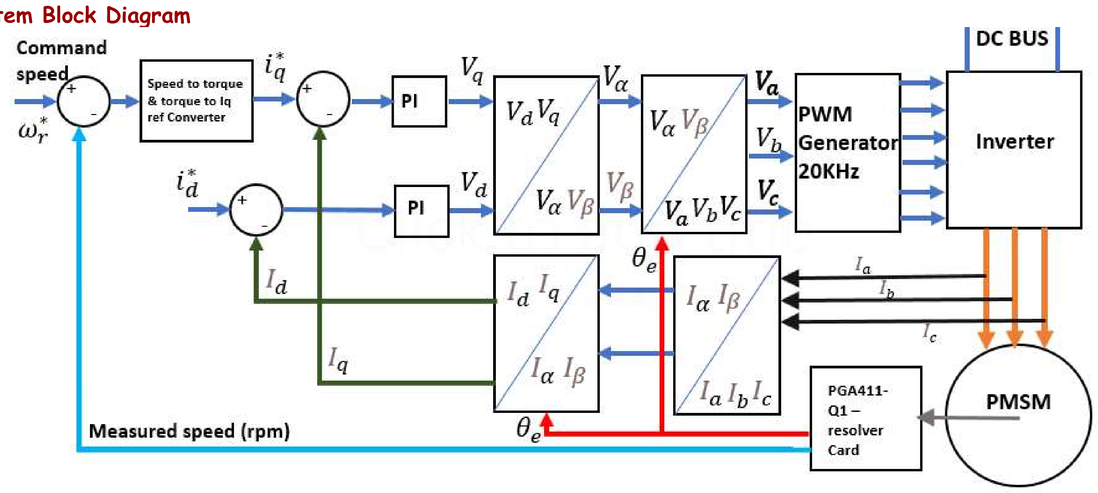
OBJECTIVE

- Develop the FOC algorithm using LabVIEW software to run the Device Under Test (DUT) Motor.
- Design the GUI to set DUT motor controls to operate in all 4 quadrants and data log.
- Validating the DUT motor speed, torque and efficiency on no-load and on-load conditions.

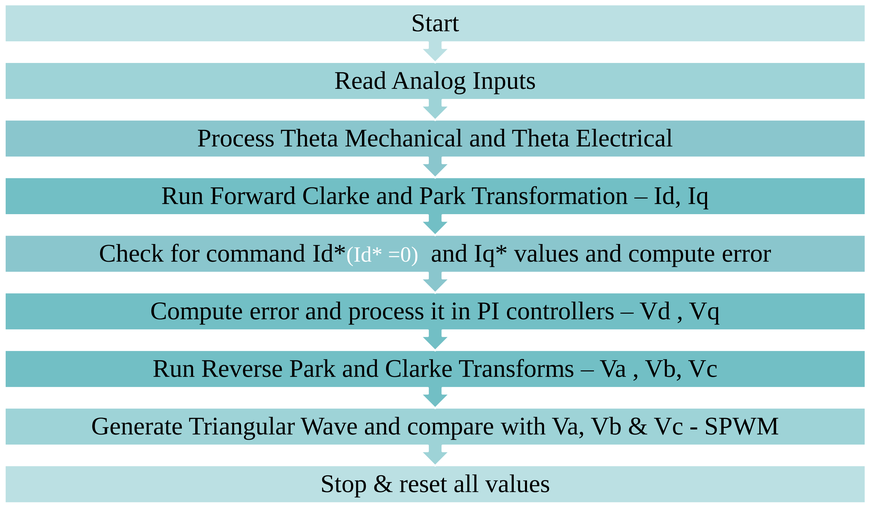
Project Methodology

The EV motor before being installed in the vehicle is to be analysed and calibrated by emulating the real time load conditions in a dyno test bench. The motor is required to operate in an error free control system for the performance analysis. The Field Oriented Control (FOC) algorithm suits the required motor control criteria to operate the motor with direct torque control and flux weakening control. In FOC the 3 phase time varying signals are transformed to 2 phase time invariant orthogonal vectors, which are modulated to achieve desired control. The modulated 2 phase time invariant signal are transformed back to 3 phase time varying control signals, which are sampled with high frequency carrier signals to generate PWM signals. The generated PWM signals drives the inverter to operate the DUT motor.

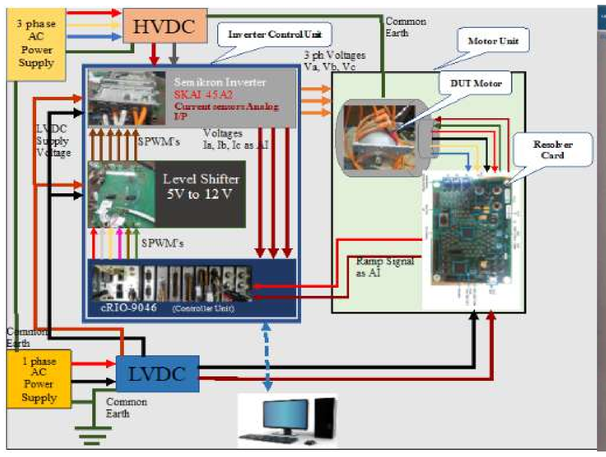
System Block Diagram



Code Flow



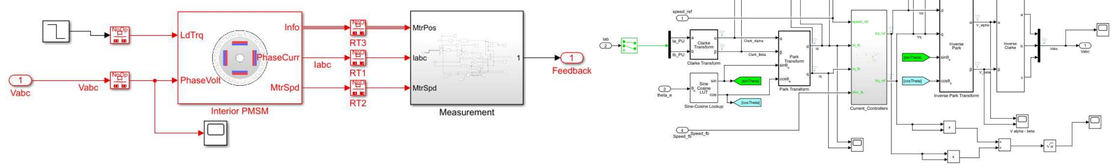
Hardware design Flow & GUI



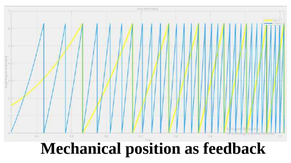
FOC – Hardware Module

FOC – GUI in LabVIEW

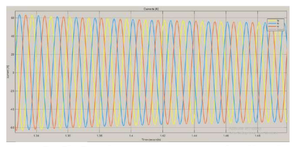
Simulation : The FOC algorithm is simulated using MATLAB



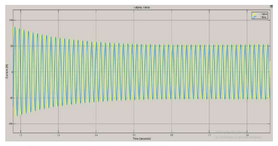
Results and Discussions : The Waveform observed in MATLAB – Forward & Reverse Transforms



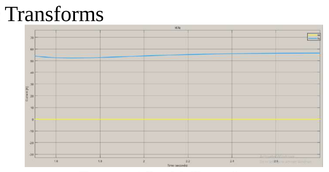
Mechanical position as feedback



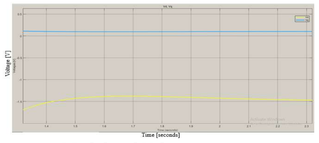
Ia Ib Ic phase currents as feedback



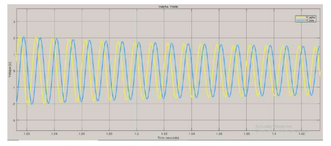
Forward Clarke's Transform



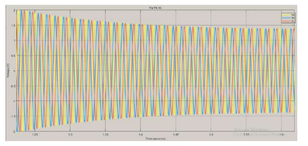
Forward Park'sTransform



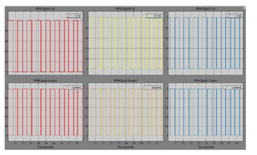
Modulated Voltage vectors



Reverse Park Transform

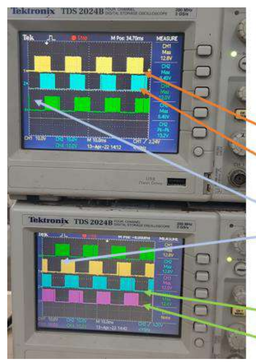


Reverse Clarke's Transform

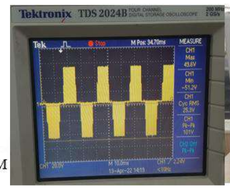


Sinusoidal PWM signals

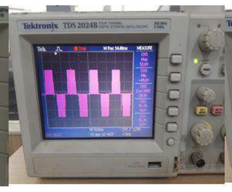
- The PWM signals, Line & Phase Voltages measured across inverter terminals on no –load condition



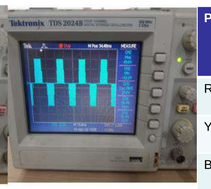
PWM Signals in hardware



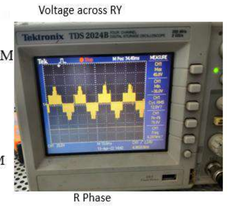
Voltage across RY



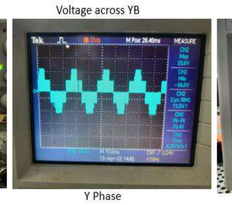
Voltage across YB



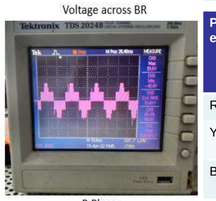
Voltage across BR



R Phase



Y Phase



B Phase

Phase	V max [V]	V min [V]	V rms [V]	V pk-pk [V]
R-Y	49.6	-51.2	25.3	101
Y-B	52.2	-49.5	25.4	102
B-R	49.5	-52.0	25.2	101

Phase	V max [V]	V min [V]	V rms [V]	V Peak [V]	Frequency [kHZ]
R	33.3	-36	12	70	6.26
Y	33.6	-36.8	11.5	70.4	6.28
B	33.6	-36.4	13.4	70	6.3

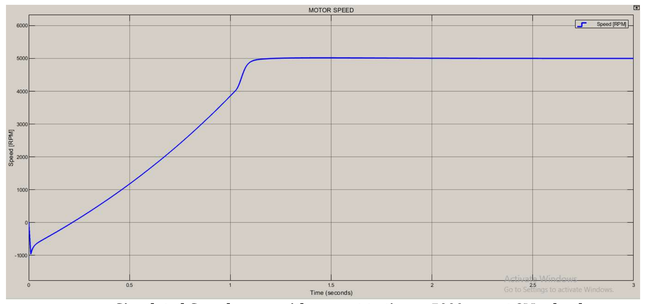
- The Motor is loaded on 350kW Dyne system at 120V DC supplied to inverter and operated with load.

Iq ref [A]	Phase Current [A]	Speed [RPM]	Load [Nm]
50	40-50	830	10
60	50-60	2050	10
70	50-60	1900	12
70	60-75	1930	14
75	60-75	1350	16
75	60-75	1250	18
80	70-85	1850	18
80	70-85	1890	22

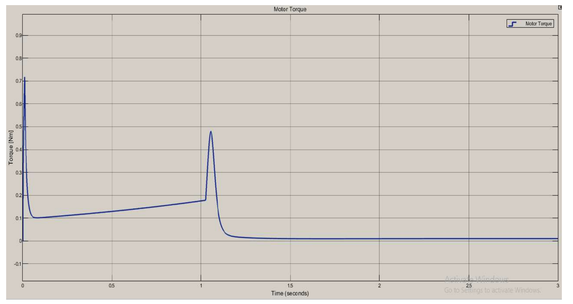
DUT Motor operated in Forward direction

Iq ref [A]	Phase Current [A]	Speed [RPM]	Load [Nm]
-50	40	800	-10
-50	40 - 50	800	-10
-60	50-65	1850	-12
-70	60-75	1950	-14
-75	60-75	1300	-16
-80	70-85	1850	-18

DUT Motor operated in Reverse direction



Simulated Speed curve with respect to time – 5000rpm at 8Nm load



Simulated Torque curve with respect to time – 5000rpm at 8Nm load

Conclusion

- The developed program in LabVIEW software offers robust control of the DUT - PMSM motor in torque mode.
- The DUT motor reaches the set speed on no-load condition in 3 seconds and on-load condition at 10Nm, the motor reaches the set speed of 800rpm in 6 seconds.
- The DUT motor drives the load at set speed with variation in phase currents compared with the set reference current of corresponding speed. The error in set reference current and measured current is observed to be less than +/-10%.
- The developed module operates the DUT motor in all 4 quadrants and performance analysis is conducted on Dyne test bench.

Future scope.

- The FOC algorithm could be developed using the FUZZY LOGIC library in LabVIEW to obtain higher accurate and precise control on speed and torque.
- The automation of the electric drives and test bench could be possible by introducing the Artificial Neural Network based controllers in the FOC algorithm and Dyne test bench.

Acknowledgement

- **I deeply express my sincere gratitude to my guide Dr. M N Dinesh, Professor, Dept of EEE, RVCE, Dr. Rudranna N, HOD, Dept of EEE, RVCE, Principal & Panel Members, RVCE for the guidance & opportunity provided.**
- **I thank External guides from L&T Technology Services, Bangalore for their valuable guidance throughout this project.**

Guide Information: Dr. M N Dinesh, Professor, Dept of EEE, RVCE, e-mail: dineshmn@rvce.edu.in

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Design and Implementation of FOC and GUI for EV Test Bench in LabVIEW

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[1]Department of Electrical and Electronics,

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Abstract : The rising popularity and demand for electric vehicles have been increasing rapidly in recent years. The EV motor before being installed in the vehicle is to be analyzed and calibrated by emulating the real-time load conditions in a dyno test bench. The EV motor being tested – Device Under Test (DUT) is required to operate in an error-free control system for the performance analysis. The Field Oriented Control (FOC) algorithm suits the required motor control criteria to operate the motor with direct torque control and field weakening control. The FOC algorithm is developed in LabVIEW using cRIO9046, FPGA modules NI9223(Analog input module – 1MS/s) and NI9401(Digital IO – 10MHz) to process at 47us operating in real-time. The PMSM motor is considered a DUT motor, the control of the DUT motor is achieved in torque mode to test DUT in all 4-quadrant operations of the motor. The GUI developed allows the user to set the speed, and display all waveforms. Speed to the equivalent Iq reference value is obtained through a look-up table and the motor operates in direct torque control (DTC) mode up to the base speed of the motor. The Id reference control using the lookup table provides speed control up to the peak speed of the motor with reduced torque on on-load conditions. The DUT motor tested is an 8-pole PMSM motor with peak power of 60kW and peak speed of 4000rpm. The FOC control system in LabVIEW offers robust control of the motor by operating the motor in all 4 quadrant operations, the motor achieves the set speed from standstill in 3 seconds on the no-load condition and achieves the set speed in 6 seconds on the on-load condition at 1000rpm, 10Nm.

IndexTerms **- LabVIEW, Field Oriented Control, Permanent Magnet Synchronous Motor, Device Under Test.**

I. INTRODUCTION

EV motors need to be analyzed and calibrated before being installed in a vehicle by emulating the real-time load conditions in a dyne test bench. The loading capacity of the vehicle, maximum driving speed, acceleration, deceleration rate, maximum power, torque on wheels etc. can be analyzed based on the load driving capacity of the motor. The EV motor being tested – Device Under Test (DUT) is required to operate in an error-free control system for the performance analysis. Compared to the six-step commutation control and hysteresis current control the field- oriented control (FOC) delivers fast acceleration and deceleration of motor giving more accurate and better speed control with less torque ripple and fast torque response. The Field Oriented Control (FOC) algorithm suits the required motor control criteria to operate the motor with direct torque control and field weakening control.

The FOC algorithm is developed in LabVIEW – the real time graphical software tool, to run the DUT motor in all 4 quadrant operations – forward motoring, forward braking, reverse motoring and reverse braking. The reverse re-generative braking with damping load may be considered in EV test bench. The National Instruments' cRIO-9046, real time module is considered for the interface of the FPGA modules NI9223 – analog input module as analog to digital converter (ADC) to read physical feedback signals and NI9401 – digital input-output module to generate pulse width modulation (PWM) signals on processing the FOC algorithm.

The conventional drive system uses the three types of motors that have become popular in electric drive applications- PMSM motor, brushless DC motor and three - phase induction motor [1]. The PMSM motor is considered for user end application and testing – Device Under Test (DUT) as it is more reliable, less noisy, has higher efficiency, delivers high torque and offers better `performance in both low and high-speed operations than other motors.

The FOC algorithm developed in LabVIEW processes each iteration in 47us to operate the DUT motor in real-time with less torque ripple and fast torque response. The DUT motor is mounted on a 350kW dyne test-bench and operated in torque mode to drive the DUT -PMSM motor at various load conditions up to rated speed of 2500rpm with load torque of 22Nm.

II. EV DYNE TEST BENCH AND FIELD ORIENTED CONTROL

2.1 EV DYNE TEST BENCH

The EV dyne motor test bench is a platform which evaluates the measure of torque and rotational speed, giving a reading that indicates the power of the motor. In dyne load test the DUT motor is initially operated at the no-load condition at its peak power assuring safe operating conditions. The DUT motor is now loaded lightly by the dyne motor, gradually loading the DUT motor to its full load operating capacity. The dyne motor is operating below the rated speed of DUT motor to avoid stalling

. The speed of the DUT motor is set at a fixed value and the load is applied to a known value and the variation in speed and load torque experienced is recorded. These recorded data is now used to analyse the maximum operable speed, torque and power of the motor. The load conditions equivalent to the load experienced by EV motor in an electric vehicle on road and the 4 quadrant operations – forward motoring, forward braking, reverse motoring and reverse braking of motor loading is tested. The performance and efficiency of the DUT motor is now evaluated and the benchmarking is done for the electric vehicle's maximum rated speed, torque and power.

2.2 FIELD ORIENTED CONTROL

The Field Oriented Control is a vector control method in which the three phase stator currents – I_a, I_b and I_c of the DUT motor are transformed as equivalent two-phase orthogonal components that can be visualized as constant vectors I_d and I_q. The d-q current components are modulated according to the set speed in the PI controllers. The modulated output from the PI controllers is the equivalent voltage components V_d and V_q. These d-q voltage components are transformed to equivalent 3 phase voltages V_a,V_b and V_c. These 3 phase voltage components are compared with high frequency triangle wave of 5kHz to obtain the sinusoidal pulse width modulation (SPWM) signals. The summary of the FOC algorithm is shown in fig.1 – Summary of FOC.

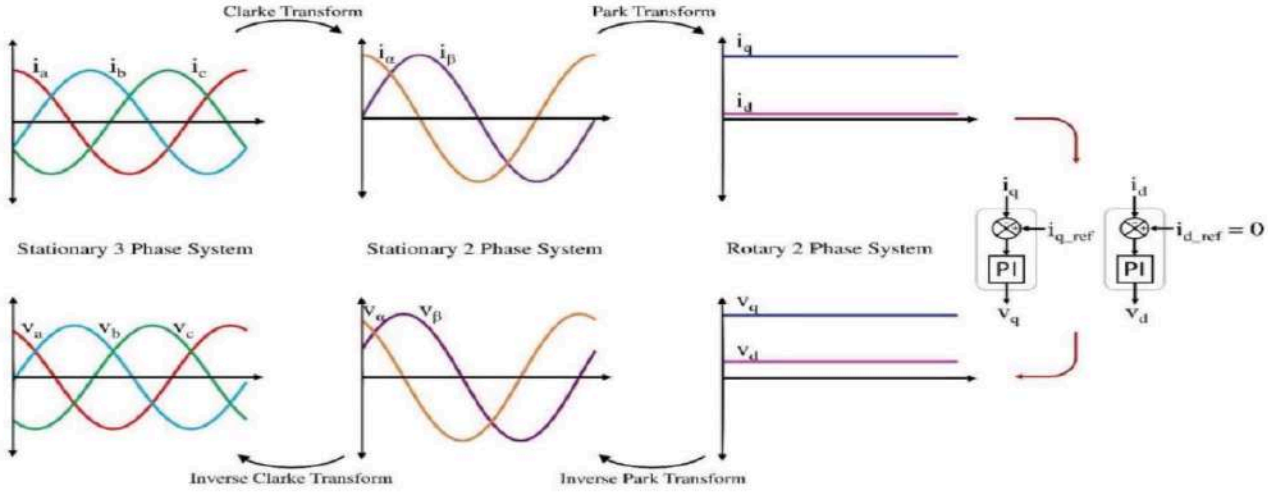

Fig-1: Summary of Field Oriented Control (FOC) algorithm

III. FUNCTIONAL BLOCK DIAGRAM AND METHODOLOGY

3.1 FUNCTIONAL BLOCK DIAGRAM

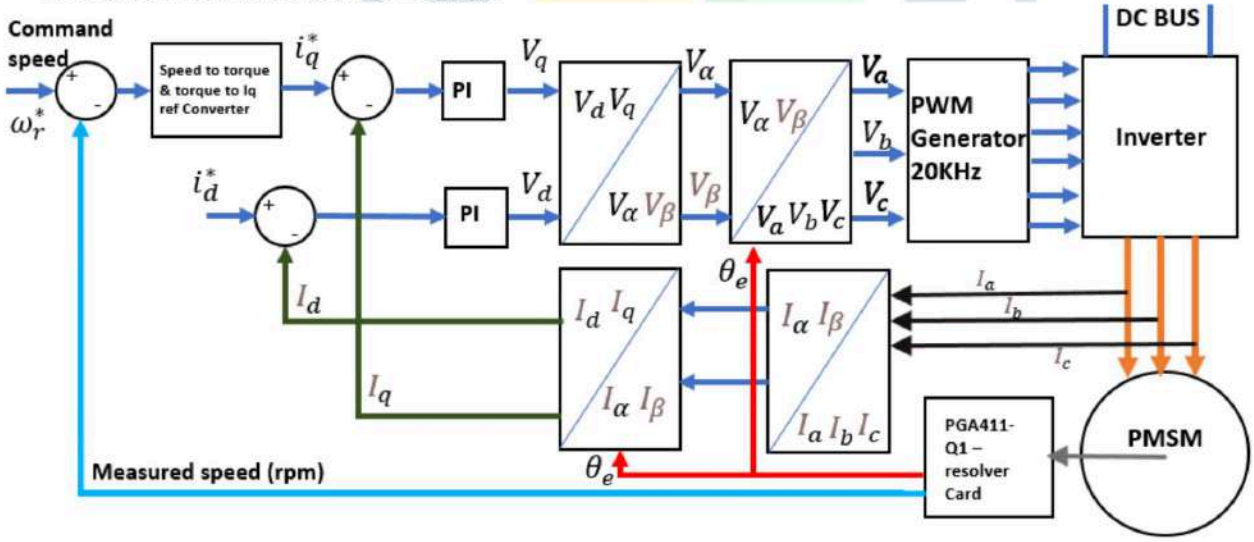

Fig 2. Functional Block Diagram of FOC algorithm

The position data of the rotor shaft of DUT motor is encoded using a position encoder. The position of the rotor shaft is decoded as the equivalent angular displacement (θ_r). The three phase currents I_a, I_b and I_c are considered as feedback inputs along with the position data. The three-phase time varying current components are transformed into equivalent two-phase time varying currents I_α and I_β in forward Clarke's transform using equations 3.1 and 3.2.

$$I_\alpha = \frac{2}{3}(Ia) - \frac{1}{3}(I_b + I_c) \quad \text{.....(3.1)}$$

$$I_\beta = \frac{1}{\sqrt{3}}(I_b - I_c) \quad \text{.....(3.2)}$$

The two-phase equivalent time varying current components are transformed into two-time invariant orthogonal vectors I_d and I_q in forward Park's transform using equations 3.3 and 3.4.

$$I_d = I_\alpha \cos(\theta_r) + I_\beta \sin(\theta_r) \quad (3.3)$$

$$I_q = I_\beta \cos(\theta_r) - I_\alpha \sin(\theta_r) \quad (3.4)$$

The I_d and I_q currents signify the direct axis and quadrature axis current components of the permanent magnet motors. The direct axis component provides control of the air gap flux and the quadrature axis component provides the torque control of DUT motor. The DUT motor can be operated in torque mode by modulating the I_q component by varying I_q reference value. The DUT motor can be operated beyond the rated speed by modulating the I_d component by I_d reference value in flux weakening control.

The modulation of I_d and I_q components is done in PI controllers to obtain the voltage equivalent d-q components – V_d and V_q. The time invariant V_d and V_q vectors are transformed into two phase time varying voltage components V_α and V_β in inverse Park's transform using equations 3.5 and 3.6.

$$V_\alpha = V_q \cos(\theta_r) - V_d \sin(\theta_r) \quad (3.5)$$

$$V_\beta = V_d \sin(\theta_r) + V_q \sin(\theta_r) \quad (3.6)$$

The two-phase time varying voltage components are transformed to equivalent three-phase time varying components Va, V_b and V_c in inverse Clarke's transform using equations 3.7, 3.8 and 3.9.

$$V_a = V_\alpha \quad (3.7)$$

$$V_b = -\frac{1}{2}(V_\alpha) + \frac{\sqrt{3}}{2}(V_\beta) \quad (3.8)$$

$$V_C = -\frac{1}{2}(V_\alpha) - \frac{\sqrt{3}}{2}(V_\beta) \quad (3.9)$$

The three – phase voltages Va, V_b and V_c are compared with the high frequency triangle waves to generate the sinusoidal pulse width modulation (SPWM) signals in 180° conduction mode. The motor is operated through the inverter module using the generated SPWM signals.

3.2 METHODOLOGY

Fig.3 shows the flow diagram of the proposed methodology of the FOC algorithm with various modules in LabVIEW.

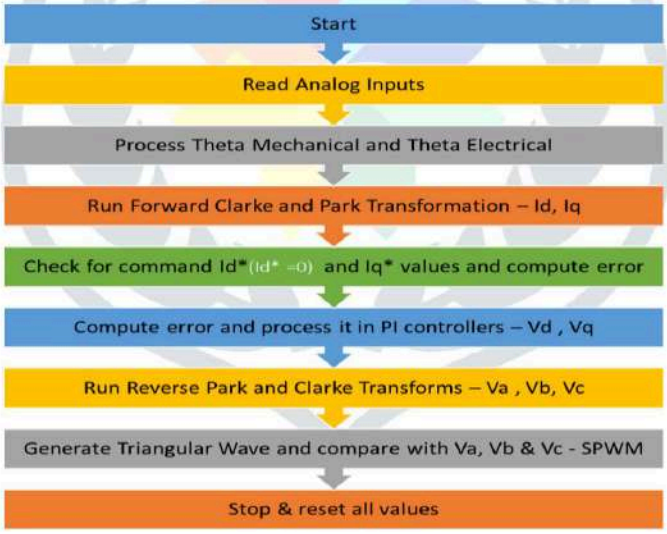

Fig 3. Flow chart of the proposed methodology

The proposed technique requires the per phase current and the actual rotor position and speed data to generate the control signals using the FOC algorithm in LabVIEW.

In Module – 1 (read analog inputs), the position of the rotor is obtained using the resolver mounted to the DUT motor shaft. The resolver data is obtained as continuous sine and cosine signals. These continuous sine and cosine signals are processed as an up-ramp voltage varying from 0.4V to 4.5V in the resolver decoder. The phase currents are also obtained as variable voltage signals through current sensors as feedback input to the FOC algorithm. The analog data is passed to FPGA NI 9223. The position signals are normalized to obtain the mechanical angular displacement values. (θ_m).

In Module - 2 (Theta M to Theta E), the theta mechanical values are then normalized to vary from 0 to 2π radians using the equation 3.10. The equivalent electrical angular displacement (θ_e) is obtained by the conversion of theta mechanical to theta electrical using the equation 3.11.

$$\theta_m = \frac{ResVoltage - V_{min}}{V_{max} - V_{min}} \times 2\pi \text{ [rad]} \quad (3.10)$$

$$\theta_e = \frac{P}{2}\theta_m \text{ [rad]} \quad (3.11).$$

Module-3 (Forward Clarke's Transform) The three phase currents I_a, I_b and I_c aretransformed in to two phase equivalent orthogonal currents I_α and I_β. The three - phase stationary reference phasors are transformed to equivalent two phase orthogonal stationary reference currents in forward Clarke transform.

In module-4 (Forward Park's Transform), The two-phase orthogonal stationary reference equivalent currents I_α and I_β are transformed into two phase equivalent orthogonal rotating reference current vectors I_d and I_q. I_d is the direct axis component which is considered at rotor pole's maximum flux interaction with stator poles, the I_d component is also considered as flux controlling component. I_q is in quadrature to I_d at the quadrature axis, the I_q component is considered as the torque controlling component.

In module 5 (PI Controllers), On performing the Clarke and Park transforms, the AC quantities are now considered in Synchronous rotating reference frame eliminating the frequency, thus the I_d and I_q values are equivalent DC components of three phase AC components. The Command Speed reference value is fed to the controller. The error in speed is converted to equivalent torque current command Iq*. The equivalent command torque current 'Iq*' and flux current 'Id*' (Id =0) are computed and fed to the PI controllers.

In module-6 (Inverse Park's Transform), The inverse Park transformation (dq0 to alpha beta 0) transforms the signals (V_q and V_d voltages) in the rotating reference frame to two phase stationary reference frame. The two orthogonal DC components are now considered as two-phase orthogonal AC equivalent components V_α and V_β.

In Module-7 (Inverse Clarke's Transform), The two-phase AC voltages are converted to the three phase voltages V_a, V_b and V_c.

In Module 8, (SPWM Generator), The triangular wave is generated at high frequencies equivalent to the switching frequency of 5kHz. The 3 phase Sine waves V_a, V_b and V_c obtained is normalized and then is sampled using the high frequency triangular wave to generatethe SPWM pulses.

IV. SPECIFICATIONS AND DESIGN DETAILS

The hardware systems considered in the implementation of the FOC algorithm in LabVIEW is as follows.

1. **Selection of Motor**

The motor considered is an 8-pole interior permanent magnet, IPM - PMSM motor with 41 KW – continuous power and 60KW peak power. The base speed of the motor is 2800 rpm and the peak speed is 5000 rpm. The voltage rating of the DUT motor is 150 V, with peak current rating of 450 A.

2. **Selection of Resolver**

The Resolver is also the 8-pole hollow shaft resolver – 2367254-1 is used to match the motor pole pairs.

3. **Selection of Inverter**

The inverter is chosen based on the maximum switching frequency required to operate the motor at the top most speed. The maximum Switching frequency considered is 12 kHz and the minimum optimal switching frequency is 2kHz. The Semikron Inverter SKAI 45 A2 GD12-WDI is considered The DC input voltage = 800V, DC input current = 300A, 12kHz switching frequency IGBT module.

4. **Resolver Decoder**

The resolver's sine and cosine signals are converted to the real time analog voltage signals observed as an up-ramp signal varying from 0.4V to 4.5 V, using Texas Instruments PGA411-Q1 development board.

5. **Selection of Real time interface**

The National Instruments CRIO9046, NI9401 and NI9223 modules are used for real time interface, where CRIO9046 is an FPGA interface cubicle and NI9223 is the high-speed analog input (AI- 1MS/s) FPGA module and NI9401 is the high-speed digital input – output (DIO- 10MHz) FPGA module.

V. SIMULATION ANALYSIS AND DISCUSSION

5.1 MATLAB model of the FOC algorithm

The vector control algorithm – FOC for the direct torque control and the flux weakening control of the DUT motor in torque mode is designed using the mathematical model of PMSM motor and the simulation results are verified with mathematical values obtained.

The Mathematical model of the motor is considered based on the desired torque and speed values to be achieved by the motor using the following equations.

$$\frac{di_d}{dt} = \frac{1}{L_s}\left[V_d - Ri_d + \omega L_s i_q\right] \quad (5.1)$$

$$\frac{di_q}{dt} = \frac{1}{L_s}\left[V_q - Ri_q - \omega L_s i_d - \omega\psi\right] \quad (5.2)$$

$$T_e = 1.5P\left[\lambda i_q + (L_d - L_q) I_d I_q\right] \quad (5.3)$$

$$\frac{d\omega}{dt} = \frac{1}{J} T_e \quad (5.4)$$

The inductance, resistance of the windings of the motor, air gap flux, torque and inertia of the motor are known from the equations. The mathematical model of the PMSM motor is developed as shown in fig 4.

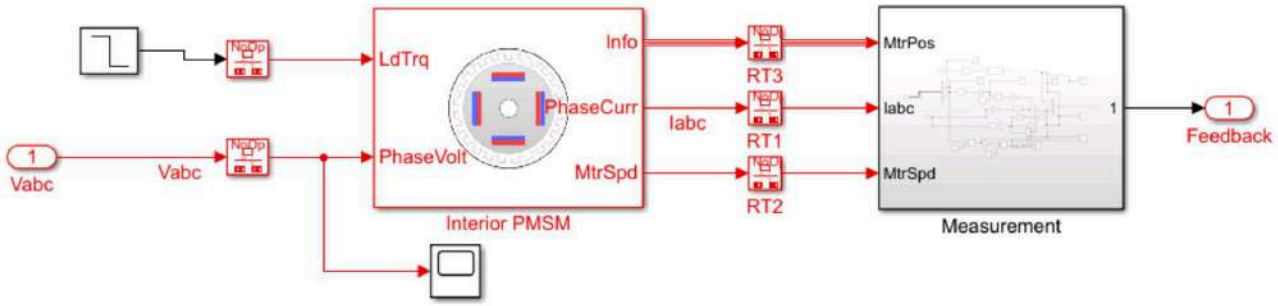

Fig.4 MATLAB model of PMSM DUT motor

The Interior PMSM motor is simulated with a constant light load torque of 8E-3 Nm. The Motor's rotor position and speed is sensed using the resolver to get Theta Mechanical – angular displacement. The Currents from each phase is taken as feedback from motor terminals – Ia, Ib and Ic.

5.2 Mechanical angular displacement to Electrical angular displacement

The rotor position is identified as ramp signals which is obtained by the resolver decoder. The measured rotor position is normalized to vary from 0 to 2π radians using equation 3.10. Each mechanical rotation is considered as one mechanical angular displacement (θ_m) and the equivalent electrical angular displacement (θ_e) using equation 3.11. The electrical equivalent rotation of the mechanical rotation, depends on the number of poles of the motor.

The Block Diagram of Resolver data and computation of θ_m and θ_e values simulated in MATLAB is shown in fig 5.

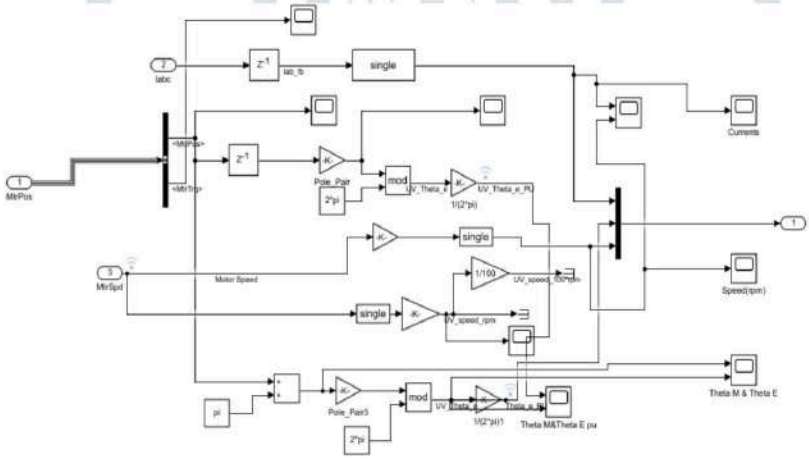

Fig.5. Computing θ_m and θ_e in MATLAB

Fig 6 shows the θ_m and θ_e values plotted in MATLAB

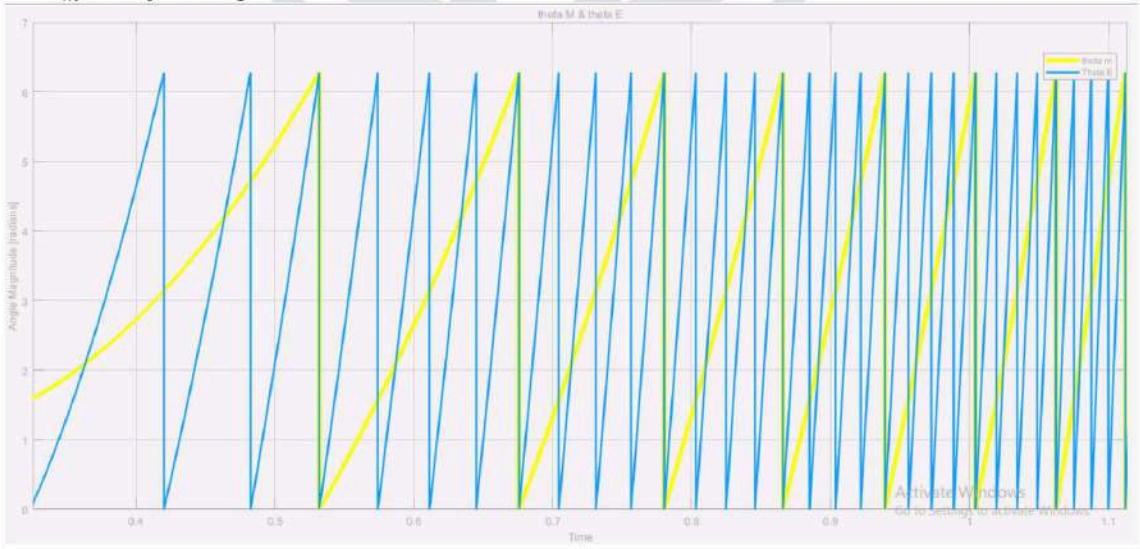

Fig.6. Plotting θ_m and θ_e in MATLAB

The Currents from each phase is considered as the feedback for the forward Clarke's and Park's transformations is shown in fig 7.

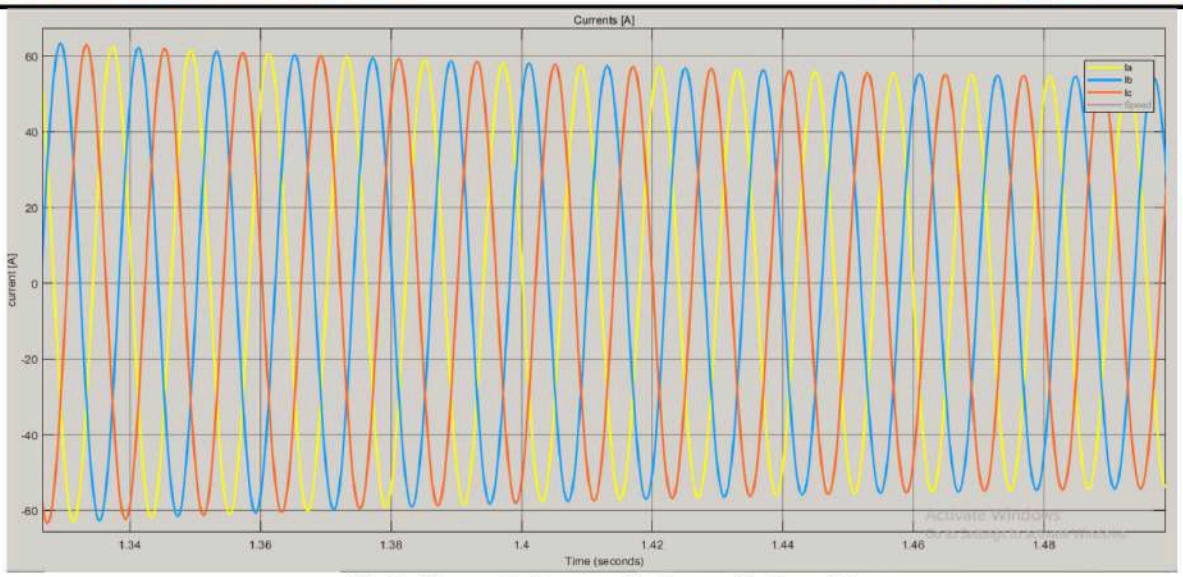

Fig 7. Currents from each phase – I_a, I_b and I_c

The control blocks of the FOC – forward Clarke's transform, forward Park's transform and reverse Park's transform and reverse Clarke's transformations is shown in fig 8.

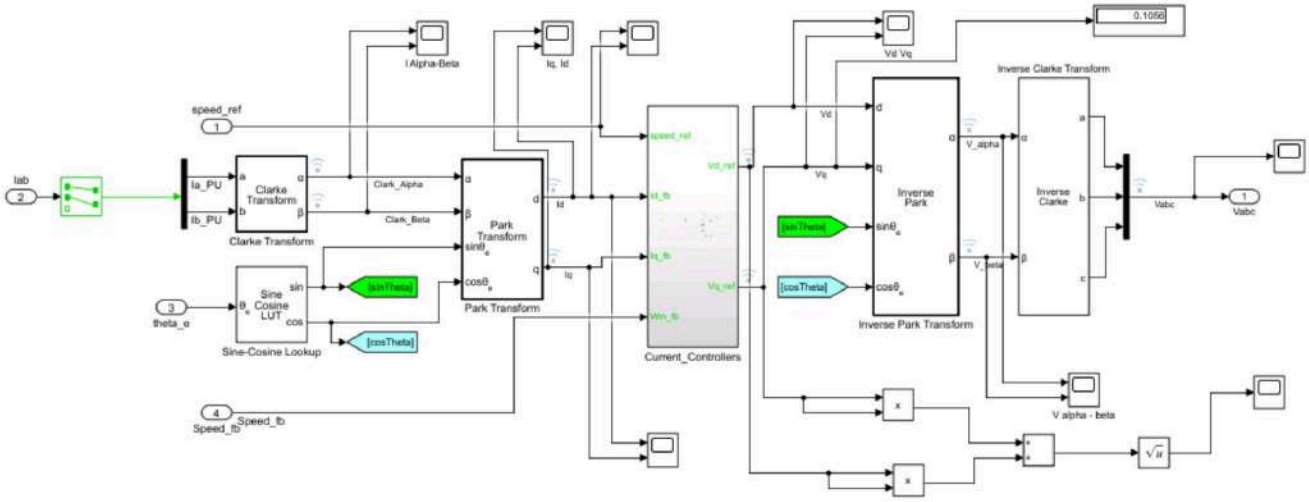

Fig 8 FOC Blocks – forward Clarke's, forward Park's transform and reverse Park's, reverse Clarke's transformations

5.3 Forward Clarke's Transform

The three phase currents I_a, I_b and I_c aretransformed in to two phase equivalent orthogonal currents I_α and I_β. The three - phase stationary reference phasors are transformed to equivalent two phase orthogonal stationary reference currents in forward Clarke transform using equations 3.1 and 3.2. The orthogonal currents I_α and I_β are plotted in MATLAB, shown in fig 9.

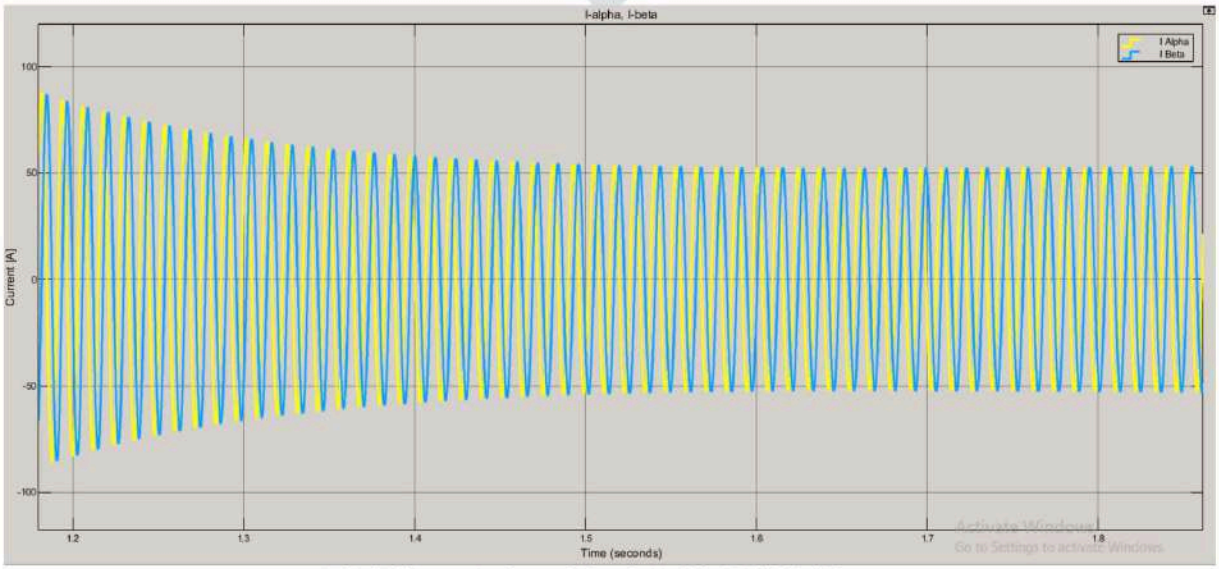

Fig.9 Currents I_α and I_β plotted in MATLAB

5.4 Forward Park Transform

The two-phase orthogonal stationary reference equivalent currents I_α and I_β are transformed into two phase equivalent orthogonal rotating reference current vectors I_d and I_q, using equations 3.3 and 3.4. The two-phase equivalent orthogonal current vectors I_d and I_q is shown in fig.10.

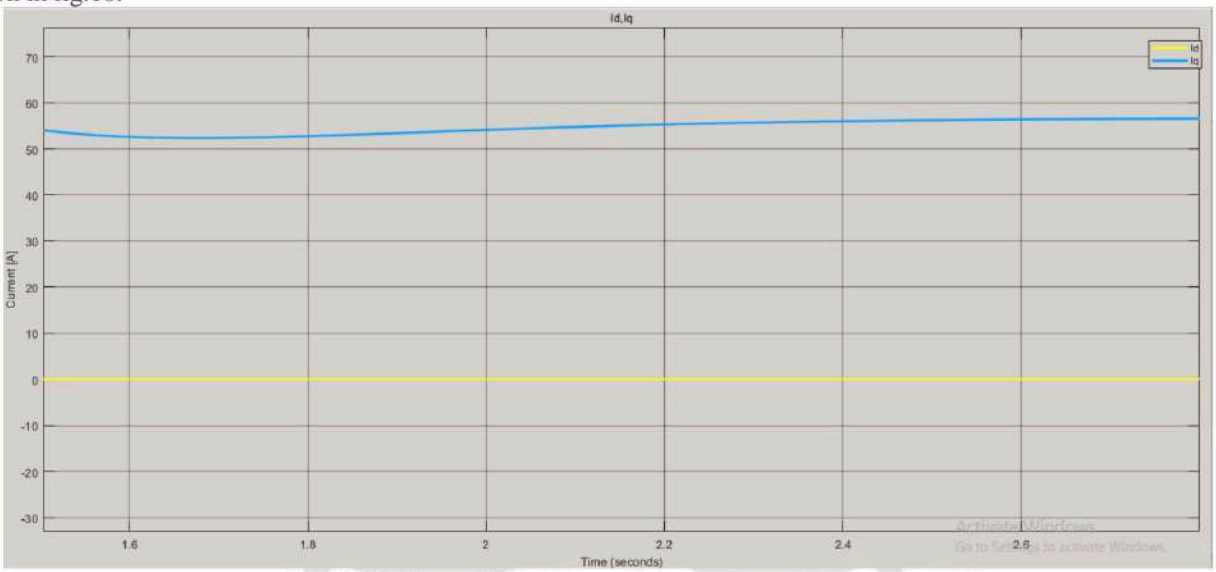

Fig.10 Orthogonal rotating reference current vectors I_d and I_q

5.5 PI Controllers Block

On performing the Clarke and Park transforms, the time varying AC quantities are now considered in Synchronous rotating reference frame eliminating the frequency, thus the I_d and I_q values are equivalent DC components of three phase AC components. The Command Speed reference value is set to the controller. The error in speed is converted to equivalent torque current command Iq*. The equivalent command torque current 'Iq*' and flux current 'Id*' (Id =0) are computed and fed to the PI controllers to obtain the correction modulated voltage d-q components V_d and V_q. The proportional gain - Kp and integral gain - K_i, values for parallel PI controller is computed for the DUT PMSM motors using the following equations 5.1 and 5.2.

$$K_P = L_s \omega_0 \quad \text{.....(5.1)}$$

$$K_i = R\omega_0 \quad \text{.....(5.2)}$$

Where: L_s is the Line inductance between RY phases
R is the Line resistance between RY phases
ω_0 is the current bandwidth

The correction modulated output d-q voltage components, Vd and Vq are plotted in MATLAB as shown in Fig.11.

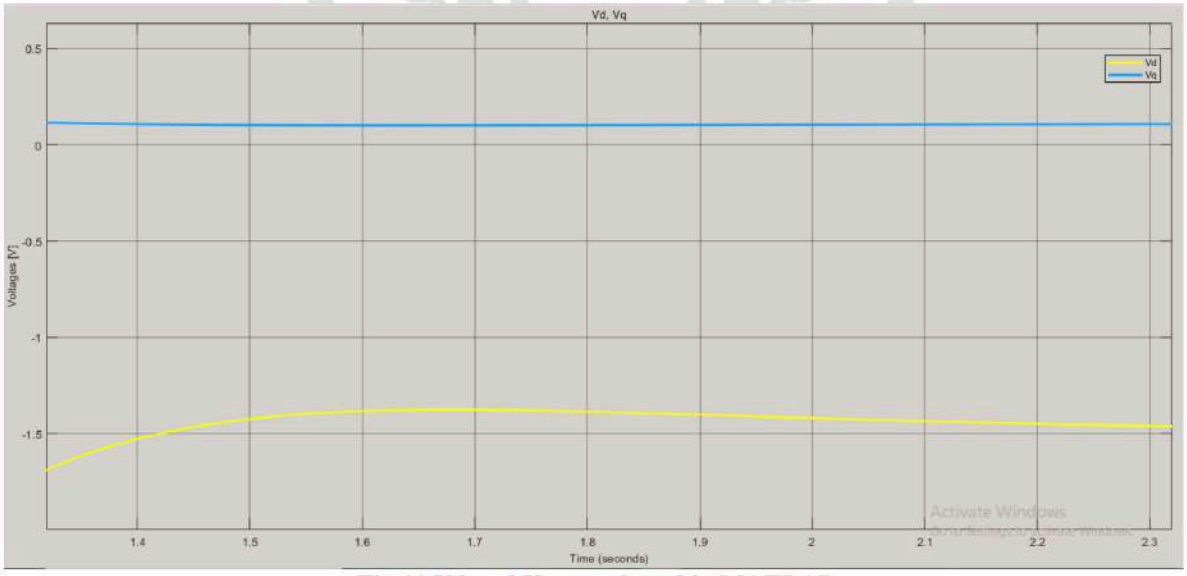

Fig.11 Vd and Vq are plotted in MATLAB

5.6 Inverse Park Transform

The inverse Park transformation (dq0 to alpha beta 0) transforms the signals (V_q and V_d voltages) in the rotating reference frame to two phase stationary reference frame. The two orthogonal DC components are now considered as two-phase orthogonal AC equivalent components V_α and V_β using equations 3.5 and 3.6. Fig.12 shows the plot of V_α and V_β.

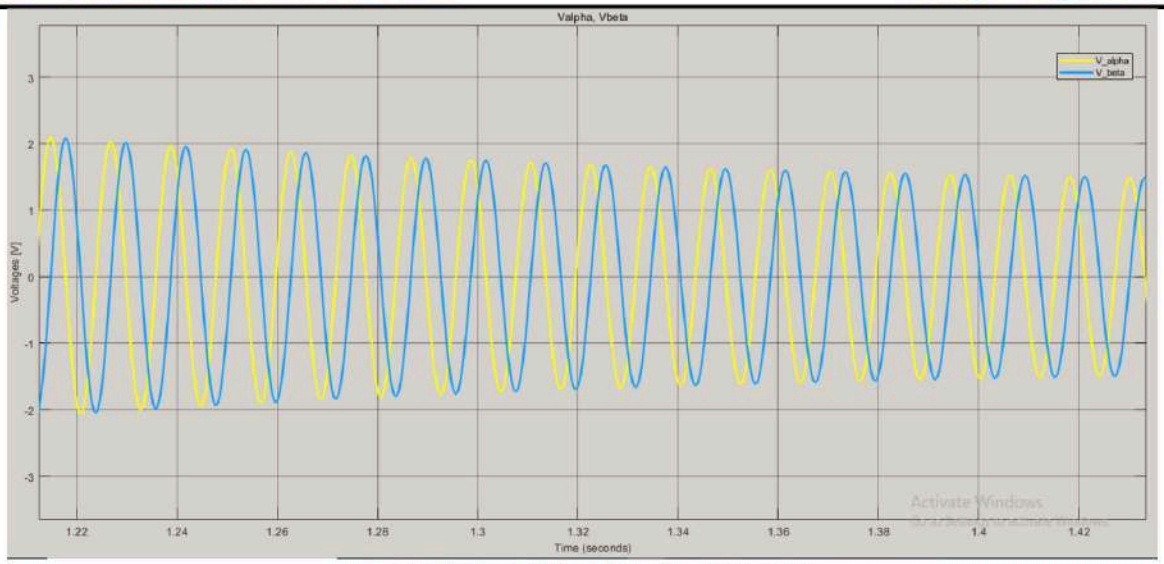

Fig.12 V_α and V_β plotted in MATLAB

5.7 Inverse Clarke's transform

The two-phase AC voltages are converted to the equivalent three phase voltages V_a, V_b and V_c using equations 3.7,3.8 and 3.9. The three phase voltages V_a, V_b and V_c are plotted in MATLAB, shown in Fig.13.

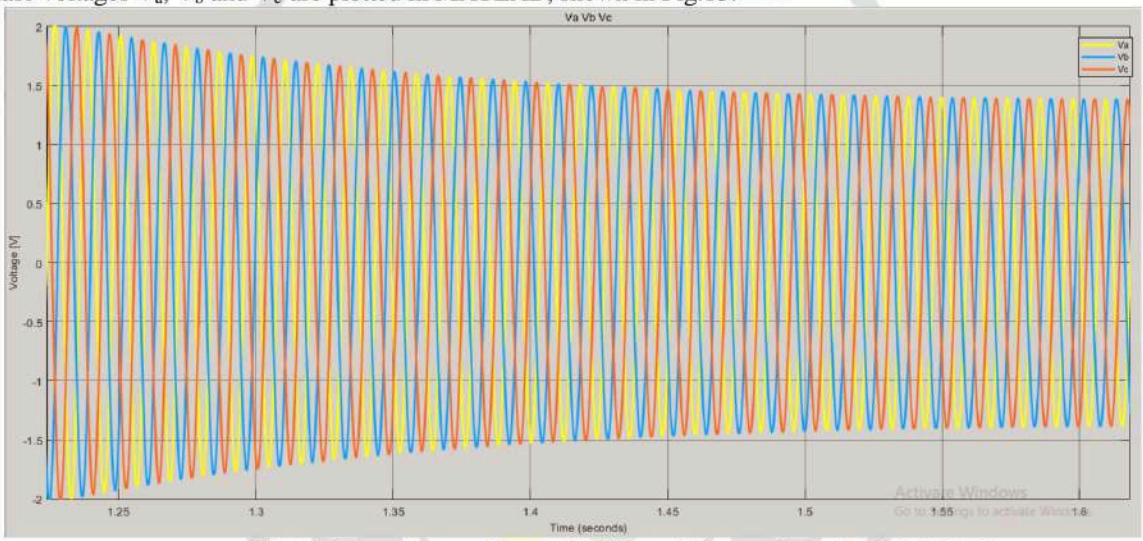

Fig.13 three phase voltages V_a, V_b and V_c are plotted in MATLAB

5.8 Sinusoidal Pulse Width Modulation (SPWM)

The three – phase voltages Va, V_b and V_c are compared with the high frequency triangle waves to generate the sinusoidal pulse width modulation (SPWM) signals in 180° conduction mode. The motor is operated through the inverter module using the generated SPWM signals. The block diagram of SPWM logic simulated in MATLAB is shown in Fig.14.

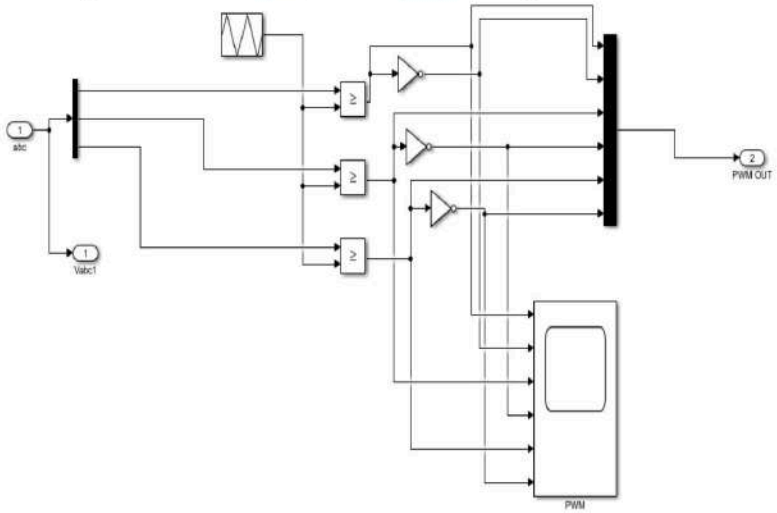

Fig.14 SPWM logic for 180° conduction mode

The sinusoidal PWM signals generated in MATLAB is as shown in fig.15.

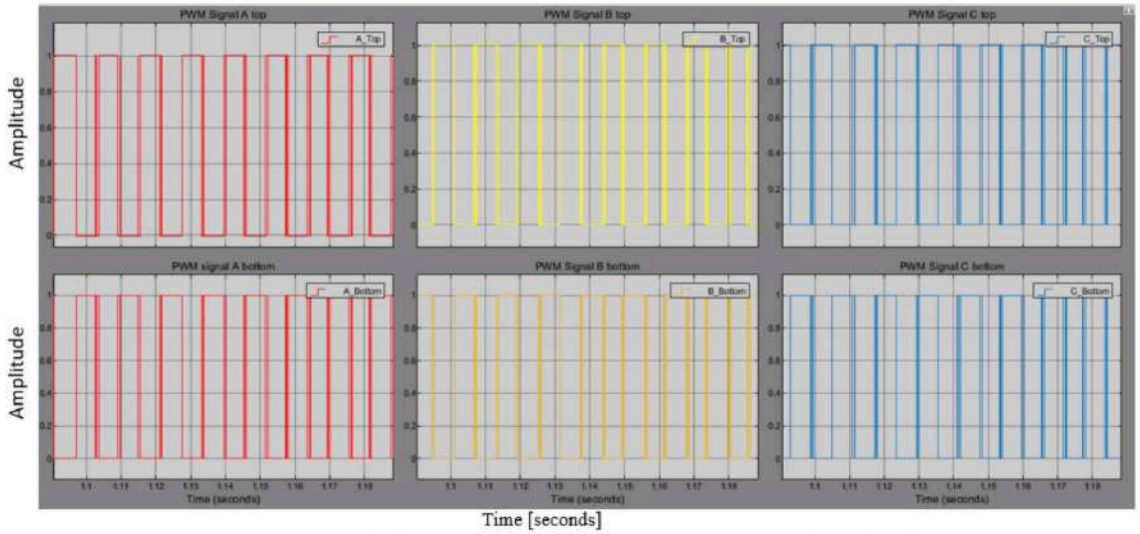

Fig.15 Sinusoidal PWM signals generated in MATLAB

The speed and torque response of the FOC algorithm simulated in MATLAB for set speed of 5000 rpm with load torque of 80mNm is shown in Fig.16 and Fig17.

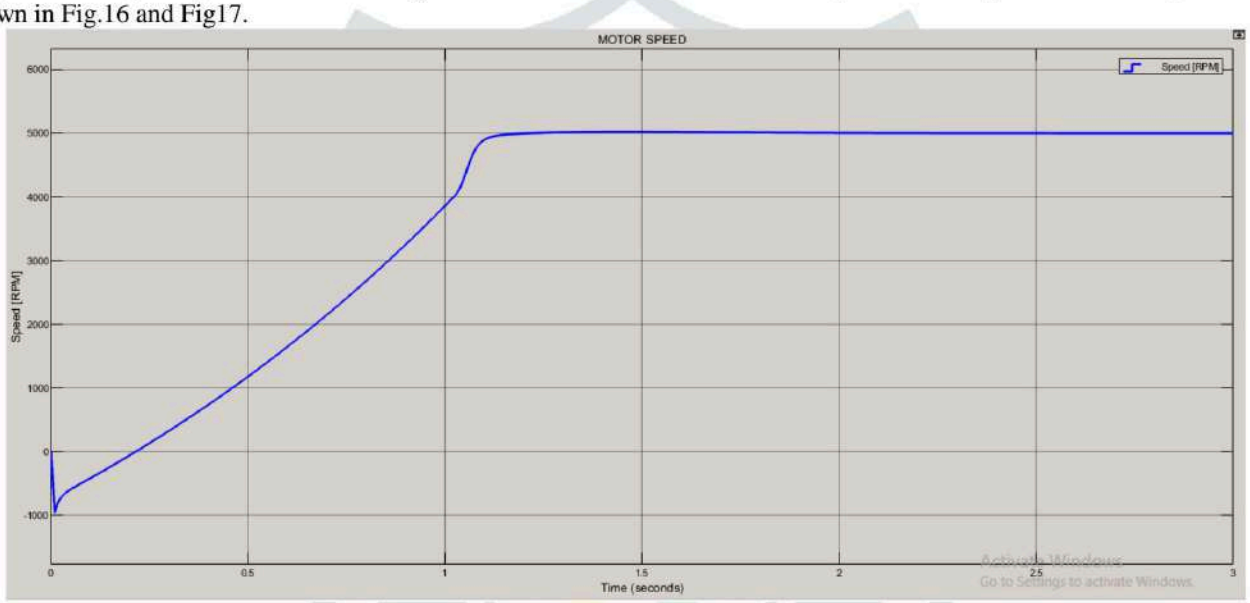

Fig.16 Motor Speed response in MATLAB at 5000 rpm.

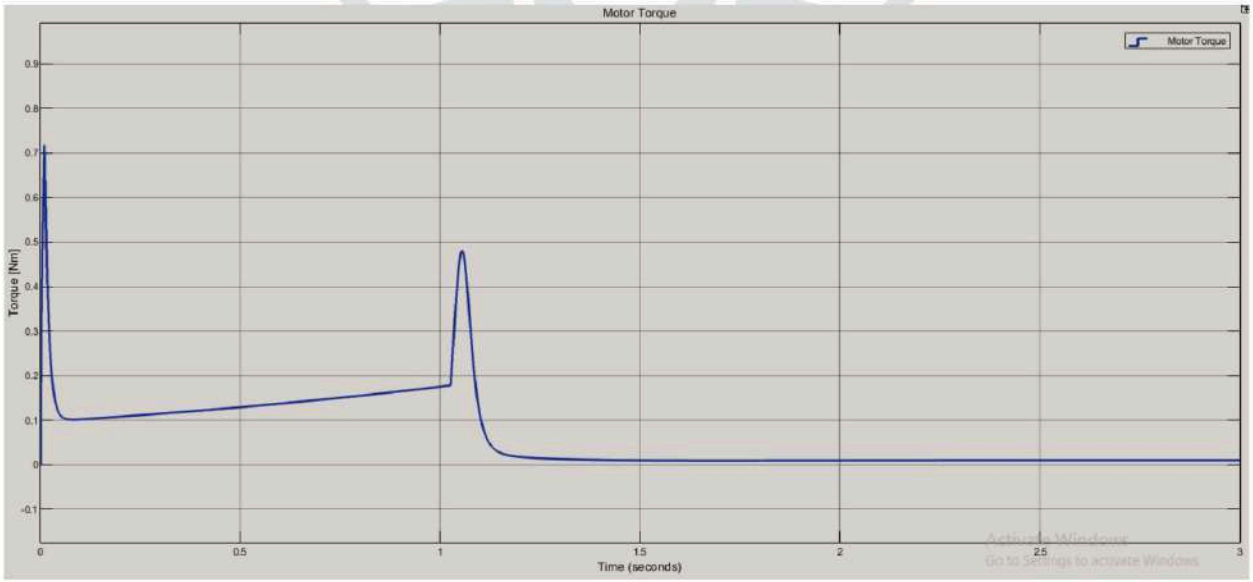

Fig.17 Motor Torque response in MATLAB at 80mNm.

VI. HARDWARE IMPLEMENTATION RESULTS AND DISCUSSION

6.1 Graphical User Interface

The graphical user interface (GUI) designed for speed setting and monitoring real time data is shown in Fig.18.

Fig.18 GUI developed for FOC in LabVIEW

6.2 Hardware Results of FOC Control of DUT Motor

The DUT- PMSM motor is tested in 350kW dyne test bench to operate in forward motoring, forward braking, reverse motoring, and reverse breaking operations by applying varying loads on the DUT motor by dyne motor.

1. **Forward Motoring**
   - The Motor is loaded on 350kW Dyne system with 120V DC supplied to inverter.
   - The Motor is operated in forward direction.

Table-1 shows the variation of speed for load conditions of DUT motor

Set Speed [rpm]	Iq ref [A]	R- Phase Current [A]	Actual Speed [rpm]	Load [Nm]
800	50	40-50	830	10
2000	60	50-60	2050	12
2000	70	60-70	1900	14
2000	75	60-75	1890	18
2000	80	70-80	1850	22

Table-1 Variation of speed for varying load in forward direction

2. **Reverse Motoring**
   - The Motor is loaded on 350kW Dyne system with 120V DC supplied to inverter.
   - The Motor is operated in reverse direction.
   - The negative sign indicates that the rotor shaft direction is in opposite direction from previous case.

Table-2 shows the variation of speed for load conditions of DUT motor in reverse direction

Set Speed [rpm]	Iq ref [A]	R- Phase Current [A]	Actual Speed [rpm]	Load [Nm]
-800	50	40-50	-800	10
-2000	60	50-60	-1950	12
-2000	70	60-70	-1900	14
-2000	75	60-75	-1890	18
-2000	80	70-80	-1850	22

Table-2 Variation of speed for varying load in reverse direction

6.3 Hardware Results – Sinusoidal PWM signals

The 180-degree conduction mode- sinusoidal PWM signals from the developed FOC algorithm is read at the FPGA module NI-9401 ultra-high speed DIO pins – 0 to 5. The sinusoidal PWM signals are then amplified from 5V to 12V.The PWM signals generated are shown in Fig.19.

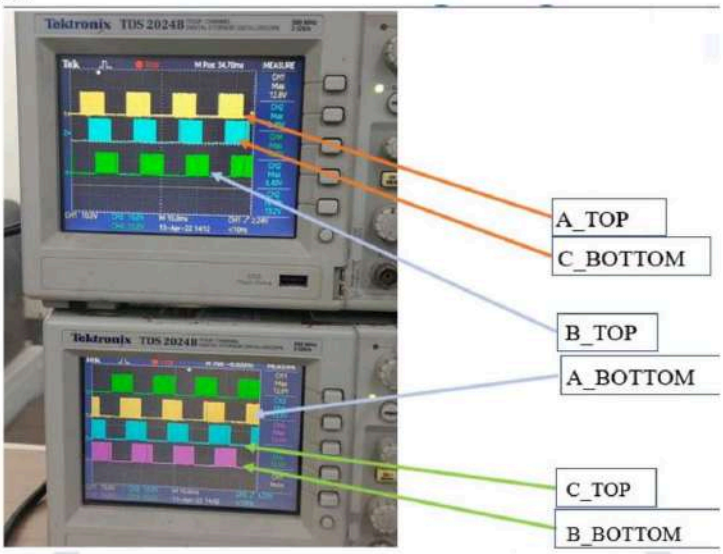

Fig.19 Sinusoidal PWM signals generated in 180-degree conduction mode

6.5 Hardware Results – Line Voltages across the DUT motor terminals

The line Voltages across RY, YB and BR phases on no-load condition are as shown in Fig.20.

Fig.20 Line Voltages across RY, YB and BR terminals of the DUT motor on no-load

Table-3 shows the measured values of the line voltages of DUT motor in no load conditions.

Phase	V_{max}[V]	V_{min} [V]	V_{rms} [V]	V_{pk-pk} [V]
R-Y	49.6	-51.2	25.3	101
Y-B	52.2	-49.5	25.4	102
B-R	49.5	-52.0	25.2	101

Table -3 Measured Line voltages of DUT motor on no-load

6.6 Hardware Results – Phase Voltages across the DUT motor terminals

The phase voltages across each phase terminals with respect to dedicated neutral wire of the DUT motor is shown in Fig 21.

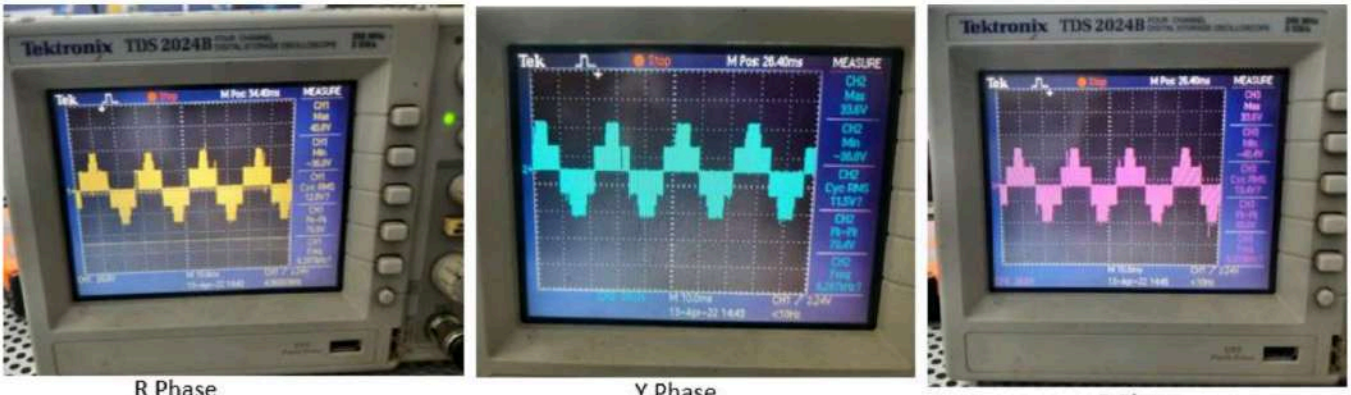

Fig.21 Phase voltages across each phase terminals with respect to dedicated neutral wire of the DUT motor

Table-4 shows the measured phase voltages across each phase and dedicated neutral wire of the DUT motor

Phase	V_{max}[V]	V_{min} [V]	V_{rms} [V]	V_{pk-pk} [V]	Frequency [kHz]
R	33.3	-36	12	70	6.26
Y	33.6	-36.8	11.5	70.4	6.28
B	33.6	-36.4	13.4	70	6.3

Table-4 Phase voltages across each phase terminals with respect to dedicated neutral wire of the DUT motor

VII. CONCLUSION

The developed program in LabVIEW software offers robust control of the DUT - PMSM motor in torque mode. The DUT motor reaches the set speed on no-load condition in 3 seconds and on-load condition at 10Nm, the motor reaches the set speed of 800rpm in 6 seconds. The DUT motor drives the load at set speed with variation in phase currents compared with the set reference current of corresponding speed. The error in set reference current and measured current is observed to be less than +/-10%. The developed module operates the DUT motor in all 4 quadrant operations and performance analysis is conducted on Dyne test bench.

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Major Project: Phase-II Report

on

DESIGN, DEVELOPMENT AND VALIDATION OF NFC SYSTEM FOR LOW POWER APPLICATIONS

18MPE41

Submitted by

MONISHA J R

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Under the Guidance

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Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY

in

POWER ELECTRONICS

2021-22

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CERTIFICATE

Certified that the project work titled **"Design, Development and Validation of NFC System for Low Power Applications"** carried out by **Monisha J R, USN: 1RV20EPE07**, a bonafide student of **RV College of Engineering, Bengaluru** in partial fulfilment for the award of **Master of Technology** in **Power Electronics** of **RV College of Engineering, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi,** during the year **2021-22**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

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DECLARATION

I, **Monisha J R**, student of fourth semester M.Tech in **Power Electronics**, **Department of Electrical and Electronics Engineering,** RV College of Engineering, Bengaluru declare that the project titled **"Design, Development and Validation of NFC System for Low Power Applications"**, has been carried out by me. It has been submitted in partial fulfilment of the course requirements for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

Date of Submission: 14-07-2022 **Signature of the Student**

Student Name: Monisha J R

USN: 1RV20EPE07

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Date : 28 June, 2022

To Whomsoever It May Concern

Ongoing Internship Certificate

This is to certify that **Ms. Monisha J R, ID - NXF78037**, is undergoing an internship at **NXP India Pvt. Ltd., Bangalore**. She started the internship on **1 September, 2021** on the project titled: **Design, Development and Validation of NFC system for Low Power Applications under the guidance of Mr. Vinay Singh P and Mr. Rajesh Sugasi.**

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Monisha J R

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ABSTRACT

Near Field Communication (NFC) is a standard-based short-range wireless connectivity technology that makes life easier and more convenient for consumers around the world by making it simpler to make transactions, exchange digital content, and connect electronic devices with a touch. NFC is compatible with millions of contactless cards and readers already deployed world-wide. Just like Bluetooth and Wi-Fi, and all manner of other wireless signals. NFC works on the principle of sending information over radio waves. The technology used in NFC is based on older RFID (Radio-frequency identification) ideas, which used electromagnetic induction in order to transmit information. The transmission frequency for data across NFC is 13.56 megahertz. Data can be sent at either 106, 212, or 424 kilobits per second.

The project work aimed at the design and development of an NFC system with NXP PN5190 reader chip and an antenna operating at 13.56 megahertz. The proposed NFC system operated in low power mode like Standby which minimized the chip current and in turn reduced the power consumption. The NFC system code implementation was carried out in Eclipse IDE tool and an antenna with symmetrical matching was designed for 13.56 megahertz. The test framework to validate the low power modes of NFC reader IC for different wake up scenarios and clock management unit on RTL environment was developed in Eclipse IDE tool. The need for a low power voltage converter to provide isolation increases as technology progresses. The supply in the designed NFC system included a proposed Flyback converter for providing output voltage of 3.3V.

The NFC system was designed and developed to operate in low power mode and reduce power utilization. From the RTL waveforms it was observed that the NFC reader IC entered Standby mode and woke up when an external RF field was detected. The rectangular antenna was designed successfully for operating at 13.56 megahertz. The flyback converter was designed and simulated in PSIM tool for DC-DC conversion required for supplying the NFC reader IC incorporated in the NFC system. The designed Flyback converter achieved an output voltage and current of 3.3V and 0.1A respectively from an input supply of 12V. The test framework with 45 tests was carried out for validating the designed NFC system power modes and clock unit. The tests was carried out in Links application and all 45 tests passed with proper transition to low power modes.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Monisha J R, Dr. S G Srivani "Design of NFC System for Low Power Applications", *International Research Journal of Engineering and Technology (IRJET)*, Volume: 09, Issue: 06, June 2022

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GLOSSARY

DUT : Device Under Test

IC : Integrated Circuit

LPCD : Low Power Card Detection

NFC : Near Field Communication

PMU : Power Management Unit

RF : Radio Frequency

RFID : Radio frequency Identification

RTL : Register Transfer Level

SWD : Serial Wire Debug

ULPCD : Ultra Low Power Card Detection

CHAPTER 1

INTRODUCTION

Near Field Communication (NFC) is a wireless standard for data transmission within a short-range at high frequency based on Inductive coupling. NFC technology has evolved from existing Radio-frequency Identification (RFID) technology. NFC technology is opted when there is a need to transfer data immediately and fast. The basic principle of operation is "touch to communicate" that indicates bringing NFC enabled devices in close proximity to each other establishes connection for data transmission. The transmission range of the NFC standard is close to 10cm and frequency of operation is 13.56 megahertz. The rate of data transmission offered by NFC is in the range of 106 Kbit/s to 424 Kbit/s [1]-[4].

The NFC comprises of a poller and at least one listener. The poller/initiator has the ability to power up the passive listener/target device by generating RF field actively. The NFC technology allows an NFC enabled device such as mobile to accept data from a tag that is in close proximity to the poller. The NFC passive tag consists of a silicon chip and an antenna. The passive tag does not contain an internal power source rather it makes use of the RF field generated by the reader to power up its inner circuitry. The average power consumption of the NFC system is increased due to reading of such passive tag. NFC is backward compatible with Sony FeliCa card standards as well as the Smart Card infrastructure based on ISO/IEC 14443 standard for proximity contactless smart cards. A new protocol was created and specified in the ECMA-340 and ISO/IEC 18092 standards for the information exchange between two NFC devices [5]-[7].

NFC is just not an interface to exchange data but also provides a way to transfer energy to the communication partner called the transponder. Communication with such transponder increases the average power consumption of the system consisting of NFC Reader, Wireless communication channel and a transponder. The NFC finds its application in lock/unlock and ignite car, payments, transportation, door access etc, [8]-[9].

The integration of NFC into devices has the drawback of increasing the device's energy consumption. Especially when the NFC Reader is a smart phone, during the reading process the average power consumption of NFC-Reader increases by up to 107%. Using NFC systems for applications like wireless payment, it is mandatory to add security. All the weak spots must be secure to prevent attackers from gaining unauthorized access to the system. To secure the wireless

transmission, encryption algorithms like Advanced Encryption standard (AES) is used. The usage of such algorithms leads to an increased energy consumption during transmission. As compared to other wireless standards such as Bluetooth or Wi-Fi, NFC technology presents several advantages in short-range communications. NFC ICs are cheaper, and have capability to store data within NFC IC, avoiding the use of microcontrollers thus reducing price, complexity, size and power consumption [10]-[13].

The Flyback converter have been used for DC-DC conversion and electrical isolation since the flyback topology is simple to operate with minimum component count and small size. Due to the requirements to reduce energy and cost of electronic devices, switch mode power supplies has to operate in high frequency in order to use smaller and cheaper magnetics inductors and transformers [14]-[15].

The project work attempted to show the reduction of energy consumption of NFC system by deploying the low power modes into the system. The rectangular antenna design aimed to achieve equal power distribution due to the symmetric nature of the antenna. The flyback converter in the power supply unit of the NFC system aimed at providing low output voltage required for the applications operating at low power.

1.1 Literature survey

Credit card payments, information transfer, access control, vending machines, and automation systems all make extensive use of NFC technology. The application of NFC technology in the real world creates order, boosts productivity, and improves communication reliability. Numerous scholars have conducted extensive research on the subject and have produced numerous academic papers and journal articles on security in NFC applications [1].

The NFC IC producers recently released sophisticated integrated circuits with energy-harvesting capabilities on the market. These chips utilise the magnetic field energy received at the reader to generate voltage that is used to power external devices [2]. Extremely low power consumption becomes a design requirement as the need for extended battery life grows. Methods of system level power management are essential for achieving low power usage. A variety of sleep modes are implemented using different levels of clock and power gating as part of power management techniques. Software-commanded entrance and exit are among these modalities [3]. A system-on-chip (SoC) with different power states can optimise consumption in the suspend mode by using adaptive power management (APM). The SoC has the option to choose the most effective low power mode for its activity thanks to the APM [4].

Pulsed RF transmission is used by LF RFID tags to connect with the reader. The electronics inside passive tags is powered by the incoming RF energy sent by a reader because they lack an internal power source. The chip keeps operating even when there is very little RF power available by drawing current from a sizable on-chip storage capacitor that is adjusted by the PM system when there is RF power available [5]. The three components of software power management are battery management, device management, and CPU management. Dynamic voltage scaling (DVS) refers to runtime changes in the supply voltage levels given to various components in a system in order to reduce overall system power consumption, is a component of CPU power management. The CPU voltage is lowered to reduce power consumption when the system workload is reduced. Due to the fact that the processor's power consumption is inversely related to operational clock frequency, the Real Time clock (RTC) is used to regulate the system clock to reduce power consumption [6]. All of the devices in the system is controlled by the device power management. Each device must cooperate with the system's state transition when it is put into normal mode from sleep mode. The device can refuse to enter sleep mode when the system is switched from normal mode to sleep mode to prevent the system from entering sleep mode if the device in the system is in a busy state [7]-[8].

The NFC technology included in mobile phones has a wide range of uses, including ticketing, payment, and identification. Because NFC requires a reader to be active, the incorporation of NFC into mobile devices causes an increase in battery depletion. The aim of the power-management algorithms deployed in software and hardware is to minimise consumption [9]-[11]. Working frequency and dynamic power usage are inversely correlated. When in low performance or waiting mode, the SoC can lower the work frequency to reduce the dynamic power consumption [12]. Internal power and switching power consumption make up the dynamic power consumption. Adjusting the clock frequency and SOC supply power to fulfil the relevant application and use little power are influencing aspects for the dynamic power [13]-[14].

The concept of flyback converter and the simulations are presented in [15]. For low power applications, flyback converter arrangement is advantageous. To provide an effective yet compact supply, this design is appropriate for the power supply unit. A step-down voltage supply is provided by the flyback converter.

1.2 Motivation

The integration of NFC into devices has the drawback of increasing the device's energy consumption. Especially when the NFC Reader is a smart phone, during the reading process the average power consumption of NFC-Reader increases by up to 107% [8]. Using NFC systems for applications like wireless payment, it is mandatory to add security. All the weak spots must be secure to prevent attackers from gaining unauthorized access to the system [11]. To secure the wireless transmission encryption algorithms are used and the usage of encryption algorithms leads to an increased energy consumption during transmission. Hence the project deploys the low power modes in the NFC system to reduce the current drawn and in turn reduce power consumption.

1.3 Problem definition

Design and Development of the NFC system to operate in low power modes to minimize the power utilization using Eclipse IDE tool and designing Flyback converter for NFC reader IC to serve as power supply unit. Validation of low power modes and clock sources to verify the functionality.

1.4 Objectives

The main objectives of the project are:

- Design and Development of an NFC system to operate the NFC reader IC in various power states, reducing the power consumption by deactivating certain on-board peripherals and reactivate only when an event occurs.
- Development of test framework for power management unit to validate the low power modes and the transition process.
- Validating the clock management unit for NFC reader IC.
- To design and simulate a flyback converter for NFC reader IC.

1.5 Organisation of the Report

The complete report presents the review of the work carried out, concepts, design and its verification. It is organised in seven chapters.

Chapter 1: Introduction briefs the introduction of the project, that includes the overview of the project, literature survey of the project that gives the cons of the project and motivation to take up the project, problem definition, and objectives of the project. It also includes the organisation of the report.

Chapter 2: Theory and Concepts gives the basics of the NFC technology including the operating modes, applications, working of the NFC standard and Power and Clock management unit of the embedded systems. It also includes the Flyback converter topology circuit and working, that has been incorporated as part of power supply unit of the system.

Chapter 3: Methodology and Block Diagram presents the methodology used in the design and development of an NFC system for low power applications. It consists of block diagram and flowchart of proposed scheme. It also explains the approach followed for the validation process.

Chapter 4: Specifications and Design explains in detail the design and specifications of the proposed NFC system including reader IC and antenna. It also explains in detail about the design of the Flyback converter incorporated in the power supply unit. The specification of the reader IC is also provided in the chapter.

Chapter 5: Simulations and Implementations provides the simulation for the proposed NFC system and converter circuit. It also includes the details for the implementation of the project.

Chapter 6: Results and Discussion discusses about the simulation results of the NFC system design, converter and hardware results for the same.

Chapter 7: Conclusion and Future Scope includes the overall conclusion drawn from the project and the future works that can be carried out.

References includes the list of references referred in the successful completion of the project.

1.6 Summary

This chapter gives an introduction to the NFC technology and the key findings of the literature review. It also describes the problem statement, objectives and methodology.

CHAPTER 2

NFC SYSTEM FOR LOW POWER APPLI CATIONS

This chapter describes the theory and underlying concepts of the NFC technology and the power and clock management unit of the embedded systems.

2.1 Near Field Communication (NFC)

Radio Frequency Identification (RFID) technology incorporates wireless radio communication technology for unique identification. Both NFC and RFID work on same principle of inductive coupling at 13.56 megahertz. NFC technology has shorter transmission range of 4cm to 10cm compared to RFID range of 100cm. NFC technology provides communication solution to non-self-powered device (passive) [1].

The NFC technology is made complementary to other wireless technologies like Wi-Fi, Bluetooth etc. to increase the data transmission range. The main advantage of NFC is the ability to save energy. Currently various devices like smart phone and smart wearables are equipped with NFC feature for use cases like data transfer between two devices and mobile payments. The smart phone applications like Samsung Pay and Google Pay facilitates contactless payment feature. NFC finds its use case in Transportation access, like in the public Metro transport ticketing where the coin has NFC tag incorporated in it [1]. The Fig 2.1 gives an overview of NFC Domain.

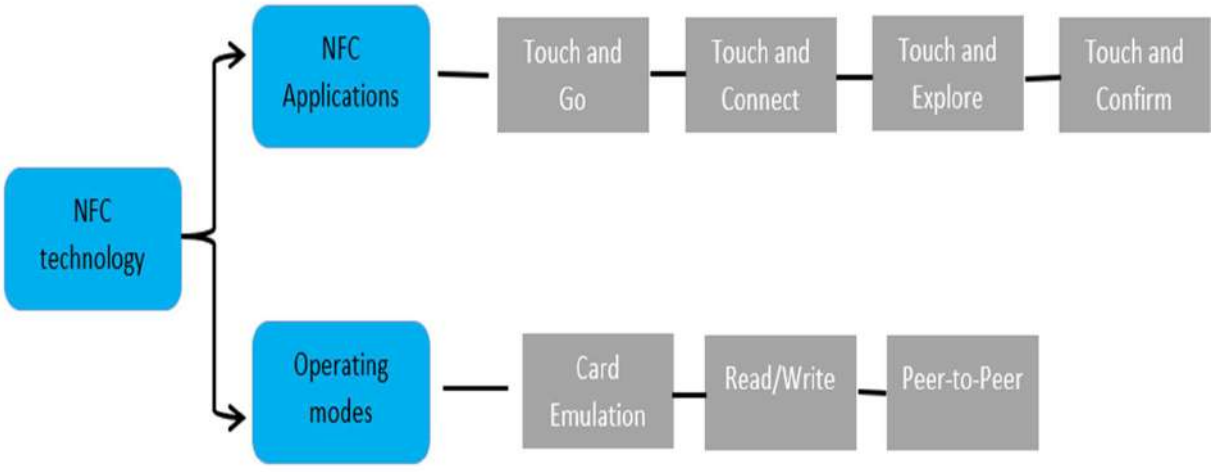


Fig 2.1: NFC Domain

2.1.1 NFC Operation modes

The three operating modes of NFC are shown in Fig 1, namely read/write mode, peer-to-peer mode and card emulation mode. The Card Emulation Mode is shown in Fig 2.2, consists of an active NFC reader and a Passive NFC card in the communication setup. The NFC reader reads the information stored in the passive tag. In Read/Write Mode shown in Fig 2.3, the NFC enabled device can read data from tag or writes information to the NFC tag. The NFC tag is powered by the magnetic field and sends response to the request. In Peer-to Peer Mode shown in Fig 2.4, two NFC enabled devices communicate with each other. The Peer-to-Peer mode enables devices to connect and interact with each other to exchange data, money transfer and social networking [4]-[8].

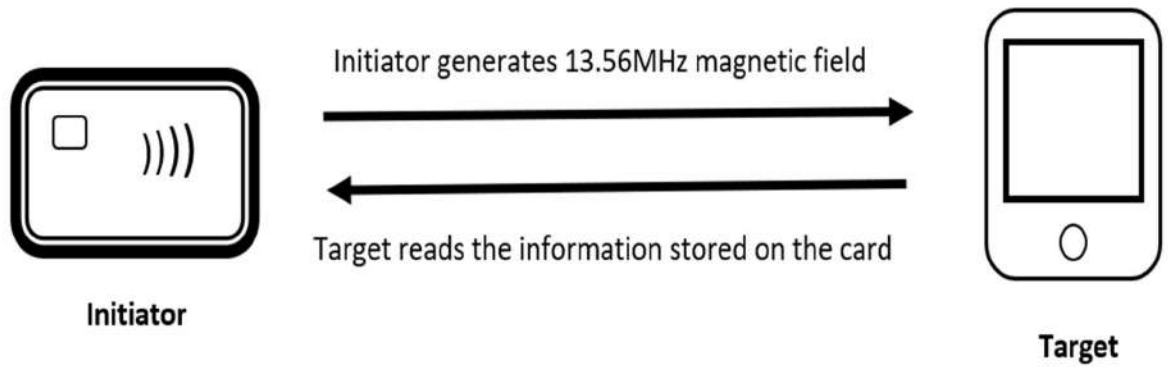


Fig 2.2: Card Emulation mode

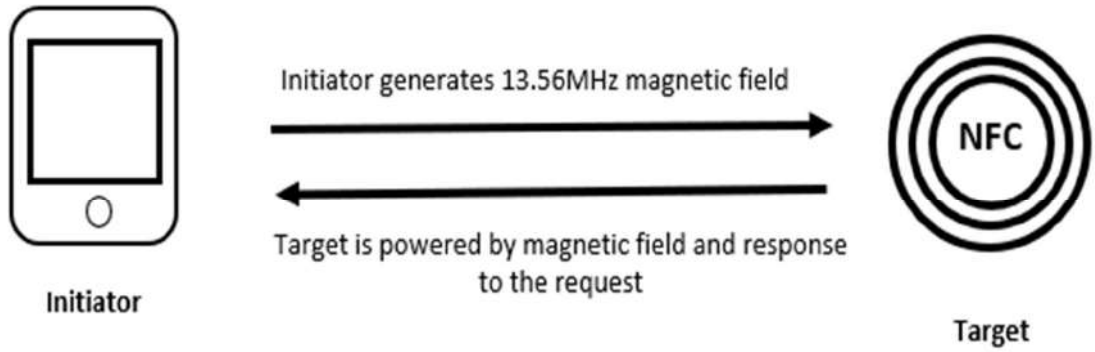


Fig 2.3: Reader/Writer mode

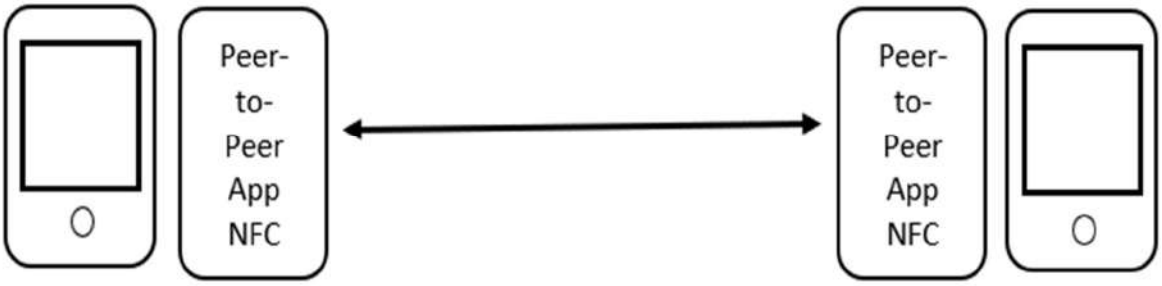


Fig 2.4: Peer-to-Peer mode

2.1.2 NFC Applications

NFC requires close range for interaction, and its behaviour is controlled through the device owners to activate NFC so it is used [15]. The classification of NFC applications are as follows:

- Touch and go application – Touch and go application requires the consumer to bring near or touch the NFC device to the NFC reader to implement the tasks in the application.
- Touch and confirm application – Touch and confirm application kind of application requires the consumer to confirm the interaction by accepting the payment transaction or entering the password for system confirmation.
- Touch and connect application – Connect to enable the peer-to-peer transfer of data between two NFC-enabled devices. For example, exchanging images, downloading music or synchronizing address books.
- Touch and explore application – The consumer is able to find and explore capabilities, functionalities and applications soon after the touch is done and connection is established by the NFC reader.

2.1.3 Working of NFC

NFC uses a frequency of 13.56MHz, it is contactless communication technology designed for data exchange between the devices by a simple tap. Passive mode NFC communication is used. Mainly three tasks are involved in establishing NFC communication.

- The necessary power required for communication is provided by the RF field of NFC reader, the tag/ card gets energized by inductive coupling.
- By modulating the RF field, reader can send information to tag/card.

- The reader receives information from tag/card by sensing load modulation of field generated by tag/card.

Fig 2.5 shows how communication is established between NFC reader and tag.

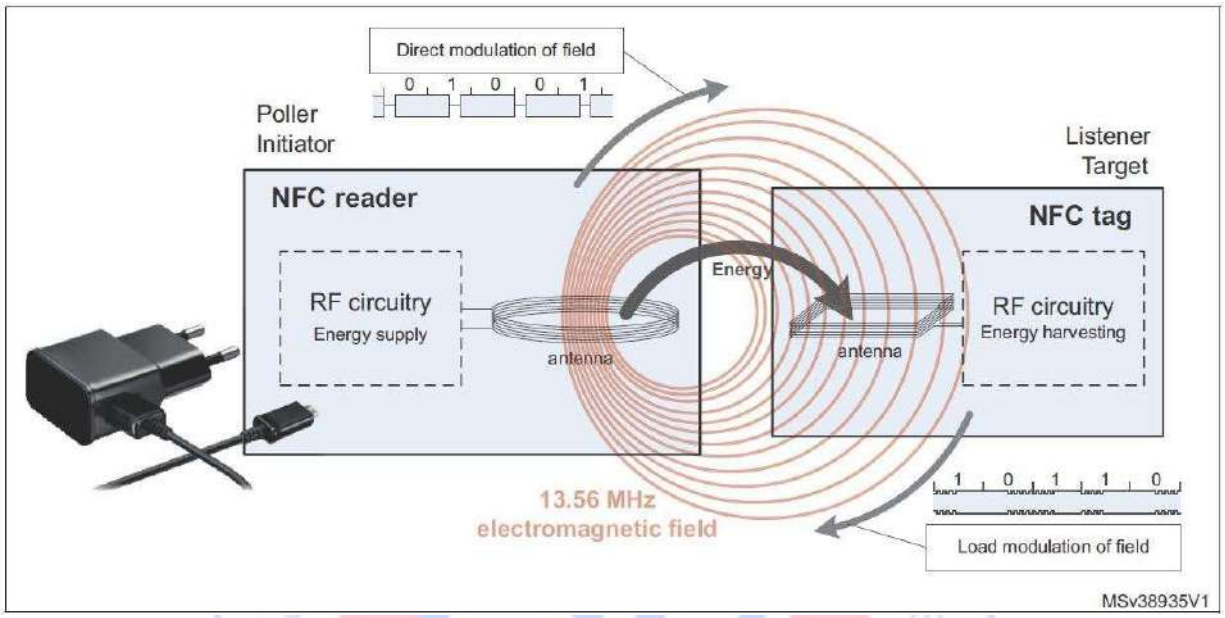


Fig 2.5: Establishment of communication

2.1.4 Basic NFC System

The basic NFC System is shown in Fig 2.6 The NFC system consists mainly of three components – a Tag, a Reader and a Controller. A Tag, also called a pulse transceiver consists of a semiconductor chip and an antenna. An electronic control module, RF module and an antenna is present in the reader device. A controller component of the NFC system is usually a PC [1].

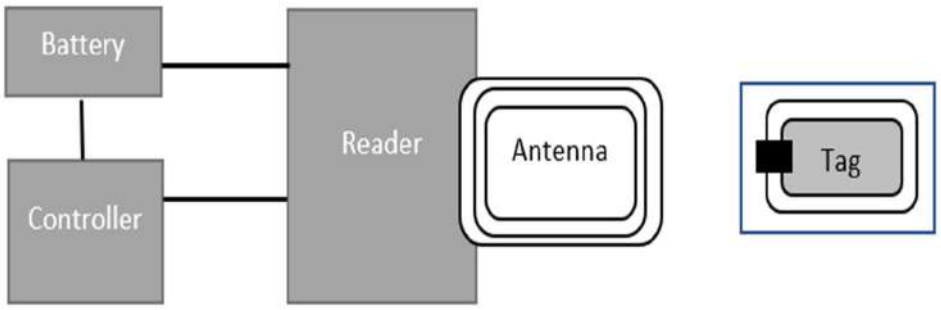


Fig 2.6: NFC System

NFC communication establishment involves three activities –

- Power transfer for communication by RF field of the NFC Reader.
- Modulation of the field.
- Load Modulation of the field.

2.2 Power Management in Embedded Systems

The critical issue in embedded devices is the power utilization due to which there is a need for extended battery life. The two scenarios in which systems power consumption is considered are when the system is in use and when the system is in idle state. The solution to this problem is the deployment of the low power CPU modes. The power management in embedded systems is achieved either by firmware power management or peripheral power down [8].

2.2.1 Firmware Power Management

The two measures firmware can into consideration to keep the power utilization minimum are –

- Switch off the system peripherals when it is not in use
- Regulate the voltage and frequency of the CPU based on the performance needs.

2.2.2 Peripheral Power-down

The very common approach to save energy in embedded system is to switch it off. The turn off of complete system when not in use is not recommended because a fully powered down device may take some time to start up. So, the embedded system is designed such a way that the peripherals and subsystems may be turned on or off by firmware temporarily. Therefore, an alternate to the system power down is the low power modes [6].

The proposed NFC reader include low voltage power domains into the architecture and offer when it is associated with power modes, embedded power states. The low power mode of operation to reduce the energy consumption is chosen by a command in application running on the system.

The various low power modes supported by NFC reader IC with the corresponding current ratings is shown in Fig.2.7.

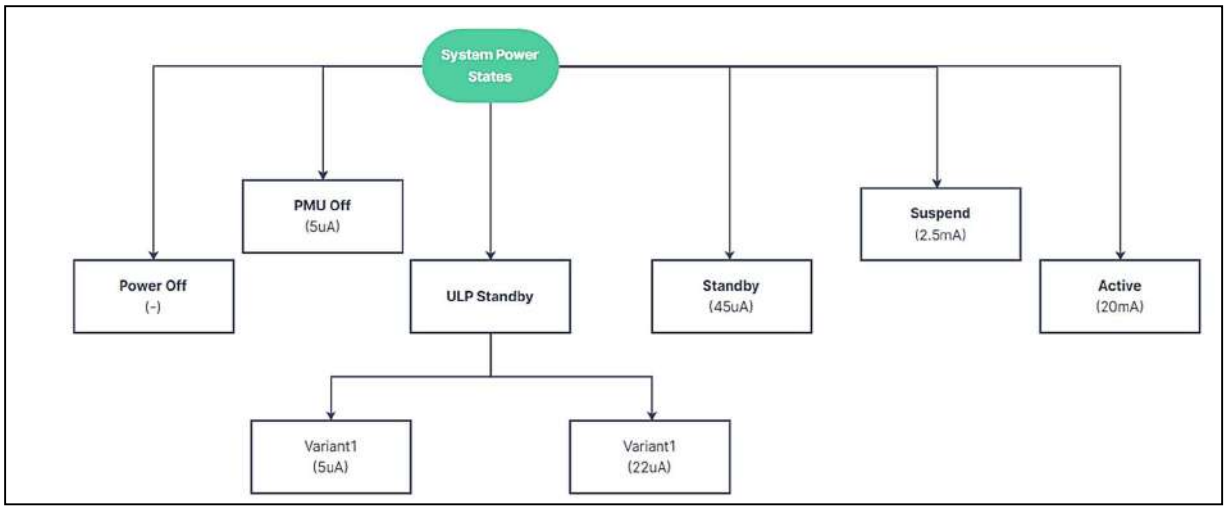


Fig 2.7: System Power States

The description of each low power mode and the wake-up sources is shown in Table 2.1.

Table 2.1. Power States

Power State	Description	Wake up sources
Power Off	• NFC System is not supplied by battery PMU	Device is not functional
PMU Off	• No active internal clocks • PMU Off is triggered by power loss on VDDIO	• Power reset on pin VBAT • VEN rising edge • RX ULPCD detect • ULP abort signal on PIN3 • VDDIO restore
ULP Standby	• The reader IC can activate the transmitter and receiver after defined time to detect the card • Only Wake up timer is active.	• Power reset on pin VBAT • VEN rising edge • GPIO3 level • Card detected
Standby	• NFC system switches to low power mode automatically after a specific time of inactivity to reduce power dissipation.	• Activity on host IF • ULPDET • LPDET • wake-up counter • power loss on VDDIO • GPIO
Suspend	• Power sources are available • LFO and HFO clocks are available	• Activity on host IF • ULPDET • LPDET • wake-up counter • power loss on VDDIO • GPIO
Active	• Allows process of internal and external events. • All clocks are active.	

2.2.3 Energy Saving Card detection

The energy-saving card polling configurations for the NFC reader IC are low-power card detection (LPCD) and ultra-low power card detection (ULPCD). A low frequency timer is implemented to drive a wake-up counter, that triggers a periodic activation of the antenna drivers to emit a short pulse allowing to detect a detuning of the antenna. In case of a detected antenna detuning, the system is woken up from power-saving mode. The SWITCH_MODE instruction allows entering the LPCD or ULPCD mode with a given standby duration value [5]. The LPCD and ULPCD configuration is shown in Fig.2.8.

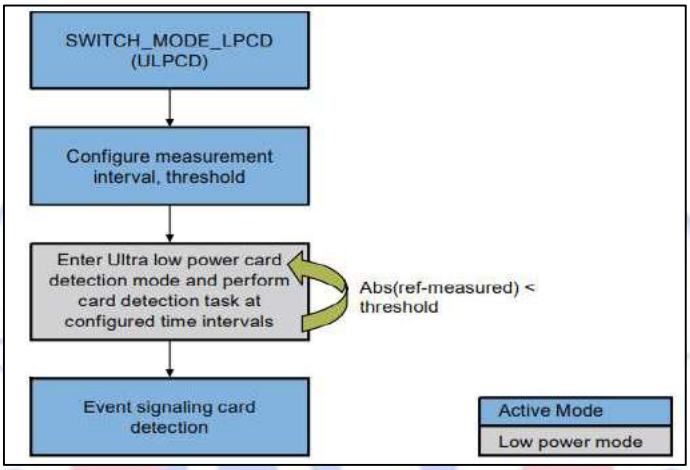


Fig 2.8: LPCD Configuration

2.3 Clock Management in Embedded Systems

Modern embedded systems have the provision to select clock sources whose frequency and power consumption differ. In the applications the workloads vary over time, the energy is saved by dynamically changing the clock [11].

The clock sources available in the reader IC are as shown in Fig.2.9.

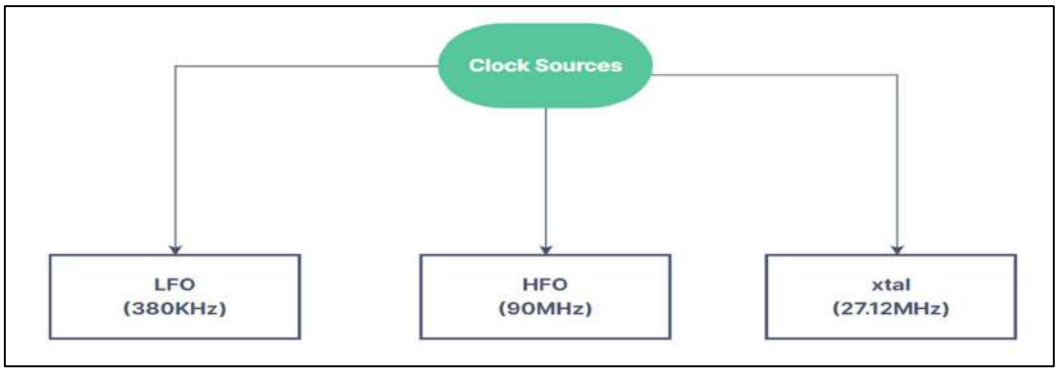


Fig 2.9: Clock Sources

2.4 Flyback converter

The Flyback converter is designed like the switch mode power supply to perform conversion like DC to DC. The flyback converter is a DC-DC converter topology like boost converter having similar structure and performance. The converter stores energy when current flows using an inductor and supplies energy when the power is removed [2].

The two stages of operation of the Flyback converter are: the power transfer from input to output side when Mosfet is turned on and no transfer of power when the Mosfet is turned off. The most common use case of the flyback converter is the SMPS for low power applications. The flyback converter has low-cost material requirements making it an economical solution for various use cases. The Flyback converter has simple design with less complexity [4]. The simple flyback converter circuit is shown in Fig 2.10.

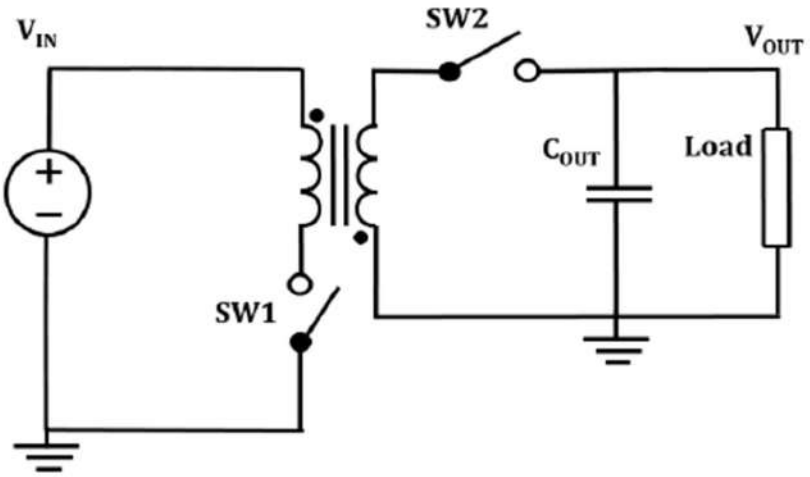


Fig 2.10: Flyback converter circuit

When SW1 is turned off, the circuit goes to another circuit operation. Since, the MOSFET is turned off, the primary winding current path is disconnected, the polarity of the voltage across the windings is reversed. Since there is voltage reversal, the diode switch becomes forward biased. During this time, the diode SW2 is turned on. Therefore, the forward biased diode completes the path for the secondary winding [11].

2.5 Summary

In this chapter the theory and concepts of NFC technology and its working is studied. The firmware power and clock management unit are analysed in brief. Also, the flyback converter circuit operation is explained.

CHAPTER 3

METHODOLOGY AND BLOCK DIAGRAM

This chapter describes the hardware and software requirement specifications for the NFC system. The flow chart and the block diagram for the proposed scheme is explained in detail in this chapter. The methodology of validation procedure on real IC as well as the RTL simulation are also discussed.

3.1 Methodology

The flowchart and the testing design flow employed for the project development are discussed here.

3.1.1 Flowchart

The Fig. 3.1 shows the flowchart adopted to carry out the proposed NFC system design and development process. The various stages in flowchart are: 1) Fundamental requirement specification; 2) Design of NFC system; 3) code implementation (Low power mode application); 4) validation.

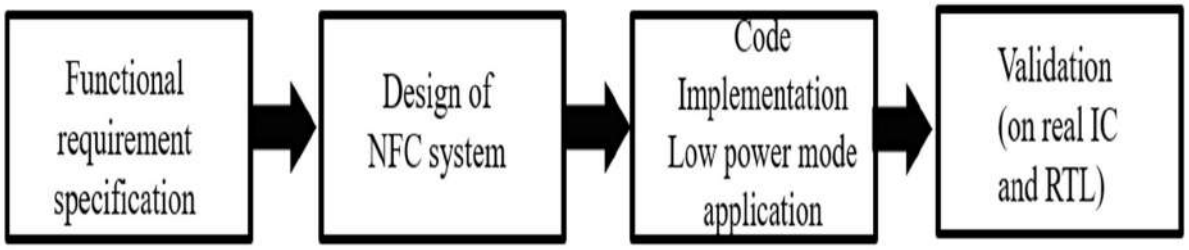


Fig 3.1: Flowchart

3.1.2 Testing

To ensure that the NFC services, NFC low power modes and the clock unit work reliably and correctly, it is necessary to validate the functionality with the help of complex test scenarios. The test cases are developed on Eclipse IDE platform. The testing and validation is carried out on the PN5190 IC. The Fig 3.2 shows the testing design flow.

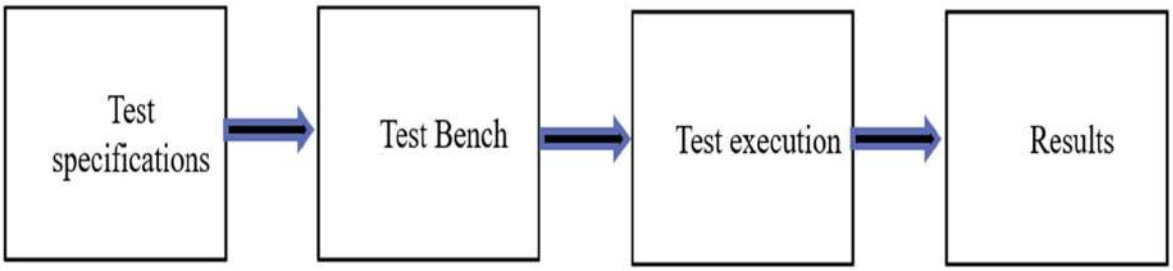


Fig 3.2: Testing design flow

The functionality of the NFC system operating in low power modes is verified by either the real IC test set up or the RTL simulation tool. In real IC test set up the code is flashed onto the NFC reader IC and debug probe is connected to the device under test. The Fig 3.3 shows the IC test set up.

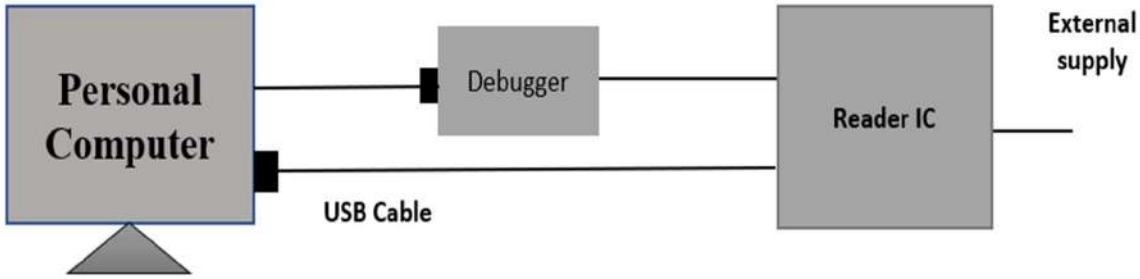


Fig 3.3: Real IC test set up

The Register Transfer level (RTL) simulation is the most widely used method to validate the NFC reader IC functionality. The RTL simulator captures the NFC reader IC signals, that is analysed for validating the functionality. The Fig 3.4 shows the RTL simulation test flow.

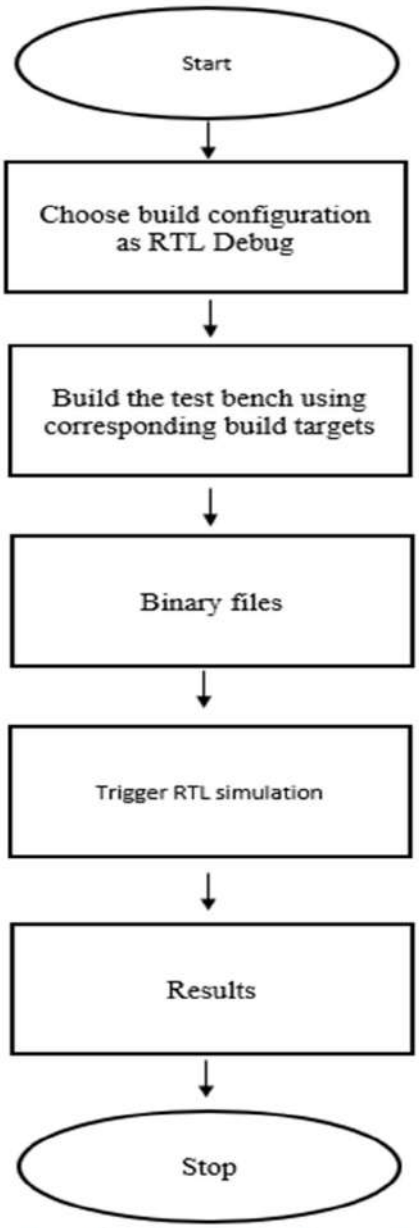


Fig 3.4: RTL simulation test flow

3.2 Block Diagram

The tag and a reader in the NFC system have radio frequency communication between them. Each tag consists of unique identification number and an antenna. The NFC Reader will use unique identification number of the tag to establish communication. The read distance of the NFC reader dependent on the antenna parameters such as the shape, size, frequency etc., surrounding environment and others [1].

The NFC Reader communicates with host PC via host interfaces, that is either of I2C, SPI, USB or serial UART. In the proposed system the Reader IC is considered to be PN5190 IC. The reader IC is customized to operate in low power mode in order minimize current consumption via a software application flashed on to it [3]. The various low power modes, the reader IC could operate are such as Standby mode, Suspend mode and ultra-low power card detection mode. The reader IC have several other features and interfaces accommodated in the chip to meet the requirements of different use cases. The NFC Reader comprises of an antenna that is chosen to be rectangular patch antenna. The main issue in the design of the NFC system is the antenna alignment with the reader.

The Fig 3.5 shows the block diagram of the NFC system consisting of NFC Reader IC operating in low power mode, battery supplying 12V, Flyback converter on the source side to step down the supply, host, antenna and NFC tag.

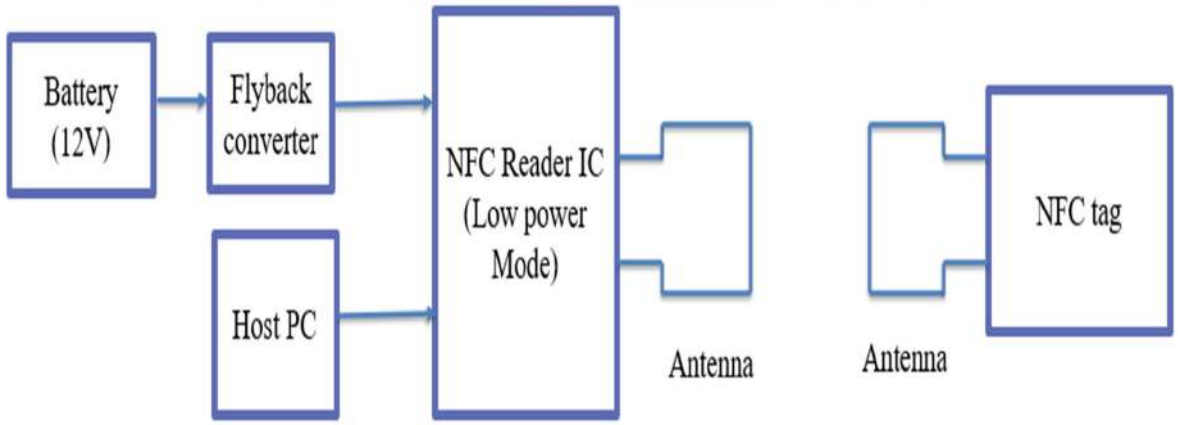


Fig 3.5: Block diagram

The power supply unit of the NFC system comprises of: Battery of 12V and a Flyback converter incorporated for DC-DC conversion. The flyback converter will step down the battery supply to voltage of 5V/3.3V. The host PC is used to send commands to the NFC IC. The host PC is also used in the debugging process, debug probe is connected between host PC and debugger. The NFC reader IC will operate in low power mode to minimize the power utilization.

3.3 Summary

The required methodology and block diagram for designing NFC system to operate in low power mode was explained in the chapter. The testing design flow and the test set up was also explained in this chapter.

CHAPTER 4

SPECIFICATIONS AND DESIGN

There are various components involved in the proposed NFC system. The process is carried out smoothly if all the components are interfaced and synchronised in the desired fashion. The process of selecting and designing the components as per required specifications plays an important role. The chapter deals with the design and selection of various components needed for the operation.

4.1 Specifications

The hardware and software requirement specifications for the designing and the validation of the NFC system are mentioned below. These are essential to carry out the project successfully and correctly.

4.1.1 Hardware requirement Specifications

The hardware requirements for the project are listed below.

- NFC Reader IC (PN5190): The PN5190 is a frontend reader. The operating features of the NFC reader is shown in Table. For the payment use cases and environment where strong RF field is necessary the PN5190 is a best choice. The PN5190 has simplified design while ensuring interoperability with a broad range of smartcards and cell phones. The Fig 4.1 shows the PN5190 development board. The operating features of the NFC Reader IC is listed in Table 4.1.

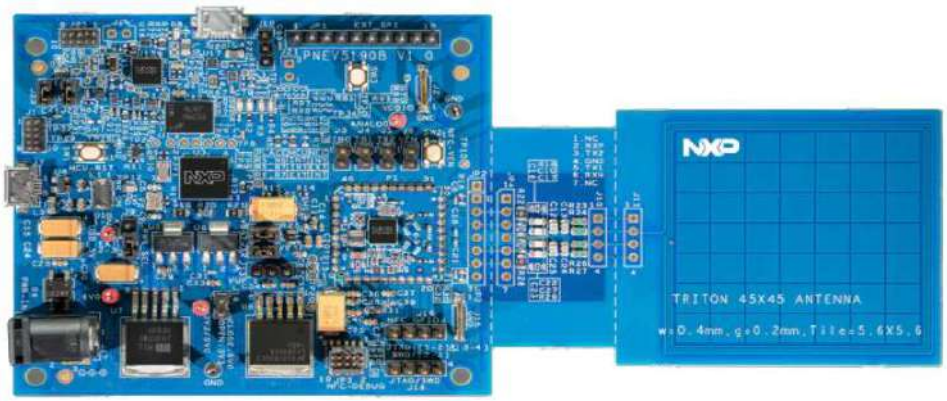


Fig 4.1: PN5190 Development board

Table 4.1: Operating Features

Parameter	Value
Read Distance (mm)	120mm
Features	NFC Reader/Writer, P2P, Card Emulation
Host Interface	SPI
Supply Voltage (V)	1.8 to 3.5
RF driver supply voltage (V)	2.4 to 6.0
RF driver current	350
Max Output Power (W)	2

- Segger Jlink – Segger J-Links are used for providing debug support. J-Links are most widely used embedded system development. The Segger J-Link Debugger is shown in Fig.4.2.

Fig 4.2: Segger J-Link debugger

- Cables – Micro-D, Usb to C type cable

4.1.2 Software requirement Specifications

The software requirements for the project are listed below.

- Tortoise SVN – Version 1.14
- Tortoise Git – Version 2.12.0
- J-Link Commander – Version 7.54

- Eclipse IDE – Oxygen3
- Cadence Simvision – Xcelium Parallel simulator

4.2 Design

The design of rectangular antenna and the flyback converter as presented in this section.

4.2.1 Antenna design

The choice of right antenna depends on the application requirements. In the process of choosing the right antenna there are tradeoffs between applications requiring maximum read distance (consumes large power) and applications with strict power budgets (results in short read range). The balance between the two extremes is achieved with a blend of power efficiency and performance, that is met with the latest high-performance readers featuring ultra-low power card detection. In the proposed system a rectangular antenna is chosen because it is a symmetrical antenna with equal power distribution. The bill of material and the number of components is reduced [1]. The Fig 4.3 gives an example of rectangular antenna and dimensions. The inductance of antenna is calculated using following formulas:

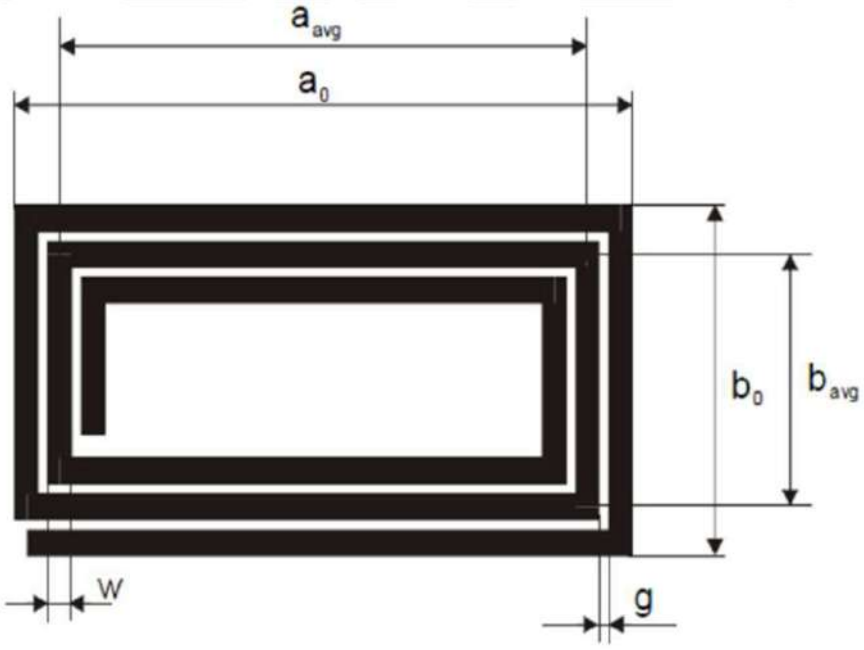


Fig 4.3: NFC Antenna

The inductance of the antenna [1] is calculated by the equation (1),

$$L_a = \frac{\mu_o}{\pi} \cdot [x_1 + x_2 - x_3 + x_4] \cdot N_a^{1.8} \quad (1)$$

where, $\mu_o = 4\pi \times 10^7$

The various parameters required to computed for calculating inductance of the antenna are listed below. The dimensions of the proposed antenna are,

a_0= 45mm, b_0= 45mm, N_a= 3, w = 200µm, g = 400µm, t = 35µm.

$$d = \frac{2(t+w)}{\pi} \quad (2)$$

$$d = \frac{2(35\mu + 1.5m\ \ )}{\pi} = 0.9772mm$$

The value of d obtained by equation (2) by substituting thickness (t) of 35um and width 1.5mm is 0.9772mm.

$$a_{avg} = a_0 - N_a(g + w) \quad (3)$$

$$a_{avg} = 45 - 3(1 + 1.5) = 37.5\text{mm}$$

The value of a_{avg} obtained by equation (3) by substituting a_0= 45mm, N_a= 3, g = 1mm and w = 1.5mm is 37.5mm.

$$b_{avg} = b_0 - N_a(g + w) \quad (4)$$

$$b_{avg} = 45 - 3(1 + 1.5) = 37.5\text{mm}$$

The value of b_{avg} obtained by equation (3) by substituting b_0= 45mm, N_a= 3, g = 1mm and w = 1.5mm is 37.5mm.

$$x_1 = a_{avg} \cdot \ln\left[\frac{2a_{avg}b_{avg}}{d\left(a_{avg} + \sqrt{a_{avg}^2 + b_{avg}^2}\right)}\right] \quad (5)$$

$$x_2 = b_{avg} \cdot \ln\left[\frac{2a_{avg}b_{avg}}{d\left(a_{avg} + \sqrt{a_{avg}^2 + b_{avg}^2}\right)}\right] \quad (6)$$

$$x_3 = 2\left[a_{avg} + b_{avg} - \sqrt{a_{avg}^2 + b_{avg}^2}\right] \quad (7)$$

$$x_4 = \frac{a_{avg}+b_{avg}}{4} \quad (8)$$

The value of parameters x_1, x_2, x_3 and x_4 obtained by equations (5), (6), (7), and (8) are 12.9965, 12.9965, 43.934 and 18.75 respectively.

where,

a_0 = length in mm

b_0 = width in mm

t = track thickness in mm

w = track width in mm

N_a = number of turns

The value of inductance L_a computed by equation (1) by substituting all the parameters is 2.33μH.

4.2.2 Converter design

The power supply unit of the NFC system comprises of a battery of 12V and a flyback converter has been incorporated for DC-DC conversion. The flyback converter will step down the battery supply voltage to 5V/3.3V. The flyback converter is a DC-DC converter topology like boost converter having similar structure and performance [9]. The converter stores energy when current flows using an inductor and supplies energy when the power is removed.

Flyback switch mode power supply is most commonly used SMPS circuit for low output power applications. The flyback converter has two operation phases: when the power from input side is being transferred to the output when the primary side switch is off and when the primary side switch is on and the output do not receive power from primary side. The basic flyback design has few low-cost material requirements just like the other dc-dc converters: the capacitor, the MOSFET as the primary switch, the diode as the secondary switch and inductor is being replaced by the flyback transformer or simply transformer [9]. The simple flyback converter circuitry is shown in Fig 4.4.

The switching frequency of the flyback converter is limited to 100KHz. The specifications of the Flyback converter are as follows:

- Input Voltage – 12V DC
- Output Voltage – 3.3V DC
- Duty cycle – 45%
- Switching frequency – 100KHz
- Output Current – 0.1A
- Transformer turns ratio ($^{N_1}/_{N_2}$) – 3

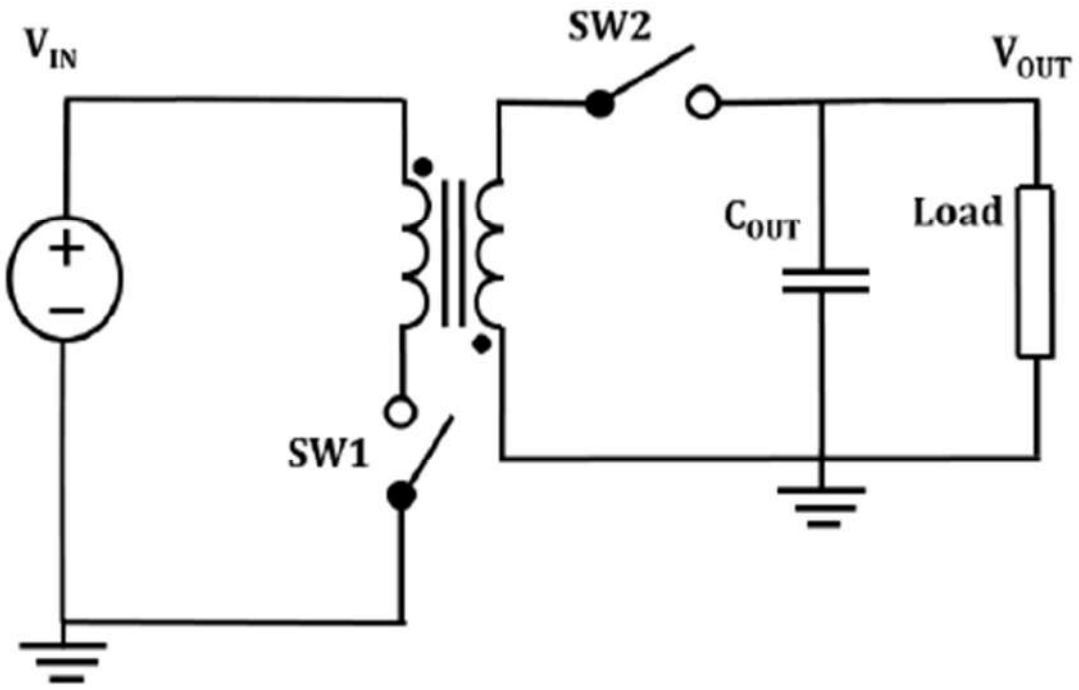


Fig 4.4: Simple Flyback Converter

The necessary equations required for the design of the flyback converter are given below. The duty cycle calculation of the converter is required to determine the conduction ratio of the circuit The converter is designed for an output voltage of 3.3V from an input voltage of 12V. The duty cycle [9] calculated from the below mentioned equation (9) is 45%.

The transformer ratio N_1/N_2, in this design is set as 3.

$$\frac{N_2}{N_1} = \frac{V_o}{V_S} \cdot \left(\frac{1-D}{D}\right) \quad (9)$$

$$\frac{1}{3} = \frac{3.3}{12} \cdot \left(\frac{1-D}{D}\right)$$

D = 0.45

The load resistance R calculated with the output current of 0.1A in equation (10) is 33Ω.

$$R = \frac{V_o}{I_o} = \frac{3.3}{0.1} = 33\Omega \quad (10)$$

In the converter design the switching frequency is taken as 100KHz with Imin as 0.06A. The value of inductance L calculated in (11) is 22.5mH.

$$L = V_{in} \cdot \frac{D}{\frac{2I_O}{1-D} - 2I_{minf}} = 12 \cdot \frac{0.45}{\frac{2*0.1}{1-0.45} - 2*0.06*100*10^3} = 22.5\text{mH} \quad (11)$$

The computed value of capacitance C in (12) is 6.81μF.

$$C = \frac{DV_{in}}{8rV_oLf^2} = \frac{0.45*12}{8*0.066*3.3*22.5*10^3*(100*10^3)^2} = 6.81\mu F \quad (12)$$

4.3 Summary

The Simulations were carried out considering the designed values for Flyback converter. The simulations were done in PSIM simulation software. A rectangular patch antenna was designed for the NFC system.

CHAPTER 5

SIMULATIONS AND IMPLEMENTATIONS

The NFC system is implemented and developed in Eclipse IDE tool. The validation of the Low Power Modes of the NFC reader IC and Clock Management unit is carried out using the RTL tool. The simulation of the flyback converter is carried out PSIM software.

5.1 Simulations

The simulation of the Flyback converter and the antenna is discussed in this section.

5.1.1 Flyback converter

The Flyback converter topology is simulated in PSIM environment. The effectiveness of the flyback converter designed is validated and performance of the converter is checked. Table 5.1 shows the parameter values considered for the PSIM simulation of the circuit.

Table 5.1: Converter Parameters

Parameters	Symbols	Values
Supply Voltage	V_S	12V
Switching Frequency	f_S	100KHz
Load Resistor	R	33Ω
Inductor	L	22.5mH
Capacitor	C	6.81µ
Duty cycle	D	0.45
Transformer turns ratio	N_1/N_2	3
Output Voltage	V_o	3.3V
Output Current	I_o	0.1A

The simulation circuit for Flyback converter is shown in Fig.5.1. The schematic of the flyback converter comprises of a MOSFET, it acts like a switch, a transformer, a diode operating complementarily to MOSFET, an inductor and a capacitor. The pulse generator module is used for the control of duty cycle of the circuit by turning on and off the MOSFET switch. The converter

circuit components are positioned to achieve the desired output condition of 3.3V output voltage and 0.1A current.

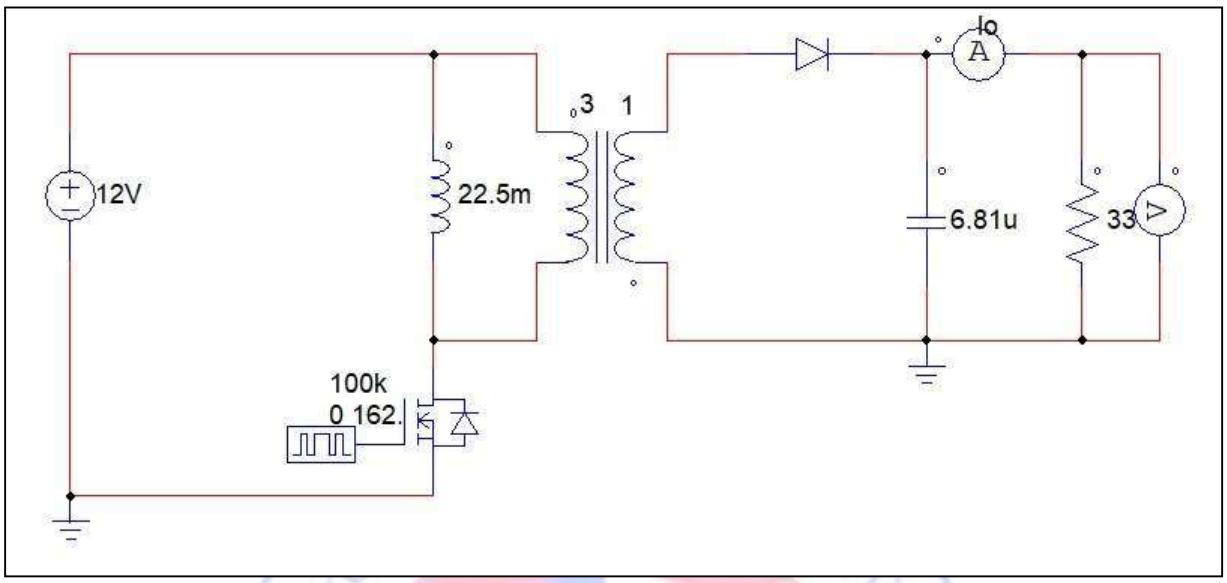


Fig 5.1: Flyback Converter

5.1.2 Rectangular Patch Antenna

The rectangular patch antenna is simulated as shown in Fig 5.2.

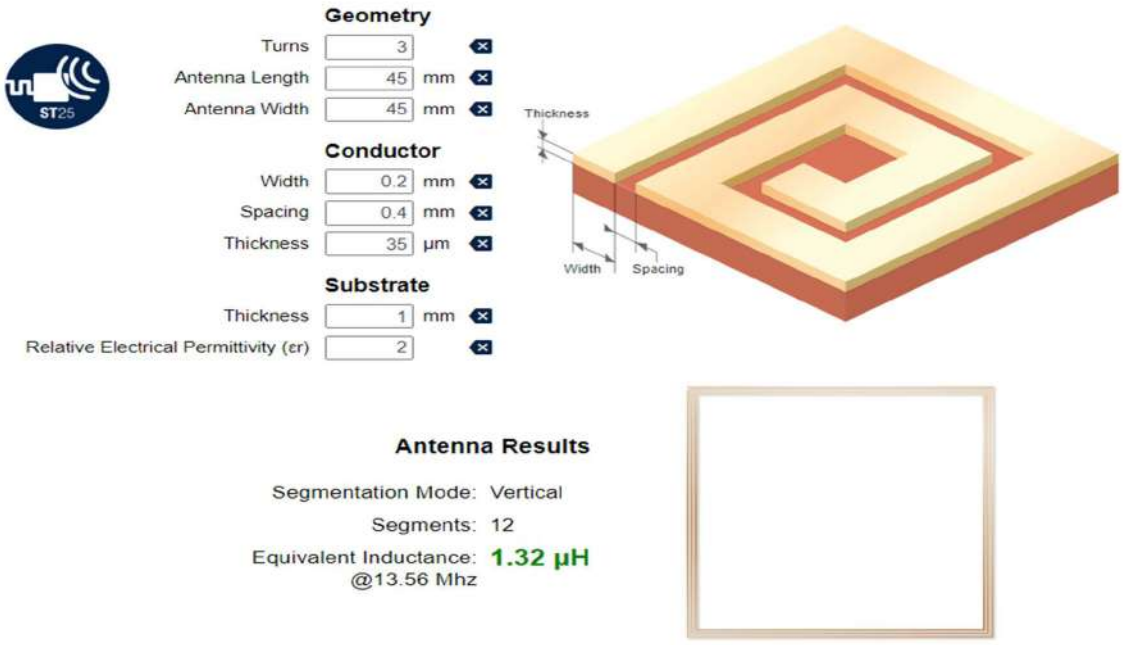


Fig 5.2: Rectangular Patch Antenna

The Table 5.2 shows the dimensions of the antenna. The effectiveness of two way read/write operations for wider range of detection distance is maximized with rectangular patch antenna.

Table 5.2: Antenna Dimensions

Parameters	Symbols	Values
Antenna Length	a_o	45mm
Antenna Width	b_o	45mm
Track thickness	t	35µm
Track width	w	200µm
Track gap	g	400µm
No. of turns	N_a	3

5.2 Implementation

The code implementation of the low power mode operation of NFC system and the low power mode validation test framework is discussed in this section.

5.2.1 Low Power Mode Operation of NFC System

The development and implementation of the low power mode operation of NFC system is carried out in the Eclipse IDE tool. The NFC reader IC flash memory is classified into Secure and Non-Secure regions as shown in Fig 5.3. The reader IC allows the end user to create own application in Non-Secure region.

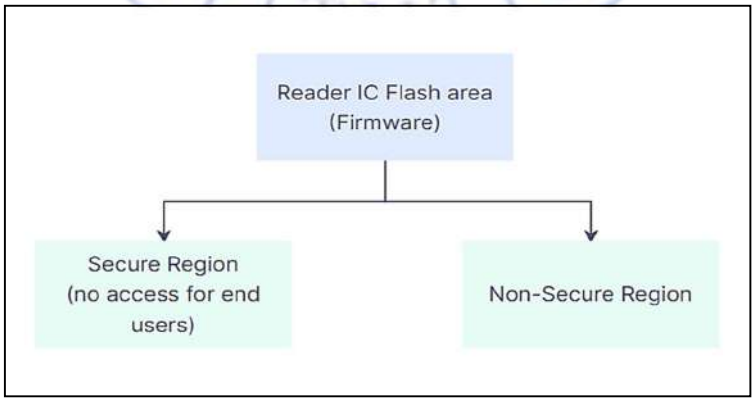


Fig 5.3: Reader Flash Area

An application to operate the NFC reader IC in low power mode is developed using a C language code. The code flow of the application is shown in Fig 5.4.

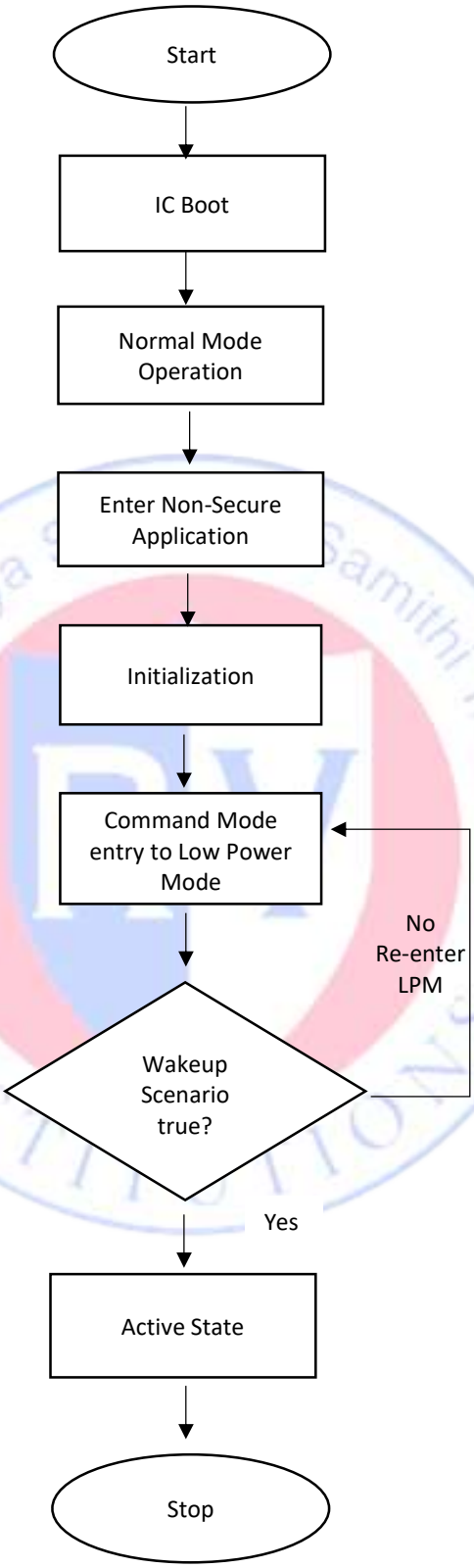


Fig 5.4: Code Flow of Non-Secure Application

The Non-Secure application is flashed on to the reader IC via a Serial Wire Debug (SWD) interface. After the application is flashed the reader IC, the NFC reader boots up and it enters into normal mode operation. The reader IC then enters the Non-Secure application that initializes power and clock unit. The reader IC then enters the Low Power Mode via a software command. During the low power mode the current consumption of the reader IC is reduced due to which it consumes less power. For example, the reader IC enters Standby mode and wakes up after the expiry of pre-defined timer count value. Once the reader wakes up from low power mode it enters active state in which the reader IC is fully functional.

5.2.2 Test Implementation Flow

The test framework for low power modes involve two parts: .cpp side and .c side. The .cpp side take care of the communication between device host i.e Personal Computer and the Device Under Test (DUT) via commands. The commands the .cpp side send include the test group ID, test ID and response buffer. The commands are mapped to corresponding test group on .c side via a dispatcher application. The test flow is shown in Fig.5.5.

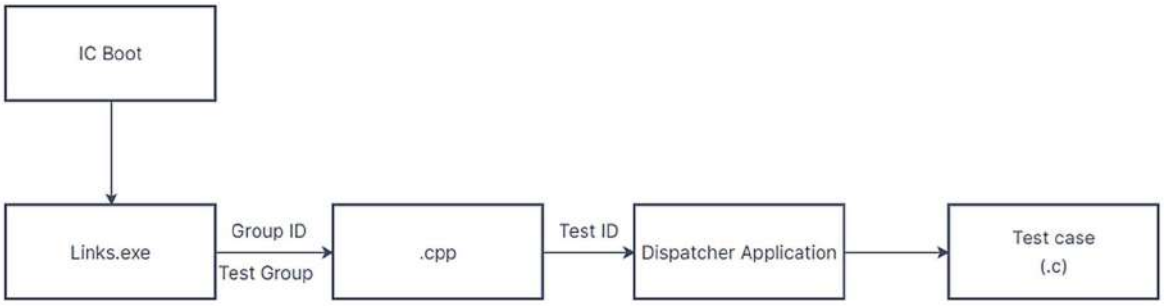


Fig 5.5: Test Flow

5.3 Summary

The NFC System was developed and implemented in Eclipse IDE tool. The NFC system developed include command-based entry to the low power mode. The simulations of the Flyback converter are carried out in the PSIM environment.

CHAPTER 6

RESULTS AND DISCUSSION

This chapter discusses about the conclusion made out of the proposed work. Also discusses about the future scope of the project work of the simulation and hardware results of the NFC system development and validation. Also discusses the results obtained in the simulation of the Flyback circuit incorporated in the power supply unit of the NFC system.

6.1 Hardware Results

The results of Non-Secure application with commanded entry to Low Power Mode is shown in Fig.6.1. The Fig.6.1 shows the RTT viewer of the Jlink-Debugger, it is used as a console for user interactions. The Non-Secure application is expecting an user input to choose the low power mode and the corresponding wake-up source.

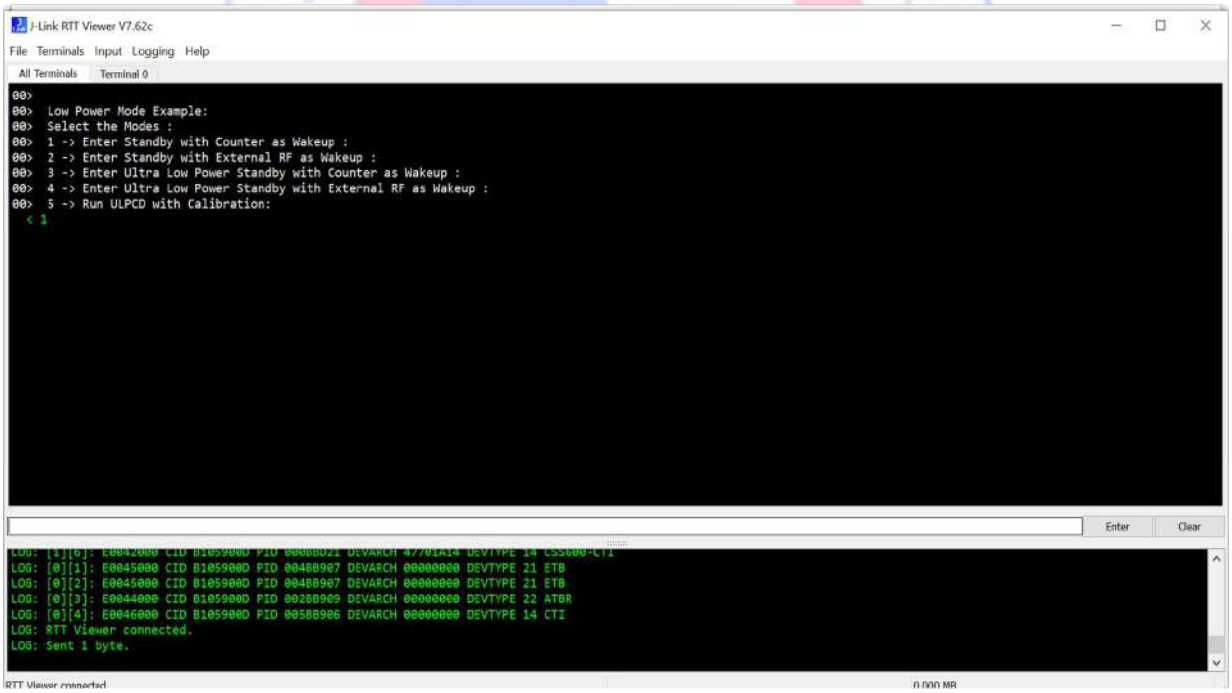


Fig 6.1: RTT viewer output of Non-Secure Application - 1

The user input ‘1’ in the RTT viewer corresponds to the Standby mode entry of the reader IC with wake up as counter expiry. The input ‘1’ will trigger the reader IC to enter Standby and the reader wakes up after a predefined counter expiry. After the reader IC wakes up IC boots up and prints the boot reason on the RTT viewer. The boot reason indicates whether the reader has

entered the active state due to the expiry of counter or any other scenario. The console after the wake up of reader from low power mode is shown in Fig.6.2. In the Fig.6.2 we can observe the reason for the reader boot. The Boot reason is obtained from a 32 bit register where each bit in the register corresponds to a different wakeup scenario.

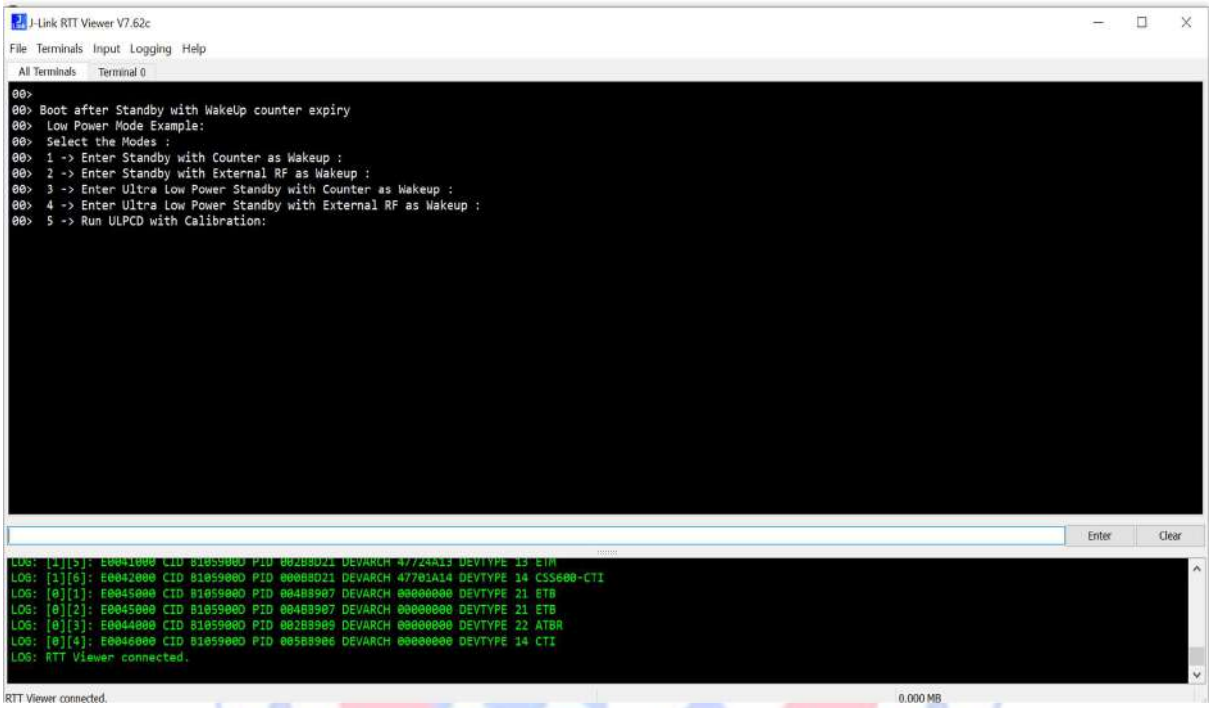


Fig 6.2: RTT viewer output of Non-Secure Application - 2

6.2 Simulation Results

The simulation results of the flyback converter and low power mode validation are discussed in this section.

6.2.1 Validation Results

The low power modes and clock sources of NFC reader IC is validated using RTL simulation tool. The RTL simulation tool allows signal level testing, the signal pads of the reader IC is pulled out to check its contents. The tests for validating low power modes are written using C language and C++ language.

The RTL logs of the standby mode entry with counter expiry as wakeup source is shown in Fig.6.3. Here we can see the general-purpose registers have some values, that is used to keep track of the flow. In the Fig 6.3 we can also see the boot sequence followed by the entry to dispatcher. The program counter waits in the dispatcher until it receives command containing the test case ID, that is sent by the .cpp side of the test. Once the test ID is received the program counter enters the corresponding .c side of the test, that contains the command to enter the standby mode. The reader simulation model enters the standby mode and stays there for predefined time interval. Once the reader wakes up, the IC boot sequence occurs and we can see that the boot_wuc signal is set high. The boot_wuc signal indicates that the reader exits standby mode and enters active mode due to the expiry of counter. The signal prev_wuc in Fig.6.3 indicates whether the entry to standby mode is prevented or not.

Fig 6.3: Standby Mode Output

The Fig.6.4 depicts the simulation waveforms of the suspend mode. The wake up scenario here is the external RF field. After the entry of the reader to suspend mode, it wakes up only when external RF field is detected by the reader. The signal TX1 in Fig.6.4 indicates the external RF and the signal boot_lpdet signal indicates that the reader exits suspend mode due to the detection of external RF field.

Fig 6.4: Suspend Mode Output

The RTL logs for the validation of the HFO clock source is shown in Fig.6.5. The frequency of HFO clock source is set to 45MHz, the same was verified on the RTL simulation tool.

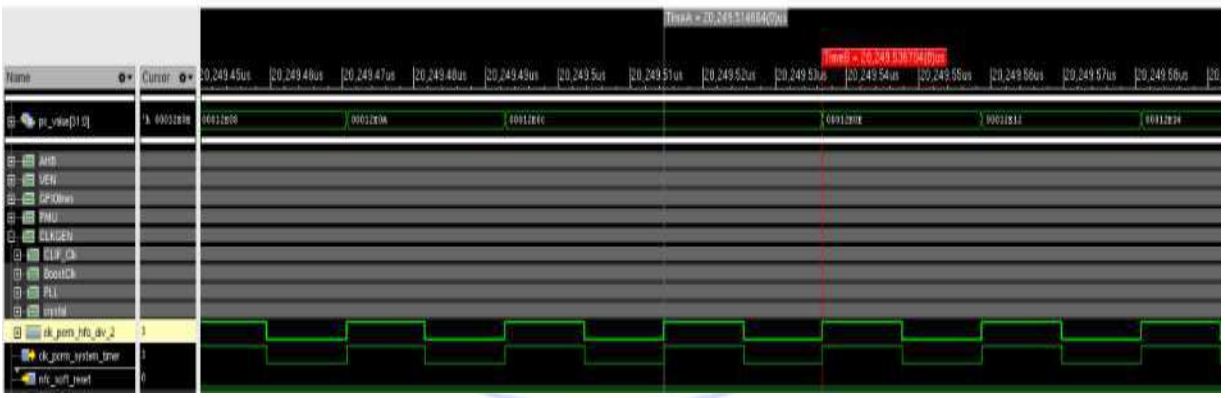


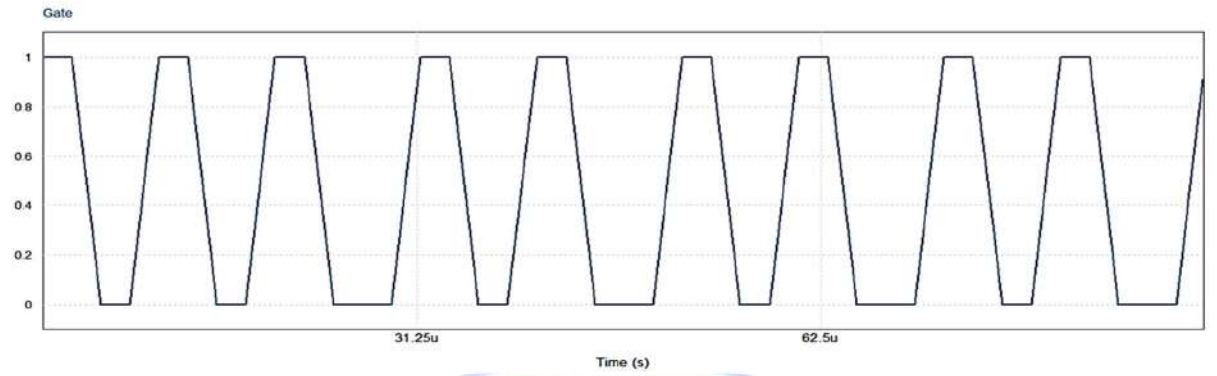
Fig 6.5: HFO clock Output

6.2.2 Flyback Converter Simulation results

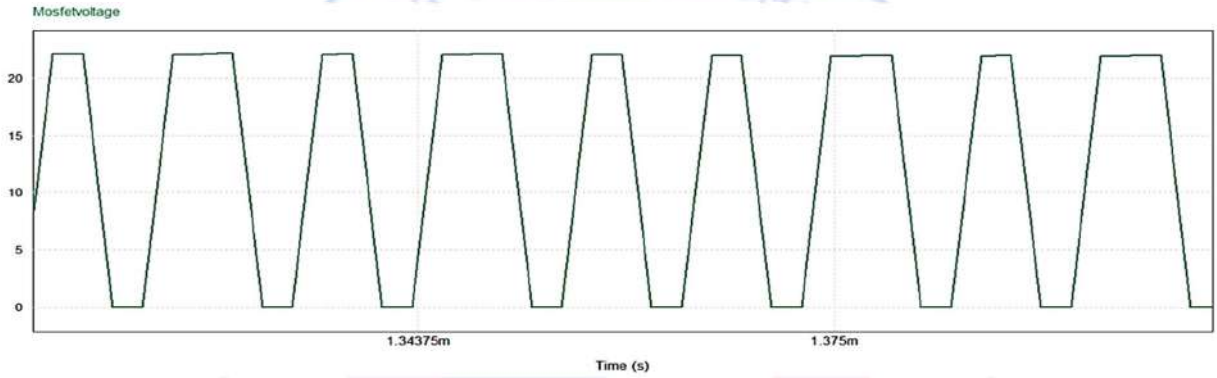
The simulation circuits are discussed in chapter 5, and results corresponding to it are included in this section. The switching pattern of all the switches in the flyback converter is shown in Fig.6.6.

The Fig.6.6 (a) shows the gate pulse given to the Mosfet in the primary side of the converter. The gate pulse of 100KHz and 0.45 conduction is shown in the Fig.6.6 (a). The Fig.6.6

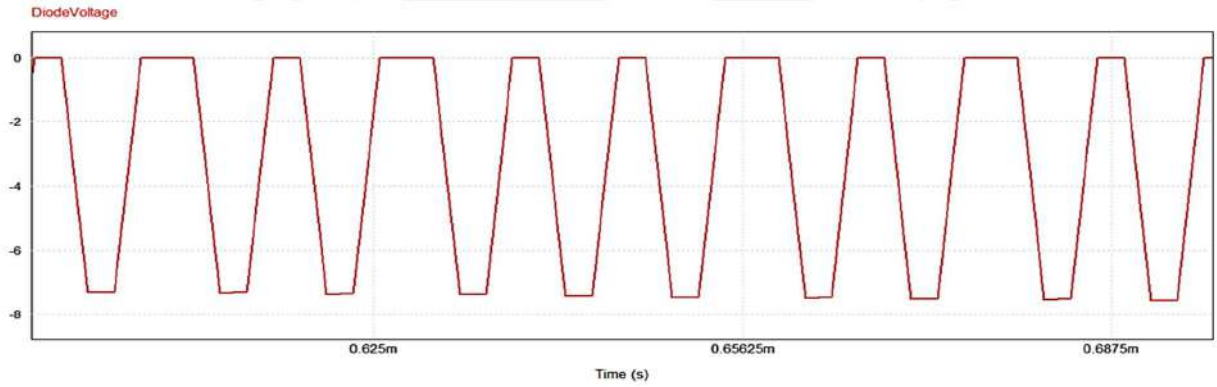
(b) shows the waveform of the voltage across the Mosfet. The Fig.6.6 (c) shows the voltage across the diode present in the secondary side of the converter.



(a)



(b)



(c)

Fig 6.6: Switching Pattern of switches

The waveforms generated by the designed flyback converter are shown below. The Fig.6.7 depicts the waveform of 3.3V output voltage obtained by the designed converter circuit. The

Fig.6.8 depicts the waveform of 0.1A output current obtained by the designed flyback converter circuit.

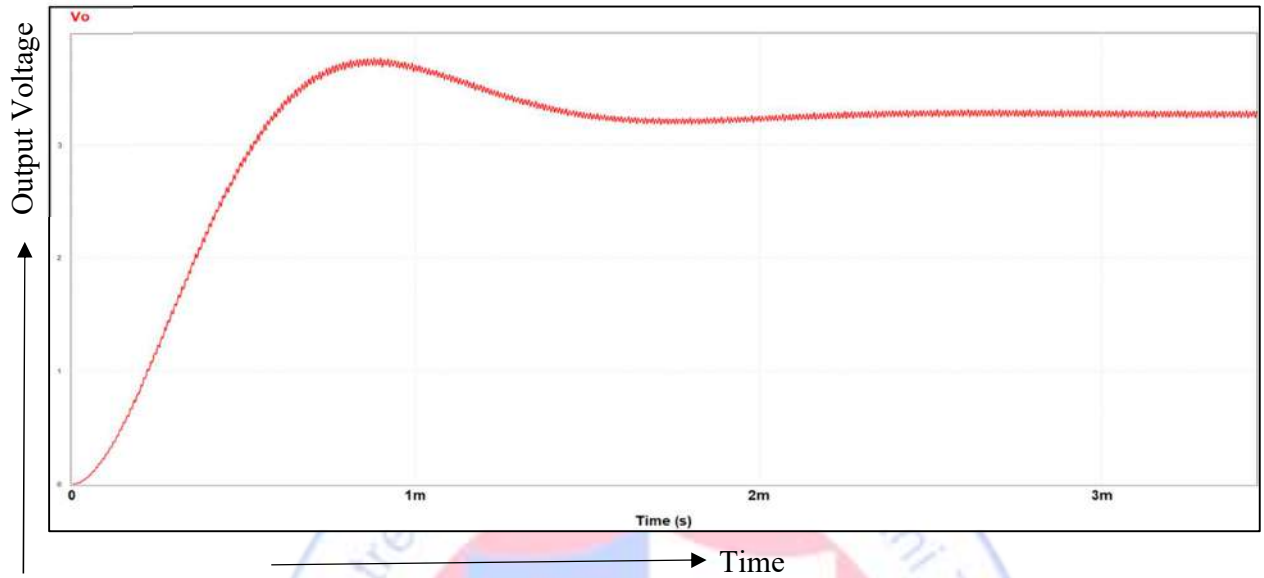


Fig 6.7: Output Voltage

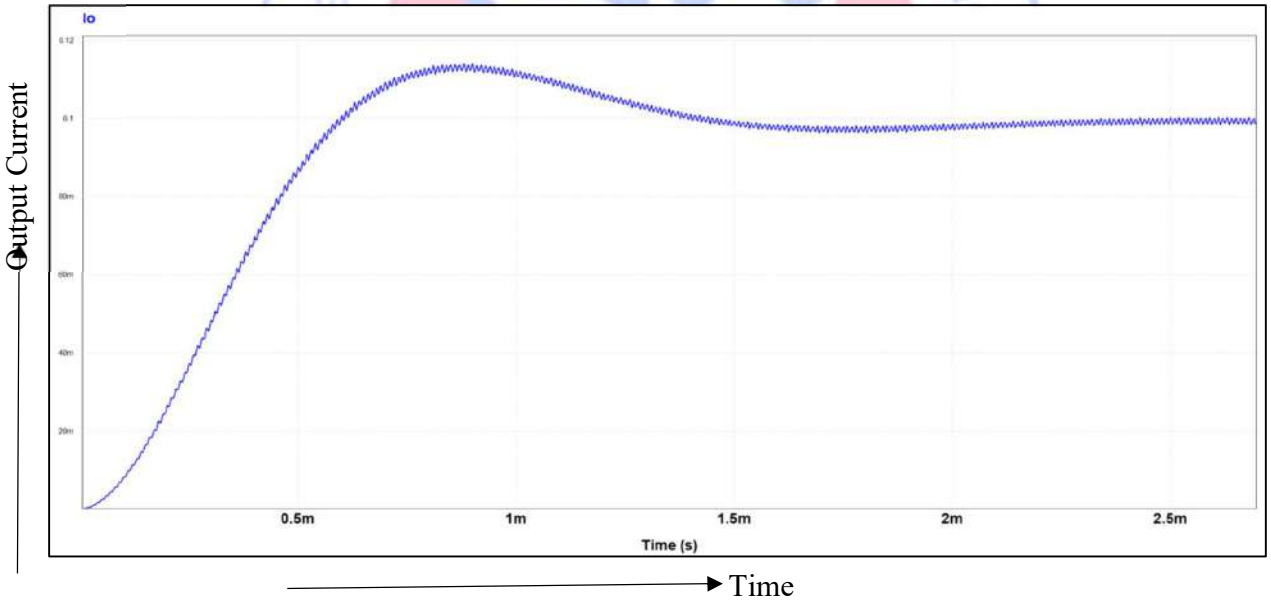


Fig 6.8: Output Current

6.3 Summary

The Hardware results of the NFC reader operating in low power mode was discussed. The simulation results of the validation of NFC Low power modes and clock sources were discussed. Also the simulation results of the flyback converter was discussed and the converter achieved an output voltage of 3.3V and output current of 0.1A.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

This chapter discusses about the conclusions made from the work carried out. Also discusses about the future scope of the proposed work.

Near Field Communication (NFC) is a wireless standard for data transmission within a short-range at high frequency based on Inductive coupling. NFC technology has evolved from existing Radio-frequency Identification (RFID) technology. NFC technology is opted when there is a need to transfer data immediately and fast. NFC technology is just not an interface to exchange data but also provides a way to transfer energy to the communication partner called the transponder. Communication with passive transponder increased the average power consumption of the system consisting of NFC Reader, Wireless communication channel and a transponder.

7.1 Conclusion

An NFC system design has been proposed that operates in low power mode to minimize the power consumption, it included an antenna operating at 13.56MHz. A rectangular antenna with inductance of 1.2837µH has been designed. A test framework was developed with 45 tests to validate the low power modes of reader IC for different wakeup sources. The power supply unit of the proposed NFC system incorporated a flyback converter. The flyback converter design was presented and simulated in PSIM tool to obtain an output of 3.3V with output current 0.1A from supply of 12V. The switch in the flyback converter conducted for 0.45 duty ratio.

The flyback converter is a viable choice for use cases requiring low voltage and power such as a portable device. The credit payments, data transfer, access control and vending machines are the various use cases of the proposed NFC system.

7.2 Future Scope

- The proposed NFC system technology can be made complementary to other wireless technologies like Wi-Fi, Bluetooth etc. to increase the data transmission range and minimize the power consumed while establishing connection between two devices.
- The Flyback converter can be further studied to design an closed loop flyback converter for low power applications.

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APPENDIX A

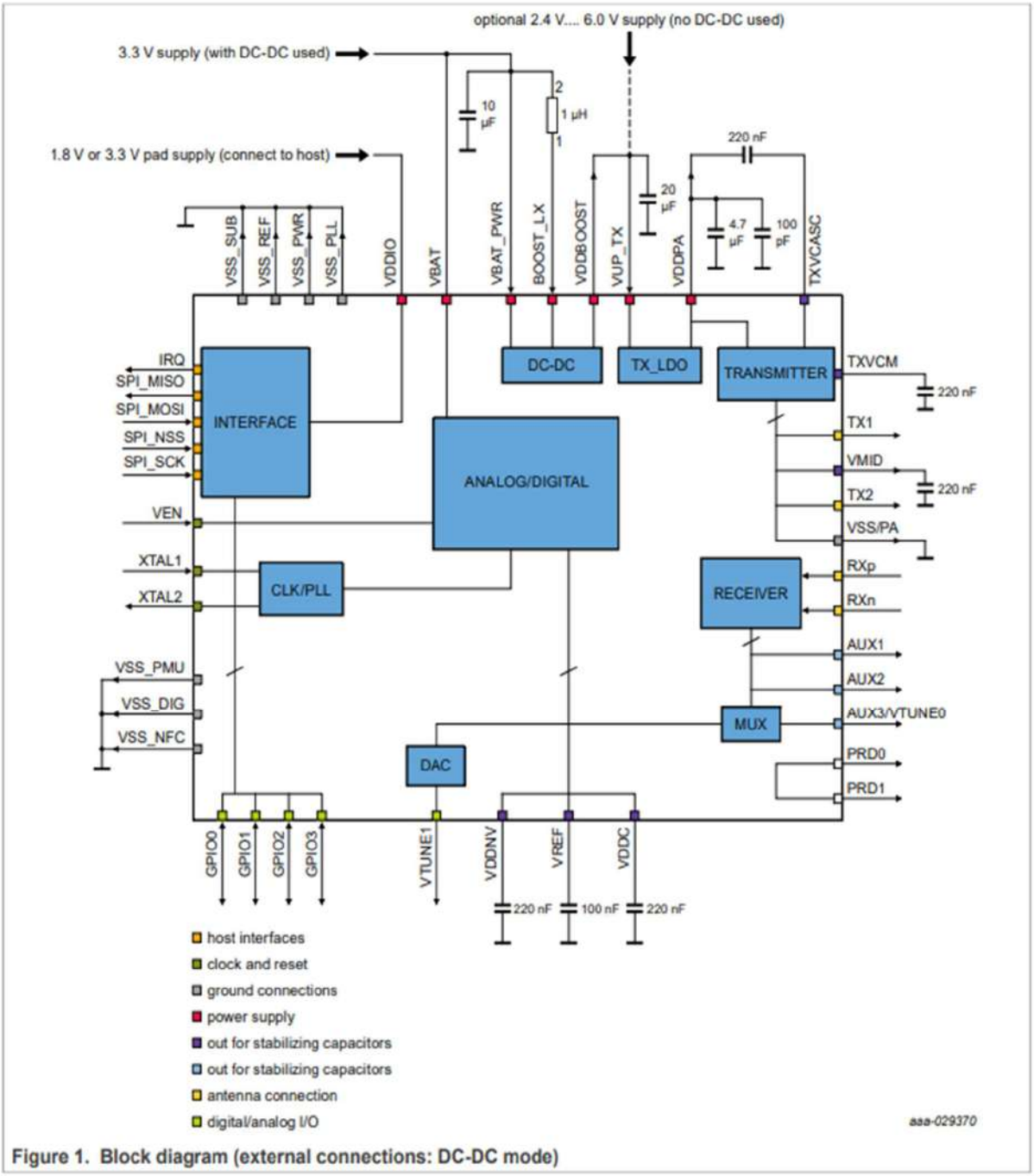
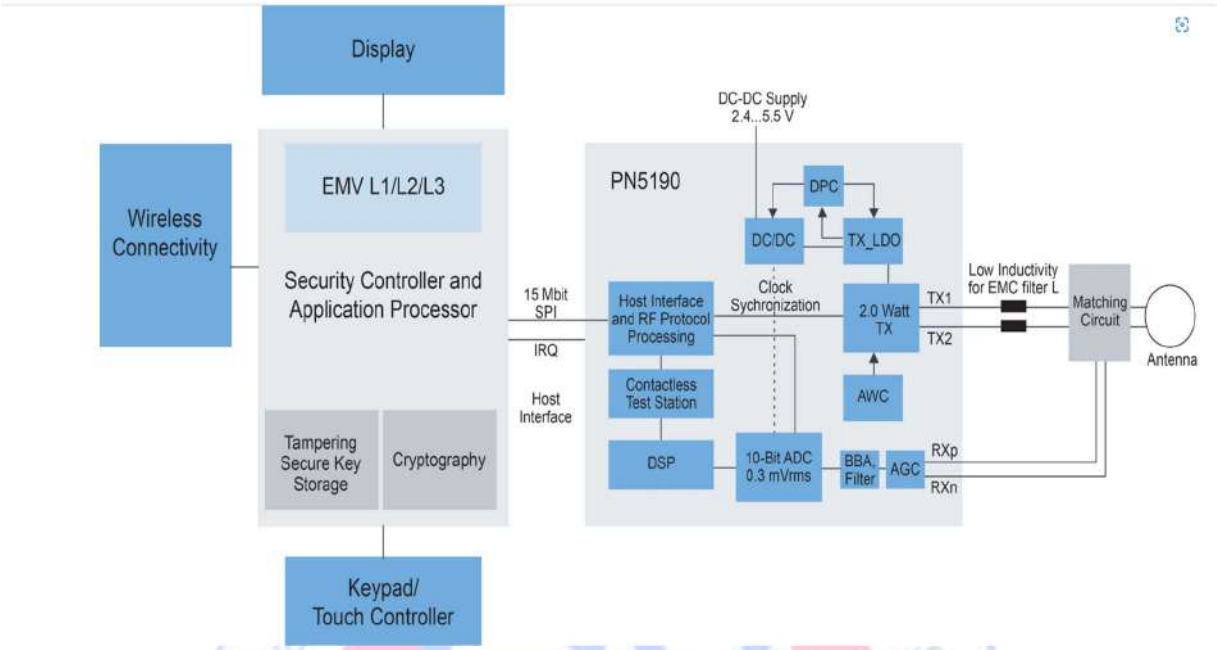


Figure 1. Block diagram (external connections: DC-DC mode)

PN5190 System Block Diagram



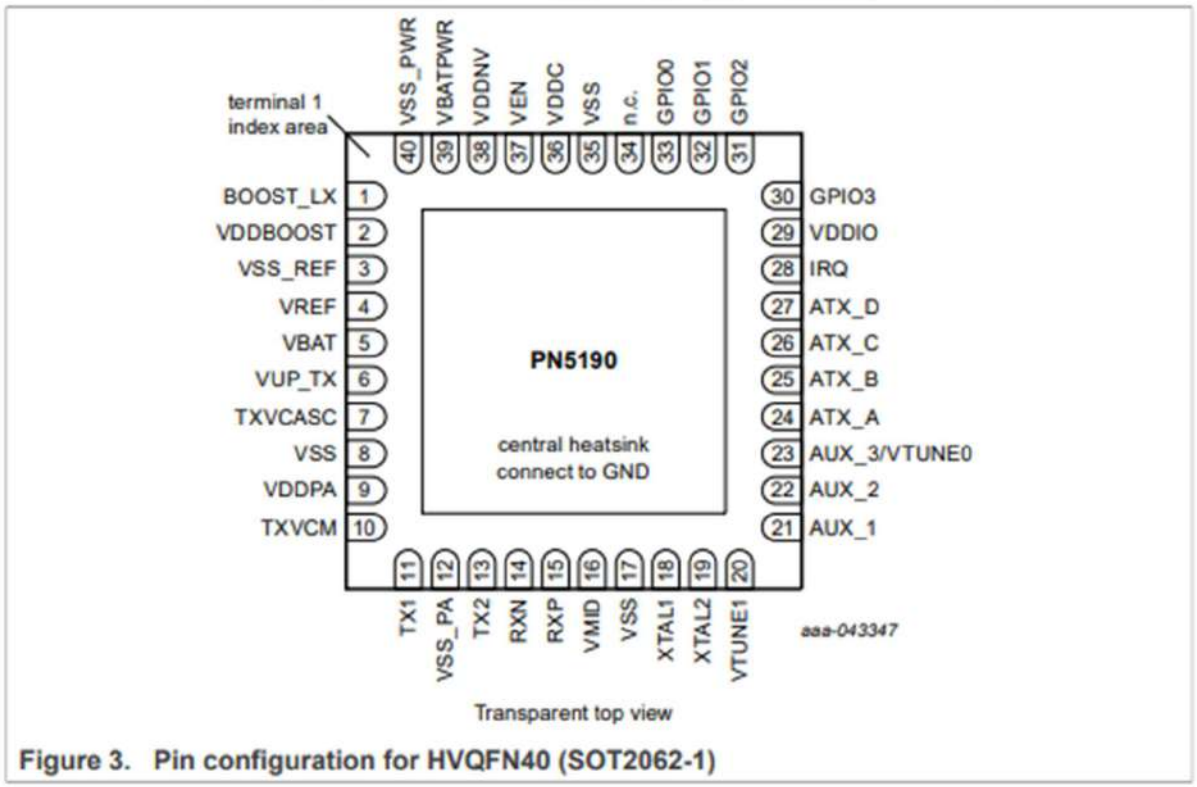


Figure 3. Pin configuration for HVQFN40 (SOT2062-1)

Design, Development and Validation of NFC system for Low Power Applications
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OBJECTIVE
Design of NFC system to operate in low power mode to reduce the current drawn using Eclipse IDE tool.
Proposing antenna and flyback converter design for the NFC system.
Validating the power modes and clock source of the NFC reader IC using RTL tool.
Project Methodology
The tag and a reader in the NFC system have radio frequency communication between them. Each tag consists of unique identification number and an antenna. The NFC reader will use unique identification number of the tag to establish communication. The reader IC is customized to operate in Standby low power mode to minimize current consumption via a software command. The NFC reader comprises of an antenna which is chosen to be rectangular patch antenna. The main issue in the design of the NFC system is the antenna alignment with the reader.
System Block Diagram
Power Modes
Flow Chart :
Functional requirement specification
Design of NFC system (Antenna design and converter design)
Code Implementation (Low power mode applications)
Validation (on real IC and RTL)
Code Flow :
Start
IC Boot
Normal Operation
Enters Non Secure Application
Test design Flow : Validation of low power modes is done using RTL simulation tool. The input to RTL simulation are files generated by the build of the project.
Test specifications
Test Bench
Test execution
Results
Rectangular Patch antenna
Flyback converter
Parameter
Value
Load Resistor, R
1.2Ω
Inductor, L
2.7mH
Capacitor, C
37.5μF
Results and Discussions
Output voltage
Output current
Parameter
Expected Value
Achieved Value
3-3V
3.294V
0.1A
0.099A
Conclusion
An NFC system design has been proposed, which incorporates an antenna operating at 13.56MHz.
A rectangular antenna with inductance of 1.2857μH has been designed.
A flyback converter design is presented and simulated in PSIM tool to step down voltage from 12V to 3.3V with output current 0.1A. The design conducts for 45% duty cycle.
The flyback converter is a viable choice for low power applications such as portable devices having low voltage requirement.
The proposed NFC system finds its application in credit payments, data transfer, access control and vending machines.
Future scope
The proposed NFC system technology can be made complementary to other wireless technologies like Wi-Fi, Bluetooth etc. to increase the data transmission range and minimize the power consumed while establishing connection between two devices.
The Flyback converter can be further studied to design an closed loop flyback converter for low power applications.
Guide Information: Dr. S G Srivani, Professor and PG Dean (Associate), Dept of EEE, RVCE, e-mail: srivanisg@rvce.edu.in
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I deeply express my sincere gratitude to my guide Dr. S G Srivani, Professor & PG Dean (Associate), Principal, HOD, & Panel members, Dept of EEE, RVCE.
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Design of NFC System for Low Power Applications

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Abstract - *Near Field Communication (NFC) is a short-range wireless standard used in data exchange and transaction applications. The NFC standard establishes the connectivity with counterpart with a touch. The NFC technology is evolved from the existing contactless identification and interconnection technologies. This paper presents an NFC system design using NXP PN5190 reader IC. An antenna with symmetrical matching is designed for 13.56 megahertz. The NFC system is designed to operate in Low Power Mode to minimize the current and power utilization. A Flyback converter present in power supply unit of NFC system is designed to operate for low power applications. The Flyback converter achieves an output voltage and output current of 3.3V and 0.1A respectively from the input supply of 12V. The NFC system designed finds its application in access control, point-of-sale (POS) and Internet-of-things (IOT).*

Key Words: **Near Field Communication (NFC), Low Power Mode, proximity, Radio-frequency Identification (RFID), Load Modulation, Rectangular Antenna**

1. INTRODUCTION

Near Field Communication (NFC) is a wireless standard for data transmission within a short-range at high frequency based on Inductive coupling. This technology has evolved from existing Radio-frequency Identification (RFID) technology. This technology is opted when there is a need to transfer data immediately and fast. The basic principle of operation is "touch to communicate" which indicates that bringing NFC enabled devices in close proximity to each other establishes connection for data transmission. The transmission range of the NFC standard is close to 10cm and frequency of operation is 13.56 megahertz. The rate of data transmission offered by NFC is in the range of 106 Kbit/s to 424 Kbit/s [1]-[8].

The NFC comprises of a poller and at least one listener. The poller/initiator has the ability to power up the passive listener/target device by generating RF field actively. The NFC technology allows an NFC enabled device such as mobile to accept data from a tag that is in close proximity to the poller. The NFC passive tag consists of a silicon chip and an antenna. The passive tag does not contain an internal power source rather it makes use of the RF field generated by the reader to power up its inner circuitry. The average power consumption of the NFC system is increased due to reading of such passive tag [1]-[8].

NFC is just not an interface to exchange data but also provides a way to transfer energy to the communication partner called the transponder. Communication with such transponder increases the average power consumption of the system consisting of NFC Reader, Wireless communication channel and a transponder. The NFC finds its application in lock/unlock and ignite car, payments, transportation, door access etc.

The integration of NFC into devices has the drawback of increasing the device's energy consumption. Especially when the NFC Reader is a smart phone, during the reading process the average power consumption of NFC-Reader increases by up to 107%.

Using NFC systems for applications like wireless payment, it is mandatory to add security. All the weak spots must be secure to prevent attackers from gaining unauthorized access to the system. To secure the wireless transmission, encryption algorithms like Advanced Encryption standard (AES) can be used. The usage of such algorithms leads to an increased energy consumption during transmission.

2. THEORY

2.1 Near Field Communication (NFC)

Radio Frequency Identification (RFID) technology incorporates wireless radio communication technology for unique identification. Both NFC and RFID work on same principle of inductive coupling at 13.56 megahertz. NFC technology has shorter transmission range of 4cm to 10cm compared to RFID range of 100cm. NFC technology provides communication solution to non.....-self-powered device (passive). The NFC technology can be complementary to other wireless technologies like Wi-Fi, Bluetooth etc. to increase the data transmission range. The main advantage of NFC is the ability to save energy. Currently various devices like smart phone and smart wearables are equipped with NFC feature for use cases like data transfer between two devices and mobile payments. The smart phone applications like Samsung Pay and Google Pay facilitates contactless payment feature. NFC finds its use case in Transportation access, like in the public Metro transport ticketing where the coin has NFC tag incorporated in it [1]. The figure 1 gives an overview of NFC Domain.

The three operating modes of NFC are shown in figure 1, namely read/write mode, peer-to-peer mode and card

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emulation mode. The Card Emulation Mode consists of an active NFC reader and a Passive NFC card in the communication setup. The NFC reader reads the information stored in the passive tag. In Read/Write Mode the NFC enabled device can read data from tag or writes information to the NFC tag. The NFC tag is powered by the magnetic field and sends response to the request. In Peer-to Peer Mode two NFC enabled devices communicate with each other. The Peer-to-Peer mode enables devices to connect and interact with each other to exchange data, money transfer and social networking.

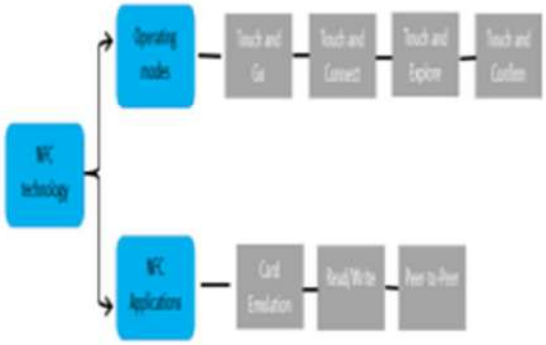

Fig -1: NFC Domain

The basic NFC System is shown in figure 2. The NFC system consists mainly of three components – a Tag, a Reader and a Controller. A Tag, also called a pulse transceiver consists of a semiconductor chip and an antenna. An electronic control module, RF module and an antenna is present in the reader device. A controller component of the NFC system is usually a PC [1].

NFC communication establishment involves three activities –

- Power transfer for communication by RF field of the NFC Reader.
- Modulation of the field.
- Load Modulation of the field.

Fig -2: NFC System

2.2 Power Management in Embedded System

The critical issue in embedded devices is the power utilization due to which there is a need for extended battery life. The two scenarios in which systems power consumption can be considered are when the system is in use and when the system is in idle state. The solution to this problem is the deployment of the low power CPU modes. The power management in embedded systems can be achieved either by firmware power management or peripheral power down.

- *Firmware Power management* – The two measures firmware can into consideration to keep the power utilization minimum are to switch off the system peripherals when it is not in use and to regulate the voltage and frequency of the CPU based on the performance needs.
- *Peripheral Power Down* – The very common approach to save energy in embedded system is to switch it off. The complete system turn off when not in use is not recommended because a fully powered down device may take some time to start up. So, the embedded system should be designed such a way that the peripherals and subsystems may be turned on or off by firmware temporarily. Therefore, an alternate to the system power down is the low power modes.

The proposed NFC reader include low voltage power domains into their architecture and offer when it is associated with power modes, embedded power states. The low power mode of operation to reduce the energy consumption is chosen by a command in application running on the system [2].

3. SYSTEM DESIGN

The Block diagram of the NFC System proposed is shown in figure 3.

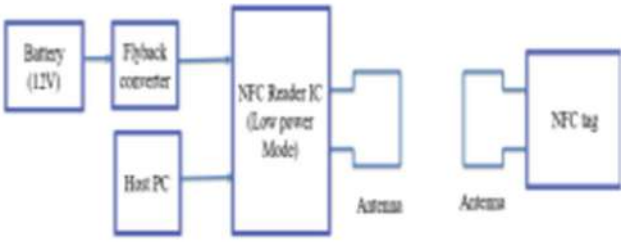

Fig -3: Block Diagram

The tag and a reader in the NFC system have radio frequency communication between them. Each tag consists of unique identification number and an antenna. The NFC Reader will use unique identification number of the tag to

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establish communication. The read distance of the NFC reader dependent on the antenna parameters such as the shape, size, frequency etc., surrounding environment and others [1].

The NFC Reader communicates with host PC via host interfaces, which can be either of I2C, SPI, USB or serial UART. In the proposed system the Reader IC is considered to be PN5190 IC. The reader IC can be customized to operate in low power mode in order minimize current consumption via a software application flashed on to it. The various low power modes in which reader IC could operate are such as Standby mode, Suspend mode and ultra-low power card detection mode. The reader IC have several other features and interfaces accommodated in the chip to meet the requirements of different use cases. The NFC Reader comprises of an antenna which is chosen to be rectangular patch antenna. The main issue in the design of the NFC system is the antenna alignment with the reader [1].

3.1 Design of an Antenna

The choice of right antenna depends on the application requirements. In the process of choosing the right antenna there are trade offs between applications requiring maximum read distance (consumes large power) and applications with strict power budgets (results in short read range). The balance between the two extremes can be achieved with a blend of power efficiency and performance, which can be met with the latest high-performance readers featuring ultra-low power card detection. In the proposed system a rectangular antenna is chosen because it is a symmetrical antenna with equal power distribution. The bill of material and the number of components is reduced. The figure 4 gives an example of rectangular antenna and dimensions. The inductance of antenna can be calculated using following formulas:

$$L_a = \frac{\mu_0}{\pi} \cdot [x_1 + x_2 - x_3 + x_4] \cdot N_a^{1.8} \quad (1)$$

$$d = \frac{2(t+w)}{\pi} \quad (2)$$

$$a_{avg} = a_0 - N_a(g + w) \quad (3)$$

$$b_{avg} = b_0 - N_a(g + w) \quad (4)$$

$$x_1 = a_{avg} \cdot \ln\left[\frac{2a_{avg}b_{avg}}{d\left(a_{avg} + \sqrt{a_{avg}^2 + b_{avg}^2}\right)}\right] \quad (5)$$

$$x_2 = b_{avg} \cdot \ln\left[\frac{2a_{avg}b_{avg}}{d\left(a_{avg} + \sqrt{a_{avg}^2 + b_{avg}^2}\right)}\right] \quad (6)$$

$$x_3 = 2[a_{avg} + b_{avg} - \sqrt{a_{avg}^2 + b_{avg}^2}] \quad (7)$$

$$x_4 = \frac{a_{avg} + b_{avg}}{4} \quad (8)$$

where:

a_0 = length in mm

b_0 = width in mm

t = track thickness in mm

w = track thickness in mm

N_a = number of turns

The above-mentioned parameters are calculated to design an antenna for NFC reader. The antenna dimensions are a_0= 45mm, b_0= 45mm, N_a= 3, w = 200µm, g = 400µm, t = 35µm. The inductance value of an antenna obtained by the above-mentioned equations is 1.2837µH.

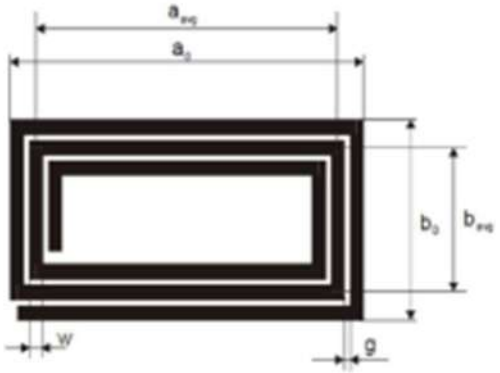

Fig -4: NFC Antenna

3.2 Converter Design

The power supply unit of the NFC system comprises of a battery of 12V and a flyback converter has been incorporated for DC-DC conversion. The flyback converter will step down the battery supply voltage to 5V/3.3V. The flyback converter is a DC-DC converter topology like boost converter having similar structure and performance. The converter stores energy when current flows using an inductor and supplies energy when the power is removed [9].

Flyback switch mode power supply is most commonly used SMPS circuit for low output power applications. The flyback converter has two operation phases: when the power from input side is being transferred to the output when the primary side switch is off and when the primary side switch is on and the output do not receive power from primary side. The basic flyback design has few low-cost material requirements just like the other dc-dc converters: the capacitor, the MOSFET as the primary switch, the diode as the secondary switch and inductor is being replaced by the

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flyback transformer or simply transformer [9]. The simple flyback converter circuitry is shown in Figure 5.

The necessary equations required for the design of the flyback converter are given below. The duty cycle calculation of the converter is required to determine the conduction ratio of the circuit The converter is designed for an output voltage of 3.3V from an input voltage of 12V. The duty cycle calculated from the below mentioned equation (9) is 45%.

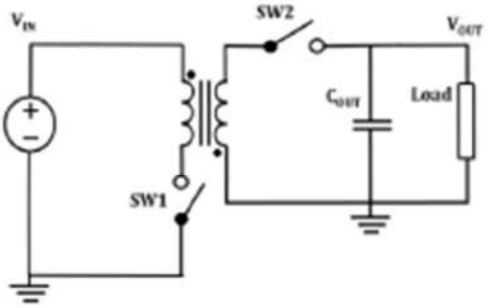

Fig -5: Simple Flyback converter

The transformer ratio N_1/N_2, in this design is set as 3.

$$\frac{N_2}{N_1} = \frac{V_0}{V_c}\left(\frac{1-D}{D}\right) \quad (9)$$

The load resistance R calculated with the output current of 0.1A in equation (10) is 33Ω.

$$R = \frac{V_0}{I_0} \quad (10)$$

In the converter design the switching frequency is taken as 100KHz with Imin as 0.06A. The value of inductance L calculated in (11) is 22.5mH.

$$L = V_{in}\frac{D}{\frac{2I_0}{1-D} - 2I_{min}f} \quad (11)$$

The computed value of capacitance C in (12) is 6.81μF.

$$C = \frac{DV_{in}}{8rV_0Lf^2} \quad (12)$$

The simulation circuit of flyback converter using PSIM tool is shown in Figure 6.

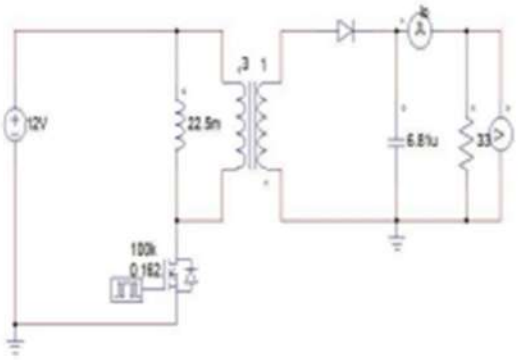

Fig -6: Flyback converter

The schematic of the flyback converter comprises of a MOSFET, which acts like a switch, a transformer, a diode operating complementarily to MOSFET, an inductor and a capacitor. The pulse generator module is used for the control of duty cycle of the circuit by turning on and off the MOSFET switch. The converter circuit components are positioned to achieve the desired output condition of 3.3V output voltage and 0.1A current.

The waveforms generated by the designed flyback converter are shown below. The figure 7 depicts the waveform of 3.3V output voltage obtained by the designed converter
circuit.

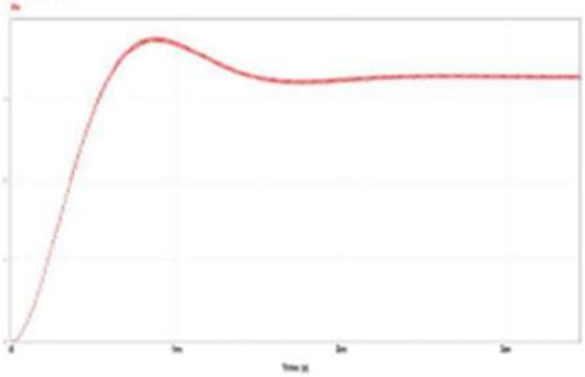

Fig -7: Output Voltage Waveform

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The output current of 0.1A waveform is as shown in Figure 8.

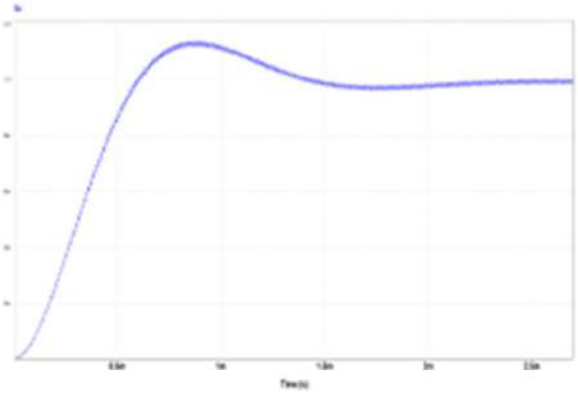

Fig -8: Output Current Waveform

4. CONCLUSION

An NFC system design has been proposed, which incorporates an antenna operating at 13.56MHz. A rectangular antenna with inductance of 1.2837µH has been designed. The power supply unit of the proposed NFC system incorporated a flyback converter. The flyback converter design is presented and simulated in PSIM tool to obtain an output of 3.3V with output current 0.1A from supply of 12V. The switch in the flyback converter conducts for 0.45 duty ratio. The flyback converter is a viable choice for use cases requiring low voltage and power such as a portable device. The credit payments, data transfer, access control and vending machines are the various use cases of the proposed NFC system.

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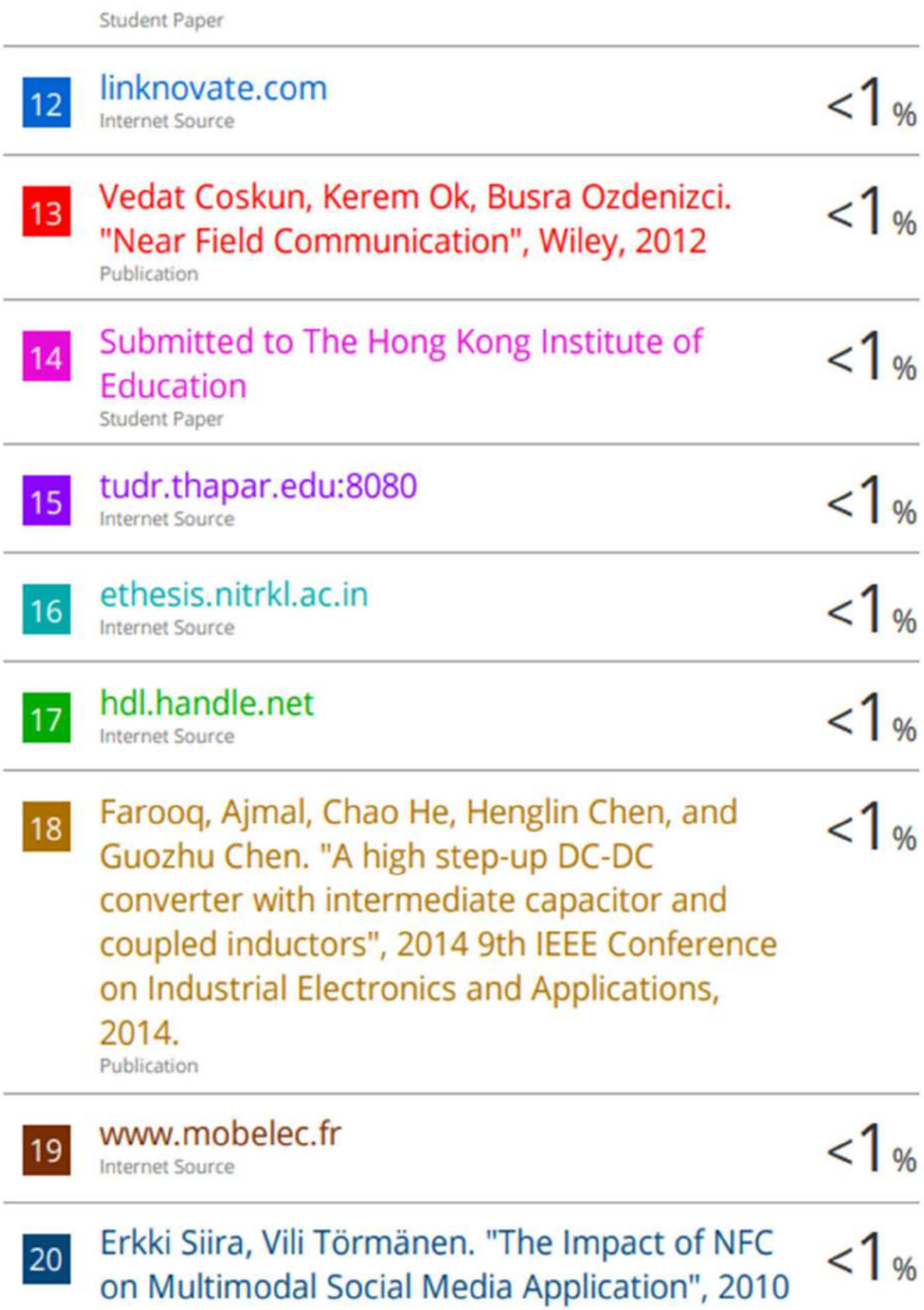

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Major Project: Phase-II Report

on

SIMULATION, TESTING AND DIAGNOSIS OF UREA TANK LEVEL DETECTION IN DIESEL ENGINE VEHICLES

18MPE41

Submitted by

KAVYASHREE A

USN: 1RV20EPE05

Under the Guidance

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Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY

in

POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

2021-22

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Certified that the project work titled **"Simulation, Testing and Diagnosis of Urea Tank Level Detection in Diesel Engine Vehicles"** carried out by **Kavyashree A. USN:1RV20EPE05**, a bonafide student of **RV College of Engineering®, Bengaluru** in partial fulfillment for the award of **Master of Technology** in **Power Electronics** of **R V College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi,** during the year **2021-22**.It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

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Power Electronics

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ABSTRACT

Exhaust emission control from internal combustion engines have become one of the most important challenges. It causes breathing problems, headache, chronically reduced lung function, eye irritation, loss of appetite and corroded teeth. Indirectly, it can affect humans by damaging the ecosystems they rely on in water and on land. Control of emission in internal combustion engines can be achieved either by controlling combustion or by treating the exhaust gas temperature. The latter is comparatively easier since there is less or no need to modify the engine itself. This project focuses on the modification of existing engine control unit for enhancing exhaust emissions and hence to improve drive ability. Also enhancement of the existing functional component in exhaust system is done to overcome the customer issues and automated testing is done.

Scramble of aqueous urea solution is mixed into the exhaust gas which acts as an impacting solution for removing SO_2 and NOx. The aqueous urea breaks into ammonia and carbon dioxide. The ammonia acts in response with NOx to create inoffensive nitrogen gas and water vapor. The urea a downgraded cause in SCR technology has been fully applied productively. It is used in stationary and to mobile diesel engines in ships and loco exclusively. The proposed method gives an outstanding result of a reduction in emissions and the reduction in efficiency of the engine is insignificant. The proposed method is a fully developed after treatment process based on the injection of urea in the upstream of the exhaust gas. The urea in SCR system will be developed to meet the demand for low NOx emissions without compromising the engine efficiency from the existing diesel vehicles

Simulation, diagnosis and testing of urea tank placed in diesel engine vehicles for certain specific required conditions is performed in ASCET ,ECU Worx, Continuous Integration Dashboard and TPT software packages. The urea spray a downgraded cause in SCR technology has been fully applied productively. It is used in stationary and to mobile diesel engines in ships exclusively. This method gives an outstanding result of a reduction in emissions and improving the efficiency.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Kavyashree A, Dr. Dinesh M N "Simulation and Testing of Urea Tank Level Detection in Diesel Engine Vehicles", *International Research Journal of Emerging Technologies and Innovative Research (JETIR)*, ISSN: 2349-5162, Volume: 09, Issue: 06, June 2022

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GLOSSARY

ASCET	: Advanced Simulation and Control Engineering Tool
BSES	: Bharat Stage Emission Standards
CI	: Continuous Integration
DEF	: Diesel Exhaust fluid
DOC	: Diesel Oxidation Catalyst
DPF	: Diesel Particulate Filter
ECU	: Electronic Control Units
EGR	: Exhaust Gas Recirculation
IC	: Internal Combustion
N_2O	: Nitrous Oxide
NO	: Nitric Oxide
NO_2	: Nitrogen Dioxide
NOx	: Nitrogen Oxides
PM	: Particulate Matter
SCR	: Selective Catalytic Reduction
TPT	: Time Partial Testing

CHAPTER 1

INTRODUCTION

Nitrogen oxides are referred to as NOx. Although the majority also includes nitrous oxide (N_2O) in this description, purists would argue that it only refers to nitric oxide (NO) and nitrogen dioxide (NO_2). There are several other variations, but its atmospheric concentrations are insufficient. NOx emissions are caused by: High temperature fuel combustion, occur if a fuel is burned at a temperature hot enough (approximately 1300°C/2370°F) to oxidise some of the nitrogen in the air to NOx fumes. Burning hydrogen falls under this category since it burns at a high temperature; burning plant matter also produces nitrogen oxides because all plants contain nitrogen; and using nitric acid, nitrates, or nitrites in industrial or chemical processes also produce NOx.[1]-[6]

NOx gases are dangerous because; a) Nitrous oxide (N_2O) is defined as being 298 times as bad as CO_2 because of its radiative effect, and the duration required to break it down. For people who are lacking, the reaction with vitamin B12 could be problematic. It degrades in the stratospheric layer and aids in the ozone's decomposition rays and be absorbed by ozone in the upper atmosphere because they are dangerous if they reach the earth's surface; b) nitric oxide (NO), easily oxidizes in the atmosphere to nitrogen dioxide and is non-toxic in small amounts; and c) nitrogen dioxide (NO_2), a major pollutant and a main ingredient in smog. It produces nitric acid if it combines with water, it irritates the respiratory system and eyes so badly. [7]-13]

Today, there is no question that air pollution poses a serious threat to everyone's health. Nearly every nation is struggling with this issue. Over time, several nations modified technology and crisis management tactics in response to the threat posed by decreasing air quality. Environmental change because of a rise in global temperature has demonstrated the severity of the problem. In the United States, Europe, China, and many other places, problems with ozone and nitrogen oxides in the air are of great concern. [14]-[20]

The Indian government has established rules known as Bharat Stage Emission Standards to control pollution produced by both commercial and passenger cars (BSES). The table 1.1 provides information on the permitted emission levels for BS6 vehicles in comparison to BS4 vehicles:

Table 1.1: Comparison of permissible emission levels of BS6 and BS4 automobiles

Fuel Type	Pollutant Gas	BS6 (BSVI)	BS4 (BSIV)
Petroleum Distillate Vehicle	Nitrogen Oxide (NOx) Limit	60 mg	80mg
	Particulate Matter (PM) Limit	4.5 mg/km	-
Diesel Fuel Vehicle	Nitrogen Oxide (NOx) Limit	80 mg	250 mg
	Particulate Matter (PM) Limit	4.5 mg/km	25 mg
	HC + NOx	170 mg/km	300 mg

Table 1.1 clearly indicates the need of some technique to cut back emission of pollutant in diesel engines. By introducing Selective Catalytic Reduction (SCR) technique, higher efficiency and reduced emissions is obtained. A sophisticated active emissions management device called selective catalytic reduction (SCR) injects a liquid reductant into a diesel's exhaust stream via a unique catalyst. Diesel exhaust fluid, often known as automotive-grade urea, is occasionally used as the reducer supply (DEF). The DEF ignites a chemical reaction that transforms nitrogen oxides into nitrogen, water, and trace amounts of carbon dioxide (CO_2), are then ejected through the vehicle pipage.[21]-[26]

Today most of the transport vehicles in countries like India where value effective is that the predominant criteria utilize diesel engines instead of the gasoline engines. However, it's some disadvantage conjointly, like because of hot temperature in combustion chamber ends up in formation of NOx and material that is harmful to human likewise as atmosphere.[27]

An air and fuel mixture are fed into the combustion chamber of an internal combustion engine. Spark plug, an electrical gadget, is then used to compress and ignite this. In a diesel engine, air is pumped into the cylinder and compressed by roughly twice as much as it would be in a gasoline or extremely petrol engine. Once the fuel is injected, the heat produced by this compression causes it to spontaneously burn. Diesel fuel generates a lot of energy from a volume despite having a lower calorific value than gasoline or other fuels. [28]-[31]

NOx reduction activities occur in an oxidising atmosphere. It is referred to as "selective" because it reduces NOx levels by using ammonia as a reductant in a catalytic system.DEF is the chemical agent that performs the "reduction" process, is the chemical transformation of pollutants into elements, water, and trace amounts of greenhouse gases. The DEF is frequently quickly countermined in order to introduce oxidising ammonia to the exhaust stream. By itself, SCR technology cut NOx by up to 90%. In this paper, urea tanks in diesel cars that use chemical activity with urea and ammonia solution as an after-treatment technique to control emissions are simulated, designed, and tested. The remedy is carried out. [32]-[34]

1.1 Overview

Due to the superior fuel efficiency and lower greenhouse gas emissions compared to the gasoline counterparts, diesel engines have been the predominate power source for medium- and heavy-duty vehicle applications and have attracted an increasing amount of attention from the automotive industry in recent years. Diesel engines, however, often produce higher NOx emissions than gasoline engines because of its low burn nature. Three-way catalysts, have been utilized successfully in stoichiometric combustion engines, are unable to work efficiently with lean exhaust gases.

Recently, completely new aftertreatment systems for decreasing the pipe NOx emissions of automobiles powered by lean-burn engines have been proposed, spurred by the strict NOx emission standards around the world. One of these technologies, urea selective chemical process reduction, is among the most promising since it has the potential to reduce over 90% of NOx emissions from diesel engines. The SCR systems are favoured by automotive business in recent years. Thanks to its lower use-cost examination to different NOx reduction aftertreatments that need additional fuel as reducing agent for NOx reduction. Hence, within the projected work, the urea tank level detection in diesel engine vehicles, SCR technique is employed as a main regulation.

1.2 Literature Survey

SCR has been used to lower stationary source emissions for a long time. Additionally, cargo ships, ferries, and tugboats all around the world are outfitted with SCR technology. SCR is also acknowledged as the emissions control technology that is particularly helpful in meeting the U.S. EPA 2010 diesel engine emission standards for heavy-duty vehicles and the Tier 4

emissions standard for engines found in off-road equipment due to its superior return in both economic and environmental benefits. The increasing number of diesel passenger cars also use SCR systems [1]-[4].

Several research that employed laboratory setups to find fundamental SCR reactions have been published. However, the development of SCR catalysts is still ongoing, and different SCR catalyst formulas are found in current catalysts. The most commonly seen formulas are Vanadium, Fe-Zeolite, and Copper-Zeolite, and each has different ammonia adsorption/desorption/storage, NOx reduction, and oxidation characteristics. Besides, with different catalyst (geometry) designs, SCR systems present very different dynamics, e.g., urea mixer and catalyst inlet geometry designs have remarkable effects on urea to ammonia conversion. Additionally, there are comparatively few investigations of control-oriented models and experimental reports using real engine aftertreatment systems and on-board emissions sensors (commonly NOx and/or NH3 sensors) [5]-[8].

To ensure continuing operation of the vehicle or equipment, DEF is always present in the tank as it is a crucial component of the emissions control system. The driver or operator is alerted by a sequence of rising visual and audio signs if the DEF supply is low. The starting system may be locked out the following time the vehicle is used once the tank reaches a specific point close to empty, preventing the vehicle from being started without enough DEF. To accommodate the demands of a developing SCR technology industry, a national DEF distribution system has quickly grown. [9]-[11].

In passenger cars, DEF storage tanks are normally found beside the spare tire and in tractor trailers often include a DEF tank next to the saddle tank for diesel fuel. Most vehicle's DEF dispensing systems feature warming devices, and proper storage of DEF is necessary to prevent the liquid from freezing at temperatures lower than 12 degrees Fahrenheit. [12]-[15].

The urea dosing system's operating concept, then the system dynamic model is constructed, and the mechanical system design is displayed. In order to achieve this, a testing procedure is used to validate the suggested system control mechanism. A succession of simulation and experimental data are used to eventually present the new urea dosing system's performance. [16]-[18].

To assess the efficacy of the suggested control technique, simulations using the ECE driving cycle are run in the enDYNA diesel model. The benefit of the proposed triple-step

approach SCR control scheme is also demonstrated by comparisons with PID controller. [19][20].

1.3 Motivation

According to recent studies, outdoor fine particles and particulate matter pollution were responsible for 7.6% of all deaths (4.2 million people) worldwide in 2015.To reduce exhaust radiations, various pretreatment and posttreatment headways are adopted. Diesel engine exhaust emissions are a serious hazard to both the environment and public health. The only way to reduce these emissions is to apply pre-treatment and post-treatment procedures together. Engine changes such as combustion cylinder adjustments, injection time delays, exhaust gas recirculation, fuel injection system strategies, and others are examples of pre-treatment treatments.

The most challenging challenge in lowering risks is to reduce the NOx emission from diesel engine exhaust, but they are still insufficient to do so. There is evidence that exposure to ambient air pollution over time increases all-cause mortality. Numerous respiratory illnesses, including chronic obstructive pulmonary disease, asthma, pneumonia, and cancer, are brought on by air pollution and made worse by it. An excessive amount of NOx in the atmosphere results in a damaging downpour and the development of smoky clouds. The ozone layer, shielding the Earth's surface from damaging radiation, is harmed by air pollution in the form of NOx. These oxides have a substantial impact on human health in addition to having negative consequences on the environment. One of the most efficient methods for reducing NOx is urea SCR, converting about 95% of the gaseous nitrogen oxides. At a temperature of 200 °C, it functions properly.

1.4 Problem definition

To design, simulate, test and diagnose the urea tank level detection in diesel engine vehicles operating using the selective catalytic reduction technique.

1.5 Objectives

The main objective of the project is to design and implement urea tank level detection in diesel engine vehicles through these steps

- Design and development of "Urea Tank Level Detection System" in diesel engine vehicles employing SCR technique in ASCET software.
- To Simulate, diagnose and test the developed system in ECU worx, CI dashboard and TPT software package respectively.
- To test the prototype in LABCAR practically

1.6 Organisation of the Report

The complete report presents the review of the work carried out, concepts, design and its verification. It is organised in seven chapters.

Chapter 1: Introduction briefs the introduction of the project that includes the overview of the project, literature survey of the project that gives the cons of the project and motivation to take up the project, problem definition, and objectives of the project. It also includes the organisation of the report.

Chapter 2: Theory and Concepts gives the basics of the SCR technology including the operating modes, applications, working principle SCR technique along with the details of exhaust engine of diesel vehicles.

Chapter 3: Methodology and Block Diagram presents the methodology used in the design and development of an urea tank level detection in diesel engine vehicles using SCR technique. It also explains the approach followed and software packages used for simulations and testing.

Chapter 4: Specifications and Design explains in detail the design and specifications of the proposed urea tank and other various sensors used.

Chapter 5: Simulations and Implementations provide the simulation for the proposed urea tank level detection in various software and its results respectively.

Chapter 6: Results and Discussion discusses about the simulation results of the urea tank level detection system in diesel engine vehicles.

Chapter 7: Conclusion and Future Scope includes the overall conclusion drawn from the project and the future works that can be carried out.

References include the list of references referred in the successful completion of the project.

1.7 Summary

This chapter gives an introduction to the urea tank level detection in diesel engine vehicles and the key findings of the literature review. It also describes the problem statement, objectives and methodology.

CHAPTER 2

THEORY AND CONCEPTS OF SCR TECHNOLOGY

In this chapter, basic working principle of exhaust system along with the theory and chemical reactions involved in SCR technology used in diesel engine vehicles are discussed.

2.1 Exhaust System

The exhaust system was initially designed as a simple duct system with the intention to safe route the toxic exhaust gas emissions from car into harmless gases to the environment at the same time providing attenuation of noise made by the engine during combustion. Today, over the years the responsibility of exhaust system has grown. Modern exhaust systems are an integral part of combustion and pollution control thereby reducing noise, minimize harmful emissions and even provide assistance in increasing fuel economy, power and hence the overall drivability. The main parts of the exhaust system cooperate to remove emissions, lessen noise, and promote smoother operation of the moving parts. Although the emission control systems may vary based on the manufacturers and the vehicles, they all are designed to meet the same goal and they work on the same principle.[1]

The primary design consideration of an exhaust system includes:

- Minimizing the gas flow resistance and confine it to specified range depending on the engine model to achieve maximum efficiency.
- Suppressing the exhaust noise to meet the automobile regulations and requirements.
- Providing sufficient clearance between exhaust system components and engine components so as to minimize the impact of high exhaust temperature.
- Ensuring that the system does not overstress engine components with excess weight as overstressing shortens the component life.
- Ensuring that the exhaust components are able to reject heat energy as intended.

The following elements make up the exhaust system typically:

• After-treatment tools to reduce the pollutants released, like particulate filters and catalytic converters.

• Mufflers to reduce noise.

• Components that serve as a decoupling link between the exhaust manifold and the rest of the exhaust system.

• Hangers and piping

The "hot end" of the exhaust system is the after-treatment equipment and its piping and the "cold end" is made up of the muffler and tailpipes. The "down pipe" or "front pipe" that joins the exhaust manifold with the catalytic converter, as well as the pipework between the catalyst and the particle filter, may be included in the hot end pipe. The "middle pipe" joins the muffler and the after-treatment system. The exposure to requirements and chemical exposure affects the material choice for the exhaust system.[2]-[3]

The exhaust manifold often thought to be a part of engine is the key component of exhaust system that collects all the exhaust gases from the combustion chamber to the exhaust pipe. The design of exhaust manifold has a major influence on the torque and performance characteristics of the engine. The flexible joint , minimises engine movement transmission to the exhaust system. It typically sits between the catalytic converter and manifold. Hence it withstands high temperature, and it is durable and strong.[4]

The catalytic converter is another important component in the exhaust system that is installed between the manifold and muffler in the exhaust line. It makes use of chemicals that act as a catalyst. Prior to exiting the exhaust system, a catalytic converter causes a chemical interaction between the pollutants in the exhaust, without causing any damage to the pollutants themselves.[5]

The IC engines usually make a whole lot of noise during operating. This noise reduction is achieved through well designed mufflers. Mufflers making use of the principle of reactive silencing is an application of wave cancellation technique to tune out certain frequencies that are harsh to human's ear. By choosing appropriate design parameter we achieve tuning for a specific range of frequencies. Since it is not possible by a muffler to reduce the engine noise by itself add-on features such as resonator is included in the exhaust system. A typical resonator is a hollow steel cylindrical tube attached to the muffler. They both work together to decrease the exhaust noise. Finally there is a tail pipe that is designed to serve as an enclosed route for the exhaust emissions to exit the system.[6]

With the emission reductions strategies being more stringent, major technologies are deployed to reduce emissions. Some of them include:

2.1.1 Oxidation Catalyst

The oxidation catalyst sown in Fig 2.1 cut CO and HC emissions by more than 90% and harmful HC emissions by more than 70%. Toxic by-products are created if there is not enough

oxygen present in an internal combustion engine to oxidise carbon fuel into carbon dioxide and water. The redox conversion of toxic fuel by-products into less dangerous compounds takes place in catalytic converters. It is made up of a steel housing, a ceramic or monolith honeycomb interior, and a metallic substrate. Platinum (Pt), palladium (Pd), and rhodium are combined to form the honeycomb structure. It maximises the surface area for greater reaction to occur (Rh).[7]

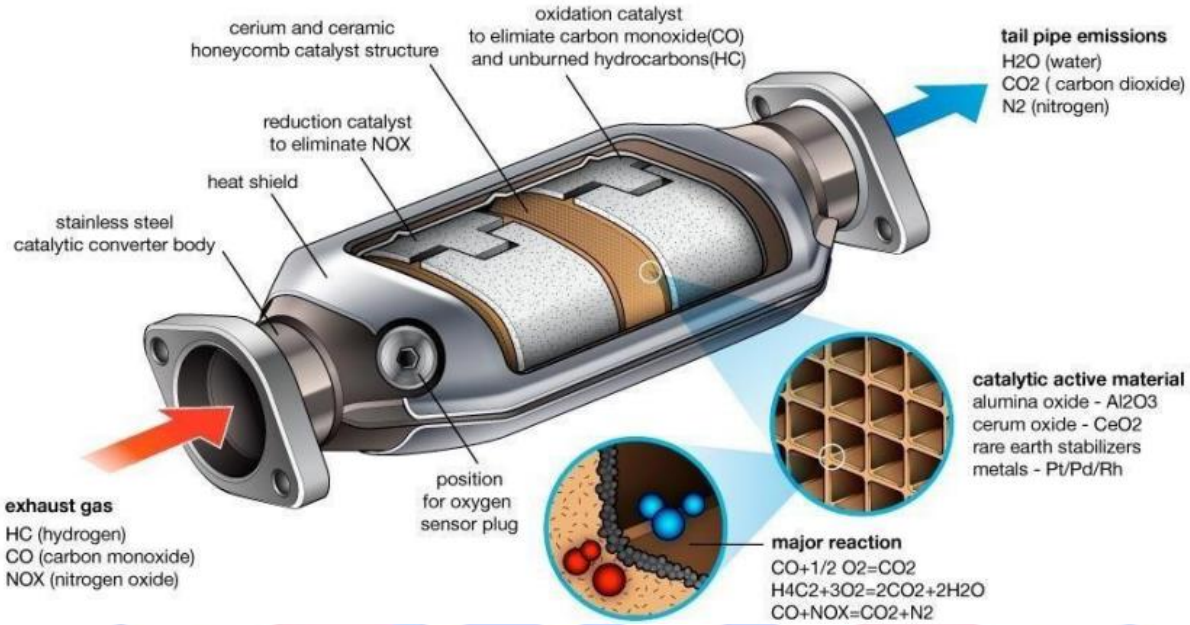

Fig 2.1: Oxidation Catalyst

The catalyst initially starts a reduction reaction to reduce nitrous oxide. The nitrogen atom in nitrous oxide is eliminated as it passes through the Pt and Rh catalyst, allowing free oxygen to produce oxygen gas O_2. The nitrogen atom then interacts with other nitrogen atoms linked to the catalyst to produce nitrogen gas N2.In the second stage, an oxidative catalyst made of Pt and Pd is used to regulate carbon monoxide (CO) and unburned hydrocarbons (HC). Carbon dioxide (CO_2) is created if carbon monoxide (CO) combines with oxygen in the air, and water is produced hydrocarbons are oxidised (H_2O). For decreasing emissions from gasoline engines, catalytic converters are dependable and effective.[8]

If coupled with diesel engines, operating more coolly than gasoline engines, they are less effective. Higher temperatures are ideal for catalytic converter operation. Particles like soot is also produced by diesel engines. Hence, combining a particulate filter and a catalyst cut down on ultra-fine particle emissions by up to 99 percent.

2.1.2 Particulate Filters

To comply with particulate matter emission restrictions, the particulate filters in Fig 2.2 are fitted (PM). Particulate filters eliminate particles smaller than 100 nm that are made up of carbon, ash, and unburned hydrocarbons. Since the filter's capacity is limited, the trapped soot increases flow resistance, necessitating its emptying or burning off in order to replenish the DPF.

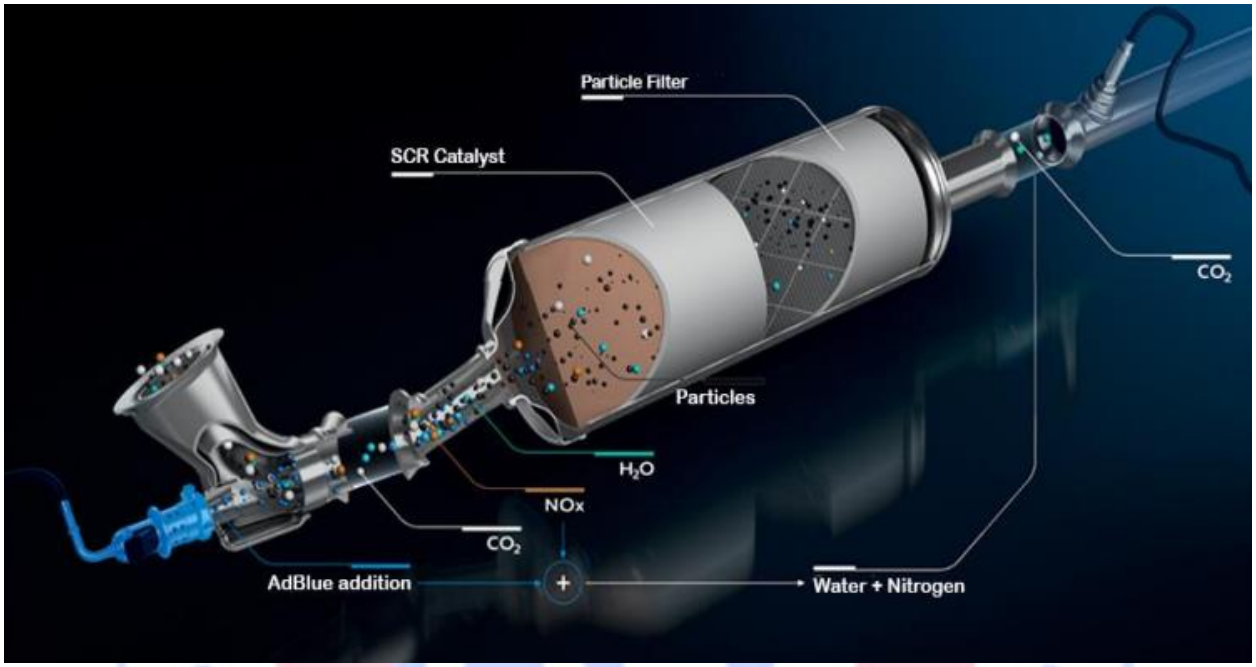

Fig 2.2: Particulate filter

The extra soot particles that gathered in the filter after about 800 to 2000 kilometres of driving are thoroughly burned during the regeneration process. At temperatures greater than 600 °C, the deposited soot is then burned off together with the exhaust fumes. Since this temperature is typically not attained during routine driving, the exhaust temperature is raised through post-injection, delayed main injection, and throttle valve air mass reduction. The exhaust outlet valve's temperature then rises as a result. The temperature is also raised by the exothermic reaction of unburned hydrocarbons in the oxidation catalytic converter. The particle filter is often placed close to the exhaust manifold and frequently used in conjunction with an oxidation catalyst in order to prevent significant heat loss.[9]

2.1.3 Exhaust Gas Recirculation

Exhaust gas recirculation (EGR), reducing the oxygen content in the combustion chamber and absorbing heat, is an efficient method for reducing NOx emissions. By using the inlet system, it is a technique for returning some of the exhaust gas to the combustion chamber. By

providing inert gases to the combustion process and limiting the amount of oxygen present in the incoming air stream, this lowers the peak in-cylinder temperatures. Fig 2.3 is a schematic illustration of an EGR system.[1]

If air oxygen and nitrogen are combined at high temperatures in the combustion chamber, typically happening at peak cylinder temperature, NOx is formed. The composition of the gas introduced into the cylinder during the engine cycle, change as a result of the mixing of exhaust gas with intake air. Significantly less oxygen is present, but more CO_2 and water from burning is produced. A drop in the peak temperature of the diesel combustion flame is the main factor causing EGR's NOx reduction impact.[2]

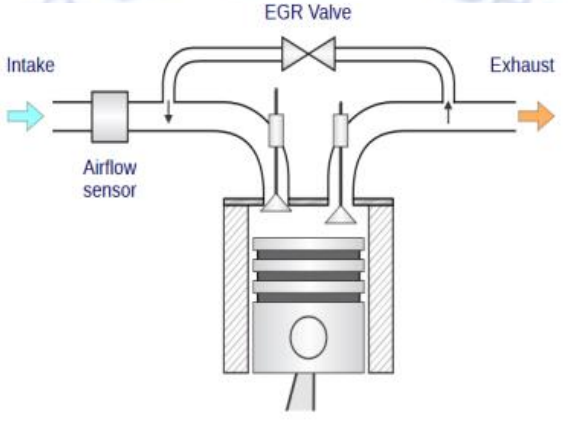

Fig 2.3: Schematic representation of EGR system

The exhaust gas added to the oxygen, fuel and combustion products increase the specific heat capacity of the cylinder lowering the adiabatic flame temperature. A properly operating EGR increase the engine efficiency. Automotive exhaust system is one of the inevitable parts of combustion and emission control system that is designed to perform one or more of the following functions: remove solid materials from the exhaust gas, muffle the exhaust noise, quench sparks and furnish energy to a turbine-driven supercharger. Hence keeping exhaust system in better working condition is vital for fuel consumption, safety and environment. The durability of the exhaust is crucial.

2.2 Engine ECU

Before the automotive industry adopted electronics, cars were thought of as mechanical machines. Through the principle of mechanics, every component in a vehicle, from the engine to the window, brake, and steering, was mechanically driven on gears. However, the inherent limitations and poor accuracy of these mechanical systems led to undiscovered failures and a

high risk of harm to the users. These restrictions made it possible for the car industry to innovate more effectively. This finally resulted in the use of electronics in vehicles.[3]

Since its introduction to the automotive industry in 1970, automotive electronic control units (ECUs) have grown to be a significant part. It has been crucial to the evolution of the automobile from a wholly mechanical to an electronic-dominant machine. To control and regulate the functionality, modern cars feature around one hundred embedded or fitted ECUs.

The electronic control unit (ECU) seen in Fig 2.4 is a computer with inbuilt programmable and pre-programmed chips that uses microprocessors and sensor data that may be processed to conduct real-time control of a number of actuators. For the gearbox, traction control or ABS, body functions, lighting control, AC, engine, air bags, and other sections of the car, there are numerous distinct Ecosite power train, body control, and chassis system are the three main units where an automotive ECU is used.

The ECU, a component of the Power-train Control Module (PCM), is in charge of controlling the combustion process, including opening and closing the inlet or outlet valve in response to input from the accelerator pedal.

The ECU regulates the timing of the fuel injection rate and spark ignition. Hence, compared to vehicles with mechanical controls, ECUs produce accurate synchronisation and increase power, efficiency, and functionality. Sensors have a significant impact on an ECU function. Instead of sending numerous wires from the sensor to various ECUs, the ECU share information with other ECUs over communication network lines for control operations. Most vehicles include an OBD connector that the ECU uses to transmit all diagnostic data to all other ECU modules.[4]

Government regulatory bodies have imposed strict restrictions on the emission levels from automobiles hence OEMs are responsible for implementing emission controls in automobiles. Implementing such restrictions would have been a mission impossible without the use of ECUs and software algorithms. With automation the regulatory bodies are able to respond to emergency situations in a better way. Also, with the advancement in mobile phones, car manufactures had slowly transformed car with the explosion of electronics to introduce web connectivity, smart devices and navigation control.

Astonishing amounts of data are processed by an ECU. To obtain maximum performance, a number of operations are carried out simultaneously. With the aid of sensors, the ECU enables the processing of all the data that the engine receives. The automakers configure the ECU in such a way that some car models have very smooth rides and others have a more

racing-inspired feel. ECU shown in Fig 2.4 hence enables us to have these two unique traits in a single car. To accommodate greater and better performance, ECUs are periodically reset. Hence, the performance provided by the ECU makes driving more enjoyable than difficult.

Fig 2.4: Engine ECU

2.3 Diesel and Gasoline Systems

The development of the gasoline engine marks the beginning of the diesel saga. The four-stroke combustion principle known as the "Otto cycle" was created by Nikolaus August Otto, who also received a patent for the idea. In the beginning, gasoline engines weren't very efficient because only 10% of the fuel they used actually moved the car. The remainder was transformed into waste heat. After learning about the inefficiency of gasoline engines, Rudolf Diesel was motivated to develop an engine with improved efficiency. He spent a significant amount of effort developing a "combustion power engine. “Diesel was able to patent a diesel engine by 1892 as a result.[6]

Diesel and gasoline engines are conceptually pretty similar. They are IC engines made to transform fuel's chemical energy into mechanical energy. The pistons inside the cylinders are then moved up and down, creating a linear motion, using this mechanical energy. To turn the wheel forward, a rotary motion is produced by a crankshaft that is coupled to the pistons. A gasoline and diesel engine's explosion process is depicted in Fig 2.5. Both diesel and gasoline engines use a sequence of explosions or combustions to transform fuel into mechanical energy. But these explosions make a significant difference. Fuel and air are combined in gasoline, then

compressed by pistons and ignited by sparks from spark plugs. In a diesel engine, the fuel is injected after the air has been compressed. Compression warms the air, causing the fuel to ignite.[7]

The following is an explosion process in a gasoline engine:

1) Intake stroke – Gasoline and air are combined.

2) Compression stroke — Piston rises, compressing the air-fuel mixture.

3) The air-fuel mixture is ignited by a spark plug during the ignition stroke.

4) The piston rises and pushes the exhaust out the exhaust valve during the exhaust stroke.

The following is an explosion process in a diesel engine:

1) The intake valve opens and fills with air during the intake stroke.

2) Air is compressed during the piston's upstroke during the compression stroke.

3) The air-fuel mixture is ignited once fuel is introduced into the engine.

4) The piston rises and pushes the exhaust out the exhaust valve during the exhaust stroke.

Spark plugs are not used in diesel engines. To produce the high temperatures required for fuel ignition, they require high compression ratios. Of comparison to a gasoline engine with a ratio of 8:1 to 12:1, the compression in a diesel engine with a ratio of 14:1 to 25:1 is significantly higher. Higher thermal efficiencies and improved fuel economies are produced by higher compression ratios. The engine's compression ratio is constrained by the compression of the air-fuel mixture. The air-fuel mixture ignites spontaneously and creates knocking. It might harm the system, if there is more air compression.

An essential part of a diesel engine is the injector. It ought to be able to withstand the pressure and heat inside the cylinder during dispensing the fuel as a fine mist. Glow plugs are used in some diesel engines to warm the combustion chamber and increase air temperature if the engine is cold.

Today, a complex system of sensors measuring everything from RPM to engine coolant and oil temperature and TDC is used to operate every function of a contemporary engine. On contemporary engines, glow 27 plugs are rarely used. ECM detects the temperature of the surrounding air and delays the engine's timing so that the injector sprays fuel later. As a result, the air is compressed more and produces more heat, helping the engine start.[8]

Diesel and gasoline engines show a number of development paths for better torque generation, fuel efficiency, emission control, and noise reduction. Improved driveability features, increased specific power, better noise attenuation, decreased fuel consumption and CO_2 emissions, decreased specific emissions (HC, NOx, CO, particulates, and dust), reduced friction,

and effective exhaust after treatment systems are some of the most recent engine technology advancements. Fig 2.5 shows the gasoline and diesel engine.

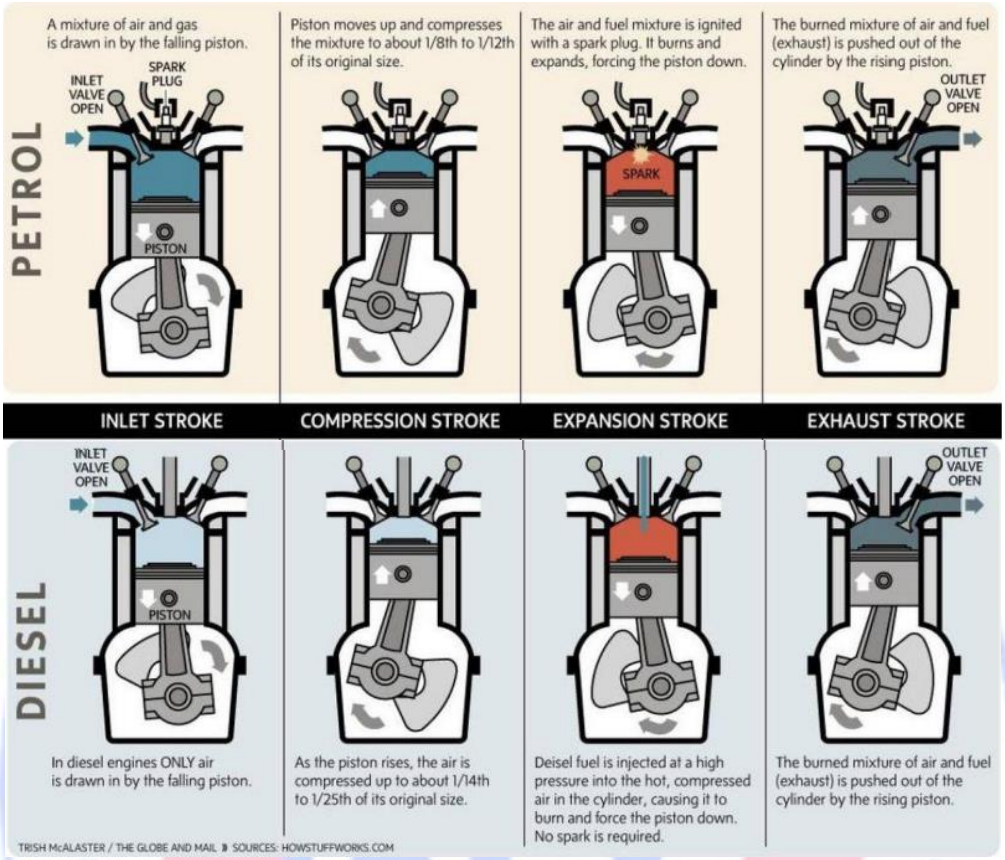

Fig 2.5: Gasoline and diesel engine

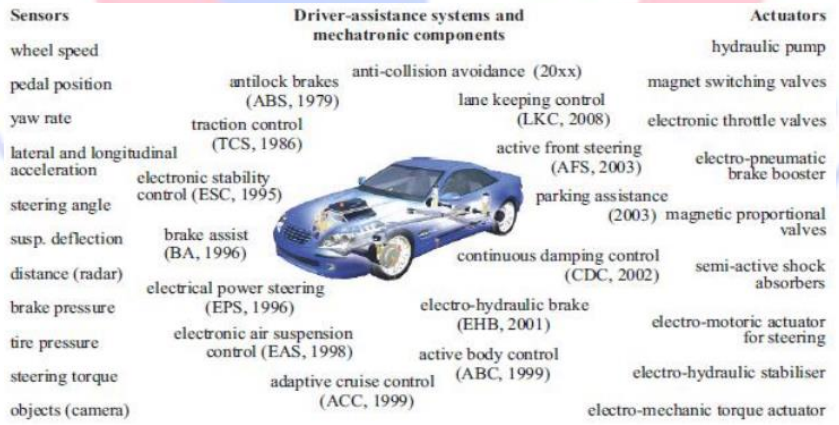

Fig 2.6: Development of sensors, driver assistance systems and actuators for automobiles

The evolution of automotive sensors, driver assistance systems, and actuators is depicted in Fig 2.6.Engines are equipped with mechatronic parts such electronic throttle intake systems, high-pressure common rail injection systems with solenoid or piezoelectric injectors, VVT, VGT, and variable camshafts to increase its variety and control functions. These parts are be

categorised as electrical, pneumatic, or hydraulic actuators, solenoid and switching injection valves, electrical drives, pumps, and fans.

Some of these are controlled centrally by an ECU and others are controlled locally by sensors that are incorporated locally. The development of hybrid drives, improving fuel efficiency and reducing pollutants, is a cutting-edge step in the electrification of automobiles. All of these developments suggest that electronics continue to increase rapidly, and that mechatronic design generally improve. The proliferation of electronic components emphasising important fault diagnosis functions are.

2.4 Working Principle

The essential parts of the urea SCR system are represented schematically in Fig 2.7, together with the DOC (Diesel Oxidation Catalyst), DPF (Diesel Particulate Filter), DEF (Diesel Exhaust Fluid), and SCR. Engine exhaust is sent to DOC, where the hydrocarbons are transformed into carbon particles. The DPF gathers and preserves the carbon atoms. These soot particles are frequently burned. SCR uses alkali and NH3 as a reductant to lower NOx emissions in the exhaust gas. DEF is an aqueous solution that is sprayed into the exhaust stream to reduce NOx. It contains 32.5 percent urea and 67.5 percent deionized water. It was discovered that DEF usage accounted for 2% of gasoline consumption.[1]

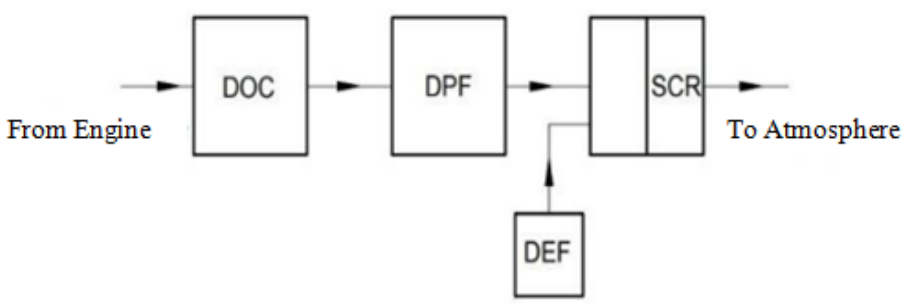

Fig 2.7: Schematic diagram of urea SCR

Pollutant emissions from diesel engines, such as soot (also known as particulate matter, or PM), and NOx, typically exceed the legal limits. Recent research has shown that cutting these pollutants by more than 46 to 90 percent is possible with sophisticated diesel aftertreatment systems. More than 90% of the particulate matter (PM) in the exhaust gas from a diesel engine is captured by a DPF, also known as a catalytic particulate filter (CPF). The DPF removes CO and CO2 after oxidising the particles it has caught using the thermally aided and NO_2-assisted

reactions described in Equations. (4) and (6). DPF regenerations are the common name for these procedures.[2]

2.5 Chemical Reactions Involved

Urea breaks down into ammonia and isocyanic acid if DEF is injected into the exhaust stream because of the exhaust temperature.

$(NH_2)CO(NH_2)$ (molten) $\rightarrow NH_3 + HNCO$ ……. (1)

Ammonia and carbon dioxide gases are created as a result of the hydrolysis of this isocyanic acid.

$HNCO + H_2O \rightarrow CO_2 + NH_3$ ……. (2)

Oxides of nitrogen are now reduced by ammonia in the presence of oxygen and an SCR catalyst.

$4NH_3 + 4NO + O_2 \rightarrow 4N_2+H_2O$ …..… (3)

$8\ NH_3 + 6NO_2 \rightarrow 7N_2+12\ H_2O$ …….. (4)

$4\ NH_3 + 2NO + 2NO_2 \rightarrow 4N_2+6\ H_2O$ …….. (5)

$2\ NH_3 + 2NO_2 \rightarrow NH_4\ NO_3 + N_2 + H_2O$ .....… (6)

Equation (1) demonstrates the high temperature of the exhaust causes molten urea to break down into ammonia and hydrocyanic acid. Ammonia and carbon dioxide are the major by-products of the isocyanic acid hydrolysis shown in equation (2). These two reactions take place without the need for a catalyst. Equation (3) represents the typical reaction involving oxygen and the equal amounts of ammonia and NO. The quick and slow SCR reactions are shown in equation (4). At temperatures 2000 °C , ammonium nitrate is formed as a result of some unfavourable reactions.

Numerous competitive & nonselective reactions with oxygen, plentiful in the system, are among the undesirable activities that take place in SCR systems. These reactions either result in additional emissions or, at worst, use ammonia ineffectively. Nitrous oxide (N_2O) or elemental nitrogen may result from the partial oxidation of ammonia, as shown in Equations (7) and (8). Nitric oxide (NO) is produced by the complete oxidation of ammonia, as demonstrated by Equation (9).

$2NH_3 + 2O_2 \rightarrow N_2O + 3H_2O$ …..... (7)

$4NH_3 + 3O_2 \rightarrow 2N_2 + 6H_2O$ ……. (8)

$4NH_3 + 5O_2 \rightarrow 4NO + 6H_2O$ ……. (9)

The ammonia injection rate needs to be precisely controlled for the SCR process.Low NOx conversions due to insufficient injection may be unacceptable. Unwanted ammonia is released into the atmosphere if the injection rate is too high. Ammonia slip refers to these ammonia emissions from SCR systems. At greater NH_3/NOx concentrations, the ammonia slip increases. The stoichiometric NH_3/NOx ratio in the SCR system is around 1, according to Equation (2), describes the primary SCR reaction. The ammonia slip is greatly increased by ratios greater than 1. In reality, ratios between 0.9 and 1 are employed to reduce ammonia slip, maintaining sufficient NOx conversions.[3]

It is clear from the chemical reactions discussed that, NO_2 is crucial to the reactions taking place inside DPFs and SCR catalysts. The presence of NO_2 hasten the regeneration of the DPF, and a higher NO_2/NOx ratio (but not more than 50%) hasten the effectiveness of the SCR's NOx conversion. Although NO makes up the majority of the NOx composition of diesel engine exhaust, it is known that a higher NO_2/NOx ratio is advantageous for DPF PM removal and SCR NOx reduction.[4]

Due to this property, diesel oxidation catalysts (DOCs) are frequently utilised upstream of DPFs and SCRs to increase the performance. DOCs catalyse the conversion of a portion of NO to NO_2 and result in a greater NO_2/NOx ratio than engine-out exhaust. Fig 2.2 depicts a typical configuration for a diesel engine's aftertreatment system (DOC-DPF-SCR). One of the key factors in the performance analysis of SCR NOx conversion is the effectiveness of NOx conversion in diesel engine cars. SCR NOx conversion = [1 – (NOx out/NOx in)] 100% provides the answer.

2.6 Summary

This chapter presents, Selective Catalytic Reduction, a promising technique in NOx reduction in diesel engine system along with the various chemical reactions involved in its process.

CHAPTER 3

METHODOLOGY AND BLOCK DIAGRAM

In this chapter, the block diagram for the proposed scheme is explained in detail. The methodology along with the design requirements for simulation, testing and diagnosis of urea tank level detection in diesel engine vehicles is also discussed.

3.1 Methodology

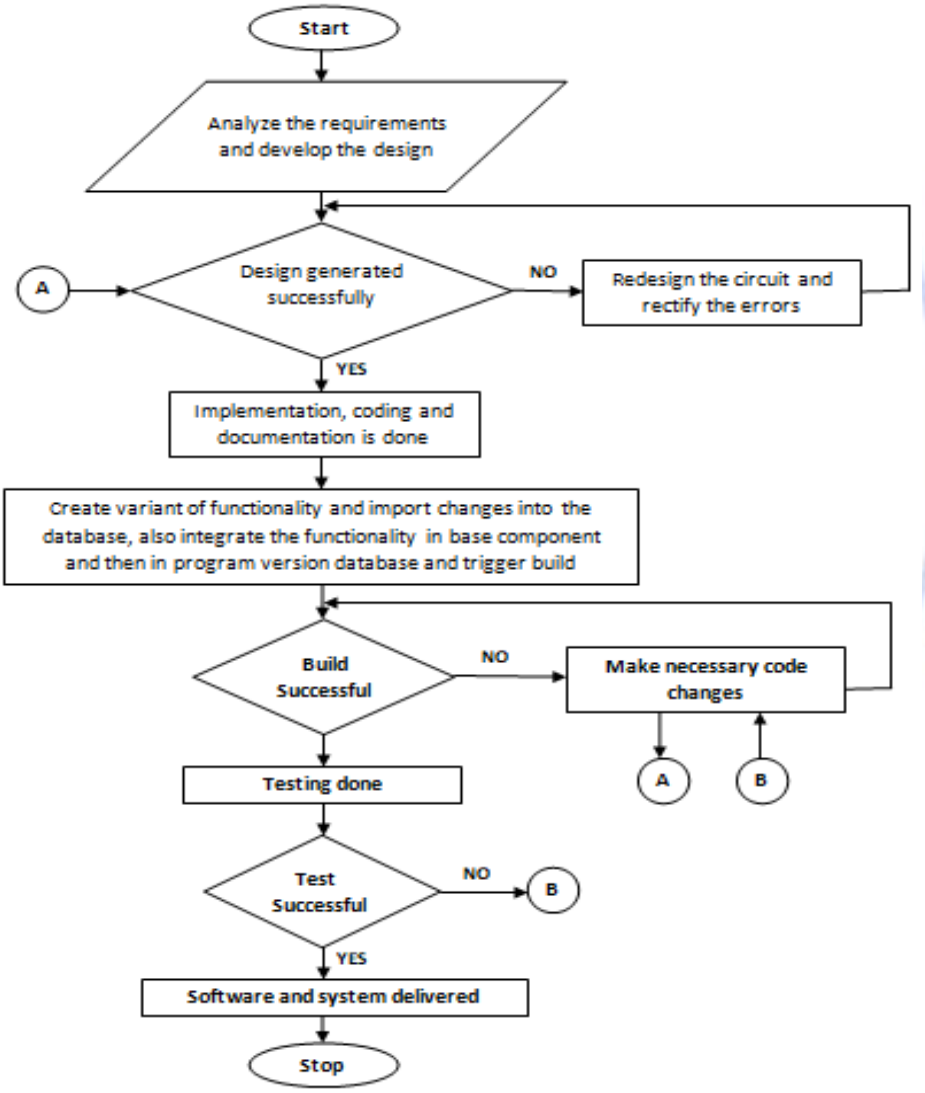

Fig 3.1: Methodology flow chart

The overall steps involved in the development of a functional component are explained by means of a flow diagram shown in Fig 3.1. Till now we discussed the working and need for

each functional component in the exhaust management package. Initially we receive a requirement request from the OEM for modification or development of a functional component. Based on this request the function developer, do the required analysis and implement the functionality by means of certain development tools. We make use of ASCET tool for the simulation purpose. It is a tool that could generate code and document automatically. This code satisfies automobile industry standards. So, we check for software warnings. These warnings are removed from functional components before integration. Once the functionality is ready, we integrate it into corresponding BC and base PVER provided by the customer.

To ensure the functionality build is triggered. Once the build fails at any stage we have to redesign or modify the necessary functions for the build to get through. Once the build is through the software is tested using testing tools such as TPT or LABCAR based on the changes. If there is any deviation in the result from the expected one, we again redesign and continue the process till the desired output is obtained. After testing the FC state is made to available in the database and the BC is delivered to the requested customer, who finally integrate it in the corresponding PVER.

3.2 Design Requirements

1. There are no sensor related errors.
2. Tank temperature is greater than threshold freezing temperature.
3. Environment temperature is greater than threshold value.
4. Vehicle speed less than a threshold value.
5. Bit mask these conditions.
6. Validate the level sensor signals.
7. Set or reset of total number of evaluations based on release conditions.
8. Fault check diagnosis be reported accordingly.
9. Calculate the number of times the error has been set, and this information is to be provided for various driving cycles.

3.3 Block Diagram

The block diagram of the urea tank level detecting system used in diesel-powered cars is shown in Fig.3.2. A block diagram is used to show the fundamental design in accordance with the particular conditions specified by the client. The block diagram shows the interconnection of

the numerous sensors as well as the timer and counter for the various fault checks, continuous monitoring, reporting, diagnostics, and data storage.

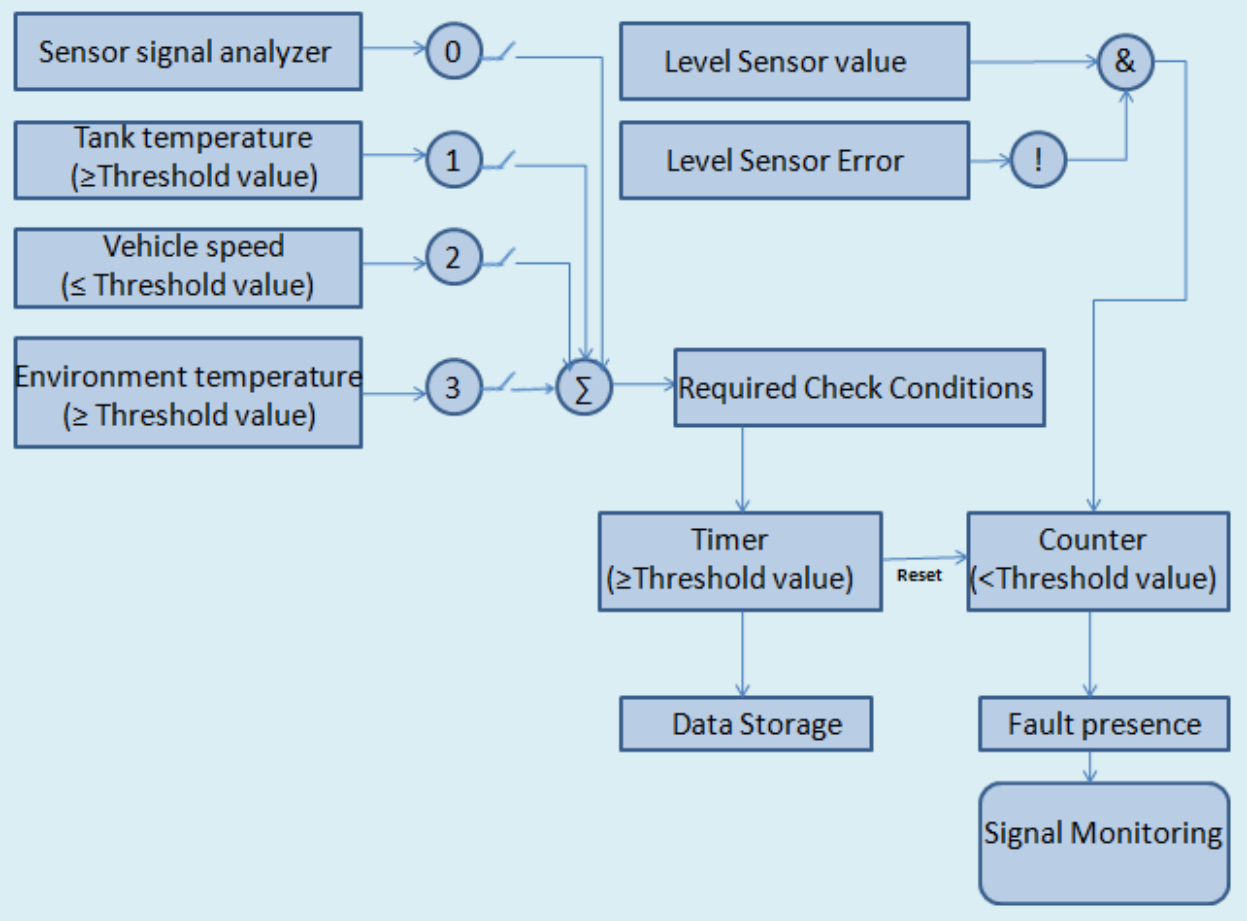

Fig 3.2: Block diagram

3.4 Summary

The required methodology and block diagram for designing urea tank level detection system in diesel engine vehicles was explained in the chapter.

CHAPTER 4

SPECIFICATIONS AND DESIGN

There are various components involved in the proposed urea tank level detection system in diesel engine vehicles. The process is carried out smoothly if all the components are interfaced and synchronised in the desired fashion. The process of selecting and designing the components as per required specifications plays an important role. The chapter deals with the selection of various components needed for the operation.

4.1 Specifications

The hardware and software requirement specifications for the designing and the testing of the urea tank level detection system are mentioned below. These are essential to carry out the project successfully and correctly.

4.1.1 Hardware requirement Specifications

- Temperature Sensor:
  The temperature sensor used in the proposed work is of PTC (Positive Temperature Coefficient) type with a voltage rating of 0-5V and temperature rating of -40ºC up to 1000ºC.
- Level Sensor:
  The level sensor used is continuous level ultrasonic senor for passenger vehicles and for commercial vehicles Reed Switch discrete level sensor with the 20 to 40 steps, depending on the tank size.
- Urea Tank:
  Urea tank size and volume varies form 10- 50 litres depending on the application such as passenger or commercial vehicle. The urea tank has a dead volume at the bottom and unused / air gap volume at the top. The net usable volume is Total volume of the tank-dead volume-unused volume. At the air gap, a breather along with the dust filter is placed.
- Power:
  The power required to operate the DNOx control system is to run the pump, dosing valve, sensors and ECU. Overall, the required power is 36W with voltage of 12V and current of 3A. DNOx system also requires power to operate the electrical heaters to defreeze the urea. The

required power for this operation is 60W with voltage of 12V and current of 5A. It is the highest power consumed by DNOx system.

4.1.2 System requirement Specifications

The table 4.1 shows the minimum requirements for ASCET software installation.

Table 4.1: System requirements for ASCET Installation

System requirements	Minimal	Recommended
Host requirements		
Hardware	2GHz Dual Core 64bit PC 4GB RAM	2GHz Quad Core 64bit PC 8GB RAM
Free Disk Space	2GB	
Required Operating System	Windows10(x64)	

4.3 Summary

The Simulations were carried out in various software packages. The details of the different software packages used for simulations along with hardware and system requirement was mentioned in this chapter.

CHAPTER 5

SIMULATIONS AND IMPLEMENTATIONS

In this chapter, the Simulation of a urea tank level detection in an ASCET software is implemented two stages and this is explained in detail.

5.1 Work Environment

The details of the various software used to carry out the proposed work is as listed.

5.1.1 Design and Code generation in ASCET

Advanced Simulation and Control Engineering Tool is referred to as ASCET. It is a multifaceted and adaptable product family that offers an original approach to the functional and software design of contemporary automotive embedded systems. With a fresh take on modelling, code generation, and simulation, ASCET supports each step of the development process, enabling improved quality, quicker innovation cycles, and lower costs. ASCET makes it simple to blend text and visuals to meet programming requirements. The logic is modelled in a variety of ways, allowing us to operate as effectively as we see fit.

As a result, we have four specification options.:

1) Graphic specification using Block Diagram.
2) Graphic specification using State Machine Editor.
3) Textual specification using ESDL Editor.
4) Textual specification using C Code Editor.

The ASCET has been specifically created to meet the difficulties in software development for sectors where goods are produced in large quantities, at a lower cost, in compliance with industry standards, and without any flaws. The ASCET tool software engineers have the ability to create embedded software that is high performing, low overhead, simple to maintain, secure, and safe. High levels of automation enable productive and safe workplaces.[10]

ASCET tool operation is depicted in Fig 5.1. Using graphical models and textual programming notations, ETAS ASCET is a tool for creating software for embedded systems. The created function models is converted by the ASCET Code Generator into extremely effective and secure embedded C-Code for AUTOSAR applications.[9]

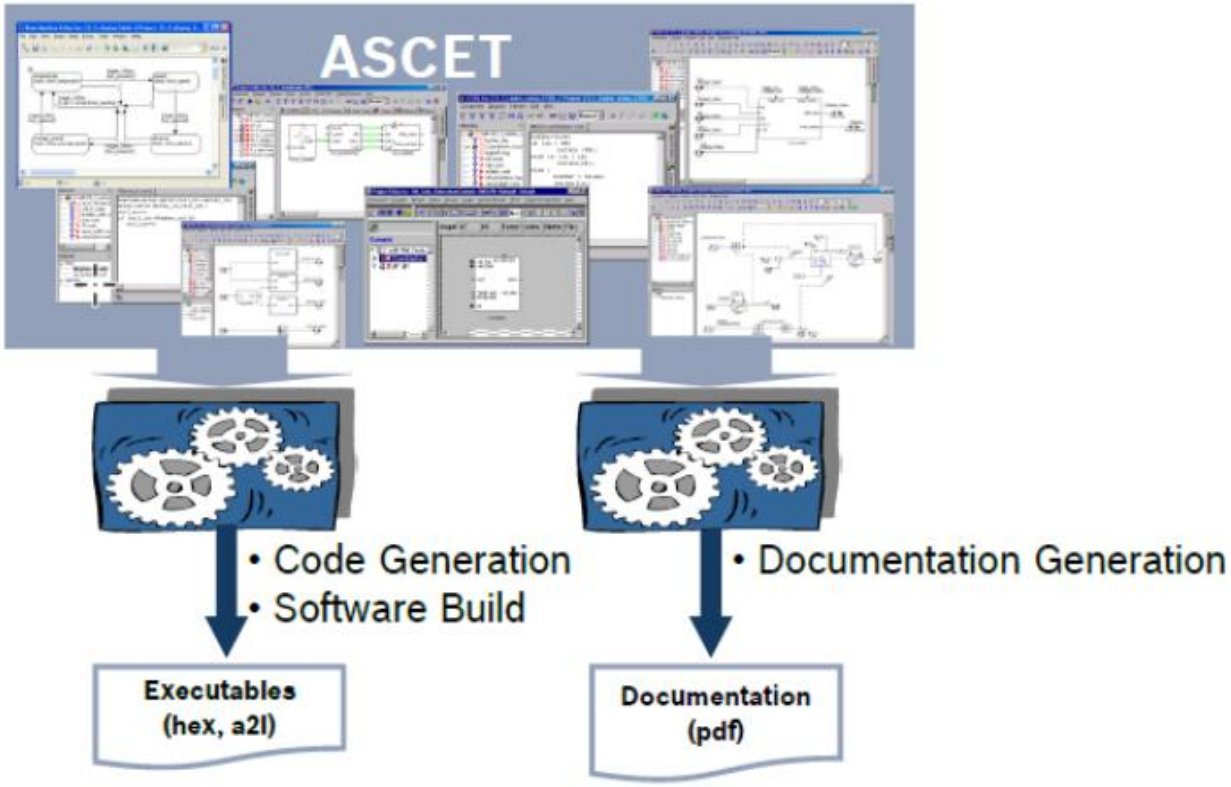

Fig 5.1: Working of ASCET tool

The ASCET tool for Automotive Software Development has the following features:

- Safe – Automatic introduction of defensive code, ISO26262 and IEC61508 TUV-certified code generation, MISRA-C:2012 compliance.
- Proven in usage – Used for brake systems (such ABS, ESP), powertrain, generation, compliance with MISRA-C:2012 Proven in use – Used for brake systems (such ABS, ESP), powertrain, Driver assistance, Battery management, 450+ million ECUs on the road are powered by ASCET produced code.
- Flexible – Multiple specification notations, Block diagram, state machine, textual editor for ESDL, and C-code editors.
- Quick and effective — Real-time static analysis for quick feedback, quicker code creation.
- A variety of testing alternatives, including unit testing, PC-based open-loop simulation, closed-loop simulation, and rapid prototyping.
- Embedded Software Development Language (ESDL), has an abstract data type, easy-to-understand syntax, and object-oriented encapsulation

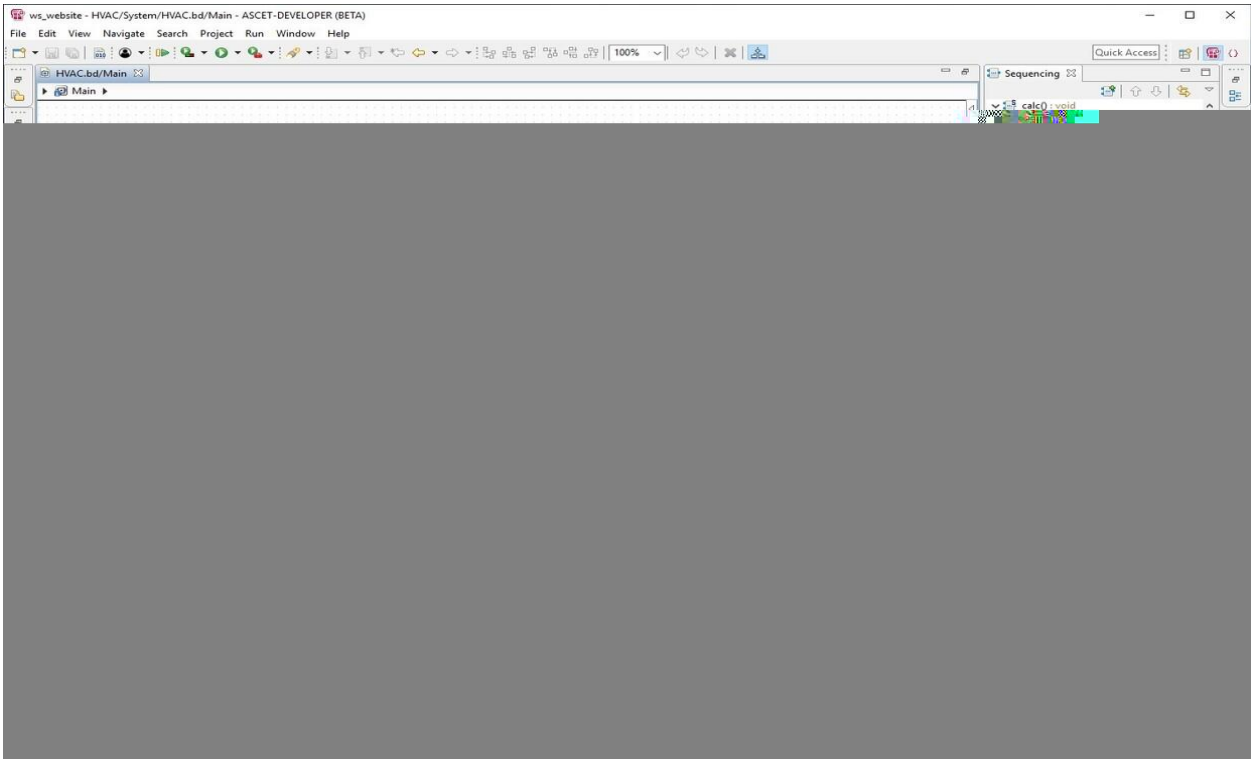

Fig 5.2: Example ASCET developer software image

Block diagram editor in ASCET makes it easy to model and visualize the data and control flow in fully deterministic execution order via explicit sequencing of calculations. Block Diagram Editor method as shown in Fig 5.2

DLL, a program is modularized into various separate components. The example of ECU Worx software is as shown in Fig 5.3.

Fig 5.3: Example ECU Worx software image

5.1.3 Software Build: CI Dashboard

The Continuous Integration dashboard displays key metrics for builds that is used to gain insight into the organization's build throughput and to bubble up any of the potential build issues. The Continuous Integration dashboard provides indicators to measure the agility of development. An example image of CI dashboard is as shown in Fig 4.4.

Fig 5.4: Example CI dashboard software image

5.1.4 Testing: TPT and LABCAR

Piketec's Time Partitioning Testing programme is known as TPT. With TPT, one may test embedded control systems and ECU software during all phases of development, including model-in-the-loop (MiL), software-in-the-loop (SiL), processor-in-the-loop (PiL), hardware-in-the-loop (HiL), and ECU and vehicle testing. TPT offers special tools to help write tests freely illustration of a TPT software image. Fig 5.5 shows an example TPT software image.

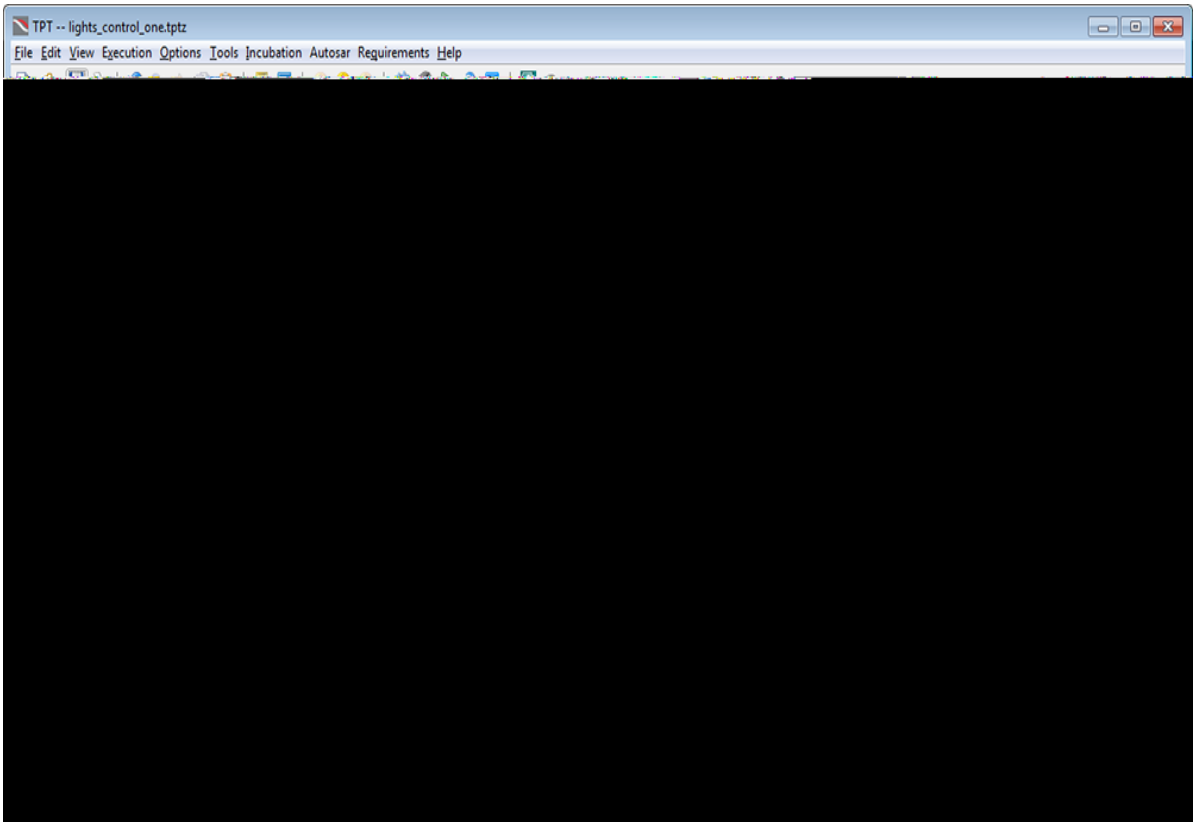

Fig 5.5: Example TPT software image

5.2 Simulations

According to the design requirements, part A design as shown in Fig 5.6 satisfies the design condition 1 to 5 mentioned under section 3.2. In Fig 5.6, function type identifies the type of incoming signal, and the sensor error detection block helps in identifying the presence of any errors. If there are no sensor related errors, it passes on the signal to the putbit. Tank temperature sensor measures the urea tank temperature and if the measured value is greater or equal to a preset threshold value, then the second bit input signal is passed onto putbit. Similarly, vehicle speed and environment temperature are measured by respective sensors and compared with the

threshold value. If the Vehicle speed is lesser or equal to its threshold value and the environment temperature is greater or equal to its threshold value, then the third and fourth signal is obtained by a putbit. Bitmask option is provided so as to select the mentioned conditions. One has an option to select the conditions as required according to the necessary demand, until the design and testing stage only.

If all the cumulative conditions are true, then the selected signal block passes on the signal to the next stage of design. Part B design shown in Fig 5.7., has continuous urea tank level sensor updating signal along with the level sensor error detection block. If there is any tank level signal update and there is no level sensor error, in the presence of the previous obtained selected signal, counter is set to compute the number of times the error has occurred between different driving cycle. If the count is less than the set threshold value then it reports, no fault to the signal monitor. If the count is greater or equals to the set threshold value, then it reports the presence of fault in the system to the signal monitor. Also, if the selected signal block passes its output, a timer is triggered to monitor the duration of fault occurrence. If the required timer value is greater or equals to the set threshold value a timer output is generated to reset the counter, timer and a trigger to non volatile memory for data storage.

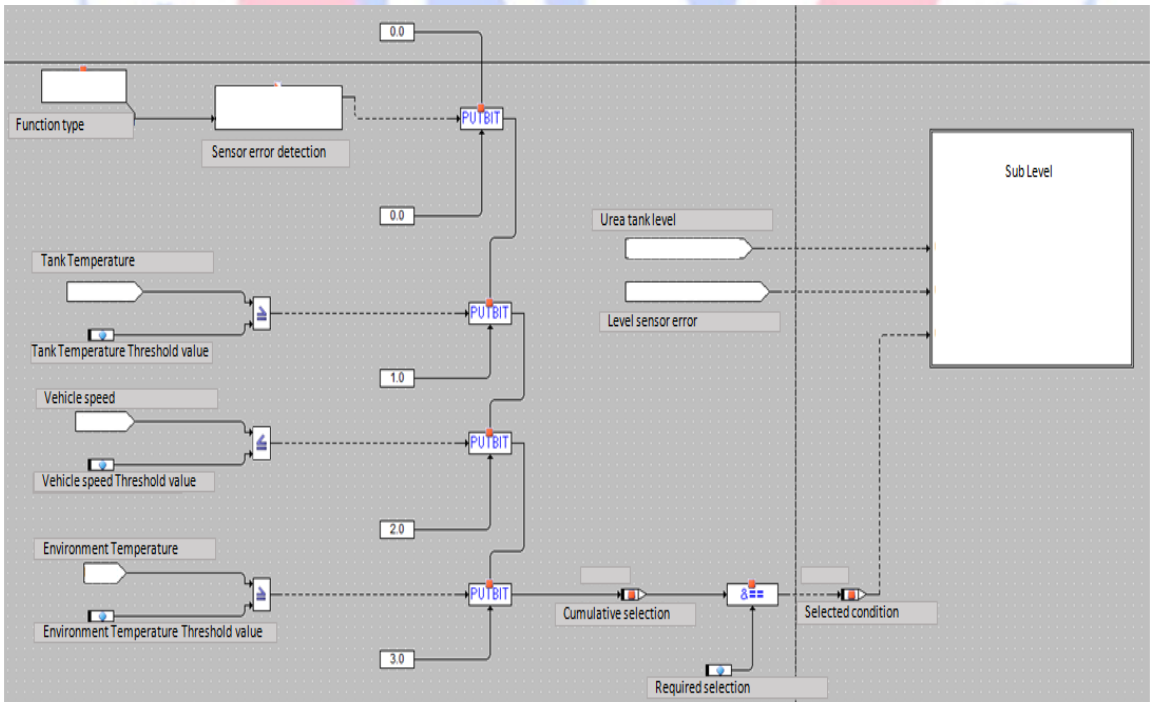

Fig 5.6 : Part A Design

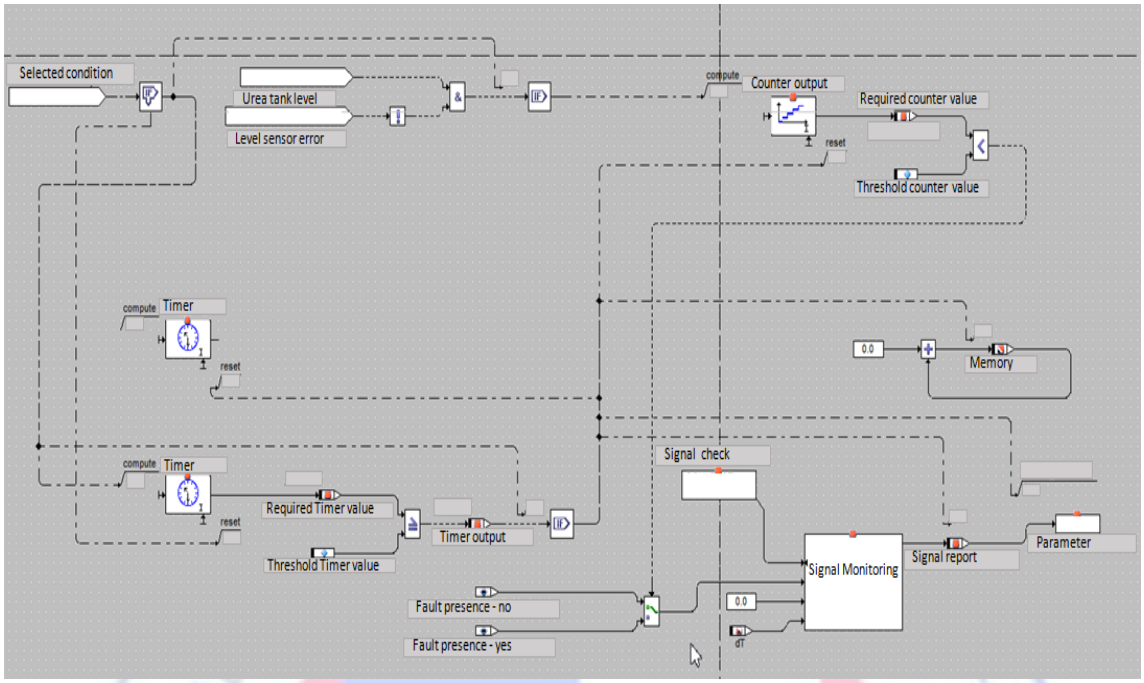

Fig 5.7 : Part B Design

5.3 Summary

The detailed ASCET design was explained in this chapter. Further simulations and results of this design in other software packages is shown in next chapter.

CHAPTER 6

RESULTS AND DISCUSSION

This chapter discusses about the conclusion made out of the proposed work. Also discusses about the future scope of the project work of the. Also discusses the results obtained in the simulation of the urea tank level detection design incorporated in the diesel engine vehicles using SCR technology.

6.1 ASCET Simulation

ASCET design is simulated and auto-code generated by ASCET is verified. If there are any errors, it has to be cleared and made zero errors.Fig 6.1 shows the ASCET simulated result.

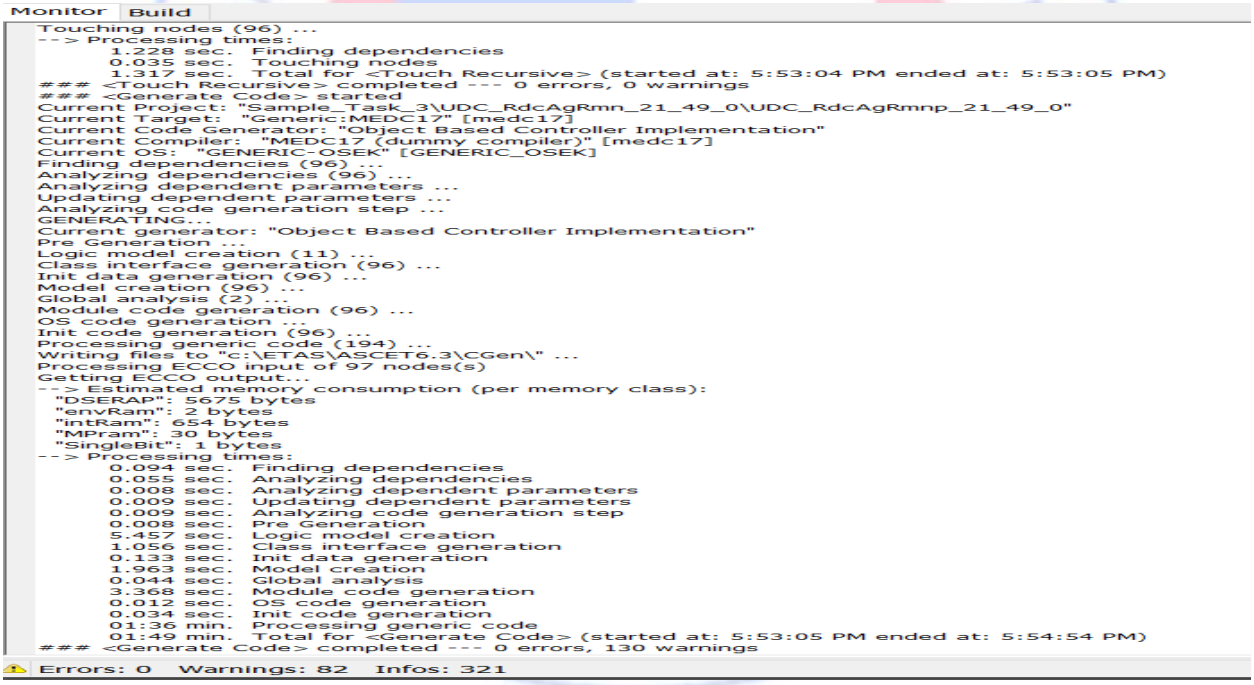

Fig 6.1: ASCET simulation result

6.2 C I Dashboard Simulation

The developed design is loaded into Continuous Integration dashboard. The design along with the code is triggered in CI dashboard.The software build result obtained is shown in Fig 6.2.

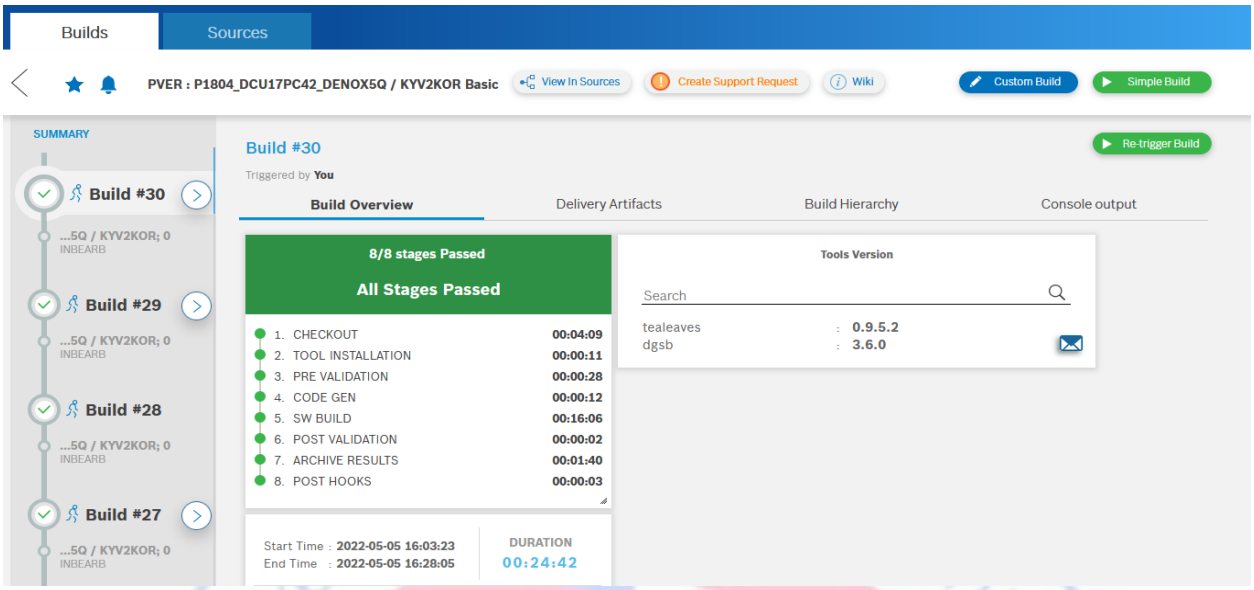

Fig 6.2: C I Dashboard simulation

6.3 ECU Worx Simulation

The delivery artifacts files downloaded from CI dashboard software build results is further loaded in ECU worx for DLL generation. Fig 6.3 shows the successful DLL generation of the urea tank level detection in diesel engine vehicles system.

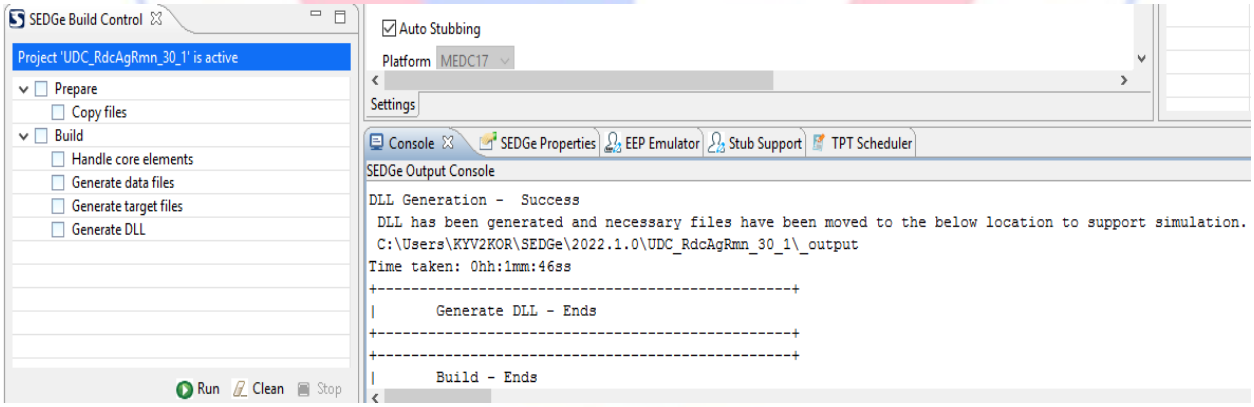

Fig 6.3: ECU Worx simulation

6.4 TPT Simulation

After successful generation of DLL file, it is loaded into piketec's TPT software and the simulation is run for testing the design as per the requirement condition. Fig 6.4 shows the simulation result of TPT and Fig 6.5 shows the overall result shown in TPT software.

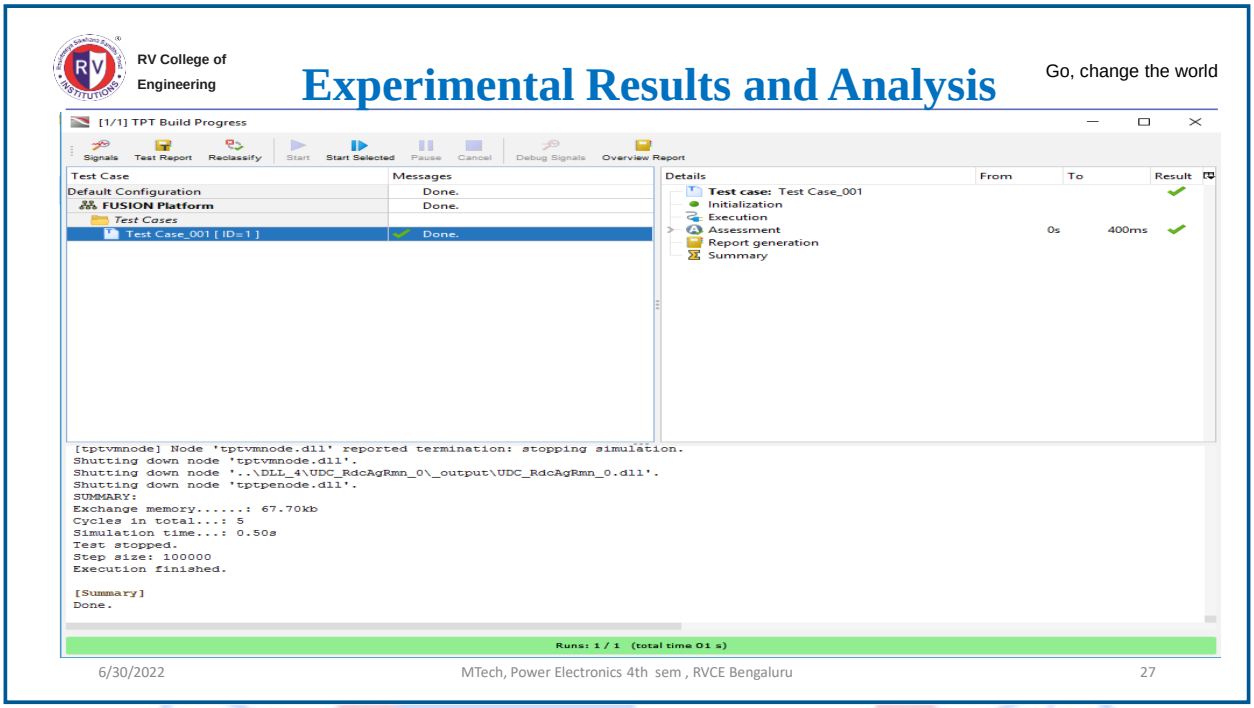

Fig 6.4: TPT simulation

Fig 6.5: TPT report overview

6.5 Summary

This chapter presents, a design satisfying all the requirements mentioned by a client for the urea tank level detection in diesel engine vehicles employing SCR technique and the simulation results of the same is laid out.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

This chapter discusses about the conclusions made from the work carried out. Also discusses about the future scope of the proposed work.

7.1 Conclusion

- A urea tank level detection system in diesel engine vehicles employing selective catalytic reduction technique is designed simulated and tested for a specific required condition.
- The literature survey explains about the importance of SCR technique and role of DEF in SCR technique.
- The objectives for the project are identified. An appropriate design satisfying the required conditions to be satisfied by the urea tank in diesel engine vehicles is developed and simulated in ASCET.
- Further the simulations are carried out in ECU Worx for documentation and DLL generation. The developed software design is build through CI dashboard and finally tested in TPT software. Lastly the developed software system is tested on a prototype in LABCAR.
- Indicators on the dash of vehicles that employ DEF inform the driver of the amount of DEF present. The level of DEF is displayed on a gauge resembling a gasoline gauge. If DEF levels are low, a warning lamp for low-DEF levels is turned on.
- The vehicle's power is significantly diminished if the DEF tank runs out completely, prompting the driver to top it off. The engine's power output is returned to normal once the tank has been filled.

7.2 Future Scope

- Efficiency gains in the future are linked to a greater adoption of technologies that have already shown to be commercially viable as these technologies become more widely used and more affordable.
- Examples of other technologies include cooled EGR, integrated exhaust manifolds, variable valve lift, variable geometry turbochargers, cylinder deactivation, and variable compression ratio.

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RV College of Engineering

SIMULATION TESTING AND DIAGNOSIS OF UREA TANK LEVEL DETECTION IN DIESEL ENGINE VEHICLES

Go, change the world

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Abstract

Exhaust emission control from internal combustion engines have become one of the most important challenges. It can affect the human's health and the ecosystems they rely on in water and land. Control of emission in internal combustion engines can be achieved either by controlling combustion or by treating the exhaust gas temperature. The latter is comparatively easier since there is less or no need to modify the engine itself. This project focuses on the modification of existing engine control unit for enhancing exhaust emissions and hence to improve drive ability. Also, enhancement of the existing functional component in exhaust system is done to overcome the customer issues and automated testing is done. Simulation, diagnosis and testing of urea tank placed in diesel engine vehicles for certain specific required conditions is performed in ASCET, ECU Worx, Continuous Integration Dashboard and TPT software packages.

Objectives

The objectives of the proposed work are:

- Define and analyze the specific required conditions specified by the client.
- Design and development of "Urea Tank Level Detection System" in diesel engine vehicles employing SCR technique in ASCET software according do the requirements.
- To Simulate, diagnose and test the developed system in ECU worx, CI dashboard and TPT software package, respectively.

Introduction

- What is NOx ?
- Causes of NOx
- Sources of NOx
- Why diesel engine vehicles?

Otto-cycle/S. I Engine	Diesel cycle/C. I Engine
Mixture of air fuel is admitted during suction stroke.	Only air is admitted during suction stroke.
Low compression ratio	High compression ratio.
charge is ignited by spark plug.	ignited by high temperature of compressed air.
Explosion takes place at constant volume process.	Expansion takes place at constant pressure process.
Quantity method of governing is used.	Quality method of governing is used.
Light in weight.	Heavier in weight.
Low thermal efficiency.	High thermal efficiency.

- Solutions for NOx reduction in diesel engine vehicles

Exhaust gas recirculation Selective catalytic reduction

Literature Gaps

- Selective Catalytic Reduction, a promising technique in NOx reduction in diesel engine system employed for the NOx reduction in this proposed work.
- DEF is an integral part of the emissions control system and must be always present in the tank to assure continued operation of the vehicle or equipment.
- Low-DEF supply triggers a series of escalating visual and audible indicators to the driver or operator. Once the tank reaches a certain level near empty, the starting system may be locked out the next time the vehicle is used, preventing the vehicle from being started without adequate DEF.

Acknowledgements

- I deeply express my sincere gratitude to my guide Dr Dinesh M N, Professor, Dept of EEE, RVCE, Principal and HOD, Dept of EEE, RVCE and Panel members for their patience and valuable guidance throught this project.
- I would like to express my deepest appreciation to Bosch Global Software Technologies, Bengaluru for providing me an opportunity to carry out the project in their organization.

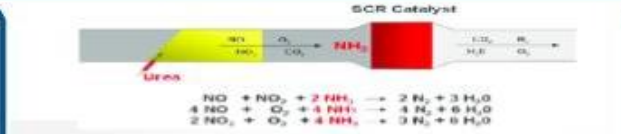


Fig. A: Basic Chemical Reaction Involved in SCR technology

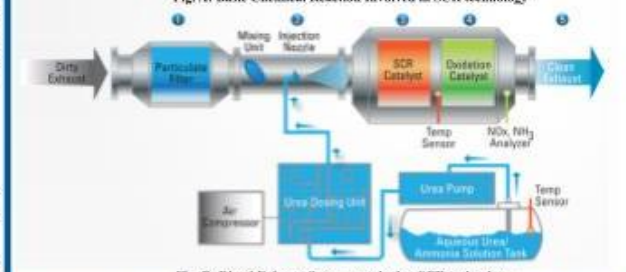


Fig. B: Diesel Exhaust System employing SCR technology

WE STILL HAVE TIME. SAVE OUR PLANET

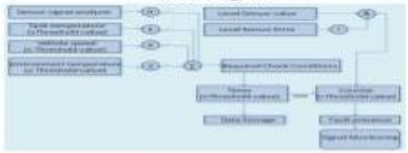
Design Requirements

1) There is no sensor related errors. 2) Tank temperature is above threshold freezing temperature. 3)Environment temperature is above threshold value. 4)Vehicle speed below a threshold value. 5)Bit mask the above conditions. 6)Validate the level sensor signals. 7)Set or reset of total number of evaluation based on release conditions. 8)Fault check diagnosis should be reported accordingly. 9)Compute number of times the error is set, and this should be available between different driving cycle.

Work Environment

1) Design and Code Generation in ASCET.
2) Documentation in ECU WORX
3) Software Build in CI Dashboard
4) Testing in TPT

Block Diagram



Results & Discussion

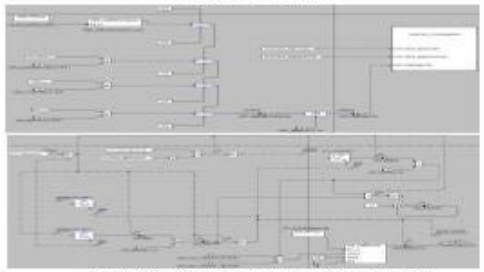


Fig. C: ASCET Design for release and level check condition

Fig. D: Simulation Results of 1.ASCET 2. ECU WORX 3. CI Dashboard and 4. TPT

Conclusion

The objectives for the project are identified. An appropriate design satisfying the required conditions to be satisfied by the urea tank in diesel engine vehicles is developed and simulated in ASCET. Further the simulations are carried out in ECU Worx for documentation and DLL generation. The developed software design build through CI dashboard and finally tested in TPT software. Lastly the developed software system is tested on a prototype in LABCAR.

Future Work

Efficiency improvements will be associated with the increased penetration of technologies in the future that are already proven to be viable for commercialisation as these technologies become more broadly accepted and cost-effective. Cooled EGR, integrated exhaust manifolds, variable valve lift, variable geometry turbochargers, cylinder deactivation, and variable compression ratio are some example technologies among others.

Dr. Dinesh M N

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JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

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Simulation and Testing of Urea Tank Level Detection in Diesel Engine Vehicles

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Abstract: One of the biggest issues now is reducing exhaust emissions from internal combustion engines. It may result in headaches, corroded teeth, permanently diminished lung function, eye irritation, and breathing issues. Indirectly, it can have an impact on people by harming the terrestrial and aquatic ecosystems that people depend on. Either combustion or the temperature of the exhaust stream can be treated to reduce emissions in internal combustion engines. The latter is easier in comparison because there is minimal, or no engine modification required. The goal of this project is to improve driveability by modifying the existing engine control unit to decrease exhaust emissions. Additionally, automated testing is performed, and the functional component of the exhaust system's existing design is improved to address customer concerns. ASCET, ECU Worx, Continuous Integration Dashboard, and TPT software packages simulate, diagnose, and test urea tanks used in diesel engine vehicles under particular needed conditions. The urea sprays, a degraded cause in SCR technology, have been used effectively to the fullest extent. It is only used in ships' mobile and fixed diesel engines. This technique significantly lowers emissions while also increasing efficiency.

Keywords: Selective Catalytic Reduction, Urea, Diesel Exhaust Fluid, NOx Reduction, Diagnosis.

I. INTRODUCTION

Nitrogen oxides are referred to as NOx. Although the majority also includes nitrous oxide (N2O) in this description, purists would argue that it only refers to nitric oxide (NO) and nitrogen dioxide (NO2). There are several other variations, but their atmospheric concentrations are insufficient. NOx emissions are caused by a) High temperature fuel combustion, which occurs when a fuel is burned at a temperature hot enough (above approximately 1300°C/2370°F) to oxidize some of the nitrogen in the air to NOx fumes. Burning hydrogen falls under this category since it burns at a high temperature; burning plant matter also produces nitrogen oxides because all plants contain nitrogen; and using nitric acid, nitrates, or nitrites in industrial or chemical processes will also produce NOx.

NOx gases are dangerous because; a) Nitrous oxide (N_2O) is defined as being 298 times as bad as CO_2 because of its radiative effect, and the time taken to break it down. For people who are lacking, the reaction with vitamin B12 could be problematic. It degrades in the stratospheric layer and aids in the ozone's decomposition rays must be absorbed by ozone in the upper atmosphere because they are dangerous if they reach the earth's surface; b) nitric oxide (NO), which easily oxidizes in the atmosphere to nitrogen dioxide and is non-toxic in small amounts; and c) nitrogen dioxide (NO2), a major pollutant and a main ingredient in smog. It produces nitric acid when it combines with water, which is why it irritates the respiratory system and eyes so badly.

Today, there is no question that air pollution poses a serious threat to everyone's health.

Nearly every nation is struggling with this issue. Over time, several nations modified technology and crisis management tactics in response to the threat posed by decreasing air quality. Environmental change as a result of a rise in global temperature has demonstrated the severity of the problem. In the United States, Europe, China, and many other places, problems with ozone and nitrogen oxides in the air are of great concern.

There is a need of some technique to cut back emission of pollutant in diesel engines. By introducing Selective Catalytic Reduction (SCR) technique it will be provided higher efficiency and reduced emissions. A sophisticated active emissions management

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device called selective catalytic reduction (SCR) injects a liquid reductant into a diesel's exhaust stream via a unique catalyst. Diesel exhaust fluid, often known as automotive grade urea, is commercially used as the reductant supply (DEF). The DEF ignites a chemical reaction that transforms nitrogen oxides into nitrogen, water, and trace amounts of carbon dioxide (CO_2), which are then ejected through the vehicle pipage.

Today most of the transport vehicles in countries like India where value effective is that the predominant criteria utilize diesel engines instead of the gasoline engines. However, it's some disadvantage conjointly, like because of hot temperature in combustion chamber ends up in formation of NOx and material that is harmful to human likewise as atmosphere.

Today most of the transport vehicles in countries like India where value effective is that the predominant criteria utilize diesel engines instead of the gasoline engines. However, it's some disadvantage conjointly, like because of hot temperature in combustion chamber ends up in formation of NOx and material that is harmful to human likewise as atmosphere.

An air and fuel mixture is fed into the combustion chamber of an internal combustion engine. Spark plug, an electrical gadget, is then used to compress and ignite this. In a diesel engine, air is pumped into the cylinder and compressed by roughly twice as much as it would be in a gasoline or extremely petrol engine. Once the fuel is injected, the heat produced by this compression causes it to spontaneously burn. Diesel fuel generates a lot of energy from a given volume despite having a lower calorific value than gasoline or other fuels.

II. EXHAUST SYSTEM

The exhaust system was initially designed as a simple duct system with the intention to safe route the toxic exhaust gas emissions from our car into harmless gases to the environment at the same time providing attenuation of noise made by the engine during combustion. Today, over the years the responsibility of exhaust system has grown. Modern exhaust systems are an integral part of combustion and pollution control thereby reducing noise, minimize harmful emissions and even give assistance in increasing fuel economy, power and hence the overall drivability. The main parts of the exhaust system cooperate to remove emissions, lessen noise, and promote smoother operation of the moving parts. Although the emission control systems may vary based on the manufacturers and the vehicles, they all are designed to meet the same goal and they work on the same principle.

The primary design consideration of an exhaust system includes:

- Minimizing the gas flow resistance and confine it to specified range depending on the engine model to achieve maximum efficiency.
- Suppressing the exhaust noise to meet the automobile regulations and requirements.
- Providing sufficient clearance between exhaust system components and engine components so as to minimize the impact of high exhaust temperature.
- Ensuring that the system does not overstress engine components with excess weight as overstressing can shorten the component life.
- Ensuring that the exhaust components are able to reject heat energy as intended.

The following elements make up the exhaust system typically:

- After-treatment tools to reduce the pollutants released, like particulate filters and catalytic converters.
- Mufflers to reduce noise.
- Components that serve as a decoupling link between the exhaust manifold and the rest of the exhaust system.
- Hangers and piping

The "hot end" of the exhaust system is the after-treatment equipment and its piping, while the "cold end" is made up of the muffler and tailpipes. The "down pipe" or "front pipe" that joins the exhaust manifold with the catalytic converter, as well as the pipework between the catalyst and the particle filter, may be included in the hot end pipe. The "middle pipe" joins the muffler and the after-treatment system. The exposure to requirements and chemical exposure affects the material choice for the exhaust system.

The exhaust manifold often thought to be a part of engine is the key component of exhaust system that collects all the exhaust gases from the combustion chamber to the exhaust pipe. The design of exhaust manifold has a major influence on the torque and performance characteristics of the engine. The flexible joint follows, which minimizes engine movement transmission to the

exhaust system. It typically sits between the catalytic converter and manifold. Hence it must withstand high temperature and it should be durable and strong.

The catalytic converter is another important component in the exhaust system that is installed between the manifold and muffler in the exhaust line. It makes use of chemicals that act as a catalyst. Prior to exiting the exhaust system, a catalytic converter causes a chemical interaction between the pollutants in the exhaust, without causing any damage to the pollutants themselves.

The IC engines usually make a whole lot of noise while operating. This noise reduction is achieved through well designed mufflers. Mufflers make use of the principle of reactive silencing which is an application of wave cancellation technique to tune out certain frequencies that are hush to our ear. By choosing appropriate design parameter we can achieve tuning for a specific range of frequencies. Since a muffler can't reduce the engine noise by itself add-on features such as resonator is included in the exhaust system. A typical resonator is a hollow steel cylindrical tube attached to the muffler. They both work together to decrease the exhaust noise. Finally comes the tail pipe that is designed to serve as an enclosed route for the exhaust emissions to exit the system.

With the emission reductions strategies being more stringent, major technologies are deployed to reduce emissions. Some of them include:

2.1 OXIDATION CATALYST

The oxidation catalyst sown in Fig 1, can cut CO and HC emissions by more than 90% and harmful HC emissions by more than 70%. Toxic by-products are created when there is not enough oxygen present in an internal combustion engine to oxidize carbon fuel into carbon dioxide and water. The redox conversion of toxic fuel by-products into less dangerous compounds takes place in catalytic converters. It is made up of a steel housing, a ceramic or monolith honeycomb interior, and a metallic substrate. Platinum (Pt), palladium (Pd), and rhodium are combined to form the honeycomb structure, which maximizes the surface area for greater reaction to occur (Rh).

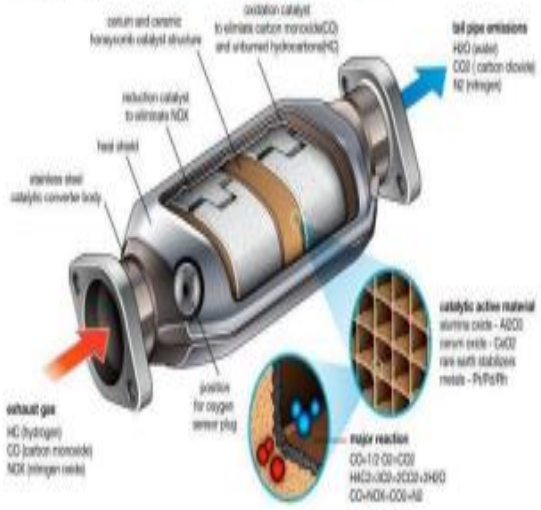

Fig - 1: Oxidation Catalyst.

The catalyst initially starts a reduction reaction to reduce nitrous oxide. The nitrogen atom in nitrous oxide is eliminated as it passes through the Pt and Rh catalyst, allowing free oxygen to produce oxygen gas O2. The nitrogen atom then interacts with other nitrogen atoms linked to the catalyst to produce nitrogen gas N2. In the second stage, an oxidative catalyst made of Pt and Pd is used to regulate carbon monoxide (CO) and unburned hydrocarbons (HC). Carbon dioxide (CO2) is created when carbon monoxide (CO) combines with oxygen in the air, and water is produced when hydrocarbons are oxidized (H2O). Water is formed when hydrocarbons are oxidized, and carbon dioxide (CO2) is made when carbon monoxide (CO) and oxygen in the air combine (H2O). When it comes to decreasing emissions from gasoline engines, catalytic converters are dependable and effective.

When coupled with diesel engines, which operate more coolly than gasoline engines, they are less effective. Higher temperatures are ideal for catalytic converter operation. Particles like soot will also be produced by diesel engines. Thus, combining a particulate filter and a catalyst can cut down on ultra-fine particle emissions by up to 99 percent.

2.1 PARTICULATE FILTERS

To comply with particulate matter emission restrictions, the particulate filters in Fig 2, are fitted (PM). Particulate filters eliminate particles smaller than 100 nm that are made up of carbon, ash, and unburned hydrocarbons. Since the filter's capacity is limited, the trapped soot increases flow resistance, necessitating its emptying or burning off in order to replenish the DPF. The extra soot particles that gathered in the filter after about 800 to 2000 kilometers of driving are thoroughly burned during the regeneration process. At temperatures above 600 °C, the deposited soot is then burned off together with the exhaust fumes. Since this temperature is typically not attained during routine driving, the exhaust temperature is raised through post-injection, delayed main injection, and throttle valve air mass reduction. The exhaust outlet valve's temperature then rises as a result. The temperature is also raised by the exothermic reaction of unburned hydrocarbons in the oxidation catalytic converter. The particle filter is often placed close to the exhaust manifold and frequently used in conjunction with an oxidation catalyst in order to prevent significant heat loss.

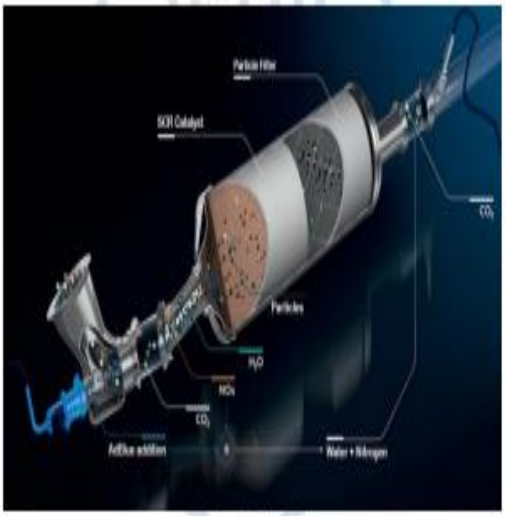

Fig - 2: Particulate Filter.

2.3 EXHAUST GAS RECIRCULATION

Exhaust gas recirculation (EGR), which reduces the oxygen content in the combustion chamber and absorbs heat, is an efficient method for reducing NOx emissions. By using the inlet system, it is a technique for returning some of the exhaust gas to the combustion chamber. By providing inert gases to the combustion process and limiting the amount of oxygen present in the incoming air stream, this lowers the peak in-cylinder temperatures. Fig 3 is a schematic illustration of an EGR system. When air oxygen and nitrogen are combined at high temperatures in the combustion chamber, which typically happens at peak cylinder temperature, NOx is formed. The composition of the gas introduced into the cylinder during the engine cycle will change as a result of the mixing of exhaust gas with intake air. Significantly less oxygen will be present, but more CO2 and water from burning will be produced. A drop in the peak temperature of the diesel combustion flame is the main factor causing EGR's NOx reduction impact.

The exhaust gas added to the oxygen, fuel and combustion products will increase the specific heat capacity of the cylinder which lowers the adiabatic flame temperature. A properly operating EGR can increase the engine efficiency. Automotive exhaust system is one of the inevitable parts of combustion and emission control system that is designed to perform one or more of the following functions: remove solid materials from the exhaust gas, muffle the exhaust noise, quench sparks and furnish energy to a turbine-driven supercharger. Thus, keeping our exhaust system in better working condition is vital for fuel consumption, safety and environment. The durability of the exhaust is crucial.

Fig - 3: Exhaust Gas Recirculation.

III. ENGINE ECU

Before the automotive industry adopted electronics, cars were thought of as mechanical machines. Through the principle of mechanics, every component in a vehicle, from the engine to the window, brake, and steering, was mechanically driven on gears. However, the inherent limitations and poor accuracy of these mechanical systems led to undiscovered failures and a high risk of harm to the users. These restrictions made it possible for the car industry to innovate more effectively. This finally resulted in the use of electronics in vehicles.

Since its introduction to the automotive industry in 1970, automotive electronic control units (ECUs) have grown to be a significant part. It has been crucial to the evolution of the automobile from a wholly mechanical to an electronic-dominant machine. To control and regulate the functionality, modern cars feature around one hundred embedded or fitted ECUs.

The electronic control unit (ECU) seen in Fig 4, is a computer with inbuilt programmable and pre-programmed chips that uses microprocessors and sensor data that may be processed to conduct real-time control of a number of actuators. For the gearbox, traction control or ABS, body functions, lighting control, AC, engine, air bags, and other sections of the car, there are numerous distinct Ecosite power train, body control, and chassis system are the three main units for which an automotive ECU can be used. The ECU, which is a component of the Power-train Control Module (PCM), is in charge of controlling the combustion process, including opening and closing the inlet or outlet valve in response to input from the accelerator pedal.

The ECU regulates the timing of the fuel injection rate and spark ignition. Thus, compared to vehicles with mechanical controls, ECUs produce accurate synchronization and increase power, efficiency, and functionality. Sensors have a significant impact on how an ECU function. Instead of sending numerous wires from the sensor to various ECUs, the ECU will share information with other ECUs over communication network lines for control operations. Most vehicles include an OBD connector that the ECU uses to transmit all diagnostic data to all other ECU modules.

Fig - 4: Engine ECU

Government regulatory bodies have imposed strict restrictions on the emission levels from automobiles hence OEMs are responsible for implementing emission controls in automobiles. Implementing such restrictions would have been a mission impossible without the use of ECUs and software algorithms. With automation the regulatory bodies are able to respond to emergency situations in a better way. Also, with the advancement in mobile phones, car manufacturers had slowly transformed car with the explosion of electronics to introduce web connectivity, smart devices and navigation control.

Astonishing amounts of data are processed by an ECU. To obtain maximum performance, a number of operations must be carried out simultaneously. With the aid of sensors, the ECU enables the processing of all the data that the engine receives. The automakers can configure the ECU in such a way that some car models have very smooth rides while others have a more racing-inspired feel. ECU thus enables us to have these two unique traits in a single car. To accommodate greater and better performance, ECUs are periodically reset. Thus, the performance provided by the ECU makes driving more enjoyable than difficult.

IV. DIESEL AND GASOLINE SYSTEM

The development of the gasoline engine marks the beginning of the diesel saga. The four-stroke combustion principle known as the "Otto cycle" was created by Nikolaus August Otto, who also received a patent for the idea. In the beginning, gasoline engines weren't very efficient because only 10% of the fuel they used actually moved the car. The remainder was transformed into waste heat. After learning about the inefficiency of gasoline engines, Rudolf Diesel was motivated to develop an engine with improved efficiency. He spent a significant amount of effort developing a "combustion power engine. "Diesel was able to patent a diesel engine by 1892 as a result.

Diesel and gasoline engines are conceptually pretty similar. They are IC engines made to transform fuel's chemical energy into mechanical energy. The pistons inside the cylinders are then moved up and down, creating a linear motion, using this mechanical energy. To turn the wheel forward, a rotary motion is produced by a crankshaft that is coupled to the pistons. A gasoline and diesel engine's explosion process is depicted in Fig 5. Both diesel and gasoline engines use a sequence of explosions or combustions to transform fuel into mechanical energy. But how these explosions happen makes a significant difference. Fuel and air are combined in gasoline, which is then compressed by pistons and ignited by sparks from spark plugs. In a diesel engine, the fuel is injected after the air has been compressed. Compression warms the air, which causes the fuel to ignite.

The following is how an explosion happens in a gasoline engine:

1) Intake stroke - Here, gasoline and air are combined.

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2) Compression stroke — Piston rises, compressing the air-fuel mixture.

3) The air-fuel mixture is ignited by a spark plug during the ignition stroke.

4) The piston rises and pushes the exhaust out the exhaust valve during the exhaust stroke.

The following is how an explosion happens in a diesel engine:

1) The intake valve opens and fills with air during the intake stroke.

2) Air is compressed during the piston's upstroke during the compression stroke.

3) The air-fuel mixture is ignited once fuel is introduced into the engine.

4) The piston rises and pushes the exhaust out the exhaust valve during the exhaust stroke.

Spark plugs are not used in diesel engines. To produce the high temperatures required for fuel ignition, they require high compression ratios. Of comparison to a gasoline engine with a ratio of 8:1 to 12:1, the compression in a diesel engine with a ratio of 14:1 to 25:1 is significantly higher. Higher thermal efficiencies and improved fuel economies are produced by higher compression ratios. The engine's compression ratio is constrained by the compression of the air-fuel mixture. The air-fuel mixture ignites spontaneously and creates knocking, which might harm the system, if there is more air compression.

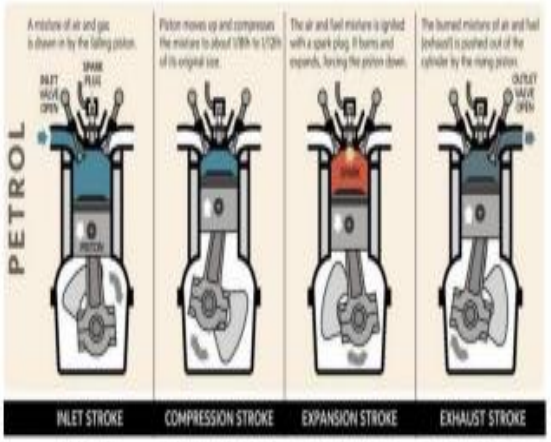
An essential part of a diesel engine is the injector. It ought to be able to withstand the pressure and heat inside the cylinder while dispensing the fuel as a fine mist. Glow plugs are used in some diesel engines to warm the combustion chamber and increase air temperature when the engine is cold.

Today, a complex system of sensors measuring everything from RPM to engine coolant and oil temperature and TDC is used to operate every function of a contemporary engine. On contemporary engines, glow 27 plugs are rarely used. ECM detects the temperature of the surrounding air and delays the engine's timing so that the injector sprays fuel later. As a result, the air is compressed more and produces more heat, which helps the engine start.

Diesel and gasoline engines show a number of development paths for better torque generation, fuel efficiency, emission control, and noise reduction.Improved driveability features, increased specific power, better noise attenuation, decreased fuel consumption and CO2 emissions, decreased specific emissions (HC, NOx, CO, particulates, and dust), reduced friction, and effective exhaust after treatment systems are some of the most recent engine technology advancements.

Engines are equipped with mechatronic parts such electronic throttle intake systems, high-pressure common rail injection systems with solenoid or piezoelectric injectors, VVT, VGT, and variable camshafts to increase their variety and control functions. These parts can be categorised as electrical, pneumatic, or hydraulic actuators, solenoid and switching injection valves, electrical drives, pumps, and fans.

While some of these are controlled centrally by an ECU, others are controlled locally by sensors that are incorporated locally. The development of hybrid drives, which improve fuel efficiency and reduce pollutants, is a cutting-edge step in the electrification of automobiles. All of these developments suggest that electronics will continue to increase rapidly and that mechatronic design will generally improve. The proliferation of electronic components emphasises how important fault diagnosis functions are



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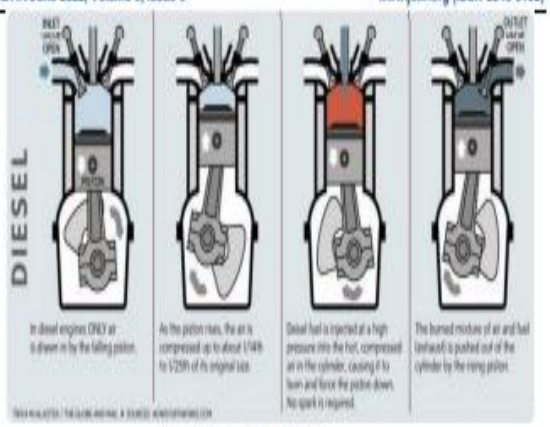

Fig – 5: Gasoline and diesel engine.

V. SCR WORKING PRINCIPLE

The essential parts of the urea SCR system are represented schematically in Fig 6, together with the DOC (Diesel Oxidation Catalyst), DPF (Diesel Particulate Filter), DEF (Diesel Exhaust Fluid), and SCR. Engine exhaust is sent to DOC, where the hydrocarbons are transformed into carbon particles. The DPF gathers and preserves the carbon atoms. These soot particles are frequently burned. SCR uses alkali and NH3 as a reductant to lower NOx emissions in the exhaust gas. DEF is an aqueous solution that is sprayed into the exhaust stream to reduce NOx. It contains 32.5 percent urea and 67.5 percent deionized water. It was discovered that DEF usage accounted for 2% of gasoline consumption.

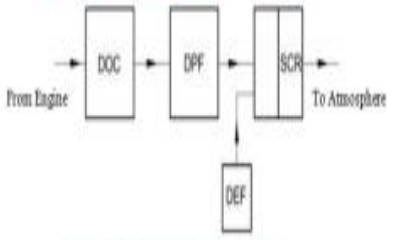

Fig – 6: Schematic diagram of urea SCR.

Pollutant emissions from diesel engines, such as soot (also known as particulate matter, or PM), and NOx, typically exceed the legal limits. Recent research has shown that cutting these pollutants by more than 46 to 90 percent is possible with sophisticated diesel aftertreatment systems. More than 90% of the particulate matter (PM) in the exhaust gas from a diesel engine can be captured by a DPF, also known as a catalytic particulate filter (CPF). The DPF removes CO and CO2 after oxidising the particles it has caught using the thermally aided and NO2-assisted reactions described in Equations. (4) and (6). DPF regenerations are the common name for those procedures.

5.1 CHEMICAL REACTIONS INVOLVED

Urea breaks down into ammonia and isocyanic acid when DEF is injected into the exhaust stream because of the exhaust temperature.

$$(NH2)CO(NH2)\,(molten) \rightarrow NH3 + HNCO \quad \ldots\ldots (1)$$

Ammonia and carbon dioxide gases are created as a result of the hydrolysis of this isocyanic acid.

$$HNCO + H2O \rightarrow CO2 + NH3 \quad \ldots\ldots (2)$$

Oxides of nitrogen are now reduced by ammonia in the presence of oxygen and an SCR catalyst

$$4NH3 + 4NO + O2 \rightarrow 4N2+H2O \quad \text{..... (3)}$$

$$8\ NH3 + 6NO2 \rightarrow 7N2+12\ H2O \quad \text{..... (4)}$$

$$4\ NH3 + 2NO + 2NO2 \rightarrow 4N2+6\ H2O \quad \text{..... (5)}$$

$$2\ NH3 + 2NO2 \rightarrow NH4NO3 + N2 + H2O \quad \text{..... (6)}$$

Equation (1) demonstrates how the high temperature of the exhaust causes molten urea to break down into ammonia and hydrocyanic acid. Ammonia and carbon dioxide are the major by-products of the isocyanic acid hydrolysis shown in equation (2). These two reactions take place without the need for a catalyst. Equation (3) represents the typical reaction in which oxygen and the equal amounts of ammonia and NO are involved. The quick and slow SCR reactions are shown in equation (4). At temperatures below 2000 C, ammonium nitrate is formed as a result of some unfavourable reactions.

Numerous competitive & nonselective reactions with oxygen, which is plentiful in the system, are among the undesirable activities that take place in SCR systems. These reactions can either result in additional emissions or, at worst, use ammonia ineffectively. Nitrous oxide (N2O) or elemental nitrogen may result from the partial oxidation of ammonia, as shown in Equations (7) and (8). Nitric oxide (NO) is produced by the complete oxidation of ammonia, as demonstrated by Equation (9).

$$2NH_3 + 2O_2 \rightarrow N_2O + 3H_2O \quad \text{..... (7)}$$

$$4NH_3 + 3O_2 \rightarrow 2N_2 + 6H_2O \quad \text{..... (8)}$$

$$4NH_3 + 5O_2 \rightarrow 4NO + 6H_2O \quad \text{..... (9)}$$

The ammonia injection rate needs to be precisely controlled for the SCR process. Low NOx conversions due to insufficient injection may be unacceptable. Unwanted ammonia is released into the atmosphere when the injection rate is too high. Ammonia slip refers to these ammonia emissions from SCR systems. At greater NH3/NOx concentrations, the ammonia slip increases. The stoichiometric NH3/NOx ratio in the SCR system is around 1, according to Equation (2), which describes the primary SCR reaction. The ammonia slip is greatly increased by ratios greater than 1. In reality, ratios between 0.9 and 1 are employed to reduce ammonia slip while maintaining sufficient NOx conversions.

It is clear from the chemical reactions discussed above that NO2 is crucial to the reactions taking place inside DPFs and SCR catalysts.The presence of NO2 can hasten the regeneration of the DPF, and a higher NO2/NOx ratio (but not more than 50%) can hasten the effectiveness of the SCR's NOx conversion.Although NO makes up the majority of the NOx composition of diesel engine exhaust, it is known that a higher NO2/NOx ratio is advantageous for DPF PM removal and SCR NOx reduction.

Due to this property, diesel oxidation catalysts (DOCs) are frequently utilised upstream of DPFs and SCRs to increase their performance. DOCs catalyse the conversion of a portion of NO to NO2 and can result in a greater NO2/NOx ratio than engine-out exhaust.Figure 2.2 depicts a typical configuration for a diesel engine's aftertreatment system (DOC-DPF-SCR).One of the key factors in the performance analysis of SCR NOx conversion is the effectiveness of NOx conversion in diesel engine cars.SCR NOx conversion = [1 – (NOx out/NOx in)] 100% provides the answer.

VI. WORK ENVIRONMENT

The details of the various software used to carry out the proposed work is as listed below:

6.1 DESIGN AND CODE GENERATION IN ASCET

Advanced Simulation and Control Engineering Tool is referred to as ASCET. It is a multifaceted and adaptable product family that offers an original approach to the functional and software design of contemporary automotive embedded systems. With

a fresh take on modelling, code generation, and simulation. ASCET supports each step of the development process, enabling improved quality, quicker innovation cycles, and lower costs. ASCET makes it simple to blend text and visuals to meet our programming requirements. Our logic can be modelled in a variety of ways, allowing us to operate as effectively as we see fit.

As a result, we have four specification options.:

1) Graphic specification using Block Diagram;

2) Graphic specification using State Machine Editor;

3) Textual specification using ESDL Editor;

4) Textual specification using C Code Editor

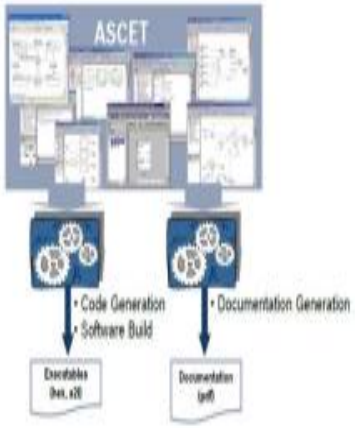

Fig - 7: Working of ASCET tool.

ASCET tool operation is depicted in Fig 7. Using graphical models and textual programming notations, ETAS ASCET is a tool for creating software for embedded systems. The created function models will be converted by the ASCET Code Generator into extremely effective and secure embedded C-Code for AUTOSAR applications.

The ASCET has been specifically created to meet the difficulties in software development for sectors where goods must be produced in large quantities, at a lower cost, in compliance with industry standards, and without any flaws. The ASCET tool gives software engineers the ability to create embedded software that is high performing, low overhead, simple to maintain, secure, and safe. High levels of automation enable productive and safe workplaces.

The ASCET tool for Automotive Software Development has the following features:

- Safe – Automatic introduction of defensive code, ISO26262 and IEC61508 TUV-certified code generation, MISRA-C:2012 compliance.
- Proven in usage – Used for brake systems (such ABS, ESP), powertrain, generation, compliance with MISRA-C:2012 Proven in use – Used for brake systems (such ABS, ESP), powertrain, Driver assistance, Battery management, 450+ million ECUs on the road are powered by ASCET produced code.
- Flexible – Multiple specification notations, Block diagram, state machine, textual editor for ESDL, and C-code editors.
- Quick and effective — Real-time static analysis for quick feedback, quicker code creation.
- A variety of testing alternatives, including unit testing, PC-based open-loop simulation, closed-loop simulation, and rapid prototyping.
- Embedded Software Development Language (ESDL), which has an abstract data type, easy-to-understand syntax, and object-oriented encapsulation.

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6.2 DOCUMENTATION IN ECU WORX

ECU Worx is software used to custom tools for tuning and modifying the Electronic Control Unit used in cars and other passenger vehicles. In this software, the documentation containing all the details of the project is prepared and necessary changes if required can be modified. Also, a DLL: Dynamic Link Library file can be generated in ECU Worx. A DLL is a library that has data and code that can be utilised by several programmes at the same time. By using a DLL, a program can be modularized into various separate components. The example of ECU Worx software is as shown in Fig 8.

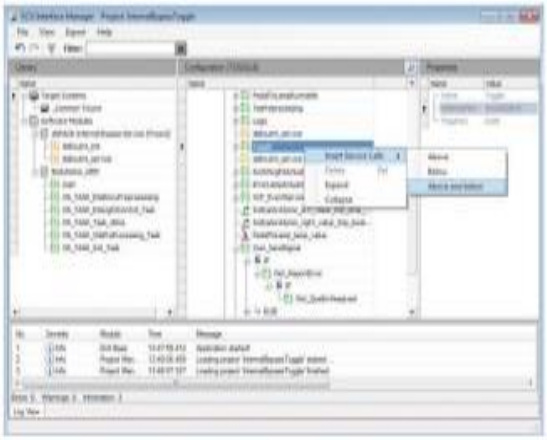

Fig - 8: Example ECU Worx software image

6.3 SOFTWARE BUILD IN CI DASHBOARD

The Continuous Integration dashboard displays key metrics for builds that can be used to gain insight into the organization's build throughput and to bubble up any of the potential build issues. The Continuous Integration dashboard provides indicators to measure the agility of development. An example image of CI dashboard is as shown in Fig 9.

Fig - 9: Example CI dashboard software image.

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6.4 TESTING IN TPT

Piketec's Time Partitioning Testing programme is known as TPT. With TPT, one may test embedded control systems and ECU software during all phases of development, including model-in-the-loop (MiL), software-in-the-loop (SiL), processor-in-the-loop (PiL), hardware-in-the-loop (HiL), and ECU and vehicle testing. TPT offers special tools to help you write those tests freely and easily, whether you're creating a basic module test or a comprehensive system test. Fig 10. displays an illustration of a TPT software image.

VII. DESIGN REQUIREMENTS

1. There are no sensor related errors.
2. Tank temperature is above threshold freezing temperature.
3. Environment temperature is above threshold value.
4. Vehicle speed below a threshold value.
5. Bit mask the above conditions.
6. Validate the level sensor signals.
7. Set or reset of total number of evaluations based on release conditions.
8. Fault check diagnosis should be reported accordingly.
9. Compute number of times the error is set, and this should be available between different driving cycle.

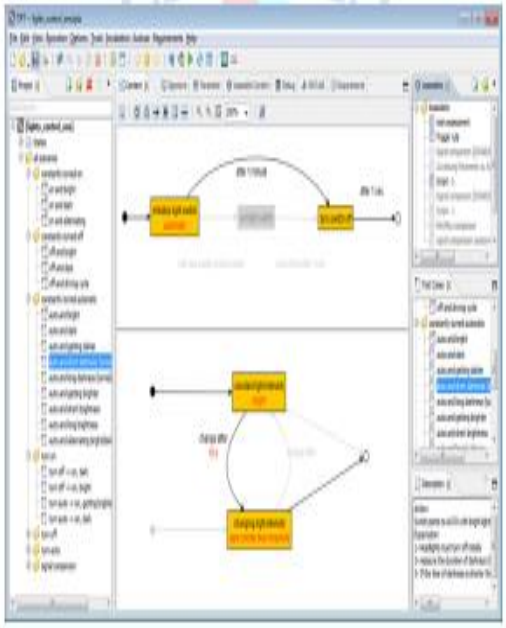

Fig - 10: Example TPT software image.

VIII. BLOCK DIAGRAM

The block diagram of the urea tank level detecting system used in diesel-powered cars is shown in Fig 11. A block diagram is used to show the fundamental design in accordance with the particular conditions specified by the client. The block diagram shows

the interconnection of the numerous sensors as well as the timer and counter for the various fault checks, continuous monitoring, reporting, diagnostics, and data storage.

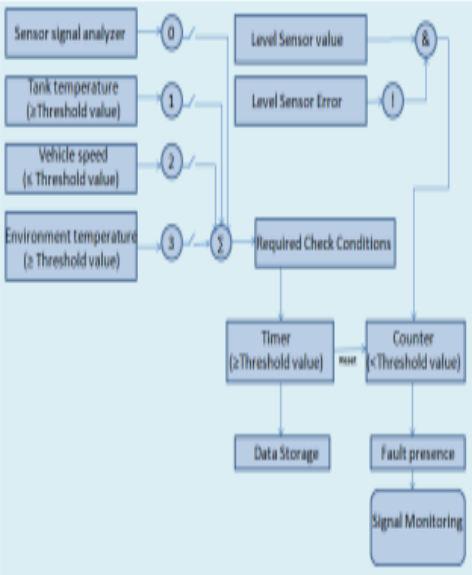

Fig - 11: Block diagram.

IX. SIMULATION AND RESULTS

According to the design requirements, part A design as shown in Fig 12 satisfies the design condition 1 to 5 mentioned under section VII. In Fig 12, function type identifies the type of incoming signal and the sensor error detection block helps in identifying the presence of any errors. If there are no sensor related errors, it passes on the signal to the putbit. Tank temperature sensor measures the urea tank temperature and if the measured value is greater or equal to a preset threshold value, then the second bit input signal is passed onto putbit. Similarly vehicle speed and environment temperature is measured by respective sensors and compared with the threshold value. If the Vehicle speed is lesser or equal to its threshold value and the environment temperature is greater or equal to its threshold value, then the third and fourth signal is obtained by a putbit. Bitmask option is provided so as to select the conditions mentioned above. One has an option to select the conditions as required according to the necessary demand, until the design and testing stage only.

If all the cumulative conditions are true, then the selected signal block passes on the signal to the next stage of design. Part B design shown in Fig 13., has continuous urea tank level sensor updating signal along with the level sensor error detection block. If there is any tank level signal update and there is no level sensor error, in the presence of the previous obtained selected signal, counter is set to compute the number of times the error has occurred between different driving cycle. If the count is less than the set threshold value then it reports, no fault to the signal monitor. If the count is greater or equals to the set threshold value, then it reports the presence of fault in the system to the signal monitor. Also, when the selected signal block passes its output, a timer is triggered to monitor the duration of fault occurrence. If the required timer value is greater or equals to the set threshold value a timer output is generated to reset the counter, timer and a trigger to non-volatile memory for data storage.

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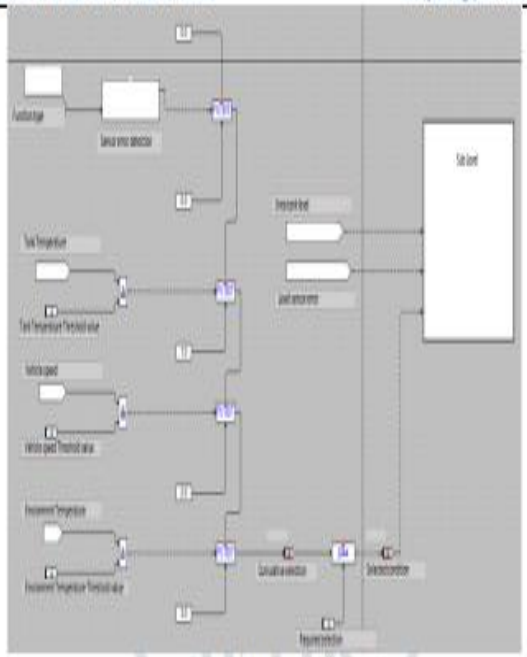

Fig - 12: Part A Design.

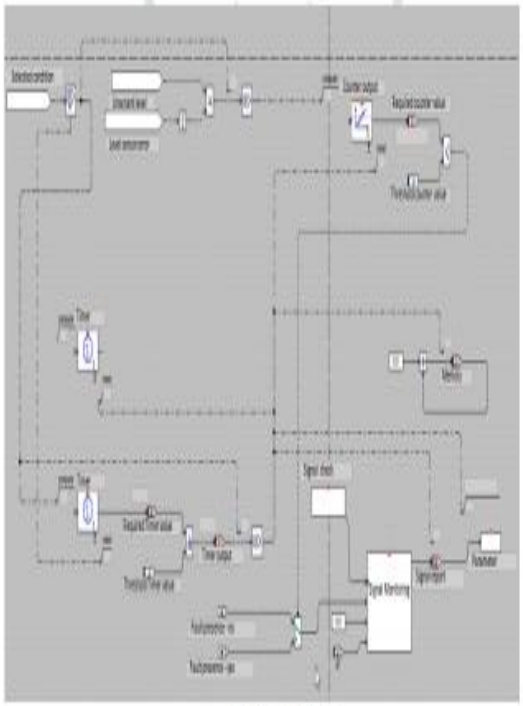

Fig - 13: Part B Design

Fig - 14: TPT report overview.

After the successful design, documentation in ECU Worx is performed by editing fs.xml file in an appropriate editor to maintain the record of the project. The modifications are made in SDOM, a project that intends to provide a comprehensive Scheme implementation of the Document Object Model API suggestion made by the W3C. To check for defects in the programme code, design, and other areas, the document is created using CI dashboard.. If the build is successful, DLL generation in ECU Worx is performed to generate a .dll file for the testing purpose in TPT software.

To determine whether the generated design satisfies all of the conditions as illustrated in Fig 14, test cases are written in the Time Partial Testing software. For test management, a thorough and customizable test report that includes the computed test results and pertinent test data is produced. Specifying expected values in test cases is the simplest type of assessment. The expected values are given as a system output in this location, right next to the test stimulus. The tolerance requirements are extremely simple to include in TPT.

X. CONCLUSION

A urea tank level detection system in diesel engine vehicles employing selective catalytic reduction technique is designed simulated and tested for a specific required condition. The literature survey explains about the importance of SCR technique and role of DEF in SCR technique. The objectives for the project are identified. An appropriate design satisfying the required conditions to be satisfied by the urea tank in diesel engine vehicles is developed and simulated in ASCET. Further the simulations are carried out in ECU Worx for documentation and DLL generation. The developed software design build through CI dashboard and finally tested in TPT software. Lastly the developed software system is tested on a prototype in LABCAR.

Indicators on the dash of vehicles that employ DEF will inform the driver of the amount of DEF present. The level of DEF will be displayed on a gauge resembling a gasoline gauge. When DEF levels are low, a warning lamp for low-DEF levels will turn on. The vehicle's power will be significantly diminished if the DEF tank runs out completely, which will prompt the driver to top it off. The engine's power output will return to normal once the tank has been filled.

Efficiency gains in the future will be linked to a greater adoption of technologies that have already shown to be commercially viable as these technologies become more widely used and more affordable. Examples of other technologies include cooled EGR, integrated exhaust manifolds, variable valve lift, variable geometry turbochargers, cylinder deactivation, and variable compression ratio.

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TO WHOMSOEVER IT MAY CONCERN

This certificate is being awarded to Mr. Manjunath DV (**USN:** 1RV20EPE01), a student from **R.V. College of Engineering** has done his internship with our Power Electronics department, Bangalore from the 1st of September 2021 to the 30th of Jun 2022.

His project title was "Design and implementation of 3ph inverter for BLDC motor using hysteresis current control technique" and has completed his project under Dr. Narasimha MV Chief of Advance Engineering, R&D.

During the tenure of the internship at Ampere, his conduct, character, and interest to learn were found good.

We wish him all the best in his future endeavors.

Thanks & regards,

Vithal Acharya

Head – Human Resources

Greaves Electric Mobility Pvt Ltd

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ABSTRACT

The use of The Brushless DC (BLDC) motor has drastically increased in domestic and industrial applications, due to several distinct advantages such as absence of bushes, higher performance, increased reliability, energy efficient and minimal maintenance requirements. The problem associated with the conventional speed control techniques like PI control method and vector control method is that they result in generation of harmonics in load current and the adopted motor control algorithm was too complex (vector control) to drive the BLDC motor. The problem can be overcome by using hysteresis current control technique, that results in increased robustness and reduced harmonic content.

This project focuses on the design of a motor control system for a three-phase brushless dc motor with hysteresis current control technique. The selected topology comprised of three phase inverter, Arduino Uno (ATmegaS128 Microcontroller), gate driver circuit, MOSFET switches, ACS712 hall sensor, IR sensor and A2212 BLDC motor. The selected motor rating was 150W (max). The inverter drives the motor resulting in optimized AC power of desired output voltage and frequency. In hysteresis current control technique, the difference between the recommended and measured currents was monitored and tracked. As a result, the reference gating signals were generated. The generated gating signals were used to trigger the switches of three phase inverter.

The proposed project was simulated using Proteus and MATLAB/SIMULINK tools. During simulation analysis speed and current characteristics were observed. The Hardware implementation was carried out on general Printed Circuit board (PCB). The Hardware module comprised of three phase inverter, microcontroller board, hall sensors and BLDC motor itself. During hardware analysis it was observed, for input a of 12V DC to three phase inverter, the output of approximately 5.8V AC was observed. The data of three line currents of BLDC motor was tabulated for a input voltage of 12V under no load condition and for a input voltage of 9V and 12V under loaded condition. The speed vs current characteristic of BLDC motor was plotted. The characteristic showed that speed control of BLDC motor was robust.

LIST OF PUBLICATIONS

Publication Type	Publication Details
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GLOSSARY

ATMEL	: Advanced Technology for memory and logic
BLDC	: Brushless DC Motor
D	: Duty ratio
EEPROM	: Electrically erasable programmable read-only Memory
HCC	: Hysteresis current control
MOSFET	: Metal oxide semiconductor field effect transistor
PCB	: Printed circuit board
PWM	: Pulse width modulation
VSI	: Voltage Source Inverter

CHAPTER 1

INTRODUCTION

The automobile industry has been rapidly changing in recent years thanks to a new path of development termed electrification. Global warming is the primary cause of this evolution, and it provides an answer for automakers of vehicles like motorcycles, automobiles, and buses to meet more stringent CO2 and emission requirements. The electrical vehicle revolution is just one of various strategies. Electric vehicles have evolved into a great emission-reduction solution.

The battery, battery management system, control unit, and the motor itself are the main components of electric vehicles. There are two different types of battery packs: one is a lead acid battery, and the other is a Li-ion battery. Because it has a higher energy density compared to lead acid, the Li-ion battery type is much more popular [1]–[5]. Different types of motors, including DC motors, brushless DC motors, magnet electric motors, three-section AC induction motors, and switching reluctance motors, are used in heat units. BLDC type and internal magnet motors are the most popular motors (type of PMSM) currently in market [6]-[8].

Brushless dc (BLDC) motor drives are getting wide utilized in many domestic and industrial systems, like servo motor drives, home appliances, laptop peripherals, and automotive applications [9], [10].

The popularity of BLDC drives has increased as a result of developments in power electronics and vector control technologies. External control of AC output voltage, external control of DC input voltage, and internal control of the inverter within the inverter itself are some of the several techniques for controlling the output voltage of inverters [11].

The three closed loops that comprise the electric motor system are the position loop, speed loop, and current loop. The performance of the entire system is significantly influenced by the present control loop, and is the inner one. The current controller's (CC) primary responsibility is to force the real current to follow the command current from speed loop [12].

The development of a dynamic FPGA based PI speed controller operating for Hysteresis Current Control mechanism. The controller is developed for the model of a BLDC motor; hall sensor signal feeds back the rotor position to the controller through rotary hall encoder. The motor attains the steady speed in very less time, thereby accomplishing the effectiveness of the designed controller. In addition, the fast response of the controller under dynamic/fault conditions makes it deployable in industries and further in the research area of motor fault diagnosis [13].

Depending on the kind of supply source and the associated topology of the power circuit, the inverter, also known as a dc to ac converter, is used in the project work Inverter generally falls under the categories of current source inverters and voltage source inverters (VSIs) (CSIs). Applications requiring low to medium power range uses single-phase VSIs topology and medium to high power range uses three-phase VSIs topology [14], [15].

Motor drives, active filters, and unified power flow controllers in power systems and uninterrupted power supplies all often employ three-phase dc/ac voltage source inverters. Various pulse width modulation (PWM) techniques are used to achieve controlled frequency and ac voltage magnitudes. It contains six switches, and the turn on of switches is determined by the modulation system. To improve the efficiency of BLDC motor drives, several machine design and control strategies have been created. The three components of the overall system are as follows: PWM inverters for power conversion, BLDC motors and loads, and speed, torque, and current controllers [17]

The fundamental drawback of hysteresis current control [HCC] is, current control switching frequency is variable over a large range, extremely high and is variable in the wide range. Additional benefits of hysteresis current controller are its simplicity, quick deadbeat transient response, immunity to load parameter fluctuations, and direct over-current protection. [18].

1.1 Overview

Due to a number of distinguishing benefits, including the lack of bushes, greater performance, increased reliability, energy efficiency, and reduced maintenance needs, the adoption of Brushless DC (BLDC) motors has significantly risen in home and industrial applications. The issue with traditional speed control methods, such as the PI control method and the vector control method, is that they generate harmonics in the load current, and the motor control algorithm that was chosen (vector control) was too complicated to operate the BLDC motor. Hysteresis current control technology, which produces enhanced robustness and decreased harmonic content, can be used to solve the issue.

The aim of the project is to design a motor control system employing hysteresis current regulation for a three-phase brushless dc motor. The selected architecture included an A2212 BLDC motor, an ACS712 hall sensor, an IR sensor, an Arduino Uno (an ATmegaS128 microcontroller), a gate driver circuit, and MOSFET switches. 150W was the selected motor

rating (max). The motor is driven by the inverter, producing output voltage and frequency that are optimal for AC power. The divergence between the prescribed and measured currents was observed and tracked in the hysteresis current control approach. The reference gating signals were produced as a consequence. Three phase inverter switches were triggered by the resulting gating signals.

1.2 Specific Details

A three phase inverter for the rating of 12V input voltage, 150 W (peak power of BLDC motor), frequency 50Hz is designed. Aa small miniature inverter is designed for a small BLDC motor control as a prototype. The project work uses a regulated power supply with input voltage of 12V to supply power to microcontroller, opto-coupler, gate driver and inverter input. Table 1.1 shows the specification details of the proposed project.

The microcontroller is used to generate the PWM pulses for the power switches. As the out voltage of the microcontroller pin is around 3.3V to 5V, it is not sufficient to drive the MOSFET switches. Gate driver IC is used to pump the charge at the required voltage, rise time and fall time depending on the switching frequency of the PWM.

Table 1.1 Specification Details

Board type	Input / Output	Rating
Power supply section	Input voltage	230V AC , 50Hz
	Output voltage	12 V DC & 5 V DC
Gate driver	Input voltage	15V
	Output voltage	10 – 15V
	Rise time & fall time	100ns & 50ns
	I source & I sink	120mA & 270mA
3 Ph Inverter	Input voltage	12 DC

1.3 Literature Survey

The development of naturally electric cars has recently picked up steam. One of the essential parts of electric vehicles is the BLDC motors, hence it is necessary to create a suitable

control system. This is significant as low power vehicles are frequently utilized in rural regions, making any advancement in model design beneficial. With the use of computer-based simulations, several control schemes that utilize the hysteresis control mechanism are proposed. The control mechanism is unique, reliable, and very inexpensive compared to commercially available controllers. [19].

The BLDC motor employs a simple torque hysteresis control (THC) in [15], it offer a robust control and quick torque dynamic performance. The current controller has been applied to a BLDC drive and the results shows that the current ripple stays within the hysteresis band as defined by the controller. The proposed current blocking strategy shows that the energy wastage from the batteries is prevented such that it can prolong the capacity of voltage battery and it also showed that the hysteresis controller can offer inherent current protection/limitation and robustness in controlling the motor torque. The hysteresis current band is computed for each On-Off switching period, based on not only the measured voltage values at computing instant [16].

Induction motor drives that employ hysteresis current control are frequently used in high performance drive applications. According to the vector control concept, the speed, flux, torque, and phase current performances are good. In [17] fixed-band and sinusoidal-band hysteresis current controllers both are proposed and developed for a direct matrix converter. A comprehensive comparative evaluation of the two methods is then carried out. Both methods have fast dynamic performance and they inherently integrate the line modulation technique of the virtual rectifier stage into the overall modulation. Surge currents are prevented with the proposed scheme. The sinusoidal-band hysteresis controller demonstrates lower total harmonic distortion at the expense of higher average switching frequency, which is only significantly observable at very high sampling frequencies. The proposed controller is integrated with the field-oriented control to drive a matrix converter fed permanent magnet synchronous machine [18] - [22].

Motor current quality is significantly influenced by the size of the hysteresis bandwidth; a smaller hysteresis bandwidth results in greater switching frequency, less current ripple, lower THD values, and better power quality overall. The system's dynamic responsiveness may be improved with less calculation time by using a hysteresis current controller, and allows for quicker tracking of the load current with the reference current. Improvements to hysteresis control make it ideal for quick, precise conversion systems [23], [24].

The performance of various hysteresis controllers is examined based on switching frequency

and THD with a set value of tolerance band (0.5 A). For DBHCC-2, the minimum THD is 2.65 percent at 20 kHz and 0.5 A of HB, whereas the minimum switching frequency is 5.5 kHz, although the THD grows. [25]. The PMSM drive system runs smoothly and with no torque ripple using a hysteresis current controller at low speeds. [26].

For FLC based indirect vector controlled three phase IM drive, the comparison of HCC and SVPWM controller is shown. Compared to SVPWM approach, the hysteresis current control system has a quicker reaction time, but it has higher torque chattering [28].

An indirect field oriented control of three phase induction motor using hysteresis current band and SVPWM technique has done. The comparative performances between both techniques were presented. From the simulation results, SVPWM technique gives better performances in elimination of the stator current harmonics and reduction of the torque ripple while maintaining the other characteristic of the system [29]-[30].

1.4 Motivation

It is necessary to develop a controller with quick reaction, low transient time, high tracking ability, low harmonic distortion, and smooth sinusoidal output in order to achieve high quality power. The performance of the PI controller is constrained by the input limitations, and optimization is typically not seen [15]. The FOC control approach is quite susceptible to errors in the parameters and measurement noise. It is discovered that the hysteresis controller provides a reliable output response. The hysteresis controllers are used to monitor the difference between the measured current and the reference load current.

The existing control strategies such as Field-Oriented Control (FOC) suffer from sensitivity to the motor parameter variations like R, L, flux etc. Even adaptive control schemes have a tendency to be sensitive and have poor flux, torque, and current estimation, especially when operating at low speeds. As a result of the torque and the load, the current fluctuates throughout operation [18].

1.5 Objectives

Following are the objectives of the proposed prototype.

- To design 3 phase inverter drive for a BLDC motor.
- To develop the Hysteresis current control algorithm.

- Simulation analysis of three phase inverter drive.
- To experimentally generate PWM pulses for the designed 3 phase inverter using Arduino uno microcontroller.
- To develop hardware module of 3 phase inverter drive to control speed of BLDC motor.

1.6 Problem Statement

Design, simulate and Implementation of Three Phase Inverter for BLDC Motor using Hysteresis Current Control Technique

1.7 Organization of Thesis

The thesis is organized in the chapter wise as mentioned below:

Chapter 1: This chapter discuss brief about Introduction of 3 phase inverter topology to control BLDC motor and relevant literature survey. It also includes objectives of the project, motivation, problem statement and the organization of the report.

Chapter 2: Electric vehicle and power converter discusses the theory and concepts of two level three phase Inverter topology, controlling techniques, driving principle of BLDC motor, High-side Low-side gate drivers.

Chapter 3: Methodology and Block diagram discusses the methodology and block diagram of hysteresis current controller using two level three phase Inverter for BLDC motor.

Chapter 4: Specification & Design explains in detail the design of the prototype of project work. The specification and detailed design is also provided in the chapter.

Chapter 5: Simulation & Implementation provides the simulation circuits, schematic diagram for proposed project.

Chapter 6: Results & discussion discusses about the simulation results of the converter and hardware results for the same

Chapter 7: Conclusion and Future scope includes the overall conclusion drawn from the project and the future works that can be carried out.

References include the list of referred in successful completion of project.

CHAPTER 2

THREE PHASE INVERTER AND BLDC MOTOR

The chapter includes introduction of electric vehicle, types of EVs, components included in plug in EVs, DC capacitor link, role of motor controller unit or traction inverter, basics of two level 3 phase inverter topology, hysteresis current control technique, high- side low- side gate drivers and working of BLDC motor .

2.1 Electric Vehicles

The conventional IC engine base automobiles are being quickly replaced by electric vehicles. Rapid replacement is used because it is very efficient, provides quick torque, and is environmentally beneficial. Motor control units, traction inverters, as well as cutting-edge motors such permanent magnet synchronous motors, switching reluctance motors, brushless DC motors, internal permanent magnet motors, and many more, are responsible for the performance and efficiency of electric power trains [8]. The majority of EVs employ BLDC and PMSM motors. In comparison to other traditional motor, permanent magnet motors are both extremely light and effective. Power electronics and embedded micro-computing devices are combined in the motor control unit to increase its reliability and efficiency while converting the energy in the batteries.

2.2 Components Included in Motor Controller Unit

Power element, microprocessor, communication interface, sensing/protection, input interface (accelerator, brakes, indicators, etc.), DC capacitor connection, and auxiliary power supply are among the components of a motor controller.

The motor controller unit's microprocessor is the brain of electric vehicle, which includes embedded firmware to implement all of the motor controller's operations. The most crucial component of an MCU is the communication interface. It enables the motor controller to exchange data with other auxiliary devices outside of it. MCU can communicate with a communication block to send and receive data. The CAN bus, SPI, I2C, and other protocols are included in the communication block.

2.3 DC Capacitor Link

It is crucial to choose the right DC-link capacitor for the inverter. Some essential characteristics need to be taken into account while building a DC-link capacitor, such as high ripple capability, high temperature durability, total number of capacitors, equivalent series inductance, and low equivalent series resistance for minimal power loss. The DC-link capacitor's size and cost should be geometrically matched to the inverter and selected as efficiently as possible. Aluminum and ceramic capacitors can be used in parallel to lower the equivalent series resistance. To reduce the equivalent series resistor, size and cost optimization, parallel combination of aluminum and ceramic capacitor can be implemented. Fig 2.1 shows the DC link capacitor in between three phase inverter and DC voltage source.

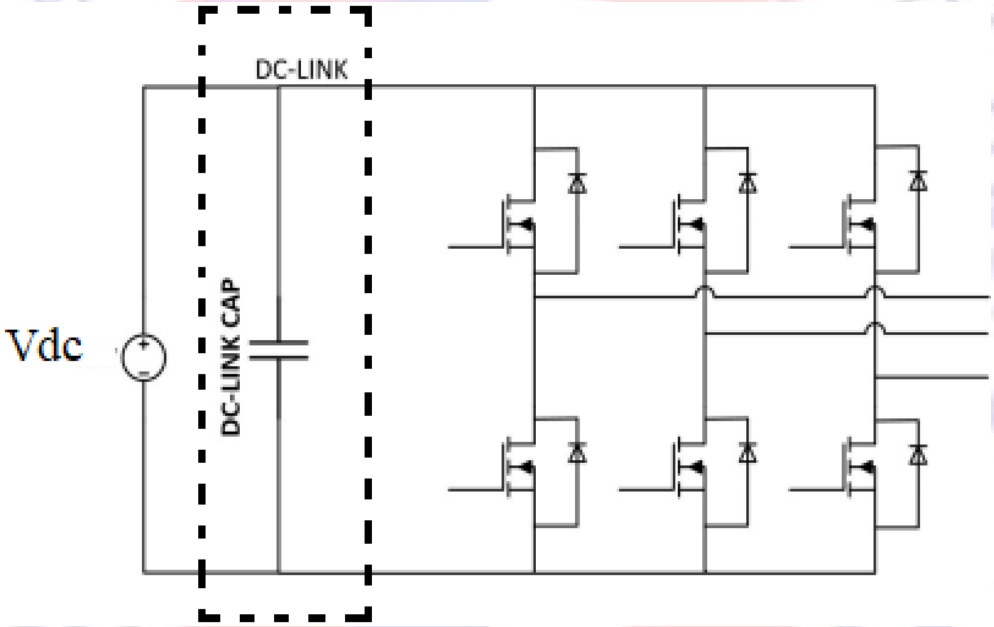

Fig 2.1 Three phase inverter with DC Capacitor Link

2.4 Role of Motor Controller Unit (Traction Inverter)

In an electric vehicle, the motor control unit does more than just transmit energy from the battery to the motor to accelerate the vehicle. During regeneration braking, the traction inverter can also transfer energy from the motor back to the batteries. By storing energy in the battery, regenerative braking extends the driving distance.

2.5 Basics of Two Level Three Phase Inverter Topology

To convert dc to ac output, a simple two-level inverter is employed. IGBTs and MOSFETs are the two best switching components for these inverters, and it has six switches in total. IGBT is used for low switching frequency and MOSFETs are used for high switching frequency They are the best choice in the industry and for commercial purposes due to its simple construction and capacity to manage the voltage and maintaining system stability. Typically, an LC filter is used to link them to the grid or the load. To increase its performance, resilience, and stability during correcting for power losses and reducing the THD value, researchers apply a variety of control methods. Standard three-phase VSI topology is shown in Fig.2.2 and the eight valid switch states are shown in Table 2.1. As in single-phase VSIs, the switches of any leg of the inverter (S1 and S4, S3 and S6, or S5 and S2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and undefined AC output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as it result shoot through. [7].

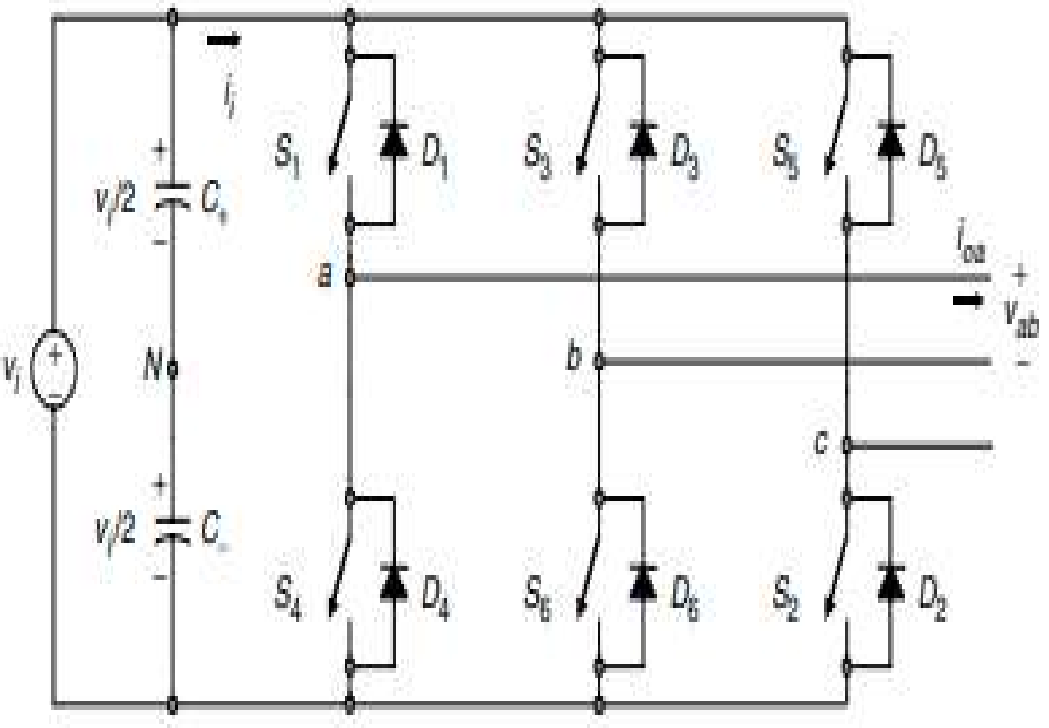

Fig 2. 2: Two Level Three phase VSI topology [7]

Table 2.1 Acceptable switch states for a three phase VSI [7]

State	State No	Vab	Vbc	Vca
S1, S2, and S6 are ON and S4, S5, and S3 are OFF	1	Vi	0	-Vi
S2, S3, and S1 are ON and S5, S6, and S4 are OFF	2	0	Vi	-Vi
S3, S4, and S2 are ON and S6, S1, and S5 are OFF	3	-Vi	Vi	0
S4, S5, and S3 are ON and S1, S2, and S6 are OFF	4	-Vi	0	Vi
S5, S6, and S4 are ON and S2, S3, and S1 are OFF	5	0	-Vi	Vi
S6, S1, and S5 are ON and S3, S4, and S2 are OFF	6	Vi	-Vi	0
S1, S3, and S5 are ON and S4, S6, and S2 are OFF	7	0	0	0
S4, S6, and S2 are ON and S1, S3, and S5 are OFF	8	0	0	0

2.6 BLDC Motor

The fundamental operating concept of a BLDC motor is , in order to provide a constant torque, the phase windings must be excited in accordance with the location of the permanent magnet on the rotor. Information about the location of the rotor magnet is necessary to carry out the job. Hall effect sensors are frequently used for position sensing. The position of rotor can also be found by measuring the back EMF, using sensorless control method. For the purpose of detecting the magnetic field flux generated by the rotor magnets, three Hall effect sensors are spaced apart from one another on the stator by 120 electrical degrees. The rotor position separated into six distinct portions can be identified using three Hall effect sensor output signals. [10]. Fig 2.3 show the representation of switching sequence for three phase BLDC motor and Table 2.2 shows the respective switching sequence for the BLDC motor.

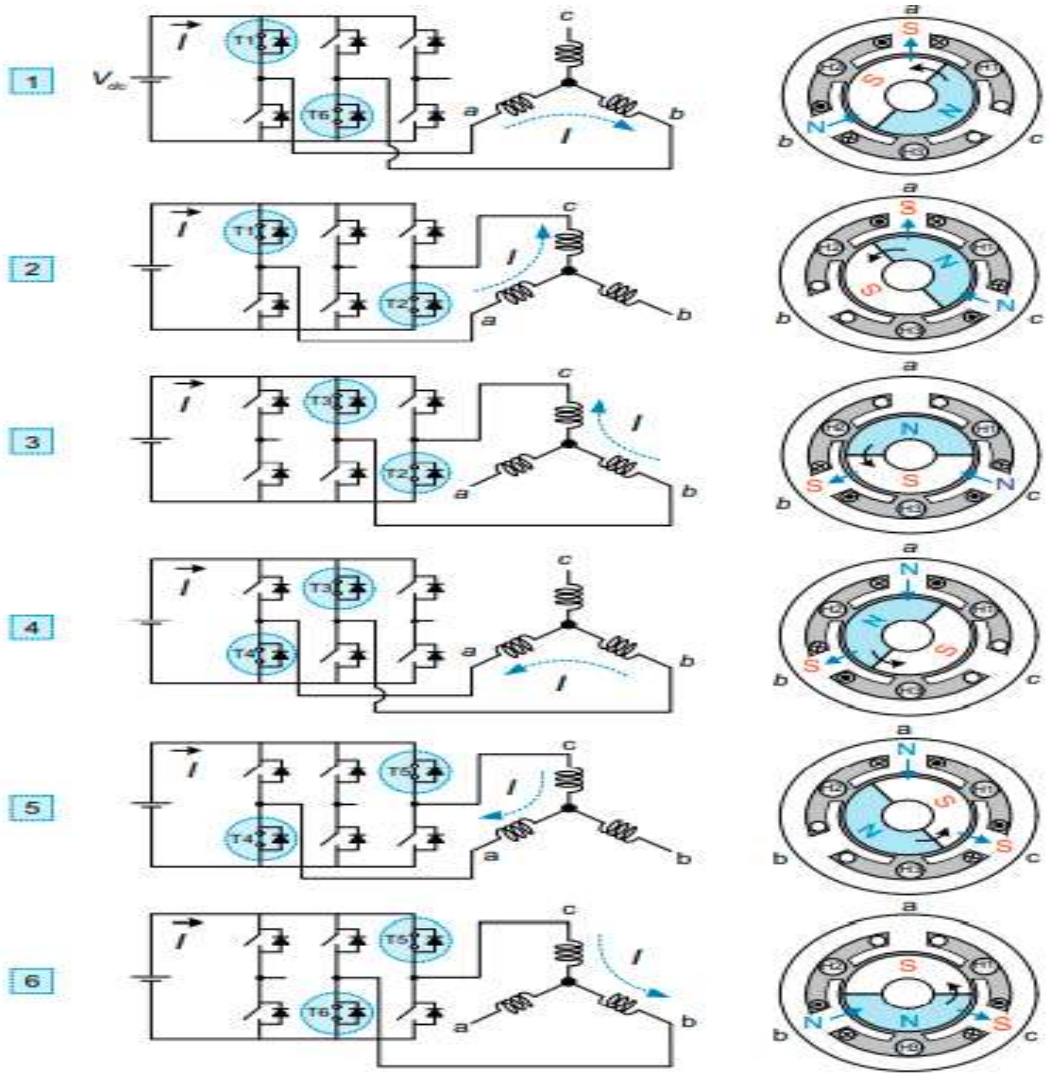

Fig 2.3: Switching sequence for two pole three phase BLDC motor [10]

From the switching sequence for the six-step drive is illustrated in Fig.2.3 only two of the three phase windings are excited during the BLDC motor drive, leaving the third winding unexcited.

Table 2.2: Switching sequence for two pole three phase BLDC motor [14]

Switching interval	Seq. number	Hall sensors			Switch closed		Phase Current		
		H1	H2	H3			A	B	C
$0° - 60°$	0	1	0	0	Q1	Q4	+	-	off
$60° - 120°$	1	1	1	0	Q1	Q6	+	off	-
$120° - 180°$	2	0	1	0	Q3	Q6	off	+	-
$180° - 240°$	3	0	1	1	Q3	Q2	-	+	off
$240° - 300°$	4	0	0	1	Q5	Q2	-	off	+
$300° - 360°$	5	1	0	1	Q5	Q4	off	-	+

To identify exactly two of the three-phase windings is energized to provide the continuous torque at each instant, rotor position feedback signals are employed. A three-phase inverter is used as a drive circuit to send current into the necessary two-phase windings. Only two phases' worth of switching devices are active at any given time in the inverter for a BLDCM drive depicted in Fig. 2.4. As a result, the conduction interval for each switching device is 120 degrees. Since the switch for the other phase changes when an active switch is switched over in the six-step drive, a dead period is not necessary for short-circuit prevention. [10].

Fig 2.4 illustrates Hall effect sensor signals (H1, H2, H3) with respect to back-EMFs of stator windings in the six-step drive as shown in Fig 2.3 and the relationship between the sensor signals and the phase currents. Each sensor is expected to have a digital high level output for the North Pole and a low level output for the South Pole. A continuous torque must be produced by switching the excited phase winding, or active phase winding, every 60 electrical degrees of rotation based on the sensor inputs. Commutation refers to the change in an active phase winding [10].

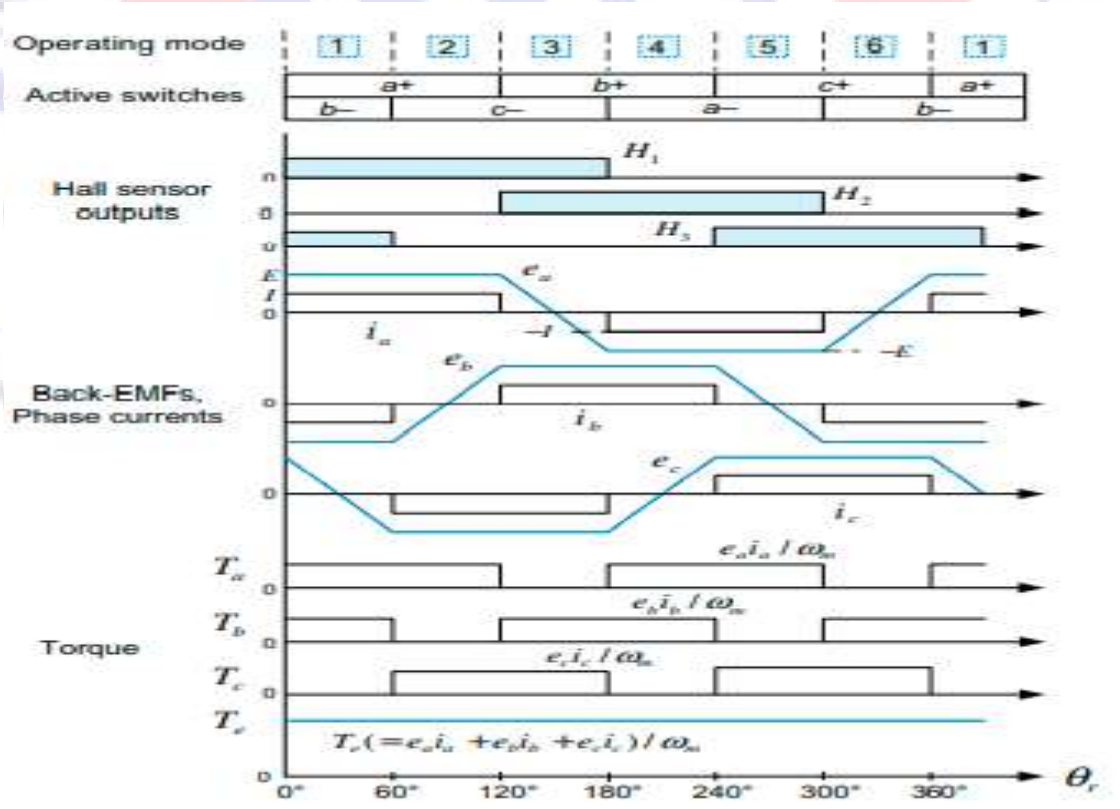

Fig 2.4: Driving principle of three-phase BLDC motor [10]

2.7 Hysteresis Current Control [HCC] Technique

HCC is a nonlinear approach of control system, and it uses hysteresis current control. The difference between the recommended and measured currents is monitored or tracked using the HCC. As a result, the reference tracking serves as the foundation for the generation of the gating signals. For the purpose of removing errors in reference tracking, hysteresis bandwidth is changed. Any modulation technique is not needed for this approach, the operating conditions for the hysteresis bandwidth and the filter parameters determine the switching frequency of an inverter. The switching frequency of a hysteresis controller is unregulated. Drive signals are created by the look-up in accordance with the size of the error signals, and error signals are produced by hysteresis controllers. HCC require very high frequency for constraining the variables in hysteresis band limits, block diagram for implementation on a digital platform as shown in Fig.2.5. Moreover, switching losses are very high in this type of controllers. So, Hysteresis controllers are found inappropriate for high power applications [18].

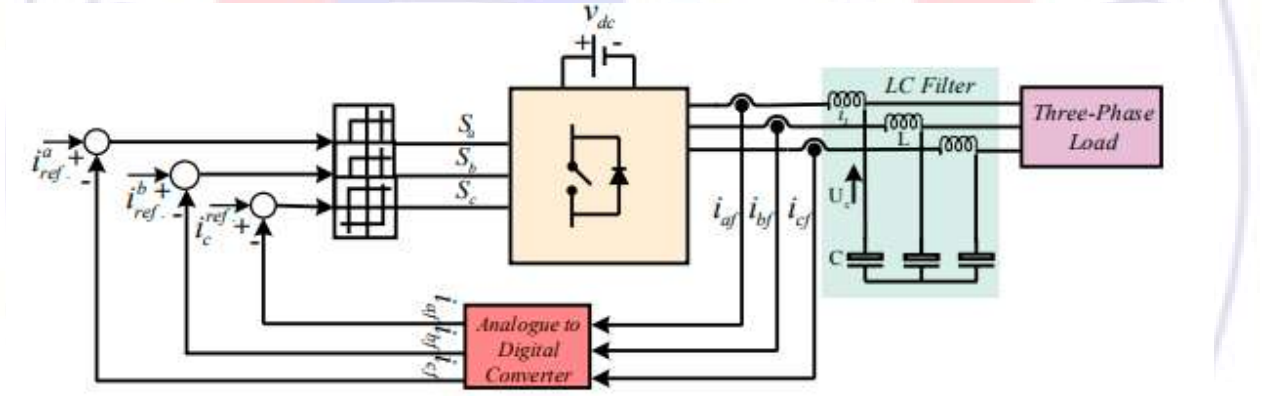

Fig 2.5 A Hysteresis current control technique for VSI [18]

2.8 High Side Low Side Gate Driver

Discrete components and specific drivers with a simple circuit, excellent reliability, and widespread applicability make up the MOSFET driving circuit. The IR2110 and IR2101 drive devices are two of the most popular ones. The major components of the IR2101 are logical input, voltage conversion, and output protection. It has a maximum working voltage of 500 V, a grid drive voltage range of 10 to 20 V, and a logical power voltage range of +3.3 to +15V. In small- and medium-power driving circuits, the IR2101 is widely used due to its low volume and fast speed. [9]. The schematic diagram for IR2101 gate driver with respect to one leg of three phase inverter is shown in Fig 2.6.

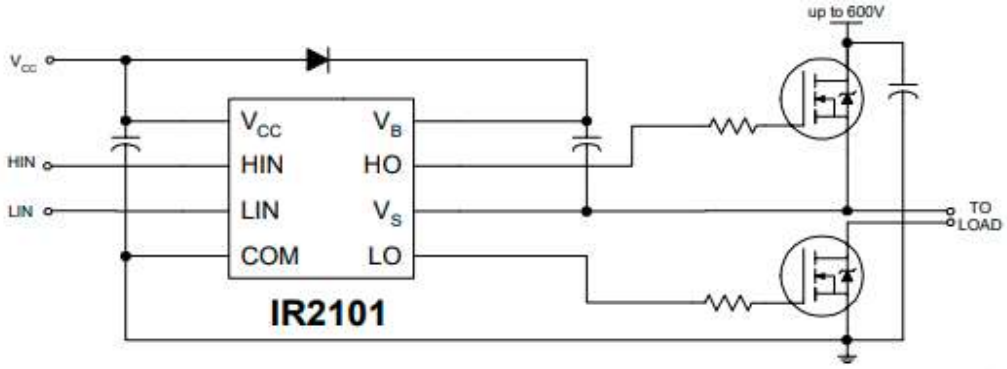

Fig. 2.6: Schematic diagram of IR2101 gate driver with respect to one leg of three phase inverter [9].

IR2101 is a high-performance three-phase bridge driver, is manufactured by IR Corporation. Similar to the IR2110, it only has one drive power source. However, it facilitates system design and creates six driving signals. Additionally, the protection feature of the IR2101 has been improved to increase the circuit's dependability. The output upper leg and under-leg drive current peak values of the IR2101 are 250 mA and 500 mA, respectively, and it is employed in circuits with voltages no greater than 600 V. Three input signal processors, three pulse-processing and level-shifting devices, three driving signal latches for upper-leg power switches, three under-voltage monitors for upper-leg power switch driving signals, six MOSFET drivers with low output impedance, and an OR gate circuit are all integrated into the IR2101. It also includes a current comparator, a current amplifier, an under voltage monitor for its own operating power supply, an error-processing unit, and a clearing blocked logic unit [9].

Three of the six PWM pulse signals used as IR2101 inputs in BLDC motor drive systems are used to drive the upper leg, and the remaining three signals are utilized to drive the under-leg. Following amplification, the three signals needed to drive under-leg power switches are fed into the control poles. In order to maintain level displacement, the other three signals used to drive the upper leg are first processed by a level shifter's pulse processor and bootstrap circuit, which then convert it into three voltage-suspended driving pulse signals. Followed by, it is tested by driving pulses before being latched through the matching three output latch devices. After power amplification, the three signals are finally applied to the control poles of the driven upper-leg power switches. [9].

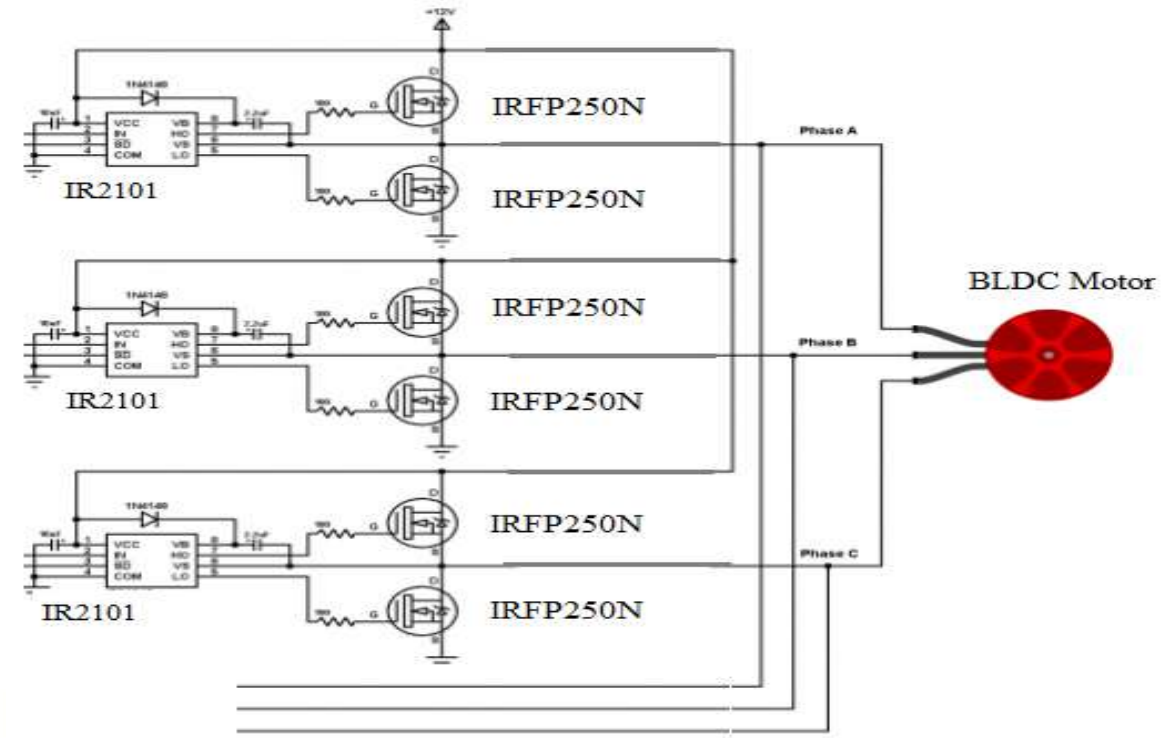

Fig 2.7: IR2101 driving circuit [9]

2.9 Summary

The concepts of three phase inverter, brief introduction on hysteresis current control technique , driving circuits , and working principle of BLDC motor with switching intervals and current wave forms using hall effect sensors were studied in the chapter.

CHAPTER 3

METHODOLOGY AND BLOCK DIAGRAM

This chapter discuss about the methodology, block diagram, component selection and implementation algorithm, flow chart of proposed prototype.

3.1 Methodology

The methodology involved in developing the project work is as shown in Fig 3.1

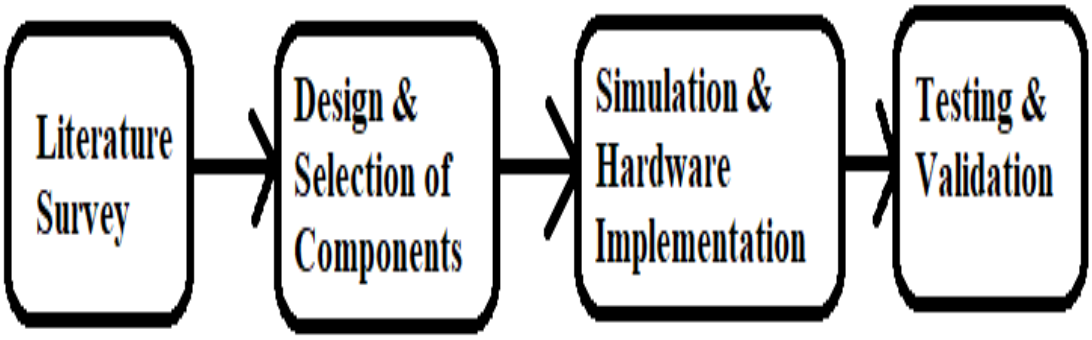

Fig 3.1: Methodology Involved in Implementation of Proposed Project Work

- **Literature Survey**

  Efficient converter topology is selected for the work by comparing various topologies. The selected topology is Three Phase Inverter.

- **Design and Selection of Components**

  A three phase inverter with 3 phase AC output is designed. The MOSFET gate driving ICs , bootstrap circuit is designed. And the passive and active components like resistor, capacitor and diodes are selected based on design value. A schematic drawing is implemented in Proteus software and the PCB layout is also designed. The tools used for design is LTspice, Mathcad, MATLAB / SIMULINK and Proteus.

- **Assembling and PCB Designing**

  Based on the designed schematic diagram the three phase inverter topology with gate driver circuitry is assembled in general PCB board as prototype. Alos various test points are

placed in PCB board.

- **Hardware implementation**

  The assembled PCB is checked and test setup is made for analysis and testing purposes like to test the gate pulses.

- **Testing and verification**

  The implemented inverter is analyzed and the performance is tested under various input voltages and different loading condition. Here Propeller is connected to the shaft of BLDC motor, equivalent to mechanical loading.

3.2 Block Diagram

The block diagram of the proposed project work is shown in Fig 3.2. It comprises of 15 V battery or it can be replaced with regulated power supply, three phase inverter (VSI), and 15V BLDC motor and microcontroller as the major components.

From the block diagram shown in Fig 3.2 hysteresis current control is used in closed loop to control the speed of BLDC motor. Here ACS712 hall sensors are used to measure the instantaneous current in each phase. The Hall Effect sensors is also used know the position of the rotor. The position of rotor can also be found by back EMF method which is also called as sensorless control method. IR sensor is used to measure the current speed of the BLDC motor. The measured currents and sped are sent to the microcontroller.

In the block diagram Fig. 3.2, W* is the speed defined the user and W is the instantaneous speed. By varying W* the speed and current drawn by BLDC can be varied. Using the microcontroller the reference current is calculated and is compared with the measured current. Across the reference current, a hysteresis band is set such that the instantaneous current is kicked back. Based on the error generated between the measured current, reference current within the hysteresis band the gate pulses are generated in the microcontroller. The pulses form microcontroller is given the three phase inverter through gate driver IC to drive the BLDC motor.

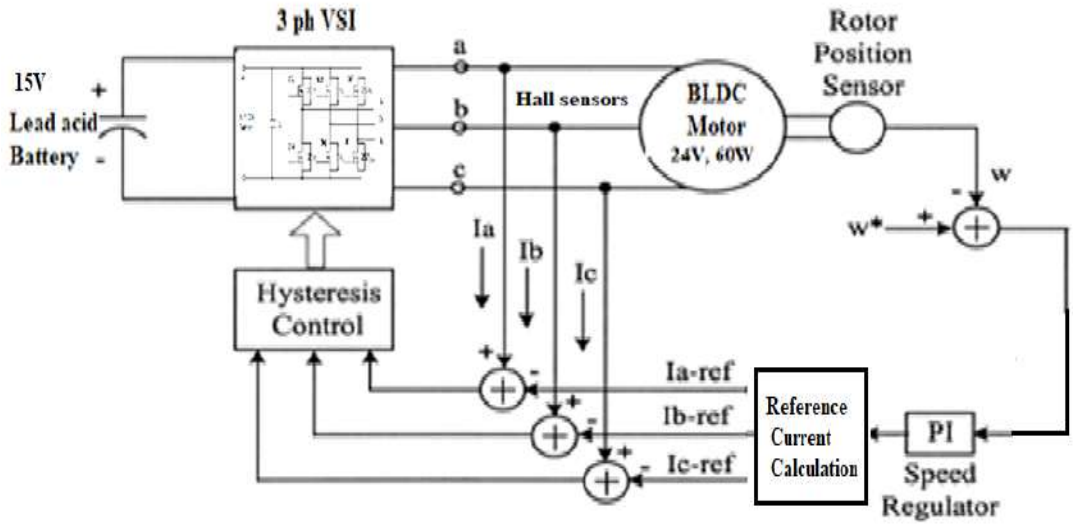

Fig.3.2: Block Diagram of 3 Phase Inverter with Hysteresis Current Control.

3.2.1 Flow Chart

Fig 3.3 shows the Flow chart of error generation between measured current value and reference current value within the tolerance band. The flow chart is with respect to phase A of the BLDC motor or leg A of the three phase inverter. In the flowchart Ia is the instantaneous current phase A of the BLDC motor, ea is the error generated, h is the hysteresis band across the reference band and W* is user defined speed. If ea is greater or equal to h then Q1 & Q4 are turned on. If ea is less than h then Q1 & Q4 are turned off. If ea is equal to 0, it means the actual current is following the reference current.

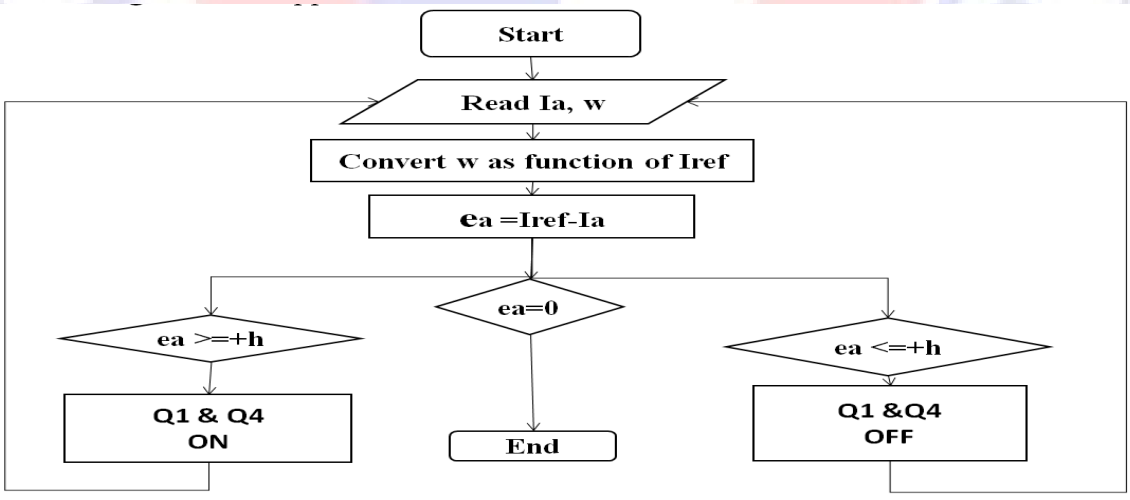

Fig 3.3 Flow Chart with Respect to Leg A of three Phase Inverter

3.3 Summary

In this chapter the methodology, block diagram, flow chart of the proposed hardware prototype is studied in brief.

CHAPTER 4

SPECIFICATION AND DESIGN DETAILS

This chapter discusses about the components involved in the project work. The project work is smoothly carried out only if ally components selected properly based on ratings, interfaced and synchronized in the desired fashion. The process of components selection and designing the circuit block by block as per specifications plays an important and also gives a clear picture of project work. The table 4.1 shows the specification details of the proposed project.

Table 4.1 Specification Details

Board type	Input / Output	Rating
Power supply section	Input voltage	230V AC , 50Hz
	Output voltage	12 V DC & 5 V DC
Gate driver	Input voltage	15V
	Output voltage	10 – 15V
	Rise time & fall time	100ns & 50ns
	I source & I sink	120mA & 270mA
3 Ph Inverter	Input voltage	12 DC

4.1 Components Used

The main components used in the work are

- Microcontroller Arduino Uno & Nano
- Gate driver IR2101
- MOSFET IRF250
- A2212 BLDC motor

4.1.1 Microcontroller: Arduino Uno & Nano

In this project, the PWM pulses produced by the Arduino Uno and Nano are utilised to operate the BLDC motor. The program for hysteresis current control is dumped in arduino Uno. Arduino Uno is based on ATmega328P. It is a 8 bit microcontroller. There are 14 digital input/output pins on it. It has 6 analogue inputs and 6 PWM outputs. It has a USB connector to upload the software, a power jack, a reset button, and a 16 MHz crystal resonator. Additionally, the Atmega328P has 1kB of EEPROM. The Fig 4.1 shows the Arduino Uno microcontroller used in the work and Table 4.1 shows the technical specification of Ardunio Uno Board.

Fig.4.1 Arduino Uno Microcontroller

With the help of the Arduino IDE software, the controller makes programming simple. A controller is utilized in this project to sense the three-phase current, create PWM pulses, and regulate the motor's speed. Hence Arduino Uno microcontroller with the mentioned required feature is selected for the project.

Table 4.2: Technical Specification of Arduino Uno Board.

Board	Arduino UNO	
Microcontroller	ATmega328P	
USB connector	USB-B	
Pins	Built-in LED Pin	13
	Digital I/O Pins	14
	Analog input pins	6
	PWM pins	6
Communication	UART	Yes
	I2C	Yes
	SPI	Yes
Power	I/O Voltage	5V
	DC Current per I/O pin	20mA
Clock speed	ATmega328P	16MHz
Memory	Atmega328P	2KB SRAM, 32KB FLASH, 1KB EEPROM

4.1.2 Current Sensor ACS712

In the project work, three ACS716 20A hall based current sensor is used to measure line current precisely and accurately. Fig 4.2 shows the photograph of ACS716 hall based current sensor. The measured current using ACS716 current sensor is given to Arduino Uno. It can measure both DC (direct current) and AC (alternating current). Fig 4.2 shows the pictorial representation of ACS716 current sensor IC. The typical pin-out diagram is shown in Fig 4.3 and Table 4.2 shows the terminal list of the pin out diagram..

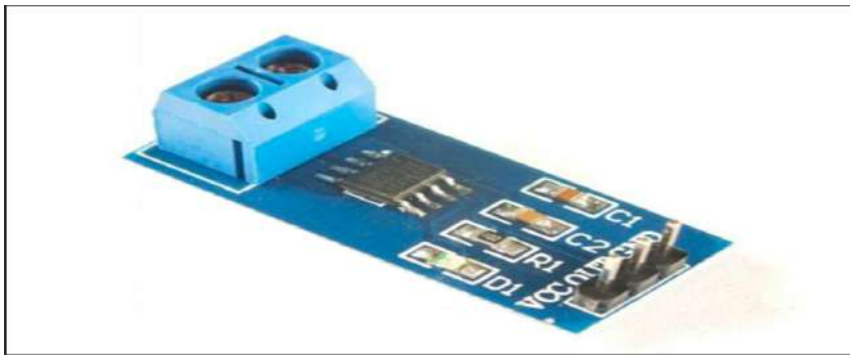

Fig 4.2 ACS716 Hall Base 20A Current Sensor

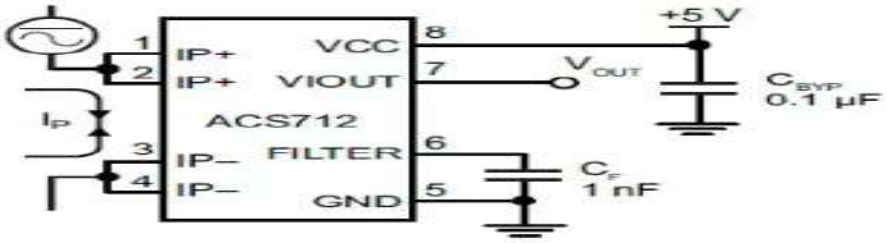

Fig.4.3 Pin-Out Diagram of ACS712

Table 4.3 Terminal List Table for the Given Pin Out Diagram

Name	Number	Description
IP+	1 and 2	Terminals for current being sampled
IP-	3 and 4	Terminal for current being sampled
GND	5	Signal ground terminal
FILTER	6	Terminal for external capacitor that sets bandwidth
VIOUT	7	Analog output signal
VCC	8	Device power supply terminal

4.2 Three Phase Inverter

The three phase inverter is shown in figure. It consist of six IRFP250N MOSFET, its Vds is 200V, Id = 30A and Rds (on) 0.075 ohm. The rise time and fall time of IRFP250N is 42ns and 33ns with Qg 123 nC. For fast switching converter operation like inverters MOSFETs with low rise time, low fall time and low Qg value is preferred. In order to drive six MOSFETs three

IR2101 high side low side gate driver with bootstrap circuitry is selected. The bootstrap circuitry design is discussed in 4.1.

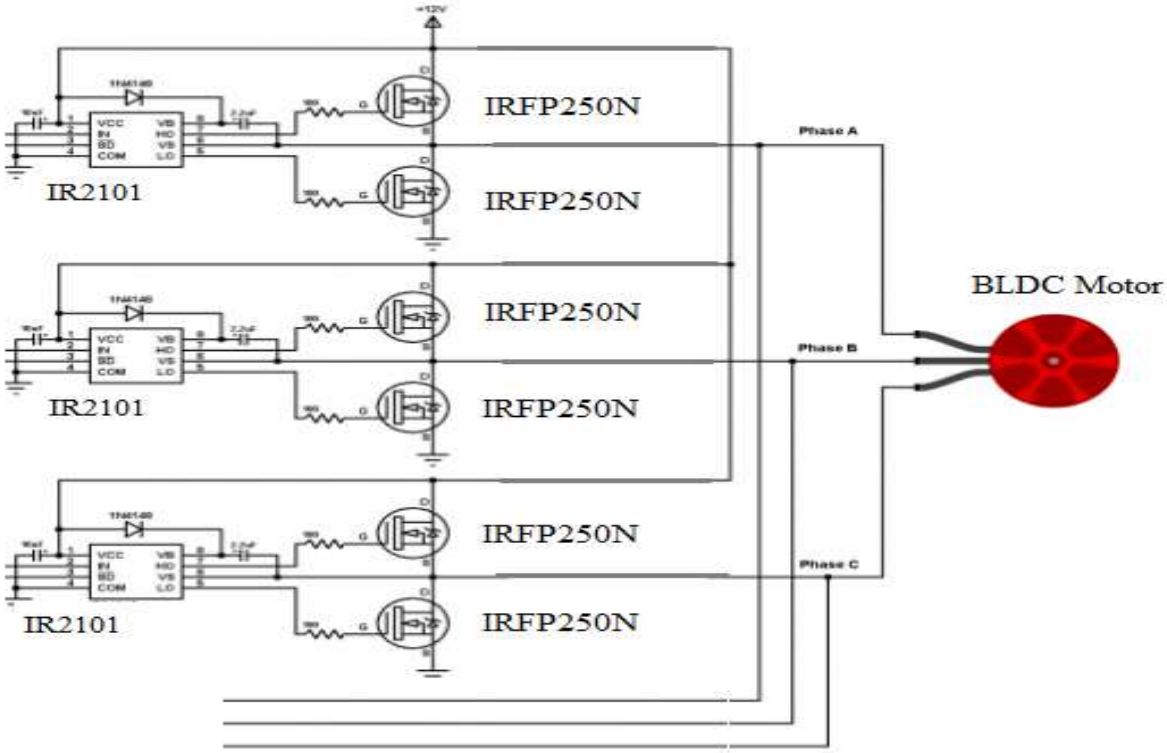

Fig 4.4: Three Phase Inverter to BLDC Motor through Gate Driver

4.2.2 Bootstrap Circuit

Designers struggle to drive high side MOSFETs in a half bridge configuration, leading to the idea of bootstrap circuitry. The usage of a bootstrap circuit, which consists of a capacitor, a diode, a resistor, and a bypass capacitor, is one of the most well-liked and economically advantageous ways for designers to do this. The high MOSFET is linked to bootstrap circuitry in the image below. Fig 4.5 shows the bootstrap capacitor circuitry design for High side MOSFET and Fig 4.6 shows the bootstrap capacitor circuitry design for Low side MOSFET.

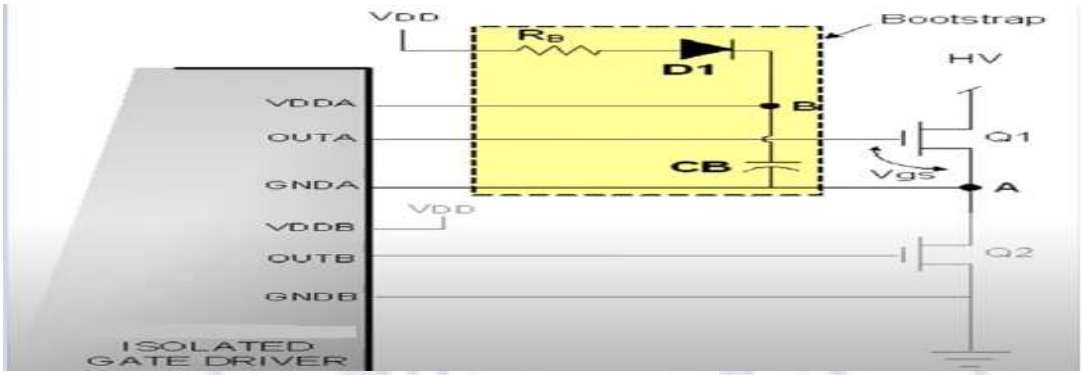

Fig 4.5 Bootstrap Capacitor Circuitry Design [22]

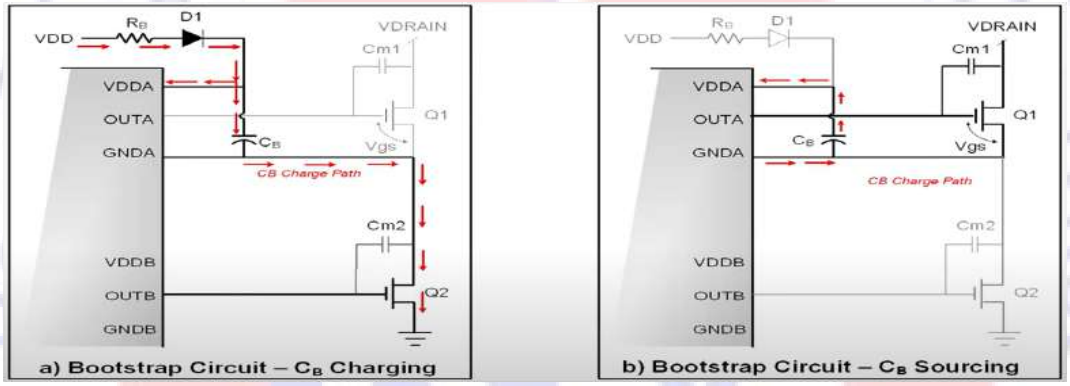

Fig 4.6 Bootstrap Capacitor Circuitry Design [22]

4.2.2.1 Low Side Switch

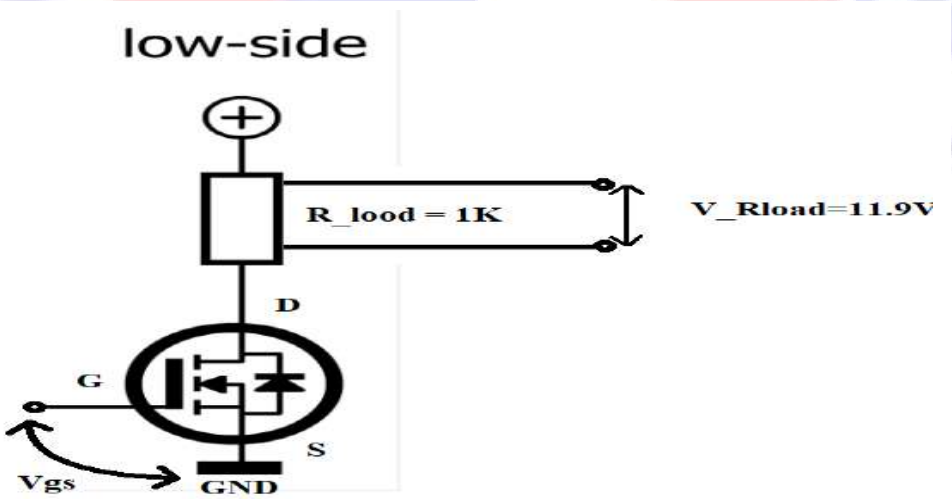

Fig. 4.7 Low Side MOSFET

To turn on the low side MOSFET as shown in Fig 4.7,

$$VGS > Vth \quad (1)$$

(VG – VS) > Vth, where VS is connected to ground so VS = 0, so the reference voltage VS is considered as 0V.Therefore,

$$(VG – 0) > Vth, \quad (2)$$

Hence if VG is greater than threshold voltage Vth the MOSFET will turn on.

Here VG is gate voltage, VS is voltage at source terminal

But in case of high side switch VS is connected to load and not to the ground. So, the reference voltage Vs is not 0V.

4.2.2.2 High Side Switch

To turn on the high side MOSFET as shown in Fig 4.7,

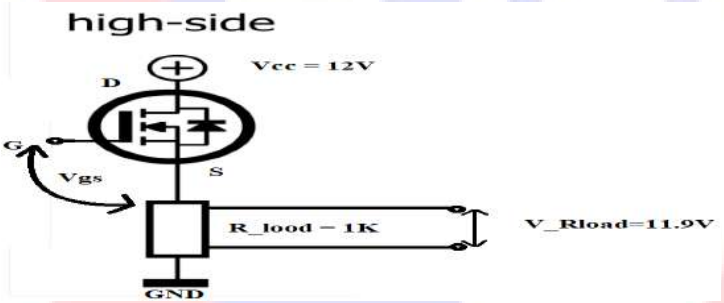

Fig. 4.8 High Side MOSFET

$$Id = \frac{(Vcc - 0)}{Rl + Rds} \quad (3)$$

$$Vs = Vrload = Id \times Rload \quad (4)$$

$$Vs = \frac{Vcc \times Rload}{(Rload + Rds)} \quad (5)$$

If Rload >> Rds then is approximately equal to Vcc ., Vcc ≈ 11.9V in the case.

To turn on high side MOSFET as shown in Fig 4.6,

$$VGS > Vth, \quad (6)$$

VG – VS> Vth, where VS is not connected to ground so VS ≠ 0, so the reference voltage VS is considered as 11.9V.

$$(VG - 11.9V) > Vth, \text{(assuming Vth = 4V)} \quad (7)$$

$$VG > (4 + 11.9V) => VG \approx 16V.$$

So, it can be observed that the gate voltage of more than supply voltage must be applied to turn on high side MOSFETs. This can be avoided by placing a bootstrap circuitry across high side driver.

4.2.2.3 Mode of Operation of Bootstrap Circuitry

Bootstrap circuitry has an easy-to-understand function. As seen in the diagram below, CB, or the bootstrap capacitor, charges up when the low-side switch Q2 is on and Q1 is off. During this time, charge current from VDD flows into the driver's VDDA input and into the charge loop through the diode, capacitor CB, and Q2 of the bootstrap resistor RB.

The bootstrap capacitor is discharged, or CB acts as source, as Q2 is turned off and Q1 is switched on. The voltage at Q1 source terminal and ground soon increases toward Q1 drain voltage, VDRAIN, as a result. The voltage at VDDA is approximately equivalent to VDD-0.7V and consists of the voltage across CB plus the voltage at the Q1 source. Diode D1 becomes reverse biased when the voltage between the Q1 source and GND increases, cutting off the VDD supply to the CB. As soon as D1 is reverse biased, CB now produces VDD-0.7 for VDDA and all the current necessary to power the high side MOSFET Q1 while Q1 is off.

4.3 BLDC Motor

In the project A2212 1400KV brushless DC motor is used and is shown in Fig.4.8, it provides excellent performance and quality. It has maximum current of 16A / 60s and its no load current is 0.7A. It has a 65 m ohm internal resistance and a maximum power rating of 180 W with 14 poles. It functions with battery input voltage ranging from 7.2V to 15V. The three phase inverter is then used to convert this battery power into AC. The BLDC motor's input voltage ranges from 5.73V to 7.64V.

Fig. 4.9 A2212 1400KV BLDC Motor

4.4 Summery

In this chapter the specification and design of the project work is discussed. Simulations were carried out considering designed values using Proteus software. Arduino uno microcontroller was utilized in the project for controlling motor. ACS712 hall base current sensor is used to measure the current of three line current individually. A schematic design, routing, layout design and 3D model of the project work was developed for prototype.

CHAPTER 5

SIMULATION AND HARDWARE IMPLEMENTATION

The simulation of the hysteresis current controller is carried out in MATLAB Simulink software. It also shows the board interface diagram and the schematic, routing and 3D modeling of the project work.

5.1 Simulation

The selected topology is simulated in MATLAB simulink environment. The effectiveness of the controller designed is validated and performance of converter is validated. Table 5.1 shows the parameter values considered for MATLAB simulation of project work. The Fig 5.1 below shows the simulink model of proposed project work. It shows three phase inverter block, SIMULINK model of BLDC motor, Hysteresis current controller block and back EMF block to know the position of rotor, speed control block and scope to measure the back EMF, torque and stator current.

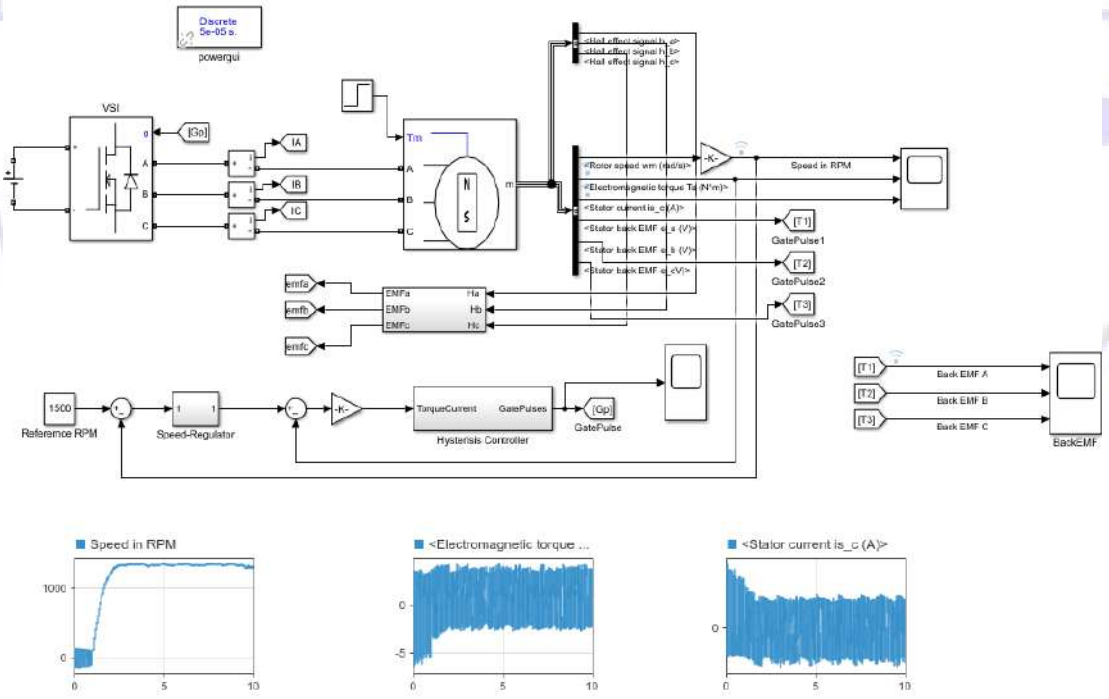

Fig 5.1 Simulink Model of Three Phase Inverter Drive to Control BLDC Motor Using Hysteresis

The Fig 5.2 shows the back EMF measurement based on hall sensor signals. It can be matches based on the Table 5.1.

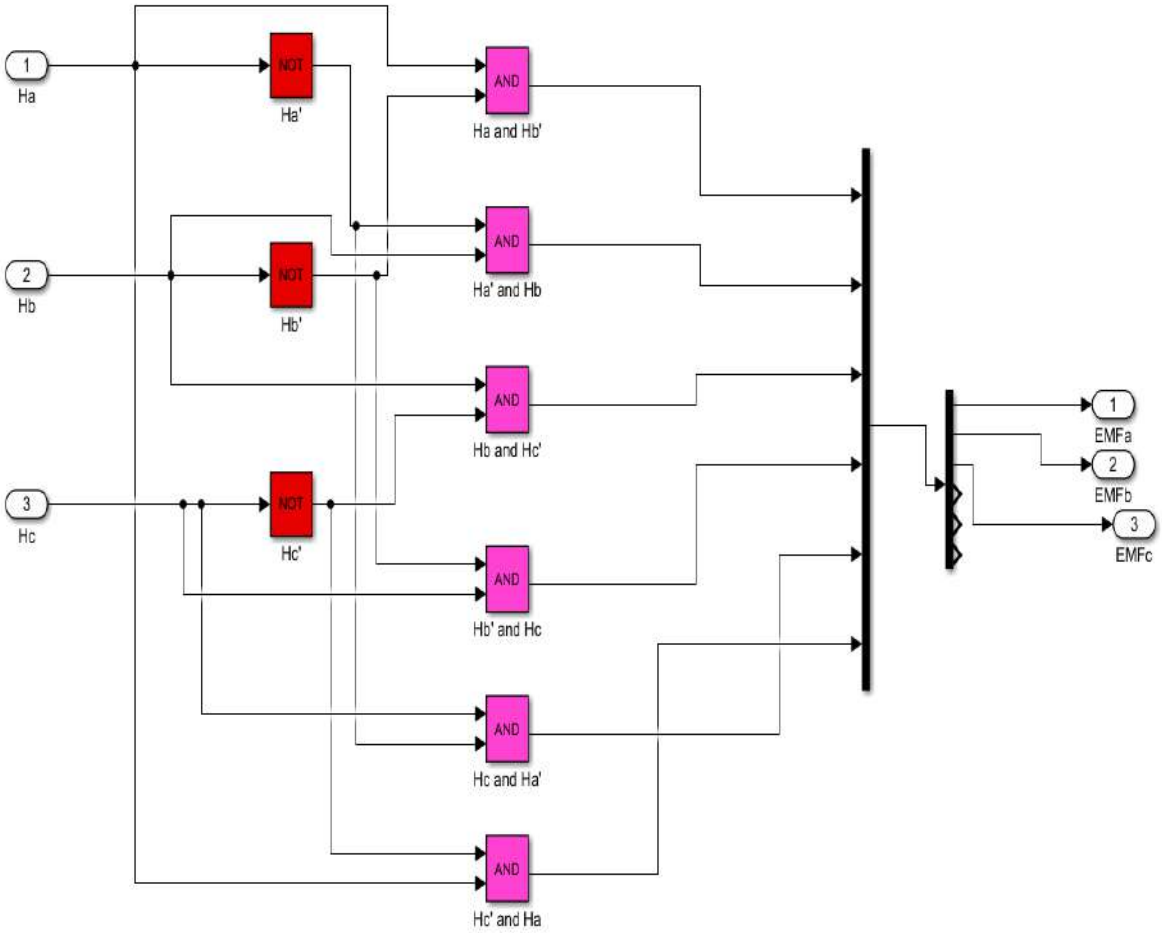

Fig 5.2: Back EMF Measurement Based on Hall Sensor

Table 5.1 Position of Rotor Based on Hall Sensor Signals

Angle θ in electrical degree	Hall Sensors		
	H1	H2	H3
0° - 60°	1	0	1
60° - 120°	1	0	0
120° - 180°	1	1	0
180° - 240°	0	1	0
240° - 300°	0	1	1
300° - 360°	0	0	1

Fig 5.3 shows the hysteresis current controller block.

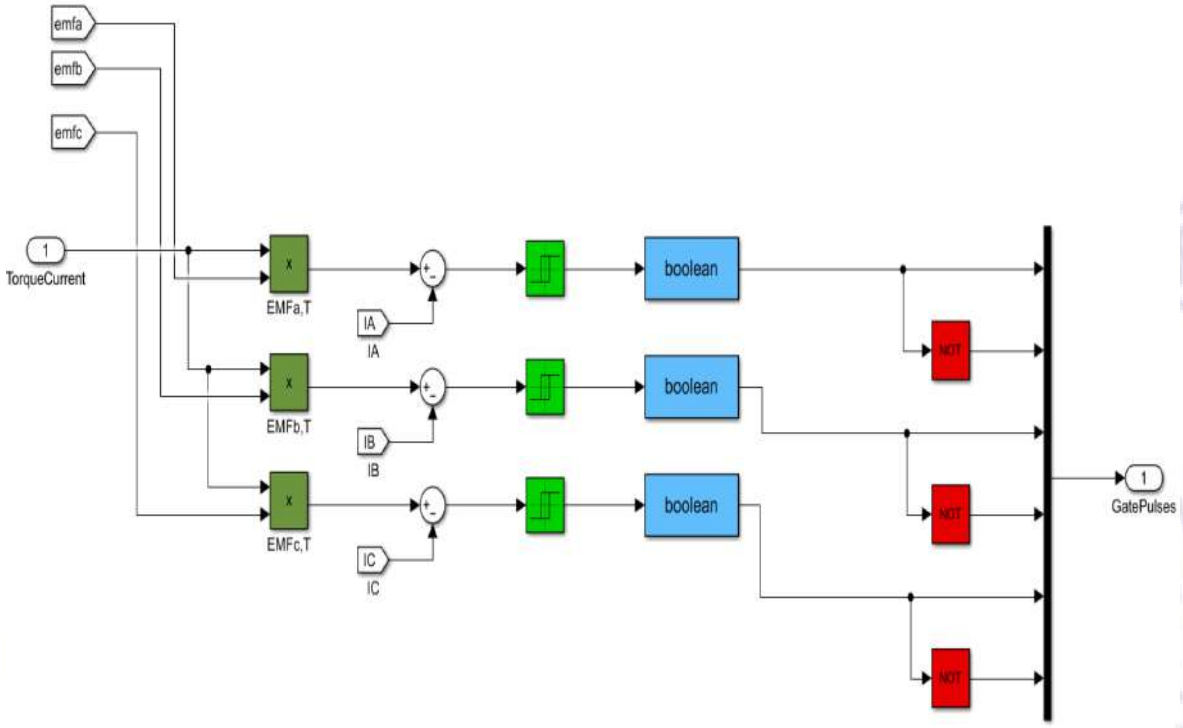

Fig 5.3 Hysteresis Current Control Block

Fig 5.3 shows the trapezoidal back EMF of the BLDC motor and Fig 5.4 shows speed, current and torque waveform of BLDC motor

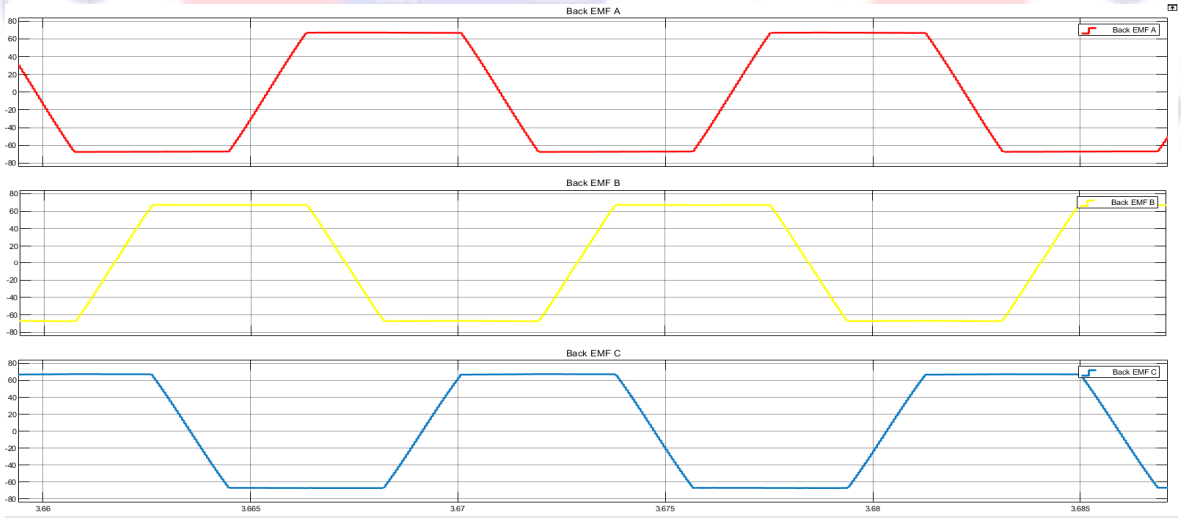

Fig 5.4 Simulated Trapezoidal Back EMF Wave Form

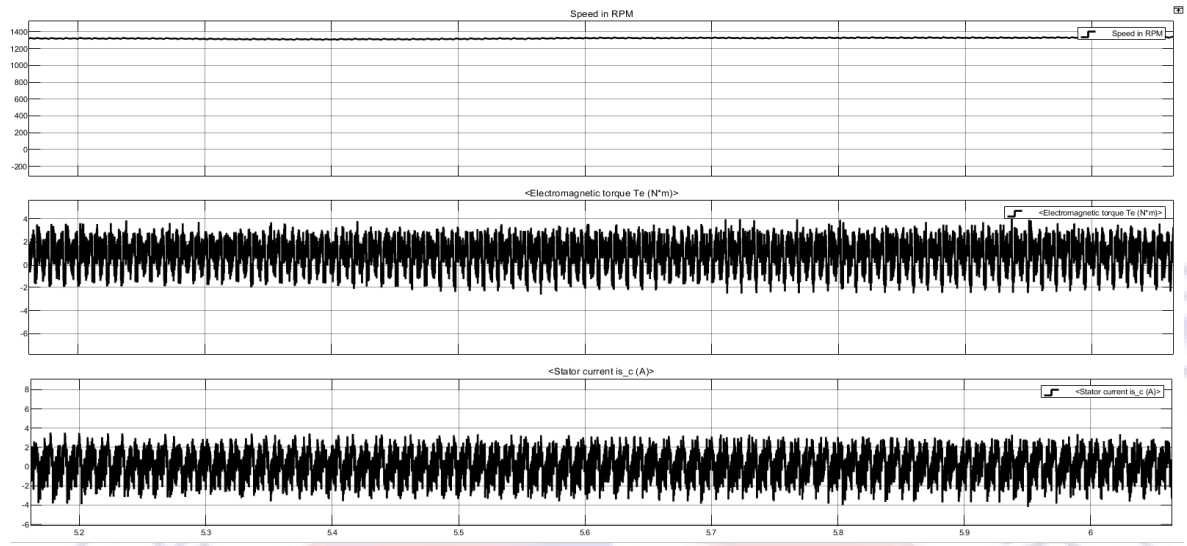

Fig 5.5 Speed, Torque, and Current Waveform of BLDC Motor

5.2 Schematic diagram

A schematic diagram is drawn relevant to the project work which includes three phase inverter section, gate driver section, power supply section and signal buffer section. A schematic diagram is a basic, two-dimensional depiction of a circuit that demonstrates the operation and connection of various electrical components. The schematic diagram of the project work is shown in Fig 5.5. Fig 5.6 shows the layout design of proposed project.

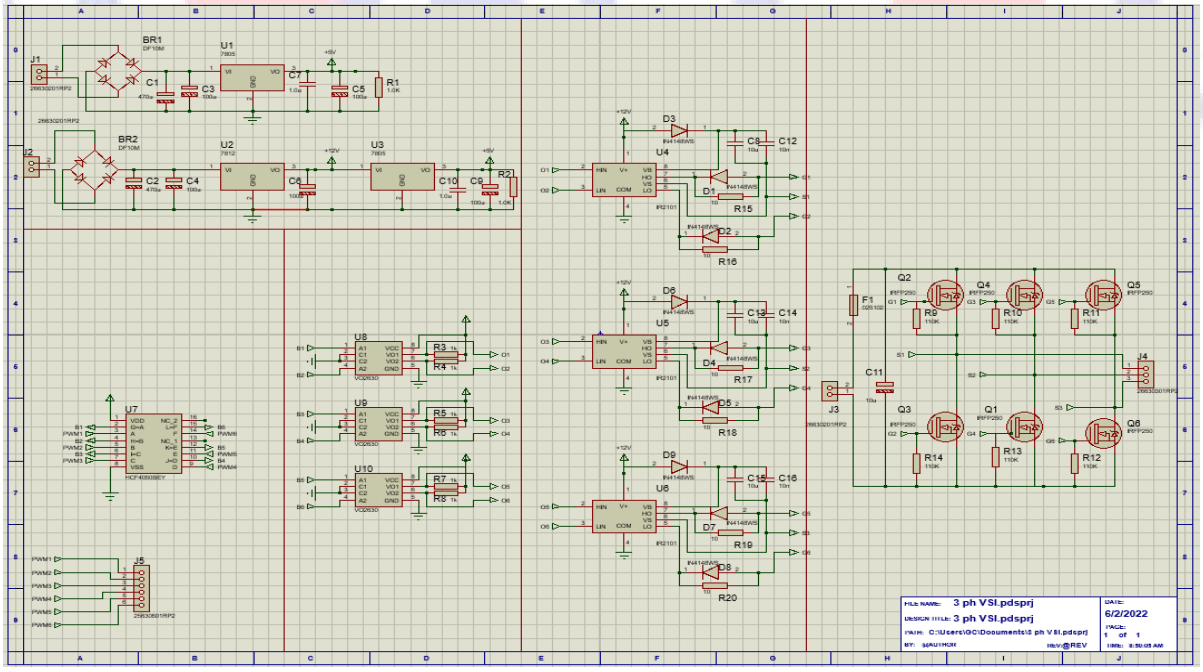

Fig 5.5 Schematic Diagram of Proposed Project Using Proteus Software

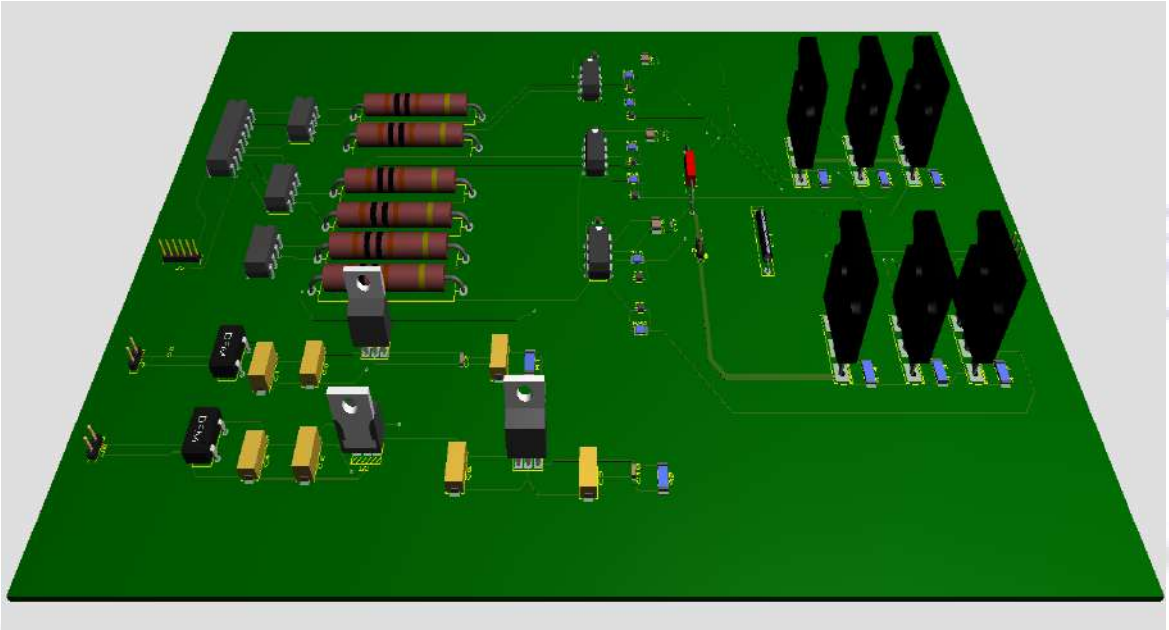

Fig 5.6 PCB Layout of Proposed Project Using Proteus Software

5.3 Hardware Implementation

Fig 5.7 and Fig 5.8 shows the hardware implementation of the proposed work under no load condition with input supply voltage of 9.1 V.

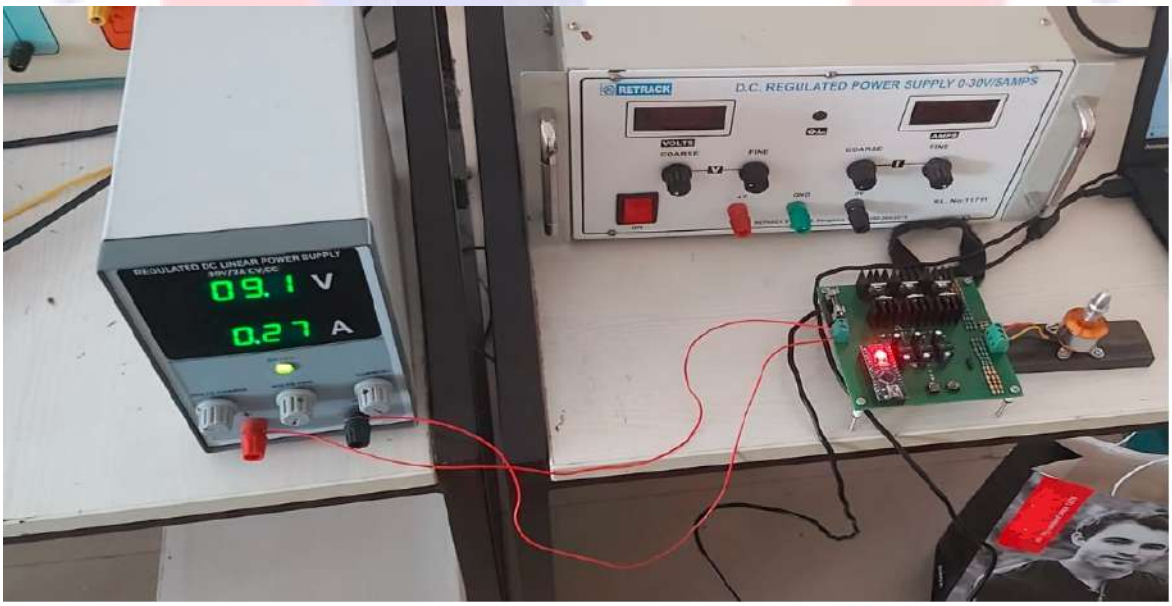

Fig 5.7 Hardware Implementation of Proposed Project.

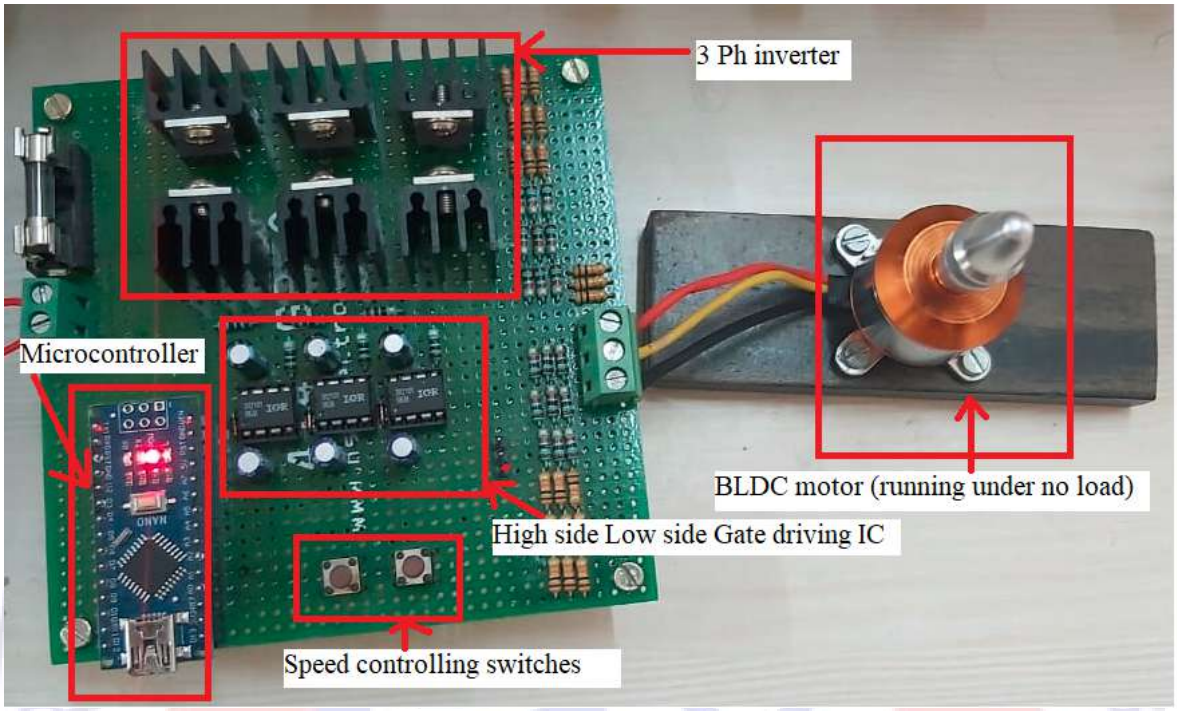

Fig 5.8 Hardware Implementation of Proposed Project Under No Load

Fig 5.9 shows the hardware implementation of the proposed work under load condition with propeller as virtual load and input supply voltage of 11V.

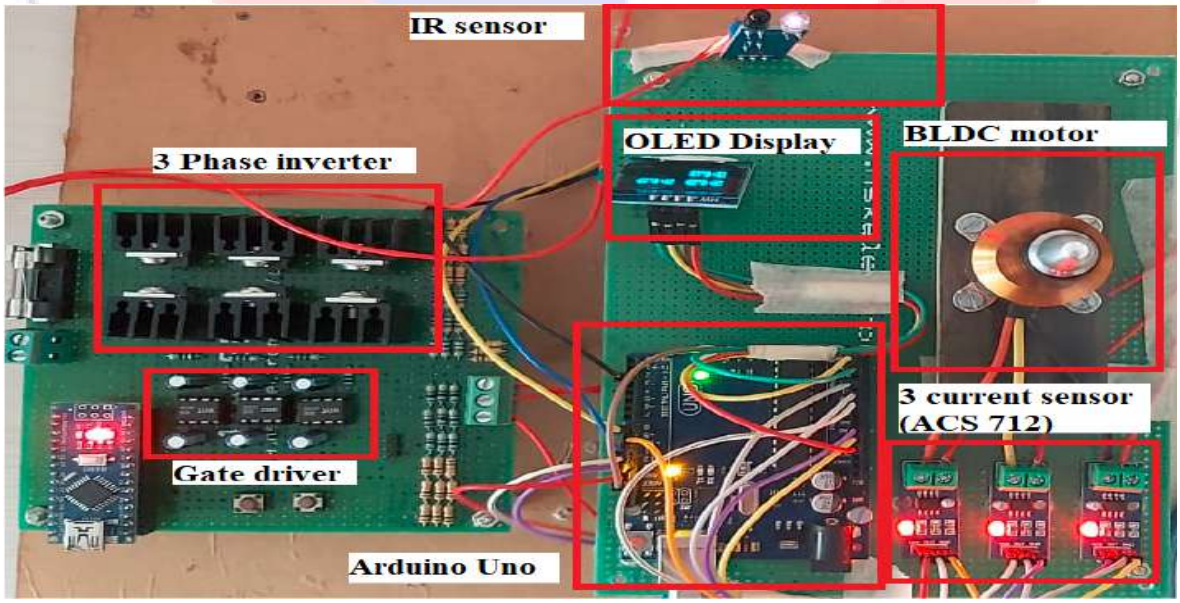

Fig 5.9 Hardware Implementation of Proposed Project with Propeller as Virtual Load

Fig 5.10 and 5.11 depicts gate signal at 40% duty cycle applied to high side MOSFETs and low side MOSFETs

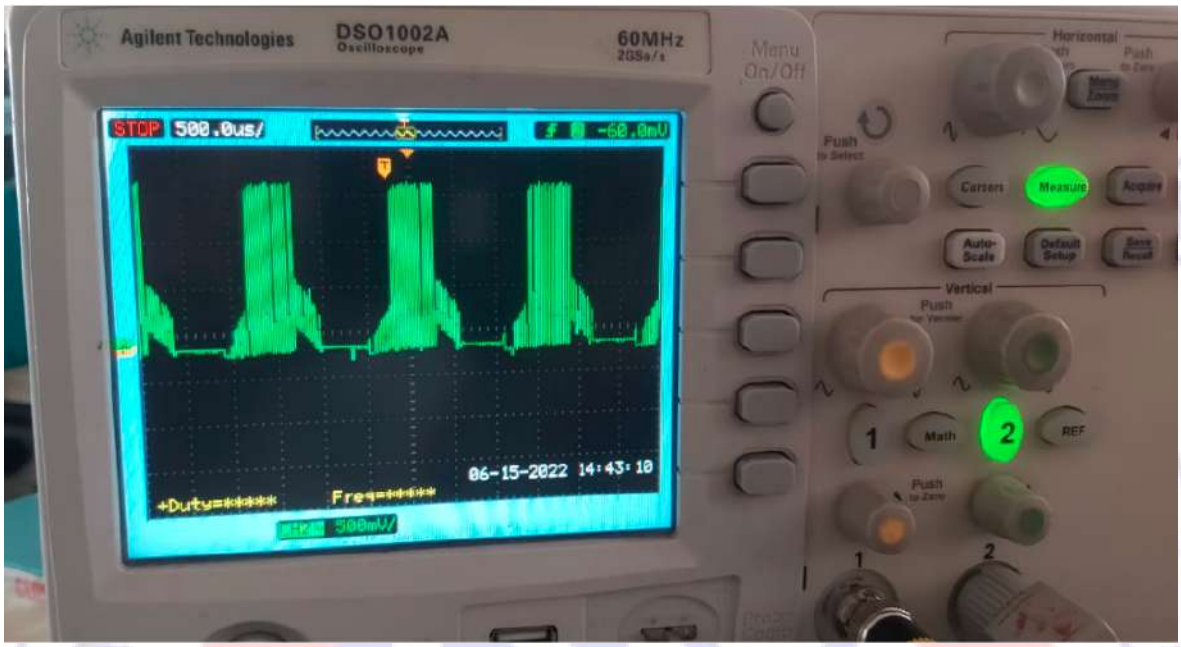

Fig 5.10 High Side Gate Signals at 40 % Duty Cycle

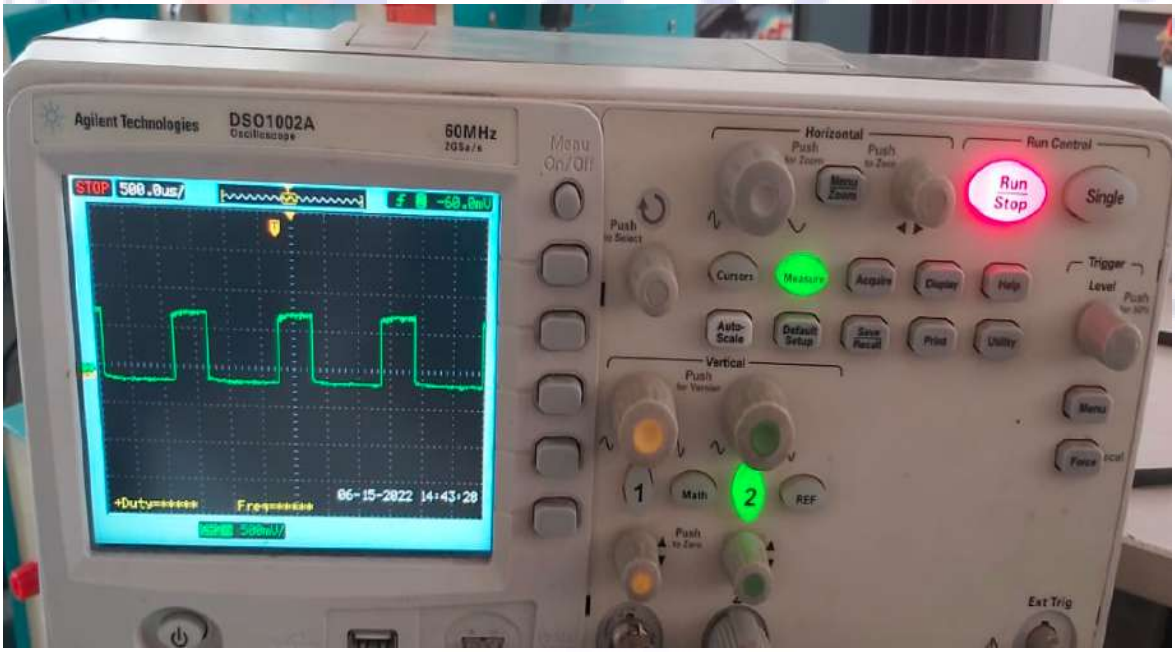

Fig 5.11 Low Side Gate Signals at 40 % Duty Cycle

Fig 5.12 and 5.13 depicts gate signal at 90% duty cycle applied to high side MOSFETs and low side MOSFETs. And Fig 5.14 shows the line to line voltage across the BLDC motor.

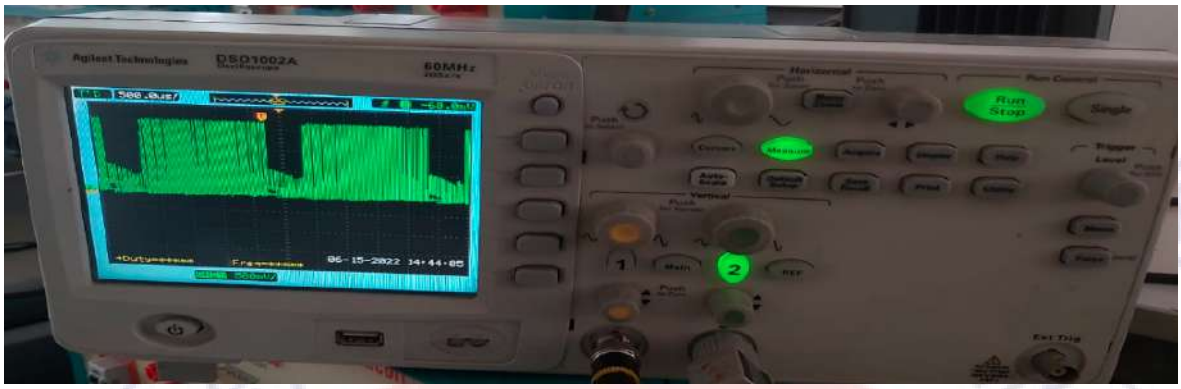

Fig 5.12 High Side Gate Signals at 90 % Duty Cycle

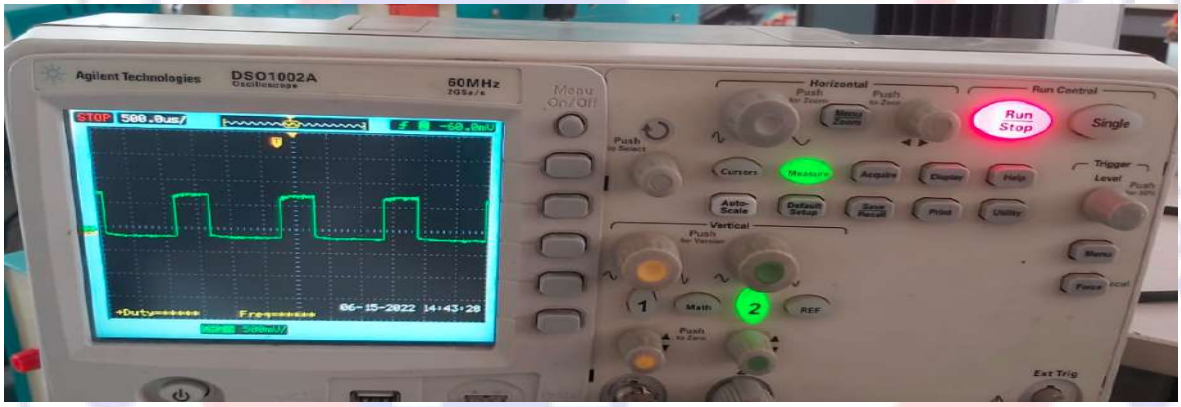

Fig 5.13 Low Side Gate Signals at 90 % duty cycle

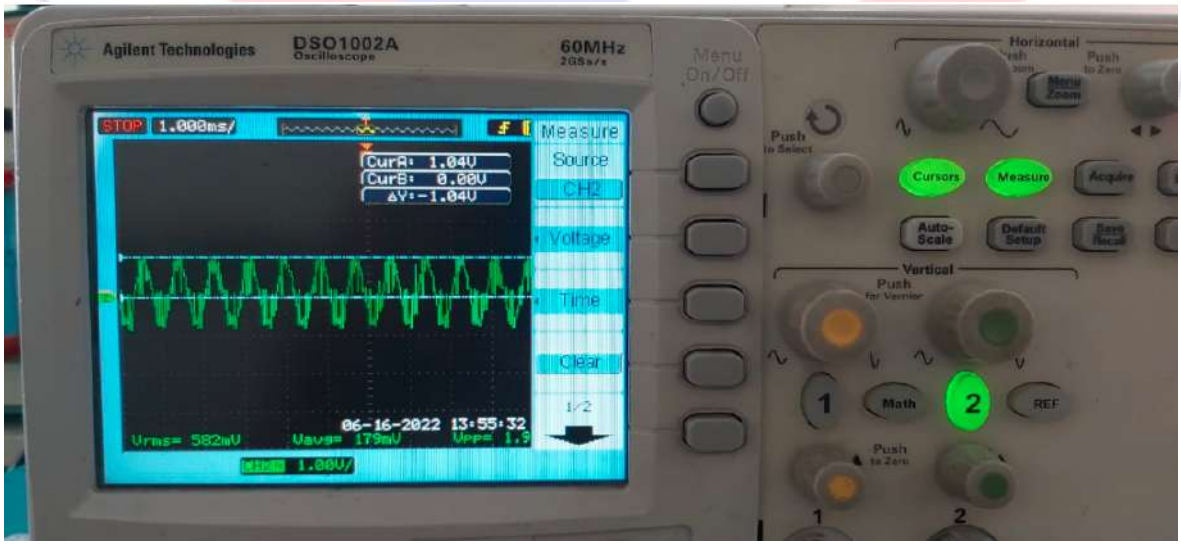

Fig 5.14 Line to Line voltage across the BLDC motor

5.4 Summery

In this chapter the simulation and hardware implementation of proposed prototype under no load and load conditions were studied in brief. The waveforms of gate pulses at different duty cycle applied to high side and low side MOSFETs were measured. Line to line voltage across the BLDC motor was also measured.

CHAPTER 6

RESULTS AND DISCUSSION

This chapter briefly discusses about the simulation and hardware results of the proposed three phase inverter using Hysteresis current controller. Also it discusses the results obtained in the hardware implementation of system.

6.1 Simulation Results

Table 6.1 shows the simulated results of speed in RPM and settling time

Table 6.1: Speed Vs Settling Time

Set Speed in RPM	Output Speed in RPM	Settling Time
200	200	4 sec
400	400	16 sec
600	600	16 sec
800	800	18 sec
900	895	20 sec
1000	1000	20 sec
1200	1200	25 sec

6.2 Hardware Results

6.2.1 Under No Load

Table.6.2 Representation of theoretical and observed input DC voltage, DC current, line voltage and R,Y, B phase currents under no load

Input DC voltage	Input DC current	Theoretical Line voltage	Observed Line voltage	Current in R phase	Current in Y phase	Current in B phase
9V	0.27A	4.05 V	2.7 V	0.17 A	0.05 A	0.043 A
10V	0.42 A	4.50 V	3.5 V	0.09 A	0.09 A	0.24 A
11V	0.7 A	4.95 V	4.2 V	0.233 A	0.116 A	0.117 A
12V	0.9 A	5.40 V	5 V	0.119 A	0.45 A	0.12 A

6.2.2 Under Load at 9V supply

Table.6.3 Representation of theoretical and observed input DC voltage, DC current line voltage and R, Y, B phase currents at 9V supply

I_load (Amps) @ 9 V Supply	Speed in RPM	Ir (Amps)	Iy (Amps)	Ib (Amps)
0.48	3010	0.20	0.10	0.19
0.54	3420	0.54	0.16	0.18
0.77	4000	0.77	0.44	0.19
0.97	4400	0.97	0.215	0.186
1.4	4960	1.2	0.254	0.244
1.5	5500	1.5	0.542	0.688
1.84	6040	1.84	0.31	0.78
2	6500	0.586	0.552	0.674

6.2.3 Under Load at 12V supply

Table.6.4 Representation of theoretical and observed input DC voltage, DC current line voltage and R,Y, B phase currents at 12V supply

I_load (Amps) @ 12V DC sypply	Speed in RPM	Ir (Amps)	Iy (Amps)	Ib (Amps)
0.5	3030	0.024	0.015	0.479
0.6	3440	0.044	0.103	0.44
0.82	4030	0.459	0.127	0.142
1.02	4460	0.166	0.674	0.137
1.3	5020	0.239	0.981	0.098
1.53	5430	0.737	0.156	0.034
2.2	6030	0.801	1.089	0.166
2.53	6400	0.72	0.53	0.166

Table 6.2, 6.3, 6.4 shows the theoretical and observed input DC voltage to the BLDC motor, DC current, line voltage and R,Y, B phase currents in amps under no load at 9V, load at 12V supply along with respective speeds in RPM is tabulated. Fig 6.1, Fig 6.2 depicts the graph plotted for speed vs current for the above mentioned table.

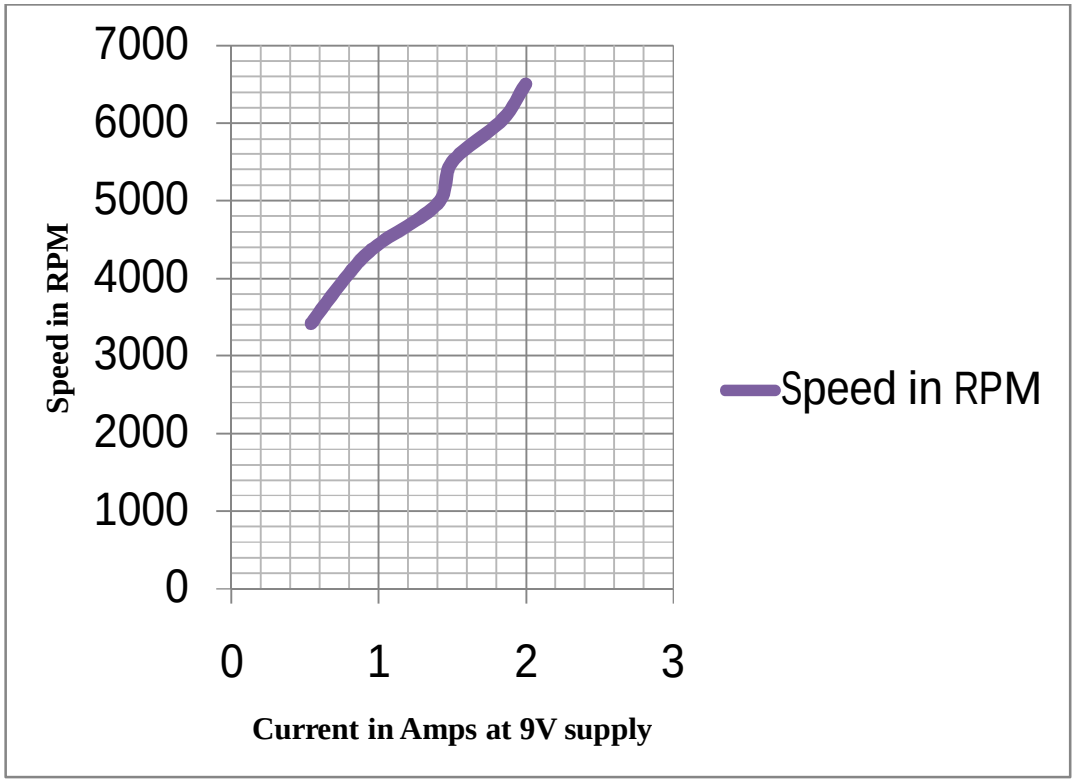

Fig 6.1 Speed Vs Current Plot at 9V Supply

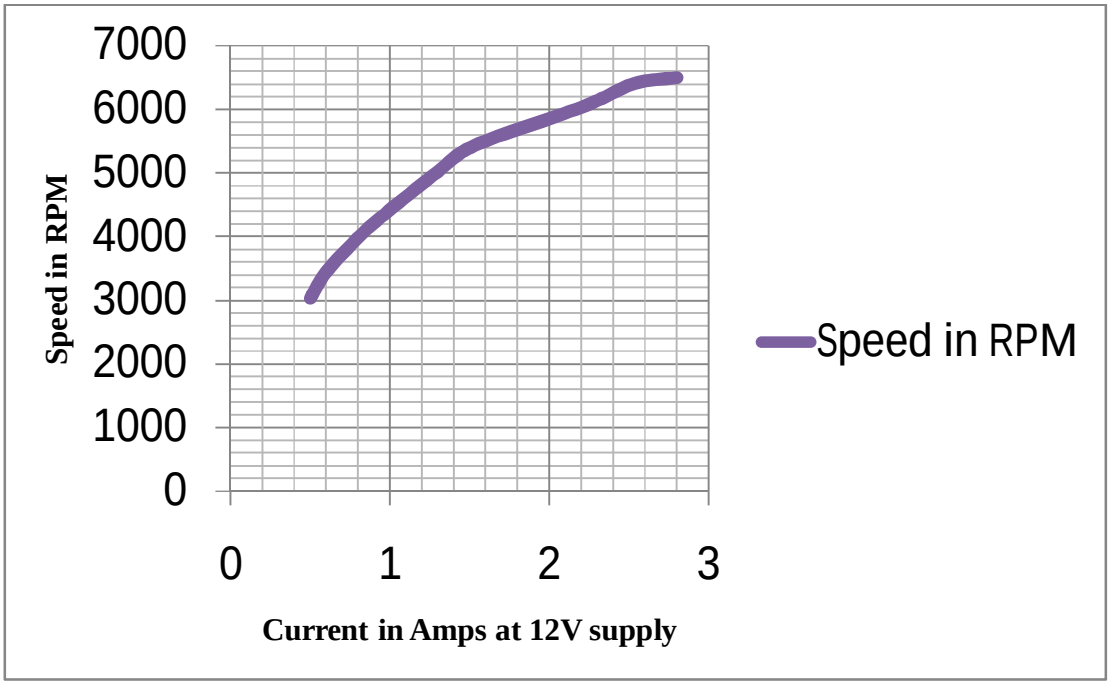

Fig 6.2 Speed Vs Current Plot at 12V Supply

6.3 Summary

In this chapter the simulation results and hardware results of speed vs current under no load and load conditions are tabulated. The three R, Y, & B line currents are measured and tabulated for different input voltages. The tabulated values are plotted in graph for different input voltages.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

Hysteresis current control (HCC) nonlinear current control has many advantages such as simple structure, fast dynamic response, robustness to the variance of load parameters, and being implemented easily. By using the conventional technique, the ripples are produced in the load current waveform. These drawbacks are overcome by developing a prototype of hysteresis current controller. Hysteresis controller is used to track error between the referred and measured currents. Hysteresis bandwidth is adjusted for error removal in reference tracking.

In order to obtain high quality power, controller with rapid response, less transient time, high tracking ability, less harmonic distortion and smooth sinusoidal output is to be designed. The ripples are produced in the load current waveform. Because of distortion in the load current the power factor will decrease. Hence these drawbacks can be overcome by developing a prototype of hysteresis current controller. As the power factor increases, the power conversion from DC to AC becomes more efficient.

7.1 Conclusion

Hysteresis current controlled method for three phase inverter to drive BLDC motor was designed, simulated and implemented in hardware. The simulation of the speed control of the BLDC motor using hysteresis current controller is simulated in the MATLAB Simulink environment. The main component includes IRF250N MOSFETS, A2212 BLDC motor, ACS712 current sensor and IR2101 gate driver. Propeller was used as virtual load for the BLDC motor. Both no load and under load condition were tested.

- The Hardware implementation of three phase inverter results shows, for input of 12V DC to the three phase inverter, the output of approximately 5.8V AC was produced.
- The three line currents of BLDC motor were tabulated for input voltage of 9V & 12V under load and no load conditions. Graphs were plotted for speed (in rpm) vs load current (in amps) for tabulated values with input voltage of 9V and 12V under load conditions.
- The output voltage and output current obtained were 5.8V and 6A respectively at load. From the results it is observed that the output current increase with increase speed both with and without load.

- It was observed that by using a 8-bit controller like Arduino Uno microcontroller, high precession in current sensing was not able to measure.

7.1 Future Scope

There is scope for future improvement of converter. They are as listed below

- The microcontroller can be further studied for controlling current. 32 bit Microcontrollers like DSP based or FPGA based with high clock frequency can be used to monitor the current precisely.
- In inverter design, MOSFETs with low Rds on and low Qg is preferred for low power loss and high switching frequency.
- Paralleling of switches in the each leg instead of single switch may be done to reduce switching loss.

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APPENDIX

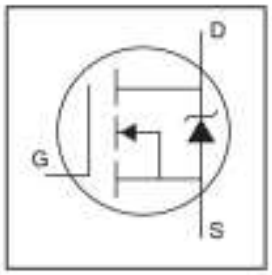
International
IOR Rectifier

PD - 95007A

IRFP250NPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free



V_{DSS} = 200V

$R_{DS(on)}$ = 0.075Ω

I_D = 30A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	30	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	21	
I_{DM}	Pulsed Drain Current ①	120	
P_D @T_C = 25°C	Power Dissipation	214	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	315	mJ
I_{AR}	Avalanche Current①	30	A
E_{AR}	Repetitive Avalanche Energy①	21	mJ
dv/dt	Peak Diode Recovery dv/dt ③	8.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

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IRFP250NPbF

International
IOR Rectifier

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.075	Ω	V_{GS} = 10V, I_D = 18A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	17	—	—	S	V_{DS} = 50V, I_D = 18A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	123	nC	I_D = 18A
Q_{gs}	Gate-to-Source Charge	—	—	21		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	57		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = 100V
t_r	Rise Time	—	43	—		I_D = 18A
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		R_G = 3.9Ω
t_f	Fall Time	—	33	—		R_D = 5.5Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	2159	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	315	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	83	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	120		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 18A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	186	279	ns	T_J = 25°C, I_F = 18A
Q_{rr}	Reverse Recovery Charge	—	1.3	2.0	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② Starting T_J = 25°C, L = 1.9mH R_G = 25Ω, I_{AS} = 18A. (See Figure 12)

③ I_{SD} ≤ 18A, di/dt ≤ 374A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

International
IOR Rectifier

Data Sheet No. PD60043 Rev.O

IR2101(S)/IR2102(S) &(PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of phase with inputs (IR2102)
- Also available LEAD-FREE

Product Summary

V_{OFFSET}	600V max.
I_O+/-	130 mA / 270 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	160 & 150 ns
Delay Matching	50 ns

Packages

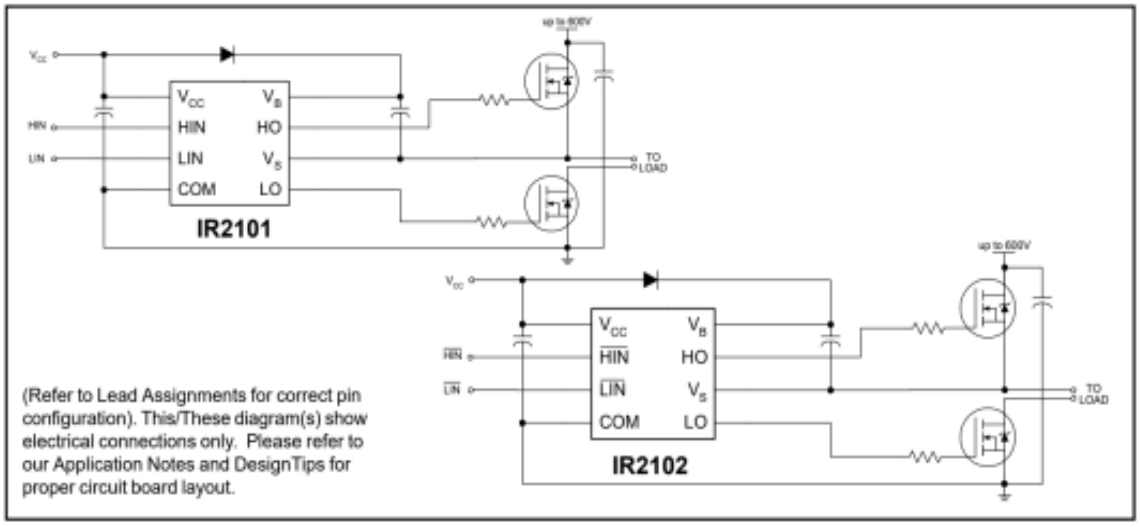
8-Lead SOIC
IR2101S/IR2102S

8-Lead PDIP
IR2101/IR2102

Description

The IR2101(S)/IR2102(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN) (IR2101) & ($\overline{HIN}$ & $\overline{LIN}$) (IR2102)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

International IOR Rectifier

IR2101(S)/IR2102(S) & (PbF)

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	160	220	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 600V
t_r	Turn-on rise time	—	100	170		
t_f	Turn-off fall time	—	50	90		
MT	Delay matching, HS & LS turn-on/off	—	—	50		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage (IR2101) Logic "0" input voltage (IR2102)	3	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage (IR2101) Logic "1"input voltage (IR2102)	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current	—	3	10		V_{IN} = 5V (IR2101) V_{IN} = 0V (IR2102)
I_{IN-}	Logic "0" input bias current	—	—	1		V_{IN} = 0V (IR2101) V_{IN} = 5V (IR2102)
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	V_O = 0V V_{IN} = Logic "1" PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	360	—		V_O = 15V V_{IN} = Logic "0" PW ≤ 10 µs

A2212/13T TECHNICAL DATA

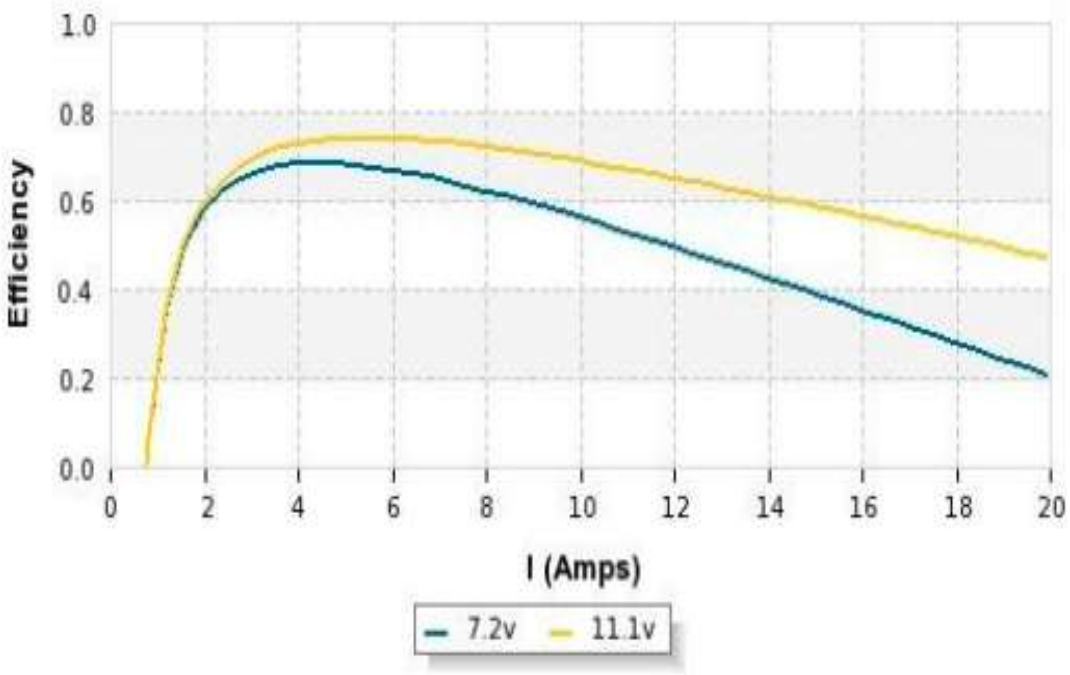
No. of Cells:	2 - 3 Li-Poly 6 - 10 NiCd/NiMH
Kv:	1000 RPM/V
Max Efficiency:	80%
Max Efficiency Current:	4 - 10A (>75%)
No Load Current:	0.5A @10V
Resistance:	0.090 ohms
Max Current:	13A for 60S
Max Watts:	150W
Weight:	52.7 g / 1.86 oz
Size:	28 mm dia x 28 mm bell length

Shaft Diameter:	3.2 mm
Poles:	14
Model Weight:	300 - 800g / 10.5 - 28.2 oz

An small yet powerful motor for planes up to 800 grams (28 oz) using 3 li-poly cells. We suggest propping for around 140 watts continuous power with short bursts up to 180 watts. An excellent higher-powered replacement for geared Speed 400-480 motors in slow-flying or 3D planes that require a larger 10" propeller. Use on sailplanes up to 28 oz, trainers up to 25 oz, aerobatic aircraft up to 18 oz and 3D airplanes up to 15 oz. Recommended prop is 10 x 5 on 3 li-poly cells.

The motor features a 3.2mm hardened steel shaft, dual ball bearings, and has 3.5mm gold spring male connectors already attached and includes 3 female connectors for your speed control. Now includes collet type prop adapter and radial motor mount. Mounting holes have 16mm and 19mm spacing on centers and are tapped for 3mm (M3) screws.

Similar to Welgard A2212-13, AXI Gold A2212/26, Welgard C2830-12, E-Flite Park 400. Great replacement motor for a 1/2A Texaco engine.



IO TEST DATA

Volts	Amps	RPM
7	0.6	7380
8	0.65	8460
10	0.75	10500

Design and Implementation of Three Phase Inverter for BLDC Motor using Hysteresis Current Control Technique
D V Manjunath [1RV20EPE01]
M.Tech in PE, Department of Electrical and Electronics Engineering
RV College of Engineering, Bangalore – 560059, INDIA
OBJECTIVE
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Speed vs load current graph
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Design and Implementation of Three Phase Inverter for BLDC Motor using Hysteresis Current Control Technique

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[1]PG Student,[2] Associate Professor,

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Abstract : BLDC motor has high torque-to-speed ratio, wide speed control range, and higher efficiency compared to traditional dc motors, brushless dc motors are widely used in daily life. To manage both its speed and torque, a BLDC motor must be connected to electrical equipment as it cannot be handled manually. For the purpose of producing commutations dependent on the position of the rotor, a three phase inverter is often necessary. The low power factor number is a result of harmonic issues caused by high frequency switching on the inverter side. It is noted that the hysteresis current controller with a speed feedback loop used in this study reduces torque ripples. Simulation is carried out using MATLAB/SIMULINK. In order to drive BLDC motors, a hardware prototype of a three-phase inverter was created. It was tested under load using various input voltages that were within the motor voltage range.

Index Terms – **Three phase inverter, BLDC motor, Hall sensor, back EMF, Hysteresis current control.**

I. Introduction

Electric cars use a variety of electric motors, including three phase AC induction motors, switched reluctance motors, brushless DC motors, permanent magnet synchronous motors (PMSM), DC series motors, and brushless DC motors (SRM). BLDC motor is one of these motors widely used in EVs.

In the modern day, brushless motors are far more popular than brushed ones. The applications for both, however, are quite diverse. In many domestic products and autos, brushed direct current motors are still in use. The flexibility to alter the torque to speed ratio, which is exclusive to brushed motors, gives it a strong industrial niche as well. The brushless DC motor is categorized in to out runner BLDC motor and in runner BLDC motor. In the in runner BLDC motor design, the stator is positioned outside, and the motor's rotor is inside. In the out runner design, stator of the motor is positioned inside, while the rotor is outside. It is also known as a hub motor as the wheel is directly attached to the external rotor.

II. Hysteresis current control method

The block diagram of hysteresis current control of BLDC motor is shown in figure 1. The output current ia, ib, ic of inverter are sensed and compared with reference current ia*, ib*, ic*. Current error signals are then applied to hysteresis current controller, which generates switching signals, to the respective six switches. The ia, ib and ic currents and be measured in two ways. One is by using hall sensors at three terminals of motor. But these hall sensor are to be placed very close to rotor. Another method is by sensorless back EMF method. In Sensorless back EMF method, the real time currents can be measured but it has 30° phase shift.

The width of the hysteresis band, denoted by h, represents the tolerance bandwidth for the controlled current. If the actual current in tries to go beyond the lower tolerance band or higher tolerance band. Gate signals are produced such that switches are triggered in the 120 commutation sequences and no two switches of same leg are triggered at same time.

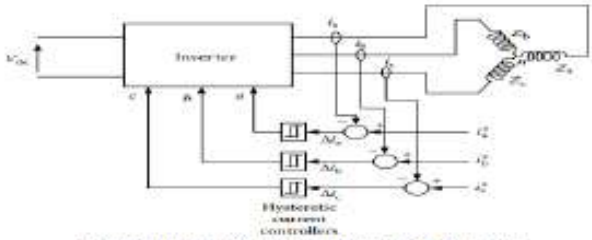

Figure.1 Hysteresis current control of BLDC motor

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III. Simulation Analysis

The figure 2 show the complete MATLAB / simulink model of hysteresis current controlled BLDC motor. Here a DC voltage source is used as constant voltage source for three phase inverter. Three phase inverter is used to drive the BLDC motor.

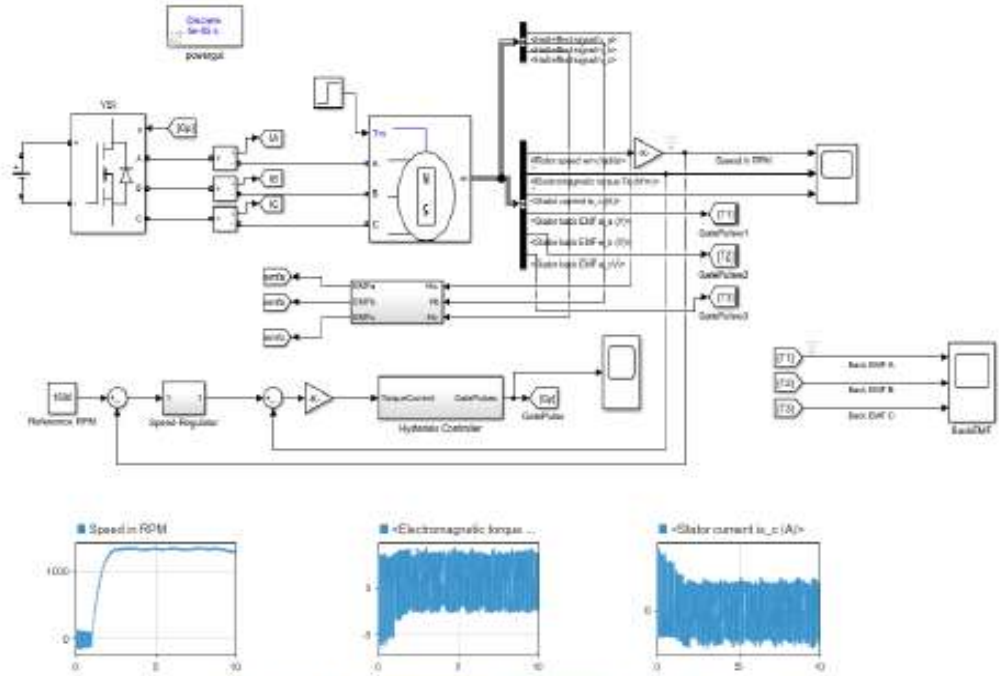

Figure 2 Simulink model of Hysteresis current controlled BLDC motor

From figure 3, the signals from the hall sensors are used to measure the back EMF signals. The back EMF signals are multiplied with torque to get the reference current and are compared with actual current ia, ib and ic. The error signal of comparator is sent to Hysteresis block as shown in Fig 4. Based on the output signals of hysteresis block gate signals are produced to trigger the switches of three phase inverter.

Figure 3 Hall sensor signals to measure the back EMF of BLDC motor

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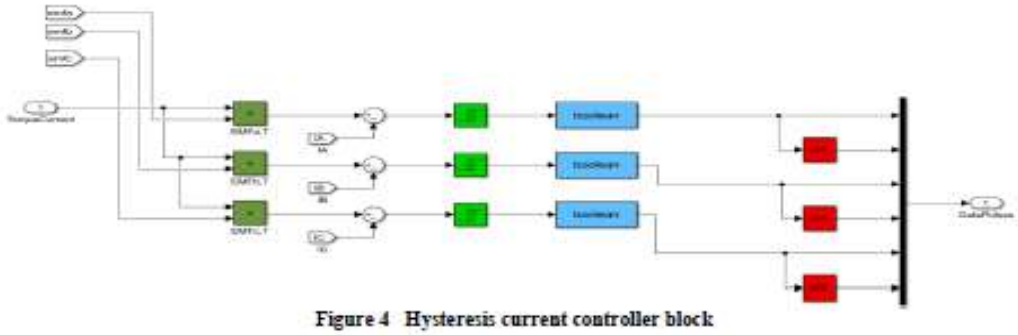

Figure 4 Hysteresis current controller block

IV. HARDWARE PROTOTYPE

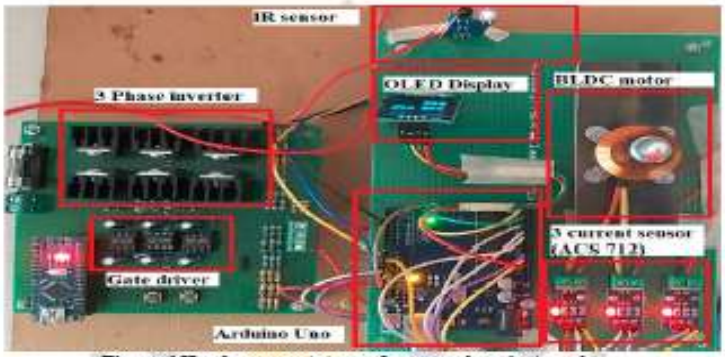

Figure 6 Hardware prototype of proposed project work

The fig shows hardware prototype of project work which includes three phase inverter, gate driver circuit, and microcontroller to generate PWM signals in left side board. And on the right side board includes BLDC motor, three hall sensors, IR sensor to measure speed and OLED display

V. RESULT

Fig.7 shows the trapezoidal back EMF of BLDC of phase A, phase B and phase C. And Fig.8 shows (a)Speed in RPM (b)Torque in Nm (c) Stator current in C phase

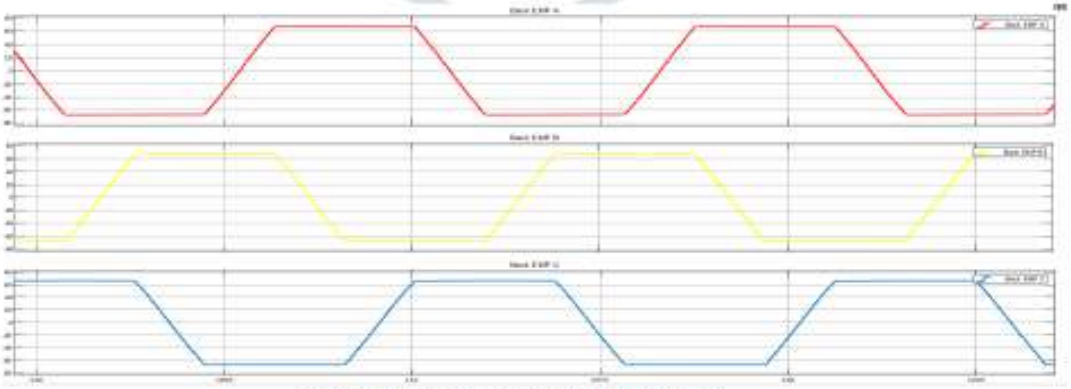

Figure 7 Trapezoidal back EMF of BLDC motor

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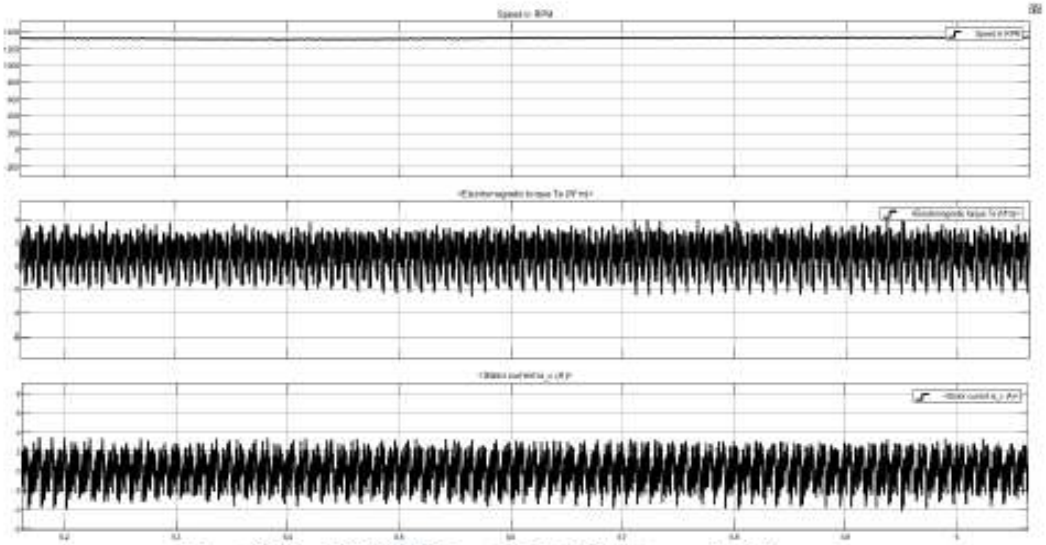

Figure 8(a)Speed in RPM (b)Torque in Nm (c) Stator current in C phase

Table 1 shows the results of hardware implementation of proposed project work. The speed vs current of motor is tabulated, under loaded condition at two different supply voltages.

Table 1a speed vs current at 9V DC supply

I_load (Amps) @ 9 V Supply	Speed in RPM	Ir (Amps)	Iy (Amps)	Ib (Amps)
0.48	3010	0.20	0.10	0.19
0.54	3420	0.54	0.16	0.18
0.77	4000	0.77	0.44	0.19
0.97	4400	0.97	0.215	0.186
1.4	4960	1.2	0.254	0.244
1.5	5500	1.5	0.542	0.688
1.84	6040	1.84	0.31	0.78

Table 1b speed vs current at 12V DC supply

I_load (Amps) @ 12V DC svpply	Speed in RPM	Ir (Amps)	Iy (Amps)	Ib (Amps)
0.5	3030	0.024	0.015	0.479
0.6	3440	0.044	0.103	0.44
0.82	4030	0.459	0.127	0.142
1.02	4460	0.166	0.674	0.137
1.3	5020	0.239	0.981	0.098
1.53	5430	0.737	0.156	0.034
2.2	6030	0.801	1.089	0.166

Fig.9 shows the graph plotted for speed vs load current at different supply voltages

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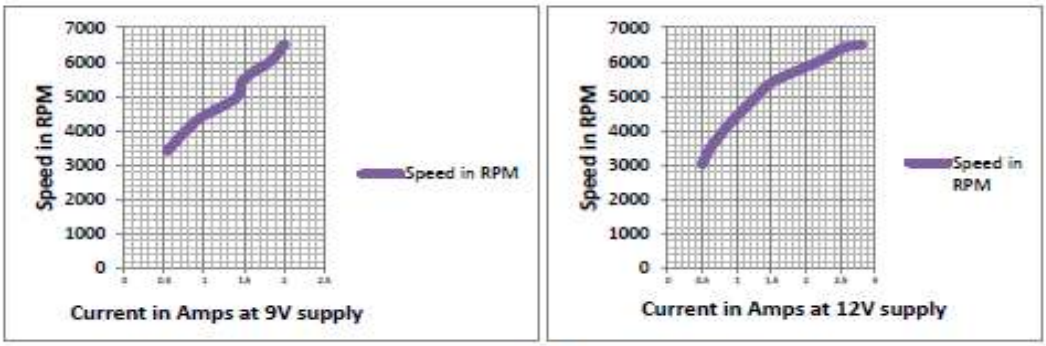

Figure 9 Speed vs load current

VI. Conclusion

1. A three phase inverter has been designed and simulated to drive BLDC motor in MATLAB simulink and the speed of BLDC controlled .
2. PWM signals was experimentally generated using Arduino nano and the current was monitored using ACS716 current sensor.
3. A hardware module of 3 phase inverter drive to control speed of BLDC was developed.
4. The current through A, B, C phase was measured using ACS716 hall based current sensor.

VII. Future Scope

The project can implemented with add on technology to operate electric vehicle more efficiently and to reduce the energy lost and cost of EV:

1. The microcontroller can be further studied for controlling current. 32 bit Microcontrollers like DSP based or FPGA based with high clock frequency can be used to monitor the current precisely.
2. In inverter design, MOSFETs with low Rds on and low Qg is preferred for low power loss and high switching frequency.
3. Paralleling of switches in the each leg instead of single switch may be done to reduce switching loss.

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18EPE41

Submitted by

SPOORTHI HB

USN: 1RV20EPE16

Under the Guidance

of

Dr. Hemalatha J.N.
Associate professor
Dept. of EEE,
RV College of Engineering®
Bengaluru - 560059

Chiranjivi Murala,
Senior Engineer,
Dept. of EET, Robert BOSCH Engineering and Business solutions.
Bengaluru – 560030

Submitted in partial fulfillment for the award of degree

of

MASTER OF TECHNOLOGY

in

POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

2021-22

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ABSTRACT

Controlling exhaust emissions from internal combustion engines has emerged as one of the most pressing issues. Breathing difficulties, headaches, persistently impaired lung function, eye discomfort, lack of appetite, and corroded teeth are all possible side effects. The Indian government amended European regulations considering environmental concerns and health risks. To fulfil the impending pollution standards, existing engine technology must be modified, and a better system developed. Exhaust temperature management is the most effective approach for controlling emissions.

The temperature in the exhaust system has a significant impact on emissions since exhaust gas treatment equipment like catalysts, oxygen sensors, and storage catalysts operate only within a narrow temperature range. Catalytic converters, on the other hand, have light-off troubles during cold start and warm-up. Thus, by efficiently managing the exhaust system temperature, emissions are reduced to a given level. Catalytic converters reduce the emissions of CO, HC, NOx, and PM from internal combustion engines, allowing them to satisfy increasingly rigorous emission laws. This is possible with the right catalyst heating techniques controlling the engine parameters such as idle speed, spark ignition timing, engine efficiency, air to fuel ratio, engine torque.

Catalyst temperature is selected based on maximum temperature available. Lambda value is brought into its range 0.9 to 1.1. Camshaft valve angle varies optimally in order to allow the desired value of air and fuel into the combustion chamber. Methods based on engine parameter control, in particular, are simple to apply since they use the key findings, results or outcome of the work including experimental data of the outcome and percentage in terms of working efficiency of the developed product or system.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	SPOORTHI HB, Dr Hemalatha J N, "Methods of Thermal Management of Catalytic Converters in Gasoline-Based Engine Exhaust Systems", International Journal of Emerging Technologies and Innovative Research, ISSN:2349-5162, Vol.9, Issue 7, , July-2022, page no.a773-a784.

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GLOSSARY

ABS	:	Anti-lock Braking System
AUTOSAR	:	Automotive Open System Architecture
BC	:	Basic Component
CO	:	Carbon Monoxide
CO2	:	Carbon Dioxide
DOC	:	Diesel-Oxidation Catalysts
DPF	:	Diesel Particulate Filters
ECM	:	Engine Control Module
ECU	:	Engine Control Unit
EGR	:	Exhaust Gas Recirculation
FC	:	Functional Component
GPF	:	Gasoline Particulate Filters
HC	:	Hydro Carbon
HCCI	:	Homogeneous Charge Compression Ignition
IC	:	Internal Combustion
LTC	:	Low Temperature Combustion
NOx	:	Oxides of Nitrogen
NSC	:	NOX Storage Catalyst
OBD	:	On-board Diagnostics
OEM	:	Original Equipment Manufacturer
PCCI	:	Premixed Charge Compression Ignition
PCM	:	Power-train Control Module

CHAPTER 1

INTRODUCTION

Nowadays, people utilise cars a lot because they have more mobility that raises their standard of living. Economic growth is significantly impacted by the constant transportation of more and more people and things between different locations. India, the second-largest nation in the world by population, has a diverse economy, one of that is dominated by the transportation industry. According to statistics, the number of vehicles in India has increased by more than 240 percent in the last ten years. Over the next 20 years, it is anticipated that continues to grow at a similar rate. There are adverse consequences associated with this massive pace of automobiles.

The severe environmental risks like climate change, pollution, global warming, decreases crop yields, and threats to living things as a result of an increased dependency on fossil fuels and increased pollution emissions, that eventually leads to an overall ecological imbalance [1]-[4].

All societal growth sectors have better socioeconomic opportunities thanks to increased mobility. Therefore, it is crucial to direct this increase in a way that reduces the negative effects of automotive pollution. As a result, pollution regulations for cars are put up. In India, the initial emission rules went into effect in 1989. The mass emission restrictions for both gasoline and diesel automobiles during the 1990s eventually took the place of these idle emission limitations. The national adoption of these emission limits and deployment of the best emission control techniques have a substantial influence on the environment, the global economy, global warming, and public health.

Conventional pollutants like Carbon Monoxide (CO), Nitrogen Oxides (NOx), Particulate Matter (PM), Hydrocarbons (HC), and other greenhouse gases like Carbon Dioxide (CO_2), Methane (CH4), and others make up the majority of vehicular emissions from Internal Combustion engines. The national adoption of Bharat V/VI standards has the potential to drastically reduce vehicle emissions by 86 percent. Thus, without even mentioning the terrible load of air pollution, the nation is able to fully benefit from the fuel savings provided by the diesel technology [5]-[9].

To obtain high performance and minimal exhaust emissions, it is strongly advised to create engine control systems. An embedded mixed signal system called the engine management system communicates with the engine via a variety of sensors and actuators. It

organises, prioritises, and then puts all the needs for the engine into practise. The control strategies are meant to regulate the air-fuel ratio, the ignition, the electronic throttle, the idle speed, the location of the accelerator, etc. By carefully planning and implementing the control system, the engine produces more power [10]-[14].

There is a lot of money invested in the pursuit of greener fuels and cars. The cost of diesel and gasoline fuels are most likely increasing by around Rs. 0.30 to 0.44 per litre if ultra-low sulphur fuels with less than 10 ppm of sulphur are supplied. In addition, because after treatment devices must be installed to meet the strict emission rules, the price of automobiles is increased as a result of these standards. Figure.1.1 displays the year during car emission rules went into effect as well as the sulphur percentage of fuel. The majority of the technologies utilised to lower emissions also improves fuel efficiency. As a result, fuel consumption are reduced, that are going to increase the cost-effectiveness of using technology.

	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
Fuel Sulphur content (ppm)	50						10				
LDV Emission standard	BS Va		BS Vb			BS VI				EURO 7/ US tier 3	
HDV Emission standard		BS V				BS VI				EURO VII/JS2010	
2/3 Wheeler Emission Standard		BS IV				BS V				BS VI	

Figure.1.1. Implementation Year of Vehicle Emission Standards and Fuel Sulphur Content

It is necessary to update the current engine technology and create a better system in order to comply with the impending emission regulations. The best method for reducing emissions is through exhaust temperature management. Since exhaust gas treatment components like catalysts, oxygen sensors, and storage catalysts only function within a narrow temperature range, exhaust system temperature has a significant impact on emissions. Therefore, the emissions are reduced to a considerable extent by effectively regulating the exhaust system temperature. The main prerequisite for carrying out all the requirements is engine torque. The study gathers information to adapt an existing functional component to improve auto emissions control by controlling exhaust temperature [14]-[18].

1.1 Overview

Thermal management's goal is to quickly raise the catalysts' temperature to an appropriate level and keep it there in order to ensure the best possible conversion of exhaust emissions. A variety of various heat-up measures are feasible, depending on the individual system setup, boundary conditions or limits, and calibration of the heat-up approach. Here are a few key heat-up strategies:

- Request heat up operation mode with tailored injection pattern. Increased idle speed to improve exhaust mass flow over the catalyst.
- Late ignition timing to increase exhaust temperature and mass flow.
- To enable exotherm reaction on catalyst, rich combustion lambda set point in combination with secondary air is used.
- To enable exotherm reaction on the catalyst, request cylinder lambda split strategy (e.g., 2 cylinder rich / 2 cylinder lean.
- Disable the fuel cutoff in cold weather to prevent further cooling.

In addition to calculating the heating requirement, the heating strategy also considers technical and physical constraints as well as optimization criteria for the various emission components. A reactivation of the heat up steps must be ensured in the event of insufficient catalyst temperatures, such as cooling out or stopped heating.
Fuel consumption and CO_2 emissions are directly impacted by the temperature state of the exhaust catalysts, as well as exhaust emissions.

1.2 Specific Details

Temperature details : Catalysts usually convert harmful emissions only during their temperature reaches certain thresholds, i.e., the so-called light-off temperature, which is normally around 250–300 °C for TWCs. Hence, high levels of exhaust emissions are transferred into the atmosphere during the exhaust temperature is low, during the engine cold start or warm up phases, in which the catalyst is not fully operational.

Emission standards : Notorious pollutants emitted by internal combustion engines are carbon dioxide (CO_2), carbon monoxide (CO), oxides of nitrogen (NOx) and hydrocarbons. The direct injection petrol engines also emit carbon soot and particulate matter (PM). The permitted levels for harmfull gases is as follows; CO(1000 mg/km), HC (100mg/km), NOx (60mg/km), PM (4.5mg/km).

Lambda value : Lambda value that is the ratio of air to fuel ratio actual to stoichiometric value. The stoichiometric value should be equal to 14:7 for gasoline based engine exhaust emissions. The lambda value should be the range of 9.9 to 1.1. Ideally lambda value is equal to unity.

1.3 Literature Survey

The literature on catalyst thermal management is reviewed in detail, with the goal of drastically reducing light-off time and emission concentrations using optimal heating methods. Methods based on engine parameter control, in particular, are simple to apply since they do not necessitate the use of additional heating equipment. They have good performance in terms of reducing catalyst light-off time, but they have substantial fuel penalties due to heat loss and unburned fuel. Other thermal management technologies, such as those based on burners, reformers, and electrically heated catalysts, need the installation of extra equipment but provide flexibility in the placement and intensity of heat injection, which can efficiently limit heat loss in the tailpipe [1].

A spark-ignited (SI) engine's air-fuel ratio (AFR) imbalance diagnosis is shown. One or more cylinders' air to fuel ratios diverge from those of the other cylinders because of cylinder-specific issues, air to fuel ratio imbalance arises. It results in the key emission control system of a spark-ignited engine, accurate air to fuel ratio management, failing. As a result, the California Air Resource Board (CARB) has implemented the legislative requirement to identify severe air to fuel ratio imbalances that cause tailpipe emissions to exceed the relevant emissions levels. The time-varying harmonic signal estimation-based AFR imbalance diagnostics are created with this objective in mind. The time-varying notch filter (TV NF) and the adaptive Kalman filter (AKF) are the two filters used. The time-varying harmonic signal estimation-based AFR imbalance diagnostics are created with this objective in mind. To estimate the imbalance signal, two distinct filters—the time-varying notch filter (TV NF) and the adaptive Kalman filter (AKF)—are applied to the outputs of exhaust gas oxygen (EGO) sensors, such as heated exhaust gas oxygen (HEGO) and universal exhaust gas oxygen (UEGO) sensors. Real-time AFR imbalance diagnosis is done by monitoring the diagnostic metric based on the filter utilised. The turbo-charged SI natural gas (NG) engine is used as an example to demonstrate the effectiveness of the proposed diagnostics [2].

It is described to use the Smooth Super-Twisting Algorithm (SSTA) to adjust the air-to-fuel ratio (AFR) of a gasoline engine. Controlling the air-to-fuel ratio has remained a crucial issue in order to save calibration effort and meet performance standards. It is crucial to run a gasoline engine at the desired air-to-fuel ratio since a three-way catalytic converter operates at

its best around the stoichiometric value of air-to-fuel ratio. The main cause of the air-to-fuel ratio's departure from the ideal stoichiometric value is the discrepancy between the actual and desired fuel mass flow rates. A self-converging and reliable Smooth Super-Twisting Algorithm-based controller is therefore suggested. The air-to-fuel ratio of Spark Ignition (SI) has been managed using Mean Value Engine Model (MVEM). The proposed controller's performance has been examined by varying the fuel delivery subsystem's characteristics. The results of the simulation demonstrated that the chattering effect has been significantly diminished during keeping model error robustness [3].

To lower the nitrogen oxides and solid particles in the exhaust of marine diesel engines, the overall design concept of the exhaust intelligent emission reduction control system was accomplished. The hardware structure design and model selection of the marine diesel engine exhaust intelligent emission control system are finished in accordance with Tier III emission regulations and marine diesel engine exhaust. In this study, the related model prediction method is built to make sure that the emission of the control system matches the demands of nitrogen oxide conversion rate and ammonia gas escape quantity simultaneously. The control system created in this study successfully meets the emission criteria of Tier III standards, as demonstrated by the analysis of experimental findings. The information presented in this study is used in the shipping industry to meet Tier III standards' requirements and get ready for stricter emission rules [4].

The study's findings on a turbocharged engine with an EGR (exhaust gas recirculation) system are presented in the report. The results show that high gaseous fuel energy shares are used during yet maintaining high engine overall efficiency and noticeably lowering particulate matter emissions. Additionally, it was discovered that adding an exhaust gas recirculation system cause a noticeable reduction in NOx emissions [5].

OBD (On Board Diagnostics), one of the key tools used for pollution management in modern cars, is covered. During a system or component is out of compliance, OBD generates fault codes. Commercially available tools retrieves problem codes from the OBD, but they only give engineers a small amount of basic data. These tools are of the "black box" variety and offer very little customization. Additionally, these diagnostic instruments have extremely little data storage space. This article provides information on a new OBD scanning tool that was built in-house. It is versatile, time-consuming, cost-effective, and has a big storage capacity, giving engineers total access. [8].

Engine management systems are introduced to achieve high performance, low fuel consumption, and low exhaust emissions. It is an embedded mixed-signal system that communicates with the engine using a variety of sensors and actuators. Additionally, it has an algorithm for controlling the engine's air-to-fuel ratio, ignition, electronic throttle, idle speed, etc. Superior output results from the control system in EMS being designed and implemented effectively. Because the functions involved in an engine control system are so complicated, designing one is a highly difficult process. The key advancements in SI engine control system techniques are summarised in this study, along with assessments of some of the fundamental engine management system control modules [9].

In order to manage combustion, this research introduces a possibly affordable oxygen sensor. The reexamined Nernst equation is the foundation of the operating theory. The sensor features a heater to activate the chemistry within the solid electrolyte that is made of yttrium doped zirconia. Contrary to the well-known oxygen lambda sensor, the apparatus functions as a wide band sensor and does not require a reference gas to function [10].

For increased engine efficiency, the vehicle industry makes considerable use of electronic components. In internal combustion engines, the engine control unit accurately manages the spark advance and injection timing to enhance driving comfort and hence cut fuel consumption. This study examines the architecture of duties for a single-cylinder engine to create an automotive engine control unit. High-level abstract flowcharts for the algorithms are suggested. The findings are used to the firmware construction of an electronic control unit, and experimental findings are also provided to support the theoretical framework by employing a microcontroller. The primary duties of the engine control unit are to guarantee proper fuel injection and ignition of the mixture in the cylinder at the appropriate crank angle. Additionally, the piston position must be synced with the engine control unit. The methodology is further altered to account for additional sensors and various cylinders [11].

In a diesel hybrid electric vehicle (HEV) offer a system for reducing the nitrogen oxides (NOx) emissions that regulates the dynamics of the engine by employing the electric motor to maintain the wheel torque demand. The tactic is paired with a static EMS and put into practise on a platform that uses software-in-the-loop and has a comprehensive engine model with NOx forecast capabilities. With only a small increase in fuel consumption, this model-based approach to transient engine torque limitation enables a large reduction in NOx. The operating ranges for diesel engines where efficiency is at its highest and NOx emissions are at their lowest are typically not the same. Keeping the trade-off between fuel use and NOx emissions to a minimum prevents NOx emissions from rising. An estimation of the transient component is also

included for engine driving cycles, along with a brief analysis of the transient NOx emissions issue [13].

A superior after-treatment system was created to meet the forthcoming emission standards. After-treatment systems are more expensive and take up more room. In order to reduce emissions, in-cylinder methods are chosen. To meet the upcoming emission standards, numerous in-cylinder solutions in conjunction with emission gas recirculation systems have been developed. Modern combustion techniques could aid with engine performance and exhaust pollution reduction. The performance and emission characteristics of diesel engines are thoroughly reviewed in this work. The effectiveness of in-cylinder and after-treatment solutions to lower emissions in CI engines has been examined [14].

The fuel efficiency enhancement makes IC engines use less gasoline that is a potential upgrade that lowers exhaust emissions. An extensive mathematical engine model is presented, and a parametric analysis is done to determine the impact of various parameters on efficiency. The fundamental and basic factors are the geometrical dimensions of the engine bore and stroke. Significant changes in efficiency is made by changing their values. In addition to increasing thermal efficiency, compression ratio is another factor that enhances brake power. The created method aids in efficiency optimization analysis judgments and decreases the cost and testing time for engines.

The design and implementation of a flexible automated Hardware-in-the-Loop (HIL) test environment that makes it easier to create control algorithms and calibrate and verify cutting-edge sensors and ECUs is discussed. Along with comfort and environmental issues, safety is of utmost importance in automobiles. As a result, electronic control units (ECU) and different sensors are becoming increasingly complicated. Thus, creating innovative control algorithms and economical verification methods becomes a crucial concern. The environment simulates the dynamic behaviour of the cars that shortens the time needed for development and testing and does away with the need to use pricey real vehicles for those purposes.

There are some existing verification and test systems that are used for unique t A model that captures the cycle-to-cycle transient behaviour of in-cylinder state variables is presented. Due to the cycle-to-cycle coupling brought on by the imbalance of cyclic combustion, regulating the cycle-to-cycle transient characteristics of the mass of air, fuel, and burned gas is a crucial challenge in 4-stroke combustion engines. To describe the transient behaviour of engine phenomena on a cycle basis, a physical model has been constructed. The engine performance, including the air fuel ratio, torque generation, and other factors, are impacted by

this cyclical change. As the amount of leftover gas in the engine cylinders grows, engine performance declines. However, it reduces the emission as NOx levels in the cylinder drop as the temperature inside the cylinder drops like the creation or verification of a particular sensor and ECU [16]. In this work, a system is treated as a time-varying linear system with total fuel mass, residual unburned air, and burnt gas mass as the state variables. [17].

Different suppliers create vehicle management systems with the use of electronics to suit incredibly complex needs. Engine Management System emerging technologies demand a number of ways to shorten the overall time for verification with high quality testing. It takes time to analyse and decode data, especially for extremely complex and essential systems. Data for a single complex output signal are first analysed and decoded. Second, a detailed explanation of the analysis and decoding of all engine synchronous or task synchronous complicated output signals with many dependencies is provided [18].

1.4 Motivation

The ever-increasing transportation of people and things across numerous locations has a significant impact on economic progress. India, the world's second most populous country, has a diverse economy, with transportation being a key component. According to statistics, the number of automobiles in our nation has increased by more than 240 percent in the last decade. This is predicted to continue increasing at a similar rate over the next 20 years. This high car rate has negative consequences. These include severe environmental risks such as climate change, pollution, global warming, poorer agricultural yields, and threats to living creatures as a result of increased dependency on fossil fuels and increased pollution emissions, it finally results in total ecological imbalance.

Major automotive emissions from internal combustion engines include traditional pollutants such as carbon monoxide (CO), nitrogen oxides (NOx), particulate matter (PM), and hydrocarbons (HC), as well as greenhouse gases such as carbon dioxide (CO_2), methane (CH4), and others. The implementation of Bharat V/VI standards across the country reduce automotive emissions by 86 percent. It is very advised to create engine control systems in order to attain high performance and minimal exhaust emissions.

To fulfil the impending pollution standards, existing engine technology must be modified, and a better system developed. Exhaust temperature management is the most effective approach to control emissions. The temperature in the exhaust system has a significant impact on emissions since exhaust gas treatment equipment like as catalysts, oxygen sensors, and storage

catalysts operate only within a narrow temperature range. Thus, by efficiently managing the exhaust system temperature, emissions are going to reduced to a specific level.

1.5 Problem Definition

To design and simulate a set of controllers that provides diagnostics to fulfil the emission standards set up by the government of India .i.e, to reduce the emission out of the exhaust system. To develop an effective system with careful modifications on the base controller functionality. The modifications mainly focus on the key intermediate emission control parameters that are spark ignition timing, inlet valve opening, outlet valve opening, exhaust gas recirculation, engine efficiency, air charge control actors, air to fuel ratio i.e., lambda value to achieve efficient control of emissions coming out of exhaust tailpipe in gasoline based engine exhaust system.

1.6 Objectives

The project's primary goals are to:

- Design a system that decreases exhaust emission by adding a feature to an already-functioning component to improve component protection through exhaust temperature management.
- To use ASCET software to simulate the designed system.
- To test the system's improved functioning using TPT software.

1.7 Organization of Report

The project work is organized in seven chapters

Chapter-1 comprises of a study of the literature done to comprehend the problems with multiple output forward converters and their fixes. It covers the problem definition, the project's goals, the reason for the project's execution, and the approach.

Chapter-2 This chapter describes the general layout of the gasoline exhaust system. This chapter provides a thorough understanding of the exhaust system, particulate filters, catalytic converter, engine ECU, gasoline engines, and their diagnostics.

Chapter-3 consists of the suggested block diagram along with a methodology and working explanation.

Chapter-4 provides a description of the simulation tools' software.

Chapter-5 covers component protection and catalyst heating.

Chapter-6 explains the findings of the simulation analysis, results and discussion.

Chapter-7. provides the general finding from the study, as well as an outlook for the future.

References includes the list of references referred in the successful completion of the project.

CHAPTER 2

GASOLINE EXHAUST SYSTEM

The basics of exhaust system are discussed in this chapter. The basics of engine control unit are also discussed.

2.1 Exhaust System

The exhaust system was initially created as a straightforward duct system with the goal of safely transferring the harmful exhaust gases from our car into the environment during also attenuating the noise produced by the engine during combustion. The responsibility of the exhaust system has increased over time. Modern exhaust systems are a crucial component of pollution and combustion control, that reduces noise, limits harmful emissions, and even helps to improve fuel efficiency, power, and subsequently the overall drivability.

The main parts of the exhaust system cooperate to remove emissions, lessen noise, and promote smoother operation of the moving parts. The emission control systems differs depending on the manufacturers and the cars, but they are always created to achieve the same objective and operate according to the same general principles.

The following are the main factors in the design of an exhaust system:

- To achieve maximum efficiency, reduce gas flow resistance to a defined range based on the engine model.
- Reducing exhaust noise to adhere to car norms and standards.
- Leaving enough space between engine parts and the components of the exhaust system to reduce the effects of a high exhaust temperature.
- Making sure the system does not place an excessive amount of weight on engine components, since this could limit the component life.
- Ensuring that the exhaust system's parts effectively reject heat energy.

Figure 2.1 shows Exhaust system of a passenger car. The exhaust system consists of the following: After-treatment tools to reduce the pollutants released, like particulate filters and catalytic converters.

- Mufflers to reduce noise.
- The decoupling components that link the exhaust system to the manifold.
- Hangers and piping.

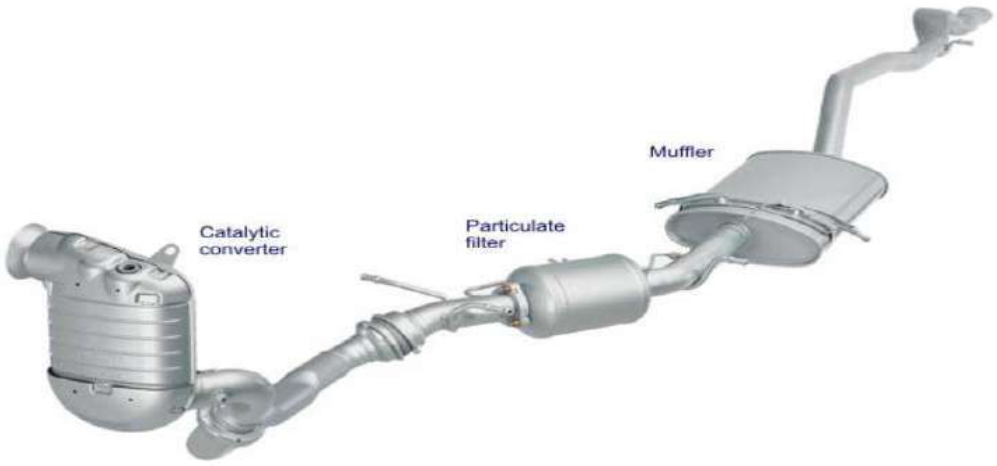

Figure 2.1: Exhaust System of a Passenger Car.

The "hot end" of the exhaust system is the after-treatment equipment and its piping, during the "cold end" is made up of the muffler and tailpipes. The "down pipe" or "front pipe" that joins the exhaust manifold with the catalytic converter, as well as the pipework between the catalyst and the particle filter, are included in the hot end pipe. The "middle pipe" joins the muffler and the after-treatment system. The components of the exhaust system are exposed to high temperatures that influences the material choice for the exhaust system along with other elements like the need for strength and chemical exposure.

The main part of the exhaust system that collects all the exhaust gases from the combustion chamber to the exhaust pipe is the exhaust manifold that is sometimes mistaken for an element of the engine. The torque and performance characteristics of the engine are greatly impacted by the exhaust manifold design. The flexible joint follows, that lowers engine movement transmission to the exhaust system. It typically sits between the catalytic converter and manifold. As a result, it must tolerate high temperatures and be robust and lasting.

The catalytic converter that is positioned in the exhaust line between the manifold and muffler, is another crucial part of the exhaust system. It makes use of catalyst-acting compounds. Prior to exiting the exhaust system, a catalytic converter causes a chemical interaction between the pollutants in the exhaust, without causing any damage to the pollutants themselves.

During functioning, internal combustion engines typically produce a lot of noise. The mufflers that are used to achieve this noise reduction are expertly made. Mufflers use the idea of reactive silencing, a wave cancellation technology application, to tune out specific frequencies that are unpleasant to our ears. A given range of frequencies are tuned by selecting

the proper design parameters. Since a muffler alone cannot minimize engine noise, the exhaust system also includes supplementary components like resonators. A typical resonator is a muffler-mounted hollow steel tube with a cylindrical shape. Together, they both help to reduce exhaust noise. The tail pipe that is the final component, is intended to provide an enclosed pathway for the exhaust.

Major technologies are used to minimize emissions as a result of more strict emission reduction initiatives. One of them is an oxidation catalyst that cuts CO and HC emissions by more than 90% and harmful HC emissions by more than 70%. Figure 2.2 illustrates the poisonous by-products produced by the oxidation catalyst as a result of the IC engine's inability to produce enough oxygen to oxidize the carbon fuel into carbon dioxide and water. The redox conversion of toxic fuel byproducts into less dangerous compounds occurs in catalytic converters. It is made up of a steel housing, a ceramic or monolith honeycomb interior, and a metallic substrate. Platinum (Pt), palladium, and other metals are combined to form the honeycomb structure that maximizes the surface area for more reaction to occur (Pd) and rhodium (Rh).

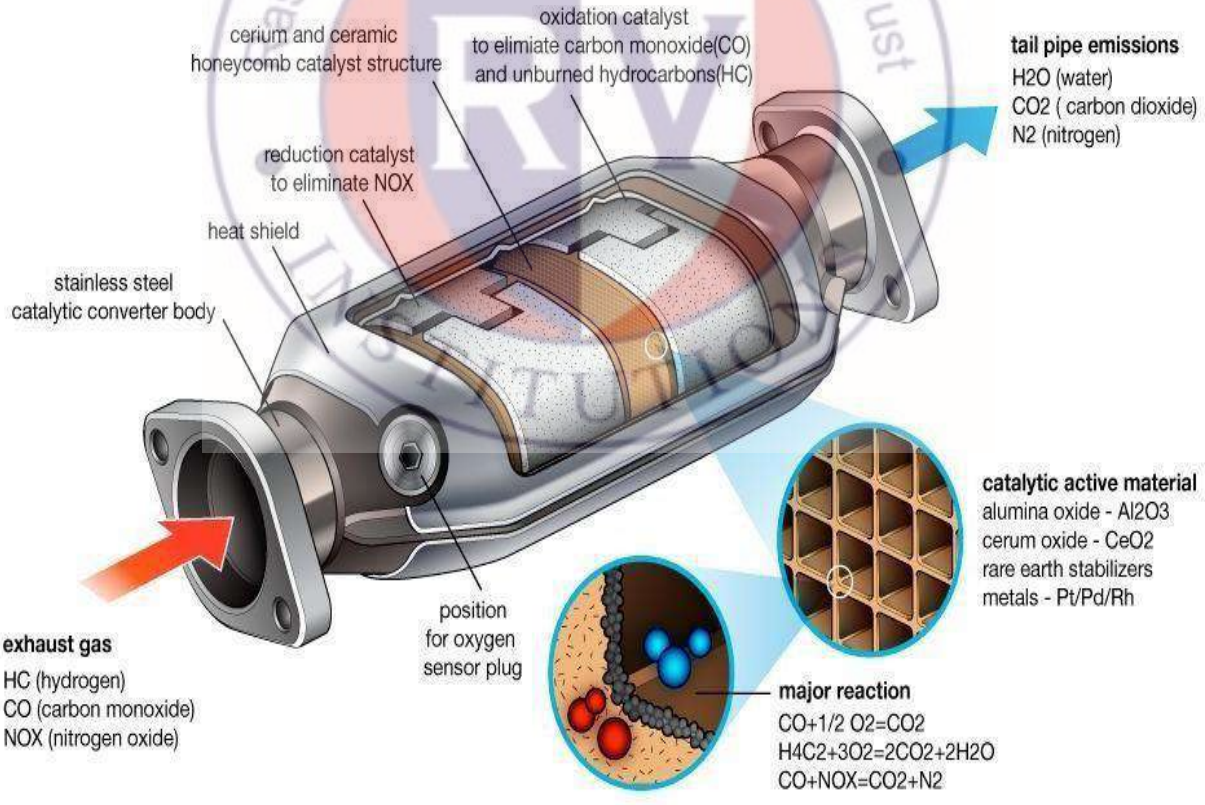

Figure. 2.2. Oxidation Catalyst

The catalyst initially starts a reduction reaction to reduce nitrous oxide. The nitrogen atom in nitrous oxide is eliminated as it passes through the Pt and Rh catalyst, allowing free

oxygen to produce oxygen gas O2. The nitrogen atom then interacts with other nitrogen atoms linked to the catalyst to produce nitrogen gas N2.

In the second stage, an oxidative catalyst made of Pt and Pd is used to regulate carbon monoxide (CO) and unburned hydrocarbons (HC). Carbon dioxide (CO_2) is created during carbon monoxide (CO) combines with oxygen in the air, and water is produced during hydrocarbons are oxidized (H2O).

Reliable and effective at cutting emissions from gasoline engines are catalytic converters. During catalytic converters are coupled with diesel engines that operate more coolly than gasoline engines, they are less effective. Higher temperatures are ideal for catalytic converter operation. Particles like soot also be produced by diesel engines in near future. Thus, combining a particulate filter and a catalyst cuts down on ultra-fine particle emissions by up to 99 percent.

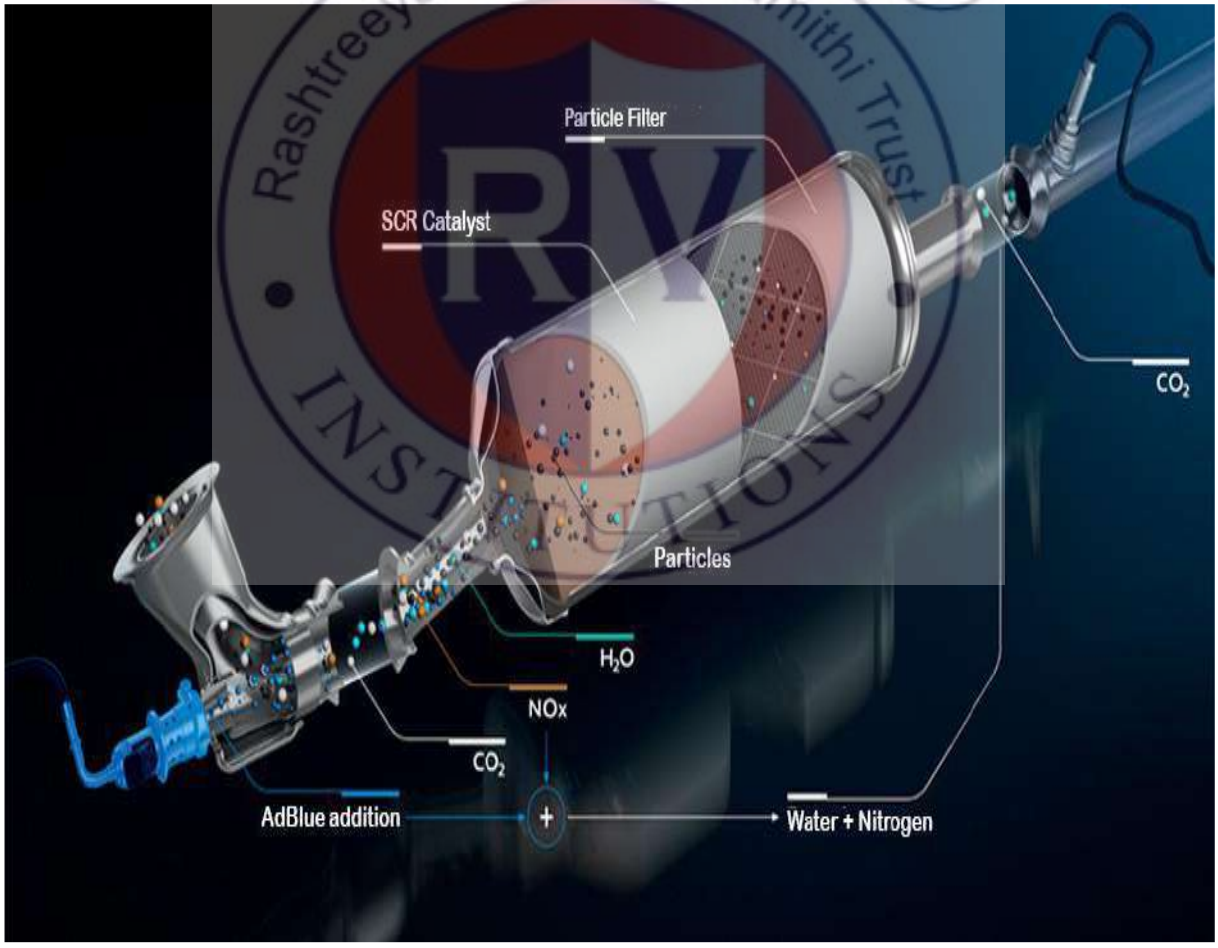

Figure. 2.3. Particulate Filter

Particulate filters that are placed to comply with particulate emission restrictions (PM). Pictured in Figure 2.3 is a particle filter. Particulate filters eliminate particles smaller than 100 nm that are made up of carbon, ash, and unburned hydrocarbons. Since the filter's capacity is

limited, the trapped soot increases the flow resistance, necessitating the need to empty or burn off the soot in order to regenerate the specific filters.

The extra soot particles that gathered in the filter after about 800 to 2000 kilometres of driving are thoroughly burned during the regeneration process. At temperatures above 600°C, the deposited soot is then burned off together with the exhaust fumes. Since this temperature is typically not attained during routine driving, the exhaust temperature is raised through post-injection, delayed main injection, and throttle valve air mass reduction.

The exhaust outlet valve's temperature then rises as a result. The temperature is also raised by the exothermic reaction of unburned hydrocarbons in the oxidation catalytic converter. The particle filter is often placed close to the exhaust manifold and frequently used in conjunction with an oxidation catalyst in order to prevent significant heat loss.

Exhaust gas recirculation (EGR) that reduces the oxygen concentration in the combustion chamber and absorbs heat to effectively decrease NOx emissions. The schematic representation of the EGR system is shown in Figure 2.4. By using the inlet system, it is a technique for returning some of the exhaust gas to the combustion chamber. By providing inert gases to the combustion process and limiting the amount of oxygen present in the incoming air stream, this lowers the peak in-cylinder temperatures. During air oxygen and nitrogen are combined at high temperatures in the combustion chamber that typically happens at peak cylinder temperature, NOx is formed.

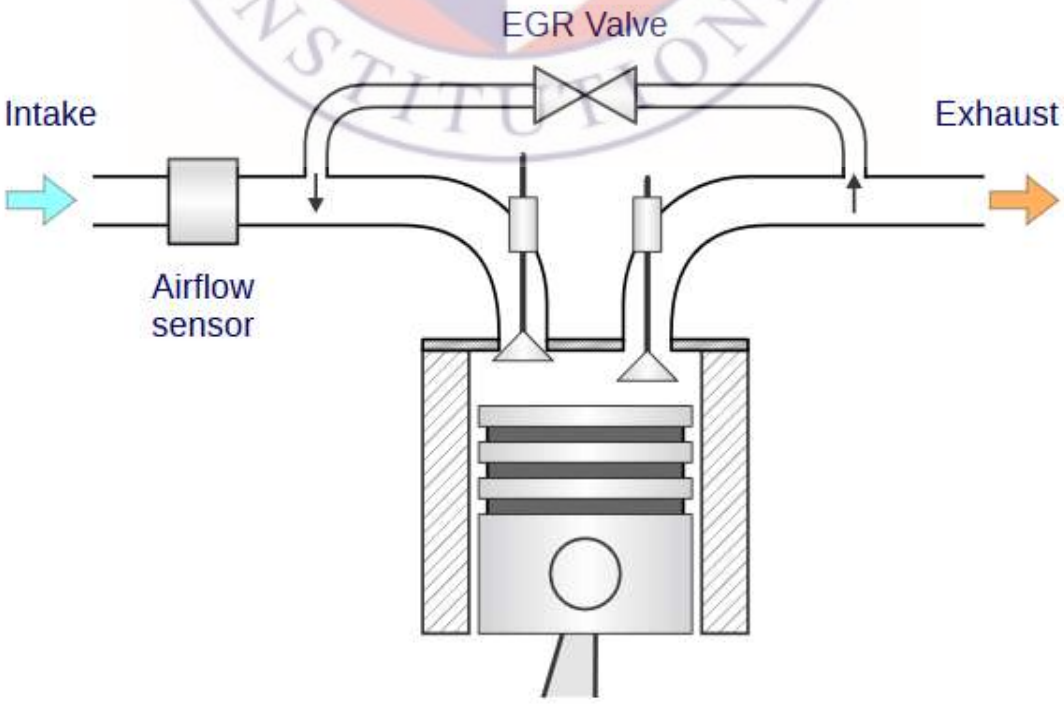

Figure. 2.4. Schematic Representation of EGR System

The composition of the gas injected into the cylinder during the engine cycle is changing as a result of the mixing of exhaust gas with the intake air. Significantly less oxygen is present, and more CO_2 and water from burning are produced. The drop in the peak temperature of the diesel combustion flame is the main factor causing the exhaust gas recirculation's NO_x reduction impact. As exhaust gas is combined with oxygen, fuel, and combustion byproducts, the cylinder's specific heat capacity increases and the adiabatic flame temperature decreases. Engine efficiency is raised by an emission gas recirculation that is working effectively.

An essential component of combustion and emission control systems, automotive exhaust systems are made to do one or more of the following: remove solids from exhaust gas, reduce exhaust noise, put out sparks, or provide power for a turbine-driven supercharger. Thus, it is essential for fuel consumption, safety, and the environment that our exhaust system remain in excellent functioning order. The exhaust's resilience is essential [23].

2.2 Engine ECU

Up until the advent of electronics in the auto industry, cars are thought of as mechanical machines. Every single part of a vehicle, including the engine, windows, brakes, and steering, was mechanically driven on gears using the mechanics concept. However, the inherent limitations and poor accuracy of these mechanical systems led to undiscovered failures and a high risk of harm to the users. These restrictions made it possible for the car industry to innovate more effectively. This finally resulted in the use of electronics in vehicles.

Since its introduction to the automotive industry in 1970, automotive electronic control units (ECUs) have grown to be a significant part. It has been crucial to the evolution of the automobile from a wholly mechanical to an electronic-dominant machine. In order to govern and regulate the functionality, modern cars feature around one hundred embedded or fitted ECUs.

Engine ECU is depicted in Figure.2.5. The ECU is a computer that uses microprocessors and sensor data that are processed to conduct real-time control of a number of actuators. It has internal pre-programmed and programmable chips. For the gearbox, traction control or ABS, body functions, lighting control, AC, engine, air bags, and other sections of the car, there are numerous distinct ECUs. The power train, body control, and chassis system are the three primary units that an automotive ECU is utilised for.

Figure. 2.5. Engine ECU

The ECU is a component of the Power-train Control Module (PCM), is in charge of controlling the combustion process, including opening and closing the inlet or outlet valve in response to input from the accelerator pedal. The ECU regulates the timing of the fuel injection rate and spark ignition. Thus, compared to vehicles with mechanical controls, ECUs produce accurate synchronization and increase power, efficiency, and functionality. The use of sensors has a significant impact on an ECU functioning. The use of sensors has a significant impact on an ECU functioning. Instead of transmitting numerous wires from the sensor to various ECUs for control operations, the ECU shares information with other ECUs using communication network lines. Most vehicles have an ECU that is attached to an OBD (on board diagnostics) connector, and it communicates all diagnostic data to all other ECU modules over this line.

Original equipment manufacturers are in charge of putting emission controls in cars since government regulatory agencies have placed severe limits on the emission levels from vehicles. Without the aid of ECUs and software algorithms, implementing such constraints have been an impossible task. The regulatory agencies reacts to emergency circumstances more effectively thanks to automation. Along with the development of mobile phones, automakers gradually changed the way cars looked by adding web connectivity, smart devices, and navigational controls.

Astonishing amounts of data are processed by an ECU. To obtain maximum performance, a number of operations must be carried out simultaneously. With the aid of sensors, the ECU enables the processing of all the data that the engine receives. The automakers configures the ECU in such a way that some car models have very smooth rides during others

have a more racing-inspired feel. ECU thus enables us to have these two unique traits in a single car. ECUs are periodically reprogrammed to accommodate greater and better performance. Thus, ECU provide a type of performance that makes driving more enjoyable than difficult.

2.3 Gasoline Engines and their Diagnostics

Diesel and gasoline engines are conceptually pretty similar. They are IC engines made to transform fuel's chemical energy into mechanical energy. This mechanical energy is then used to move the pistons up and down inside the cylinders forming a linear motion. The crankshaft that is coupled to the pistons, generates the rotary motion required to turn the wheel forward. Both diesel and gasoline engines use a sequence of explosions or combustions to transform fuel into mechanical energy.

However, the way these explosions take place makes a significant impact. During gasoline is using, air is combined with the fuel before being compressed by pistons and ignited by sparks from spark plugs. In a diesel engine, the fuel is injected after the air has been compressed. Compression warms the air that causes the fuel to ignite. The following are steps in an explosion happening in a gasoline engine:

• Intake stroke: Here, gasoline and air are combined.

• Compression stroke: As the piston rises, the fuel-air combination is compressed.

• Ignition stroke: A spark plug ignites an air-fuel mixture.

• Exhaust stroke: During this motion, the piston rises and forces the exhaust through the exhaust valve.

This strokes are shown in Figure 2.6.

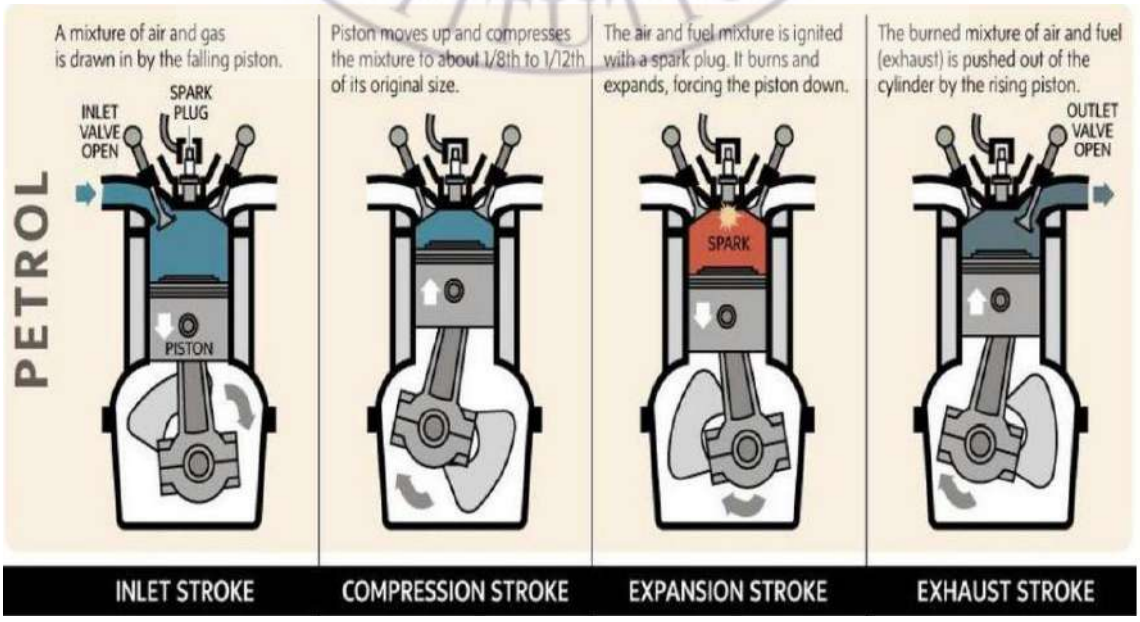

Figure. 2.6. Gasoline and Diesel Engine

For the purpose of controlling the temperature of exhaust gases, many functional components are needed. These include functionality for initialising and turning on the exhaust gas temperature controller as well as functionality for open loop, outer loop, and inner loop calculations. The various functional components send the coordinating function their requests, and the coordinating function activates the various execution functions, then communicate their results to the appropriate functionalities via the catalytic heating activation bits.There are specific capabilities that manage catalyst heating under the catalyst heating. Controllers for engine efficiency degradation, catalyst heating owing to cold starts or catalyst warming up, and desirable lambda coordination are among them. These functions all rely on specific catalyst heating techniques. They are: exhaust camshaft modification, lambda split, multiple injection, torque reserve, and increased idle speed for catalyst heating.

2.4 Summary

In this chapter the basics of exhaust system are analysed. The components of exhaust system are explained. Also its engine control unit is discussed in brief.

CHAPTER 3

METHODOLOGY AND BLOCK DIAGRAM

The chapter includes the brief explanation of methodology of the employed in the proposed work. The chapter also briefly explains process flow for the simulation and contains the description of block diagram of the project.

3.1 Methodology

The methodology involved in developing the work is as shown in Figure 3.1

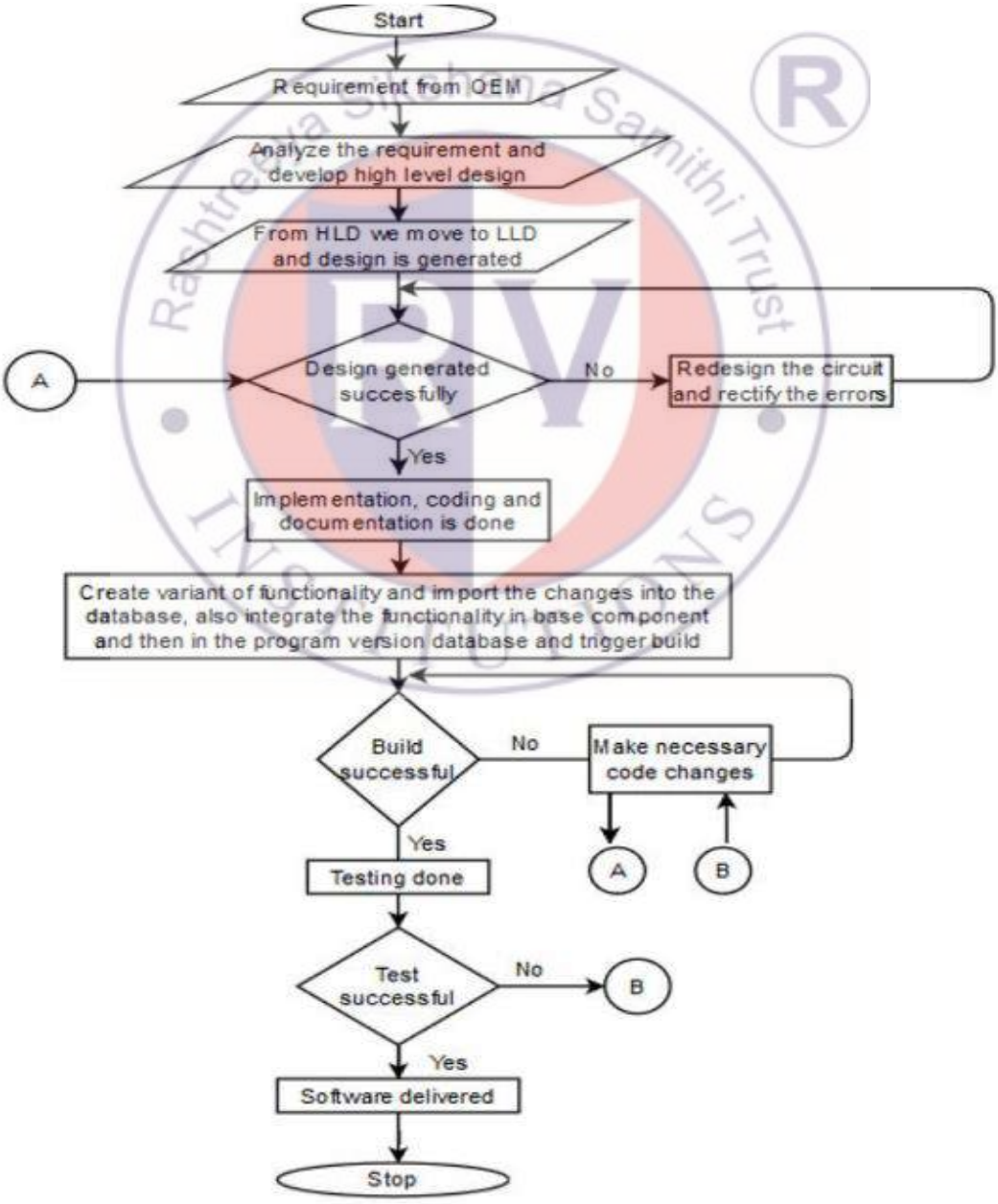

Figure 3.1: Methodology Involved in Proposed Work

A flow diagram is used to explain the overall stages involved in the creation of a functional component. Each functional part of the exhaust management package working is necessary. Whether these packages are created and provided for integration is ensured. At first, a request is got from the OEM for the modification or creation of a useful component. The function developer performs the necessary analysis based on this request, and then construct the feature using specific development tools. The ASCET tool is used in this instance for the simulation. It is a tool that has the ability to automatically document and generate code. Standards set by the automotive sector should be met by this code. Therefore, software warnings need to be checked. Before integration, these warnings must to be eliminated from the functional components. During the feature is prepared, incorporate it into the base PVER and accompanying BC that the customer has provided.

To guarantee that the functionality is provided. The required functions must be rebuilt or altered for the build to succeed if it fails at any point. After the build is finished, the software is tested depending on the changes using testing tools like TPT or LABCAR. If the outcome differs in any way from what was anticipated, restructure the procedure once more and carry it out until the desired outcome is achieved. Following testing, the database is updated to reflect the FC state, and the BC is sent to the requested client for integration into the relevant PVER.

3.2 Block Diagram

Figure.3.2 shows the block diagram of the thermal management scheme.

- **Controller to set the mode of catalyst heating:** The thermal management for catalyst heating is used to warm up a cold exhaust gas system by delivering the signal to additional functionalities to maintain the system's temperature, to desulfurize the NOx storage catalyst, or to start a quick trip at the end of the manufacturing line.
- **Controller to set desired idle speed** : It is used to establish a higher-than-normal idle speed to boost mass flow during the engine is running. As a result, during the engine is idling, the exhaust heats up significantly more quickly. Both hybrid and non-hybrid start-stop systems employ it. It configures the signal to disable the system's stop feature. This is required because, in a cold start heating request, there isn't enough mass flow available during the stop phase to warm up the exhaust system.
- **Controller for worsening of engine efficiency:** It does this by offering a desired delayed ignition angle that delays combustion in the cylinder so that more heat produced is sent into the exhaust system. For diagnostic purposes, the functions also export the

retarded ignition angle. Due to the fact that all cold start heating measures affect emissions, it is necessary to monitor them all, regardless of their effectiveness.

It is especially intended for start-stop projects or hybrid vehicles. For hybrid vehicles, the function requires a torque interval that is greater than the driver's torque requirement. The electrical engine of the hybrid vehicle uses the excess energy produced by the combustion engine to refuel the battery. The exhaust system heats up significantly more quickly due to the combustion engine's additional heat. The exporting priority of the function is applied to the start-stop systems to ensure that the catalyst heating that necessitates the operation of the combustion engine, receives the greatest priority.

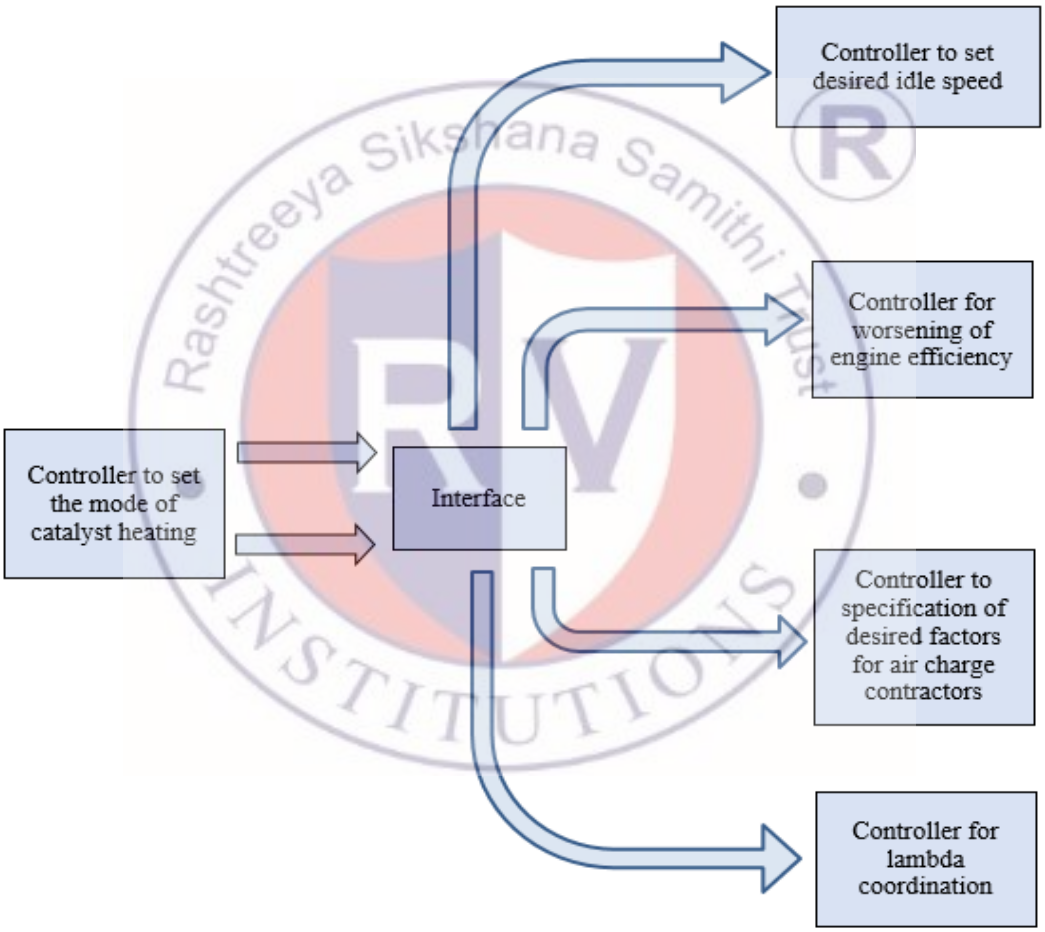

Figure. 3.2 Block Diagram for Proposed Work

- **Controller to specification of desired factors for air charge contractors:** It exports a variety of parameters, including factors for the lambda value, cam shaft intake and outlet valves, and swirl control that are used to gradually enhance or decrease the cold start heating measures.
- **Controller for lambda coordination:** If there is no secondary air pump available, it calculates a desired lean lambda during the catalyst heating, resulting in lower raw

emissions from the engine than with a rich lambda. Because the catalyst is still not converting correctly at the beginning of the cold start heating, it is extremely important to do this to maintain low emissions. The intended lambda is highly rich if a secondary air pump system is provided so that significant amounts of HC remain after combustion to interact with the oxygen from the secondary air pump in the catalyst.

3.3 Summary

The methodology used for thermal management in exhaust system was explained. The block diagram and its working was also discussed.

CHAPTER 4

SOFTWARE DESCRIPTION

This chapter includes the explanation about ASCET software. This chapter also includes the explanation MISRA software. In this chapter also describes various techniques for testing system performance.

4.1 ASCET

Advanced Simulation and Control Engineering Tool is referred to as ASCET. It is a multifaceted and adaptable product family that offers an original approach to the functional and software design of contemporary automotive embedded systems. With a fresh take on modelling, code generation, and simulation, ASCET supports each step of the development process, enabling improved quality, quicker innovation cycles, and lower costs.

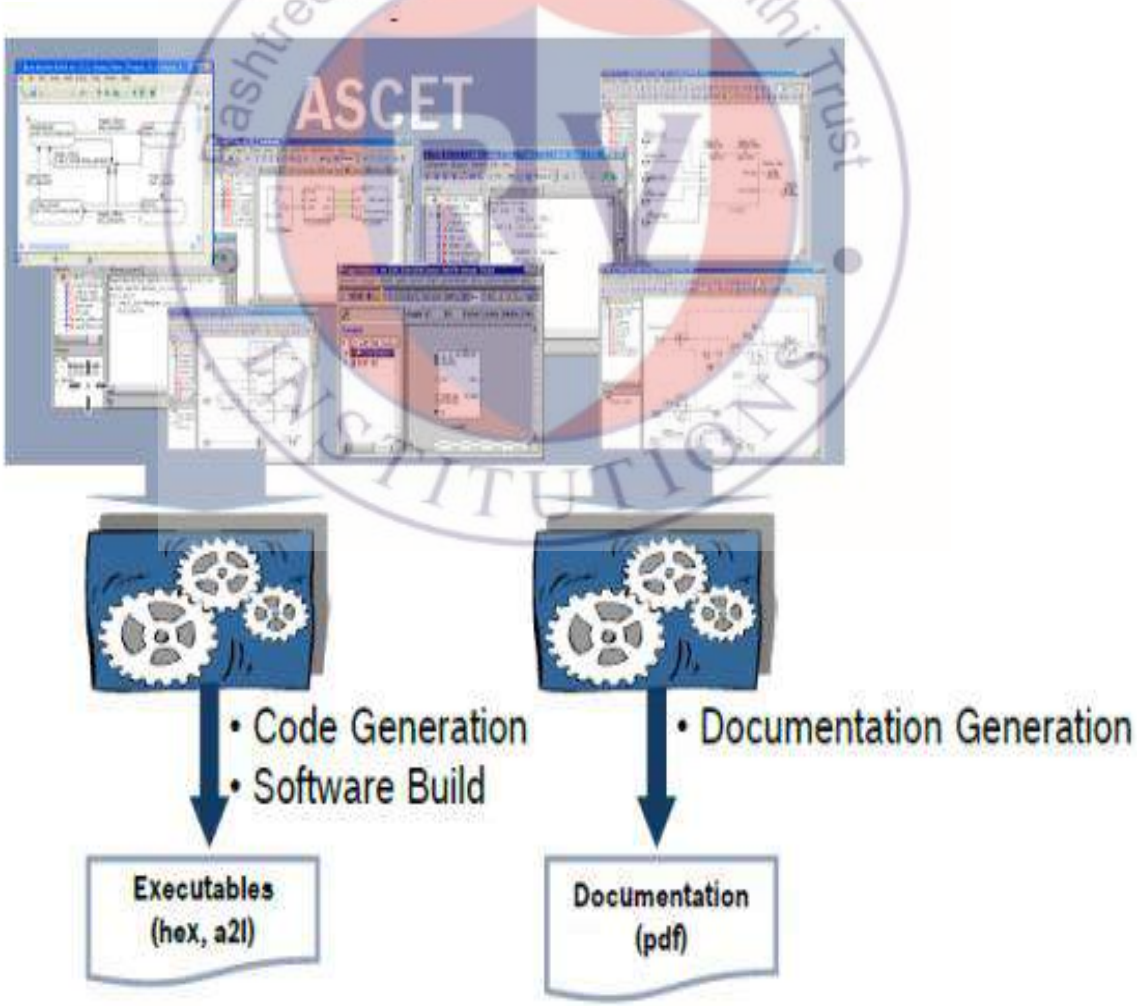

Figure. 4.1. Working of ASCET Tool

A tool for creating software for embedded systems that uses both graphical models and textual programming notations is called ETAS ASCET. The proposed function models are converted into extremely efficient and secure embedded C-Code for AUTOSAR applications by the ASCET Code Generator. The ASCET has been created primarily to handle the difficulties in software development for sectors where goods must be produced in large quantities, at a low cost, in compliance with industry standards, and without any flaws.

The ASCET tool enables software developers to create embedded software that is high performing, low overhead, simple to maintain, secure, and safe. High levels of automation enable productive and safe workplaces.

The ASCET tool for Automotive Software Development has the following features:

- Safe - Automatic introduction of defensive code, TUV-certified code generation using ISO26262 and IEC61508, and MISRA-C:2012 compliance
- Used for powertrain, driver assistance, battery management, brake systems (such ABS, ESP), ASCET-generated code powers the 450+ million ECUs in use today.
- The 450+ million ECUs in use today are powered by ASCET-generated code, that is used for brake systems (such as ABS, ESP), driver assistance, battery management, and powertrain.
- Quick and effective - Real-time static analysis for immediate feedback, quicker code generation
- A variety of testing alternatives, including unit testing, PC-based open-loop simulation, closed-loop simulation, and rapid prototyping
- Embedded Software Development Language (ESDL) that has an abstract data type, easy-to-understand syntax, and object-oriented encapsulation

4.2 MISRA

The Motor Industry Software Reliability Association (MISRA) created a set of software development recommendations for the C programming language specifically for use in safety-critical systems. Its objectives are to make code safety, security, portability, and dependability easier for embedded systems, especially those that are written in ISO C/C90/C99. UK-based MISRA understood that safety is crucial in many aspects of automotive design. They also noted that C was the preferred language for creating such systems. As a result, these systems are susceptible to C's drawbacks. Thus, the company investigated to make C safer. This led to the creation of a set of guidelines known as MISRA-C for the usage of C in automotive-based

software. The recommendations are a 70 page document that outline a usable subset of C that stays clear of many of its well-known issues. They got initially published in 1998.

MISRA C includes 127 regulations in all. Of these, 93 are necessary, and the other 34 are recommendations. It's crucial to understand the differences between these two rules. ProcMan offers the tool functionality for examining and testing MSR-based ECU software development. The ECU.WorX development environment includes ProcMan as part of the package and upon installation. Therefore, ECU.WorX needs to be installed to use ProcMan. Key functionalities of ProcMan include:

- Consistency checks
- Completeness checks
- Order checks
- Read/write analysis
- Scheduling editor

4.3 Testing

Testing is an examination that aims to reveal details regarding a software product's quality. Executing a software system or component is part of testing. Depending on the level of code knowledge, or during the code is known and during it is unknown, there are many forms of testing.

In addition, there are many types of testing based on the complexity of the testing code, including system testing that involves testing multiple functional components, and integrity testing that is done during a new component is added to the system. During a hardware component is incorporated in the testing process, hardware testing is used. During software components are to be tested, software testing is used.

4.4 System Function Testing

System Function Testing (SFT) is a behaviour test of the new and old functions in light of all system function-level requirements. Black Box testing, in that the tester is not aware of the system's internal logic, is a technique used during functional testing.

An extra test for the regression software test technique is the System Function Test. The Unit Reference Test is another component of the regression software testing technique (URT).

The test's goal is to verify that the functional requirements specified at the System Function (SF) level are being implemented correctly.

4.5 Unit Reference Testing

It is typically utilised during a new functional component is created and during a functional component's structural changes comprising elements. As a result of the lower cost of defect repair, it is commonly used. It is code for the single functional component that is being tested in URT is not overly complex, making it simple to debug during a test fails. If the testing is not too complicated, the function developer often handles it. SEDGE and TPT tools are used to test functional components. A stub needs to be implemented that is a piece of code that takes the place of the code from other functionality, during a function depends on other functions. SEDGE is used to put this into practise. For test cases that are implemented from test specifications that relate to functional components, TPT is employing DLL.

PC-based testing, often known as software-in-the-loop, is the testing of software components carried out on a desktop PC without the use of any hardware. As a result of distributed development, fewer test cars, cost- and time-saving desk testing, and model-based software development that necessitates early testing during model design, it becomes more and more crucial.

A programme called ECCo is a component of the PC Based Test Environment (PATE) that pave the way for process tool chain testing on an optional basis. An executable.DLL containing the functionality to be tested is produced by ECCo build. The useful information in the. DLL is scaled at one's desire. It is feasible to develop a. DLL is created from a single functional component, several functional components, a group component, a basic component, or a combination of all of them.

4.6 Time Partition Testing

TPT is a tool for model-based testing that is used for automated embedded system testing, particularly for testing control systems. Applications include:

- PC based testing
- Open and closed loop tests
- Test in vehicle

TPT is certified to do automated tests in vehicles in accordance with ISO 26262 standards. Signal time intervals are used by TPT. The following four test activities are covered by TPT:

- Test case modelling
- Test execution in different environments
- Test result analysis
- Test documentation

Test cases for TPT are built independent of procedure of running. Due to the so-called Virtual Machine concept, the test cases run in nearly any environment. TPT is a comprehensive tool that is used for all testing phases of development, including system testing, regression testing, integration testing, and unit test

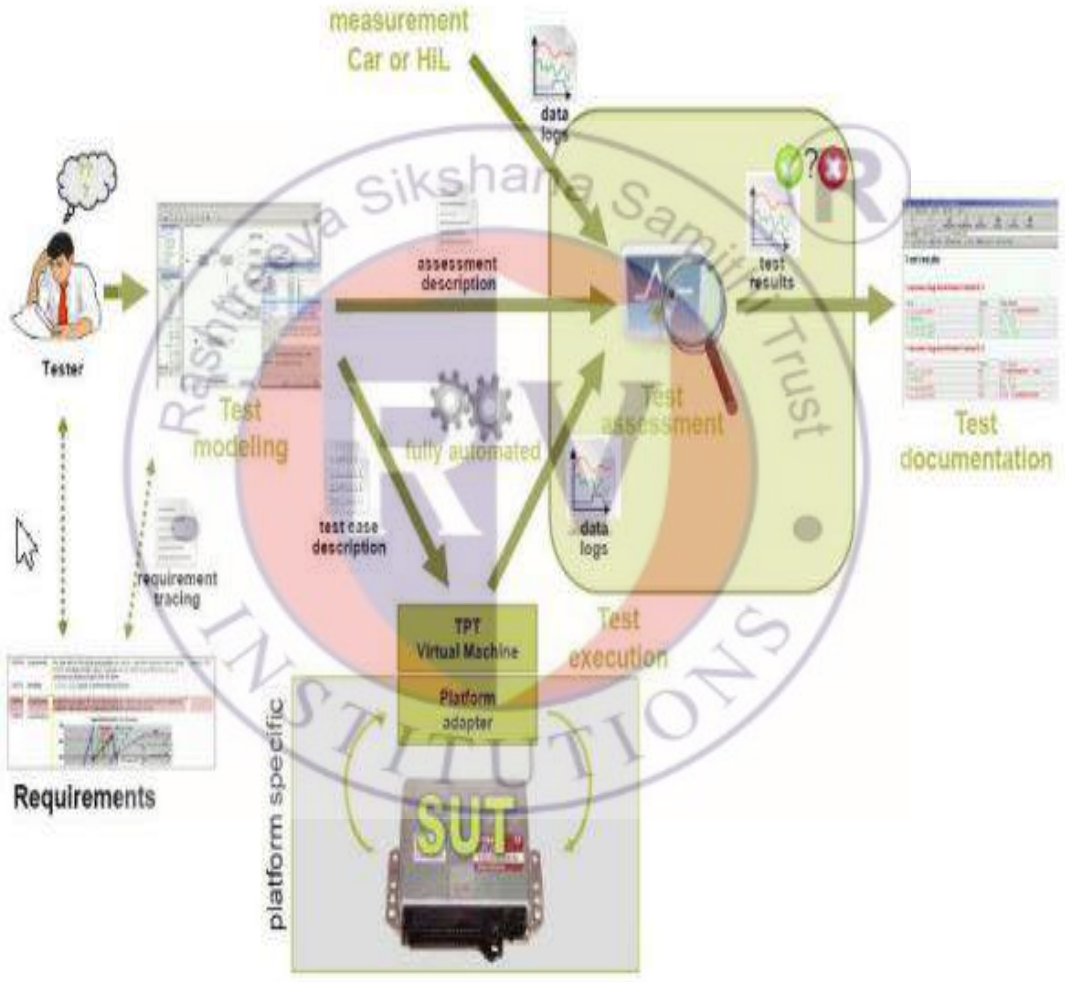

Figure 4.2. TPT Testing Tool

The HTML report used by TPT test documentation to show the tester with the results of the test assessment allows for the representation of test results for each test case other than just pure success or failure information. In addition, it is possible to see details like characteristic parameters or signals that got calculated during the test evaluation or seen during the test execution**.**

4.7 Summary

This chapter explains ASCET software. This chapter explains MISRA software. In this chapter, various techniques for testing system performance are described.

CHAPTER 5

CATALYST HEATING AND COMPONENT PROTECTION

This chapter explains about various strategies that are used in used in designing of thermal management of catalytic converters in order to bring down the exhaust emissions from the gasoline based vehicles.

5.1 Catalyst Heating for Exhaust Management

To comply with the emission regulations, catalytic converters reduce the emissions from IC engines. However, they have issues with light-off during cold starts and engine warm-up that impairs their performance. The issue of light-off and emission concentration is considerably reduced with proper temperature management of the catalyst. This is possible with the right catalyst heating techniques. Methods that depend on controlling engine characteristics are practical because they don't call for additional heating apparatus. The installation of additional equipment that effectively prevents heat loss is one of the other techniques. Materials that hold heat cuts down on fuel use, emission concentration, and catalyst light-off time.

During harmful emissions' temperature reaches a certain point, known as the "light-off temperature," catalyst often converts them. This temperature ranges from 250 to 3000C for TWC. As a result, the toxic pollutants are released into the atmosphere directly at low exhaust temperatures. Because of the inadequate exhaust temperature, the catalyst is not fully functional during the cold-start or warm-up period of the engine. This affects particle filters working. To keep the filter operating at its best, they have regeneration problems. As a result, periodic or continuous renewal is required to remove particles from filters.

In order to lower the emission concentration to acceptable levels, a thorough study on managing exhaust temperature for catalyst heating is conducted. To improve their performance, a variety of catalyst heating functionalities are examined and adjusted in accordance with customer needs and are explained as follows:

5.1.1. Functionality for Initialization of Exhaust Gas Temperature Controller.

The exhaust gas temperature controller function package's initialization is handled by this functionality. It also updates the particle filter's status during turning on the software that

controls exhaust temperature. This FC is where all the initial ECU initialization tasks are carried out.

5.1.2. Functionality for Activation of Exhaust Gas Temperature Controller

This capability regulates the temperature of the exhaust gas emission. Setting the prerequisites for the inner loop, outer loop, and open loop control functions for temperature control is its responsibility. The open loop and closed loop are two separate temperature controllers that are arranged in a cascade. The number of operating modes that are now in use, the mass flow of exhaust gas downstream of the exhaust manifold, the temperature of the catalyst, and other elements are taken into account during activating.

5.1.3. Feedback Control Monitoring Functionality

This FC keeps track of the feedback control for the function that regulates exhaust temperature. It determines whether the inner and outer control loops' reaction times fall within the predetermined range. In the event of a maximum or minimum set value, it also ensures that the set point temperature is set within a certain amount of time. If there is a divergence, it detects it and establish the proper error paths. In order to stop functioning and start substitute reactions, fault identifiers are disabled based on this error path.

5.1.4. Open Loop control Calculation Functionality

In order to control exotherms in the catalyst, a set point fuel amount and temperature for the catalyst are computed based on the inlet temperature. Additionally, based on the mass flow of the exhaust gas, the functionality determines the maximum dosage amount.

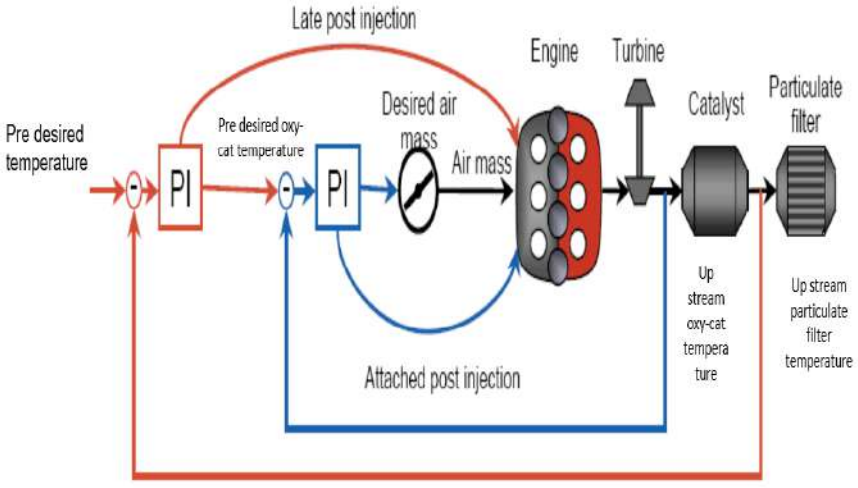

Figure. 5.1. Exhaust Temperature Management System

The local distribution of the set point temperature in the catalyst is described by breaking down the temperature calculations into multiple parts. The individual temperature computations are based on balancing a number of heat flows and thermal capabilities. It is shown in Figure 5.1. Considerations include the amount of heat in the exhaust gas, the heat storage capability, the ability of the catalyst to convert fuel, the heat exchange with the environment, and the necessary exothermic increase in energy through chemical reactions within the catalysts.

5.1.5. Inner Loop Control Calculation Functionality

Using post injection and a change in the air mass set point value, this FC regulates the desired upstream temperatures of the oxidation catalyst and the turbocharger in an inner control loop.

5.1.6. Outer Loop Control Calculation Functionality

Using the inner loop control's set point correction and the delayed post injection, the outer loop controller regulates the required upstream temperature of the particle filter. With the aid of the PI governor, it carries out the deviation correction and determines the output values for post injection. For proper operation, the temperature controller functionality and the catalyst heating control functionality must work together.

The NOx storage catalyst is desulfurized, the exhaust system is kept warm, a brief trip is initiated at the end of the production line, and the cold exhaust gas system is heated using the catalyst heating functionality.

The several FCs send the coordinating function their requests, and the coordinating function activates the various execution functions. The execution functions then communicate their output to the respective functionality via the bits for catalytic heating activation.

There are specific capabilities that manage catalyst heating under the catalyst heating. They exist as described.

5.1.7. Catalyst Heating Due to Cold Start

During the engine is started with the catalyst temperature too low to reach the light-off temperature, this functionality asks for catalyst heating. Catalyst heating is accelerated as much as possible by the FC. The catalyst heating is computed during the start phase in dependency on the engine temperature, intake air temperature, shut off time, and altitude because the measured catalyst temperature is unavailable and the modelled temperature is erroneous.

The ambient temperature, intake air temperature, and engine start temperature are approximately equal during the engine is first chilly. During the cold start heating request is set, the catalyst's light-off temperature is then gradually attained based on the catalyst ageing factor. In the meantime, a ratio between the required value for integrated air mass and the integrated air mass quality at engine start is determined. The catalyst heating is started once this ratio exceeds a predetermined threshold, failing that the catalyst heating for cold start scenarios is stopped.

5.1.8. Catalyst Heating Due to Catalyst Warming

In order to heat up the catalyst during long coasting phases, GPF regeneration requests, and during dew point end is not reached, catalyst heating is necessary. Figure 5.2 illustrates the algorithm for the controller's operation for catalyst heating owing to cold start and catalyst warming.

Long coasting conditions could be challenging for a vehicle to handle. Therefore, using an engine dyno that replicates a very long coasting phase, is advised. Here, it must be checked to make sure there are no defects caused by engine temperature. The catalyst is warmed as soon as the catalyst heating request is set to true and all necessary operating parameters are satisfied. Time should be provided to the car in the event that the dew point is high enough to soak, as a cold start is necessary and there shouldn't be any engine temperature or air pressure-related issues.

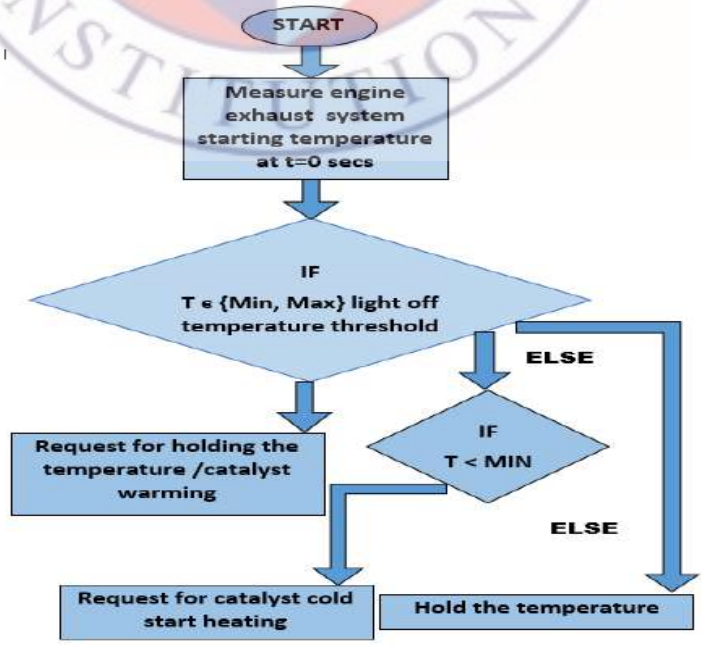

Figure 5.2. Algorithm for Operation of Controller for Catalyst Heating due to Cold Start and Catalyst Heating

5.1.9. Required Worsening of Engine Efficiency for Catalyst Heating

The catalyst heating by a cold start, the catalyst warm-up, the regeneration request, or the request for an optional secondary air diagnosis all lead to an engine's efficiency degrading. Selecting a late spark timing is a useful strategy for improving engine efficiency. The conversion of the optimal moment that is pre-controlled in the motronic over the air route, also requires a larger air mass. For the torque reserve, the spark needs to be removed later. Figure 5.3 depicts the algorithm for the controller's work flow for the worsening of engine efficiency and ignition retardation.

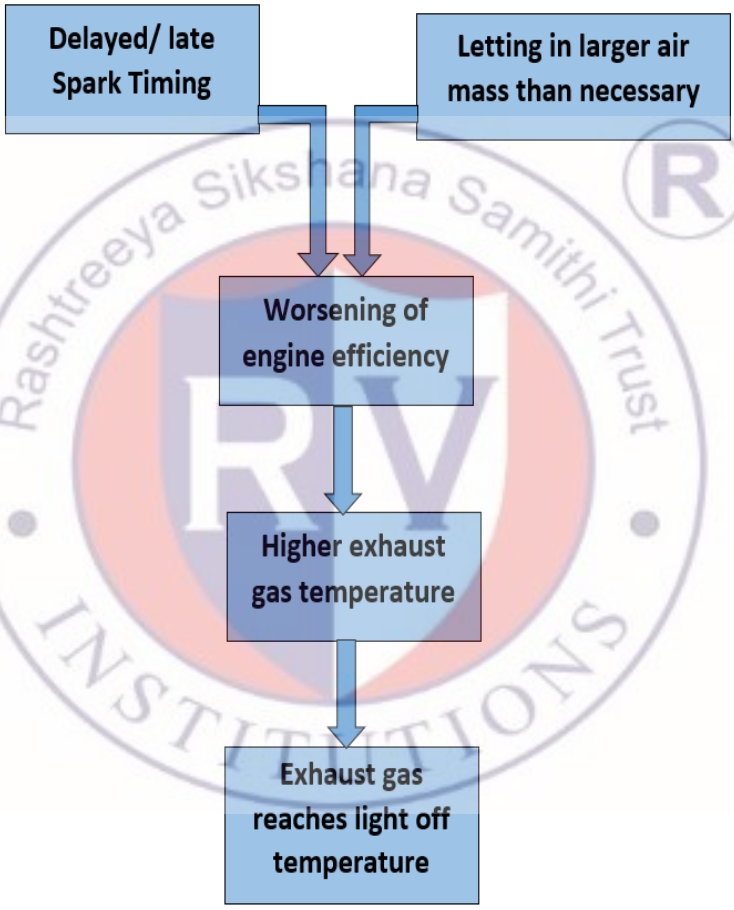

Figure 5.3. Algorithm for Work Flow for Controller for Worsening of Engine Efficiency and Ignition Retardation

5.1.10. Desired Lean Lambda During Catalyst Heating

If there is no secondary air pump available, this FC determines the appropriate lean lambda during the catalyst heating that causes the engine's raw emissions to be lower than those with a rich lambda. Since the catalyst is still not properly converting in the beginning of cold start heating, this is very important to keep emissions under control. If the secondary air pump system

is present, the required lambda is extremely rich, leaving a significant amount of HC after combustion to react with the secondary air pump's oxygen in the catalyst.

The engine is run after a cold start in such a way that an accelerated catalyst warm-up occurs for reasons related to exhaust gas emissions. The majority of the heat required for this might be provided by thermal exhaust gas energy. The engine must be run as leanly as feasible during the so-called lean warm-up in order to reduce feed gas emissions.

The energy from chemical exhaust gases is another heating strategy that is conceivable. For this, an excessive amount of fuel is used in the engine. Rich exhaust gas interacts in the catalyst or manifold during combined with secondary air. The catalyst is heated using the heat thus created by this oxidation process.

All of these features are created using specific catalyst heating techniques:

5.1.11. Ignition retardation

More heat is released towards the top dead centre during ignition happens earlier in the cycle. The peak cylinder pressure and temperature therefore increases as a result of enhanced ignition timing. NOx generation also increases as combustion temperature rises. As a result, enhanced ignition timing produces increased NO emissions. Engine damage issues and knocking also happens. The peak combustion pressure is lower during the ignition timing is delayed because more burning occurs during the expansion stroke. However, during the temperature of the exhaust gases rises, the engine efficiency declines. Additionally, with delayed ignition timing, a higher HC and CO oxidation rate is achieved with a higher exhaust temperature. As a result, retarded ignition timings produce minimal HC emissions. Workflow for controller algorithm Figure 5.3 illustrates the decrease of engine efficiency and ignition retardation.

5.1.12. Multiple Injection

The multiple injection strategy is a different way to raise the temperature of the exhaust gas. The multiple injection operation's combustion characteristics raise the exhaust gas temperature that results in a purely homogenous operation. Additionally, the divided injection technique improves ignition stability and allows for a certain late ignition angle to heat the catalytic converter.

In a multiple injection operation, the combustion chamber receives the whole amount of fuel that is to be injected into the cylinder throughout the course of an operational cycle in at least two injection phases. Initial homogenous injection takes place during the cylinder's intake

stroke in order to effectively disperse the injected fuel quantity across the combustion chamber at a later ignition time. Then, during a subsequent combustion stroke, a second late injection known as a stratified injection is carried out, creating the so-called stratified charge, where the injected fuel is concentrated in the cylinder in the area around the spark plug.

A mixed operation comprising stratified charge and homogeneous charging is represented by a multiple injection operation. In comparison to a completely homogeneous operation, the combustion properties of these systems lead to an increase in exhaust gas temperature and enable late ignition angle. Lean lambda summation is reliably ignited thanks to the rich mixture around the spark plug. Thus, it is preferable to combine both multiple injection and ignition retardation.

5.1.13. Lambda Split

The air-fuel ratio of each individual cylinder is adjusted in the opposite manner as another heating technique known as lambda split. This strategy involves operating some cylinders with a mixture that is richer than the total lambda during operating other cylinders with a mixture that is leaner. Compared to lean mode, partial combustion occurs in the cylinder during it is functioning in rich mode. The downstream catalytic converter is subsequently heated by exothermally converting the non-combusted components with the remaining oxygen fraction of the lean operating cylinder.

The catalytic converter is heated up by the exothermal catalytic conversion of the exhaust gas components that are not converted during the engine's non-stoichiometric combustion process during a significant amount of chemical energy is introduced into the catalytic converter system using this lambda split method. Because of this, it is preferred that the lambda value be controlled throughout the heat-up phase at least to a stoichiometric value of 1. If a catalytic converter that is far from the engine has to heat up quickly, this lambda detuning technique is useful.

5.1.14. Torque Reserve

By adding more fuel and air, one can make up for a torque loss brought on by thermal heating measures. The torque loss can be made up for by increasing the air charge during also reversing the ignition to account for the extra air. There are two types of torque control: air system torque and ignition system torque. The purpose of torque reserve is to maintain a range of torque that is managed by ignition timing without affecting the actual torque. As a result, the torque reserve is applied to the needed torque for the air system rather than the ignition system.

5.1.15. Increase in Idle Speed for Catalyst Heating

A few unique factors need to be taken into account during an automobile engine is operating in idle mode. The driver cannot control the throttle in idle mode by pressing the accelerator pedal. To balance the torques from all applied loads, the engine must create precisely amount of torque is required. run at a constant idle angular speed, together with the transmission, any accessories, internal friction, and pumping torques. As a result of the driver's actions, certain load torques happen. Certain additional load torques, however, happen without a driver command.

The mass flow rate of intake air determines the torque produced by the engine at idle, as it does in all engine operating phases. During the engine is fully warmed up, the electronic fuel control regulates fuel flow to maintain stoichiometry and short regulates fuel to be somewhat richer than stoichiometry during cold starts. The ECU is often designed to run the engine at a set RPM regardless of load during the engine is at idle. It accomplishes this by controlling mass air flow in response to the driver's throttle order. The throttle assembly, with the throttle at a little but non-zero angle, must supply the engine with the air flow necessary to maintain the correct idle RPM.

As an alternative, some engines have a unique air route that skips the throttle plate. An actuator is necessary for both approaches in order for the electronic engine control system to control the idle mass air flow.

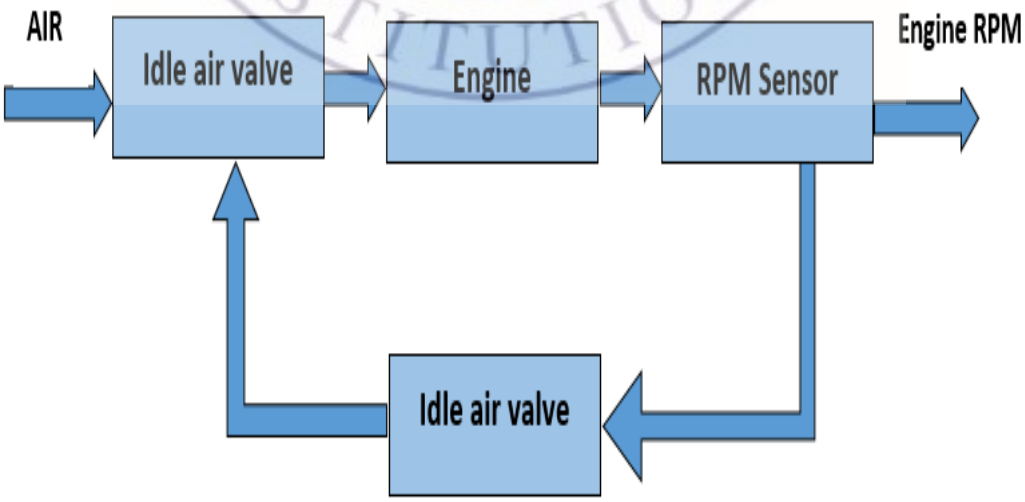

Figure 5.4. Algorithm for Controller for Idle Speed and Camshaft Adjustment

5.1.16. Exhaust Camshaft Adjustment.

With the adjustment of the exhaust camshaft, the heat flow is increased even more. The process of the exhaust valve opening as soon as feasible breaks the delayed combustion early, reducing the mechanical work produced even further. The exhaust gas contains the corresponding amount of energy in the form of heat.

Thus, implementing FC during taking these considerations into account effectively improves the catalyst heating qualities, leading to a reduction in exhaust emission. Figure 5.4 depicts the controller's algorithm for controlling idle speed and camshaft adjustment.

5.2 Component Protection for Exhaust Management

Anything that uses energy or work produces heat. The combustion process in a car generates too much heat. Due to component deterioration, this heat has a negative effect on both the engine's performance and the efficiency of emissions. Therefore, specific features that are in charge of thermal management have been designed in order to protect the heat-sensitive parts. For the goal of exhaust management, two distinct features for component protection have been established here.

5.2.1. Calculation of Combustion Chamber Lambda for Component Protection

This FC's activation is dependent on a system constant. Fuel enrichment is used for a predetermined period of time depending on the driver's input and engine speed. Next, the lambda of this function is determined. The set point lambda is calculated for component protection using this lambda value that is also used to regulate other functionalities.

This feature is required because the cylinder inter bore buckles due to thermal warming. Inter bore buckling causes the head gasket to be unable to seal the coolant that ultimately damages the engine and renders it incapable of being started again. As a result, mixture enrichment prevents the cylinder inter bore from overheating.

As a function of the present operating point, the functionality determines the relevant fuel enrichment required to safeguard the temperature between the cylinders. The idea behind its working is that by enhancing the air-fuel mixture, an exhaust gas temperature that is too high is reduced. As a result, more fuel enters the cylinder than necessary for the fuel to burn stoichiometrically. The unburned gasoline then evaporates on the cylinder walls, cooling the wall and lowering the temperature of the exhaust, protecting the exhaust components.

Here, a map that determines the lambda value for enrichment depending on engine speed and relative air charge is used by the functionality to perform fuel enrichment. Only during the simulated temperature surpasses its permissible level and the allowable wait time has passed are these enrichment mechanisms activated. A system constant is used to activate this Lower pass. Upon reaching a critically high component temperature, a filter in the FC gives the option of softening an otherwise sudden change in the enrichment factor.

To avoid the periodic switching of enrichment, temperature hysteresis functionality is activated. Only during all components must be safeguarded are all thresholds used. The corresponding threshold is set to the highest value achievable for noncritical components. As enrichment should not be utilised too late from a thermally non-critical to a thermally crucial zone, the threshold value selection should be evaluated dynamically. Otherwise, the component temperature overshoots. Low threshold values are chosen in this instance.

5.2.2. Torque Limitation for Exhaust Temperature Limitation

The exhaust gas temperature is limited by this FC that also regulates the torque limit, protecting exhaust system components from overheating. A torque limit is calculated here based on an exhaust gas temperature sensor or the modelled exhaust gas temperature. The estimated torque limit is then changed into a limitative injection mass. To manage the exhaust gas temperature so that it does not rise above a predetermined maximum temperature set point, a PI controller and pre controller are used to calculate the torque limit.

During employing injection mass limitation that is triggered by a switch, this functionality works in tandem with another FC to limit the temperature. Whether the restriction is caused by injection mass or torque is determined by the switch.

It functions on the basis that a calibrated maximum temperature limit for component safety is deducted from the sensor temperature or the temperature from the model. A PI controller is now activated based on this temperature differential, and its output determines the torque limit. The torque limit is controlled by a pre controller in addition to the PI controller and depends on the engine operation mode. It is possible to switch to a different type of pre-controller or select the modelled exhaust gas temperature in the event that the exhaust gas temperature sensor fails.

To prevent torque jumps, the outputs of the PI controller and pre-controller are combined and their gradients are constrained. The minimum torque limitation for engine protection is used in the computation of the torque limit to assure component protection in any

circumstance. Then, as an additional interface, the estimated torque limit is transformed into an injection quantity. Here, for this FC, in accordance with the needs of the customer, the filtered exhaust turbine upstream temperature is used for the selection of simulated temperature in order to prevent a sudden increase in turbine temperature that could lead to component damage. The exhaust gas temperature's maximum set point is selected as the PI controller's input.

5.3 Summary

This chapter explains about various strategies that are used in used in designing of thermal management of catalytic converters in order to bring down the exhaust emissions from the gasoline based vehicles.

CHAPTER 6

SIMULATION RESULTS AND IMPLEMENTATION

This chapter explains about the simulation analysis with prototype of designed model. This chapter also explains about results and discussions with output graphs of each of the controllers employed for thermal management of catalytic converter.

6.1 Simulation Analysis

In order to determine whether the temperature management package in the exhaust system complies with the necessary requirements, its functionality was successfully tested. The ASCET simulation programme was initially used to design the functionality. A section of the simulated design is shown in Figure 6.1. The design is depicted in Figure 6.2, serves as the basis for the automated generation of the code. To assure safety, this code is then assembled using the MISRA 2012 standard for the automotive industry. All of the FCs examined in this project's analysis are developed using this code creation procedure.

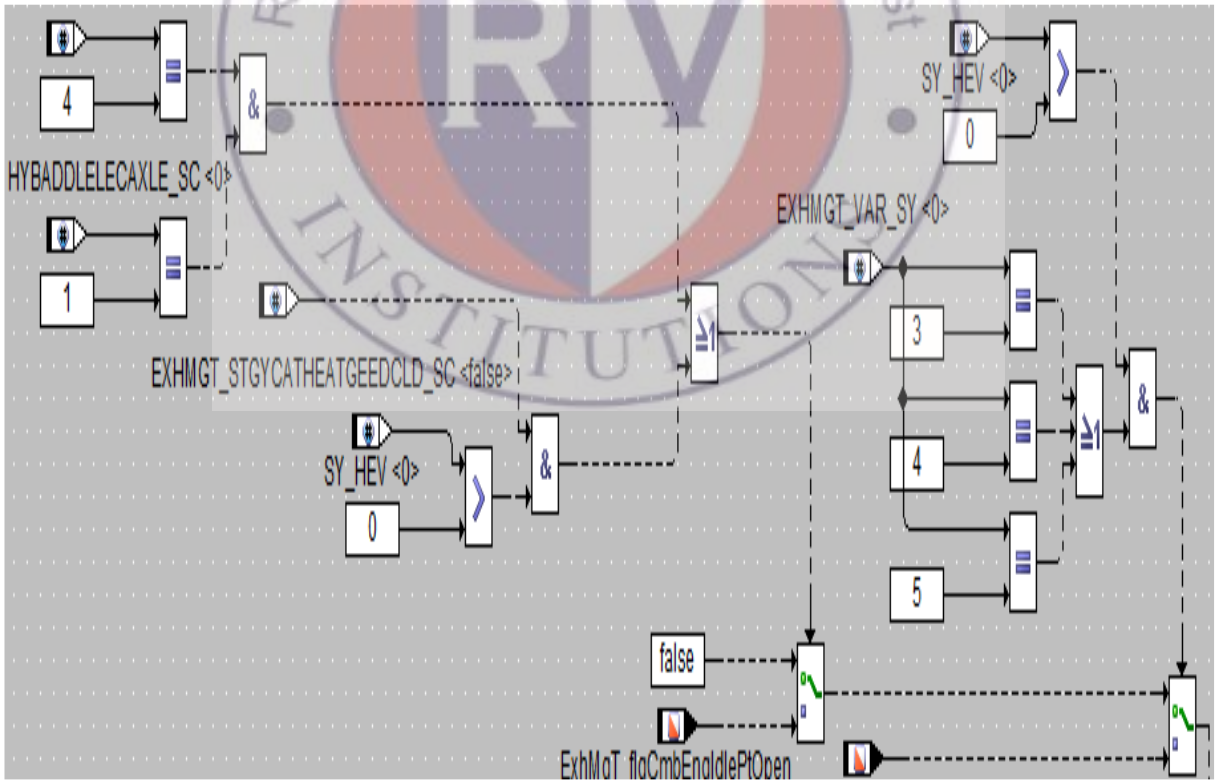

Figure. 6.1. ASCET Design

Following code creation, the FC is built and merged into the PVER variant. Once the feature construction is complete, The functionality is tested to see if the FC is functioning well or not.

The necessary FC's DLL must be produced in order to do TPT testing. Test scheduler, actual code, and sample test cases are all inputs for the TPT programme.

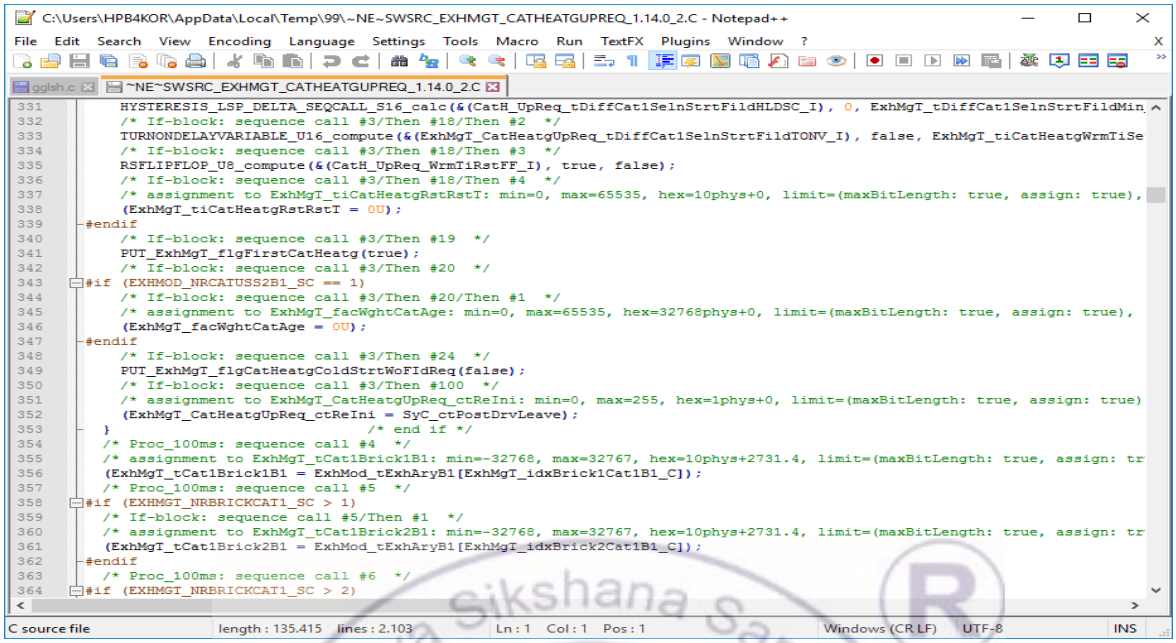

Figure. 6.2. Code Generated from ASCET

6.2 Results and Discussion

For each modified functionalities test cases are written and are tested. For each of these test cases test reports are also generated as shown in figure.6.3.

TPT Test Case Report: TC2

1 Testinformation

1.1 Report Meta Information

Test Case Name	TC2
Test Case ID	277
Test Result	✔ Passed
Execution started	12:41:45 19.03.2020
Assessment started	12:41:52 19.03.2020
Duration	21.058s (execution: 7.325s, assessment: 13.733s)
Test Case Group	<Instance 1 name>/TA_SW_ZWMINBTS_13
TPT File	zwminbts_urt_tauto.tpt
Directory	..\..\testdata_Ecco\FUSION_Platform\000__Instance_1_name_\001_TA_SW_ZWMINBTS_13\000_TC2
Test Data	Open Test Data
Execution Config	TestSuite_ECCo
Platform Config	FUSION Platform
Custom Node	..\..\..\..\SEDGe\2019.1.2\ZWMINBTS_tpt_output\ZWMINBTS_tpt.dll Package: miniPST_8.4_MDG_JDP/SEDGe 2019.1.2 // Version: ZWMINBTS/6.10.0;0 // Checksum: 0
Platform Mapping	Interface Import_014
Test Case Description:	

Figure 6.3. TPT Test Report

The TPT report provides a summary of all functionality tests carried out. It also shows failing test cases. The signal viewer allows to view each signal as it is displayed in the figures below. Figure 6 shows a graph of an engine in operation. Figure 6.4 displays a graph of time as a function of engine speed. Figure 6.5 depicts a graph of time versus catalyst brick temperatures. Figure 6.6 depicts a graph of time versus the catalyst's maximum temperature. Figure 6.7 shows a graph in that time is plotted against the catalyst's maximum temperature. Figure 6.8 displays a graph of the time v/s signal for catalyst heating brought on by a cold start. Figure 6.9. is a graph displaying the catalyst heating's time v/s signal Figure 6.10 depicts the graph of catalyst warming, Figure 6.11 the graph of time versus heating mode, Figure 6.12 the graph of controller output for air charge control actors, Figure 6.13 the graph of controller output for idle speed, and Figure 6.14 the graph of controller output for lambda coordination. Figure 6.15 displays the output graph for the controller used to set the maximum torque during idle speed.

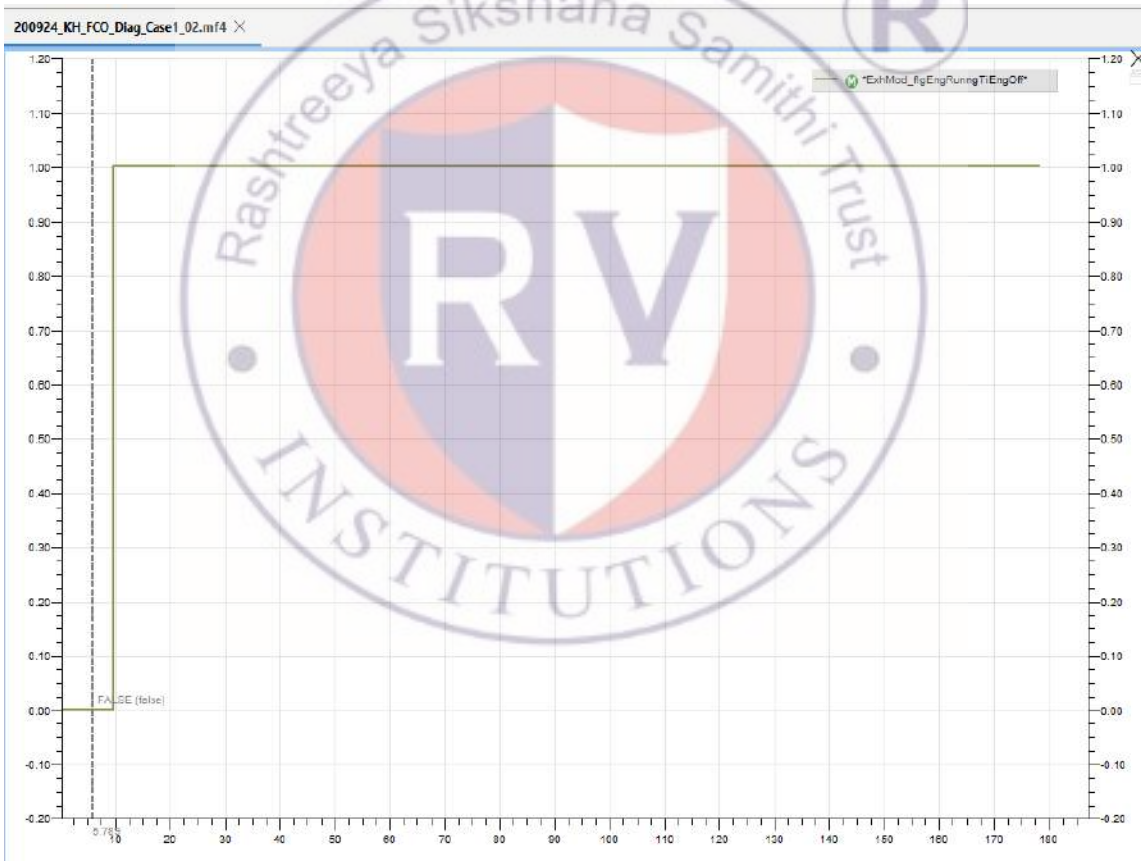

Figure 6.4. Graph Showing Engine in Running Mode

The figure 6.4 shows the engine running status it shows it is equal to one we check it actually specifies engine is in drive mode.

The figure 6.5 shows the engine speed versus time. The engine speed is varying randomly in accordance with the time. It is according to the driver’s desire.

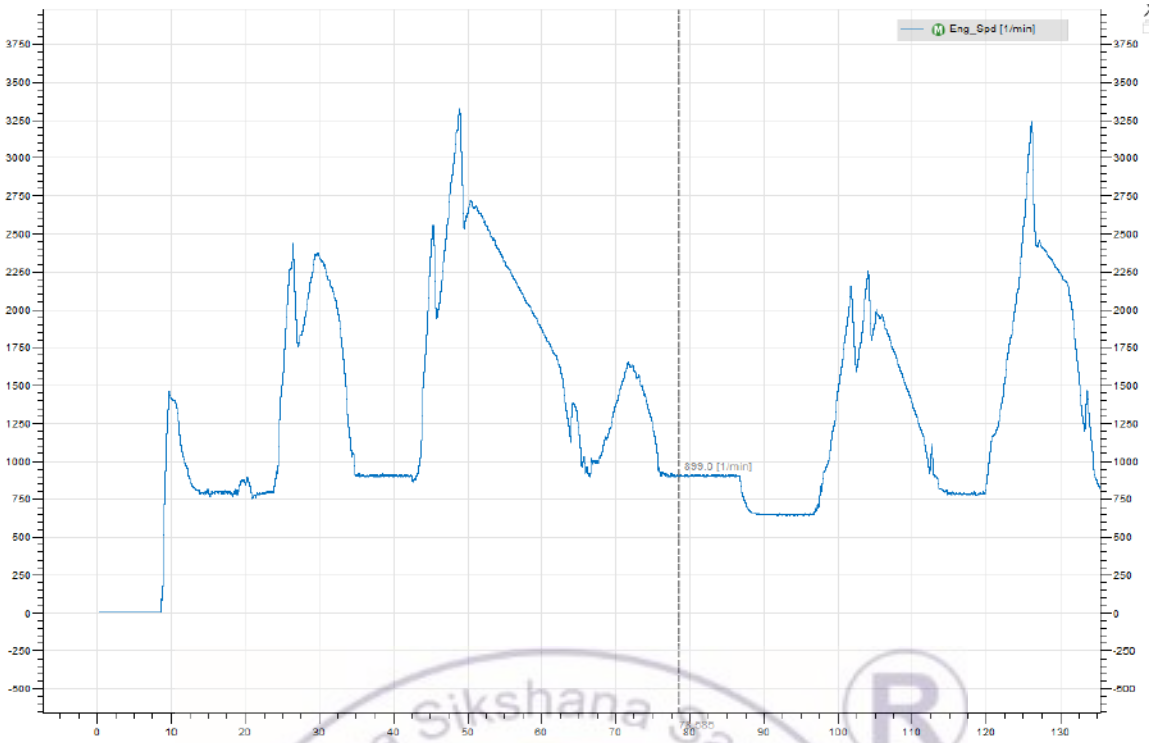

Figure 6.5. Graph Showing Time v/s Engine Speed

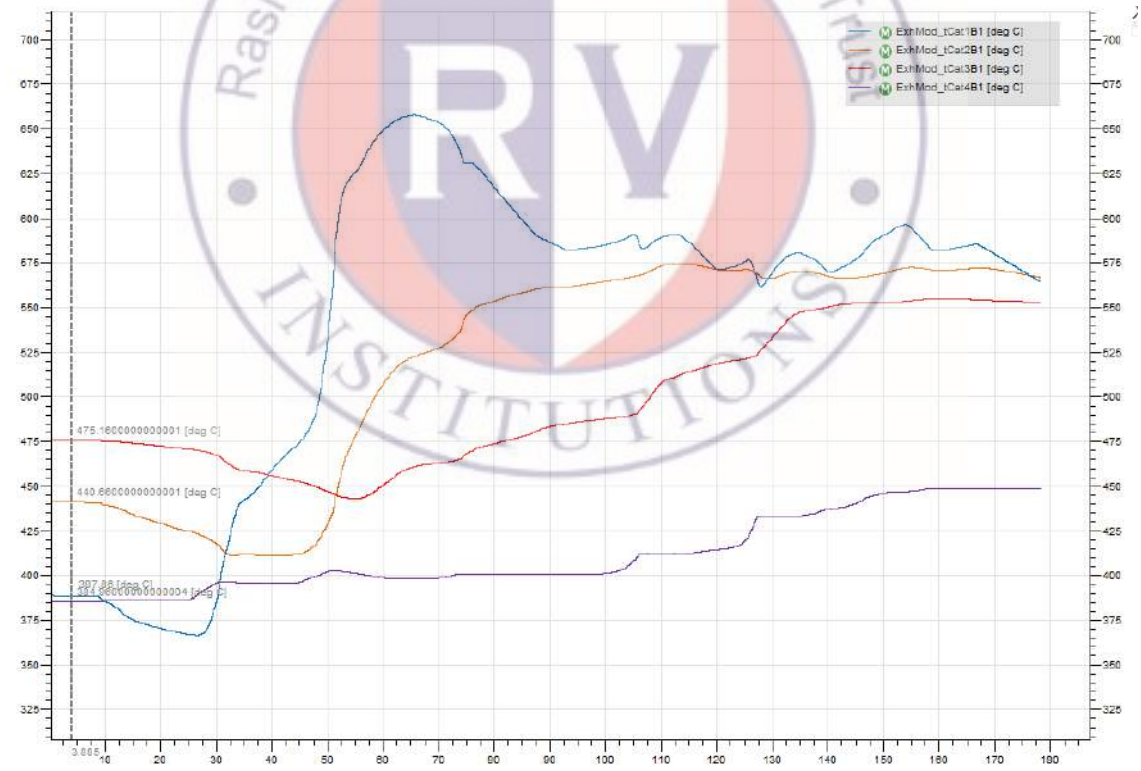

Figure 6.6. Graph Showing Time v/s Catalyst Brick Temperatures

The figure 6.6 shows the temperature of the catalyst bricks. Temperatures are the maximum temperatures that are selected from the catalyst banks. The temperatures of the catalyst bricks are wearing randomly with time.

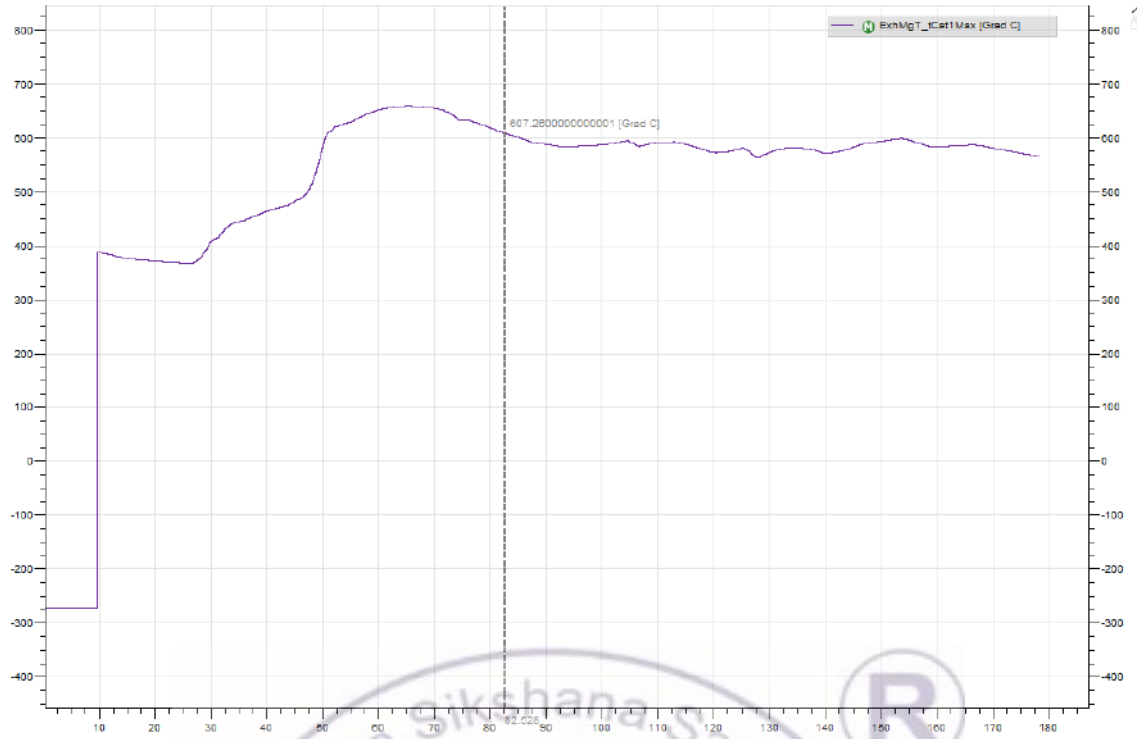

Figure 6.7. Graph Showing Time v/s Maximum Temperature of Catalyst

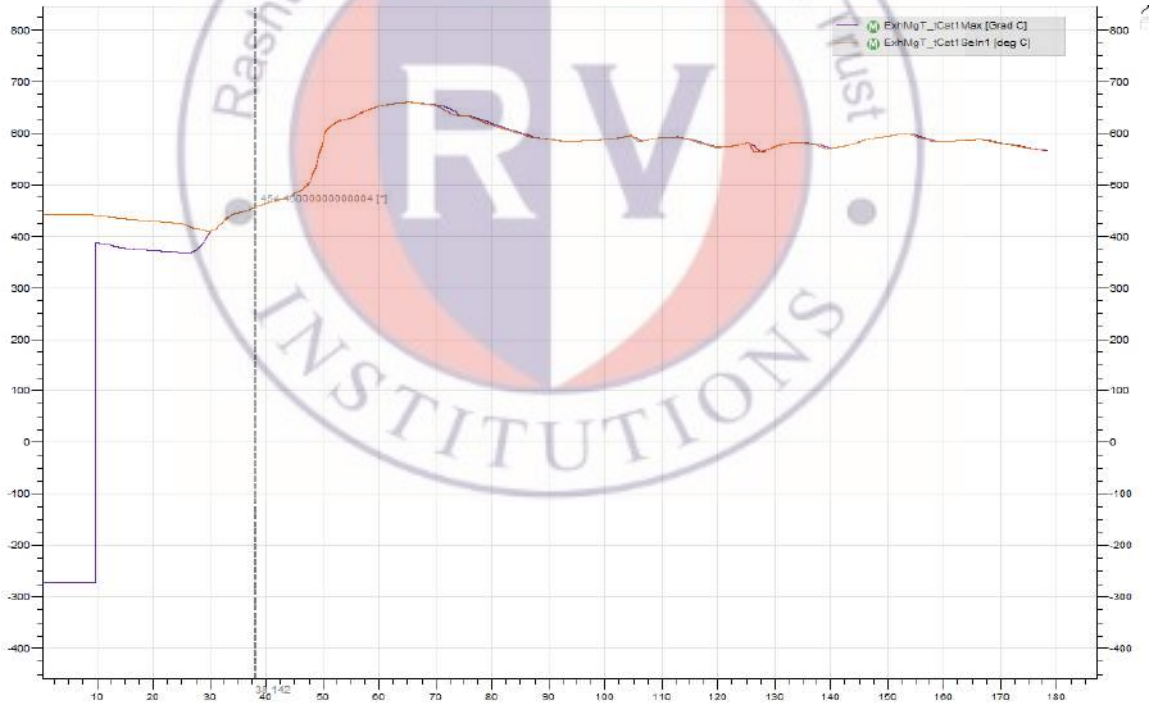

Figure 6.8. Graph Showing Time v/s Selection of Maximum Temperature of Catalyst

The figure 6.7 shows the maximum temperature for the catalyst heating it is selected among the maximum temperature of the catalyst bricks in the banks of the catalyst.

The figure 6.8 shows the selected maximum temperature for the catalyst heating it is also selected from the maximum temperature of the catalyst bricks available from the previous graph

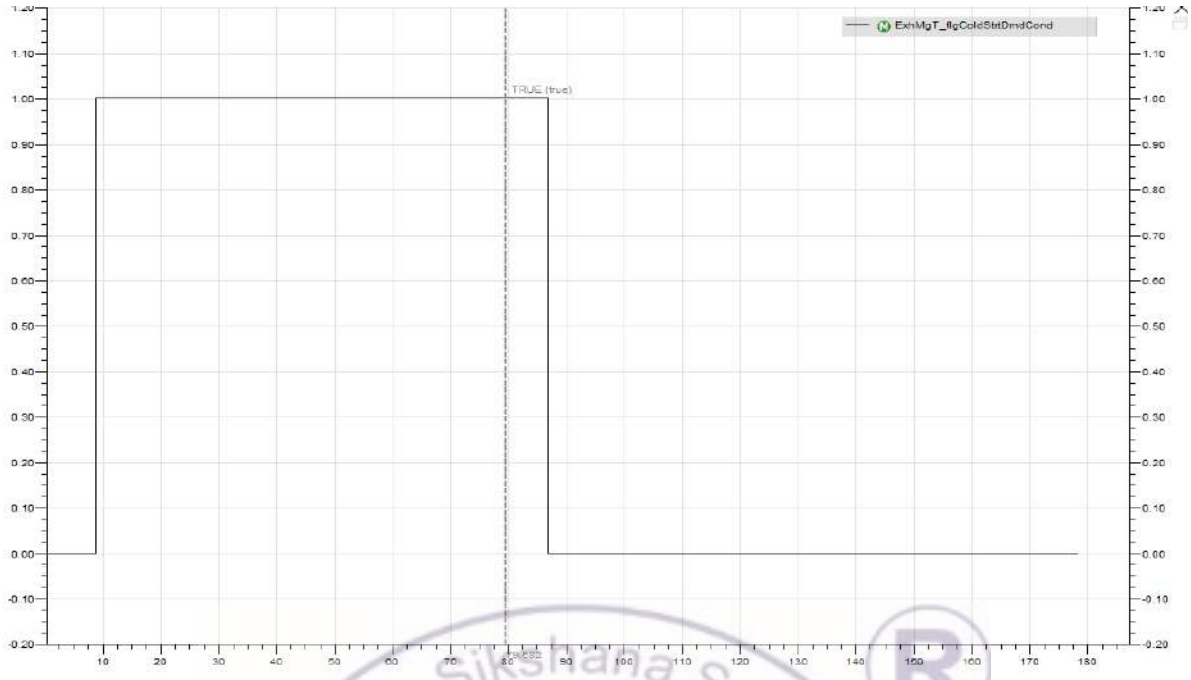

Figure 6.9. Graph Showing Time v/s Signal for Catalyst Heating Due to Cold Start

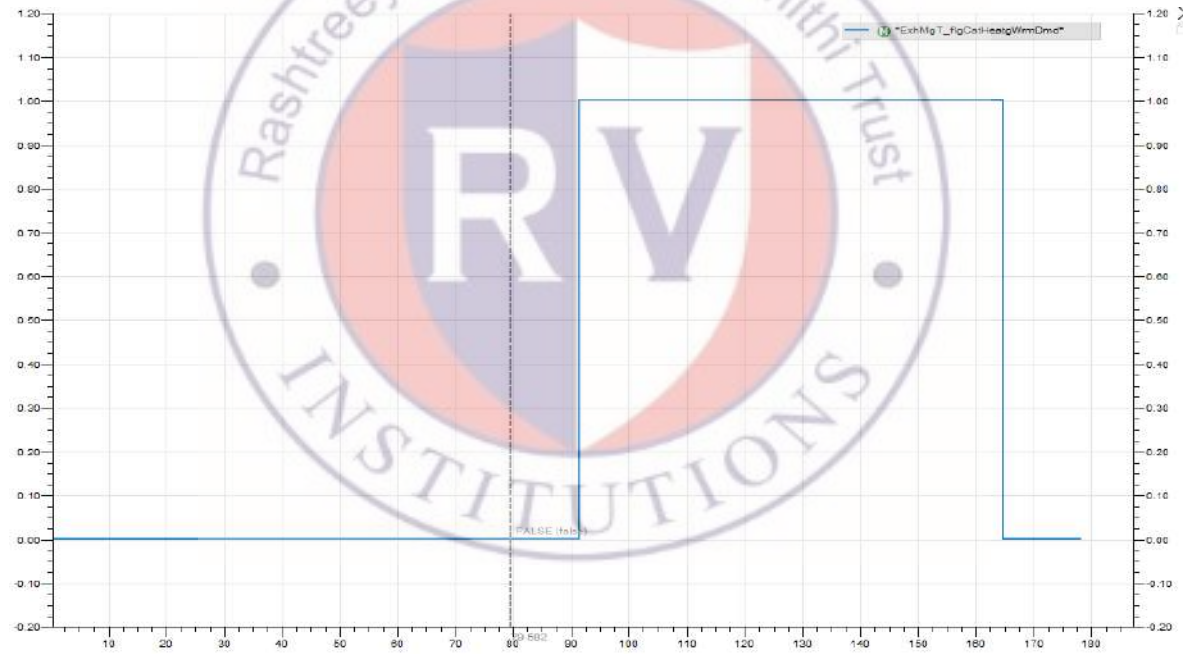

Figure 6.10. Graph Showing Time v/s Signal for Catalyst Heating Due to Catalyst Warming

The figure 6.9 shows the signal for the catalyst heating for the cold start of the engine the cold start actually happens during the engines starting time so the catalyst needs to be heated during the starting phase of the engine drive mode so the signal is set to one during the starting phase of engine driving mode

The figure 6.10 shows the signal for the catalyst heating for the catalyst warming the catalyst warming should happen during the engine running mode so the signal is set to one during the engine drive mode and it is depicted in the graph

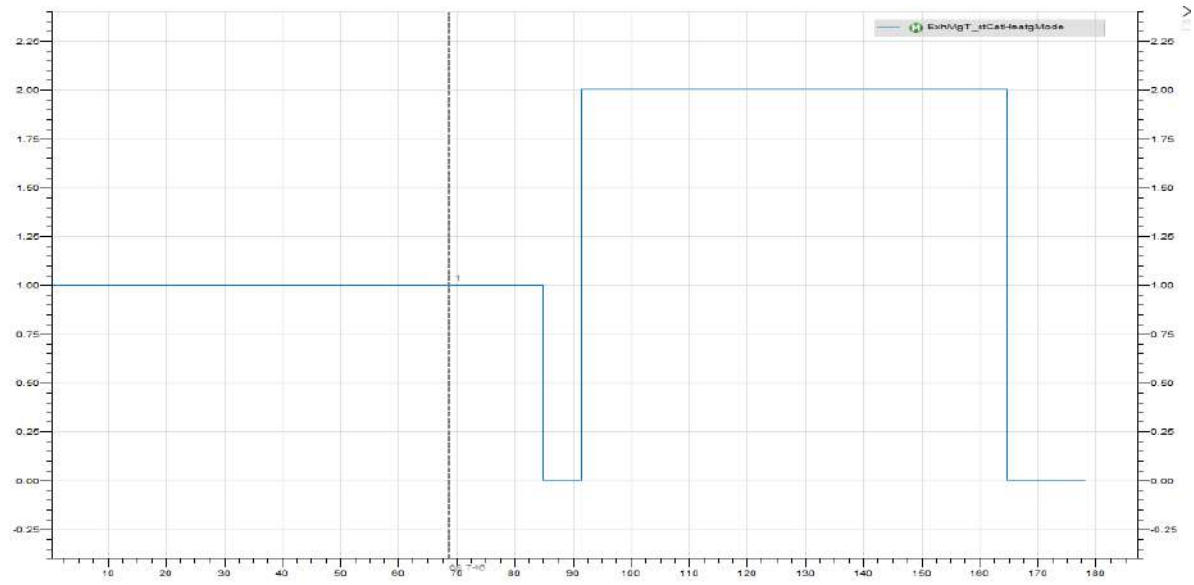

Figure 6.11. Graph Showing Time v/s Heating Mode

The figures 6.11 shows the heating mode of the catalyst that is either the cold start or catalyst warming if the calibration parameter is set to one then the heating mode selected as cold start warming of the catalyst if the calibration parameter is set to two then heating mode is selected as the catalyst warming it happens during the engine drive mode.

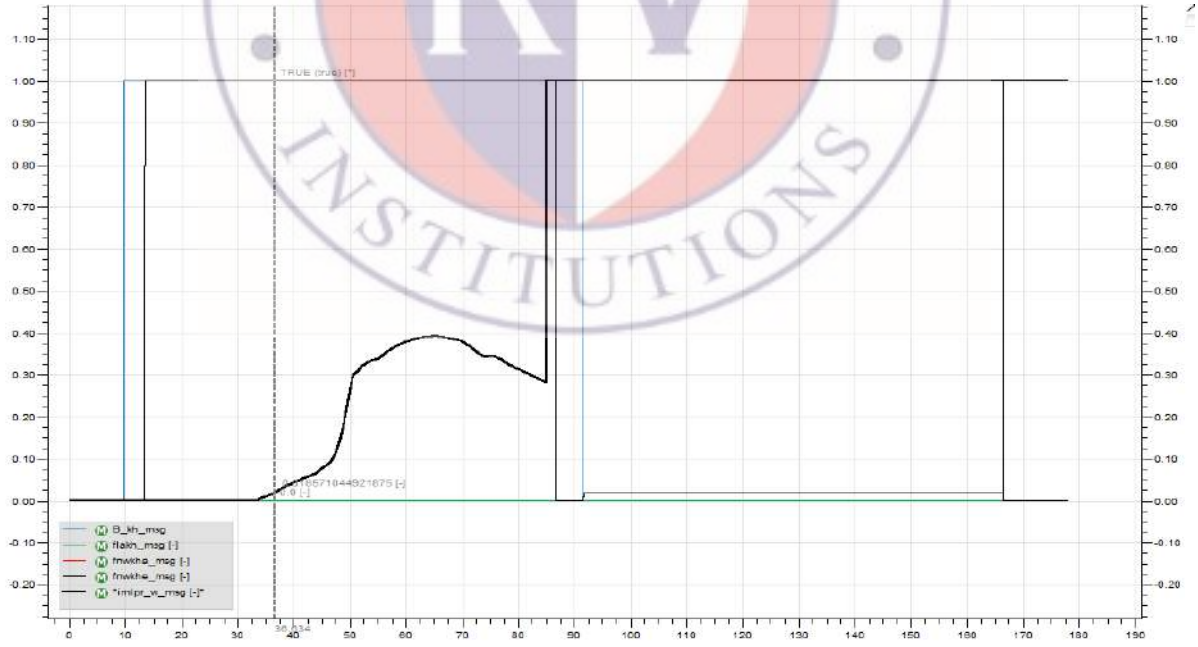

Figure 6.12. Graph Output for Controller for Air Charge Control Actors

The figure 6.12 shows the air charge control actor parameters it shows the weighting factor for the camshaft inlet valve and the weighting factor for camshaft outlet valve and the weighting factor for the swirl valve. so that the optimal amount of air and fuel or injected into the combustion to chamber for the proper combustion of the fuel for the reduction of emissions.

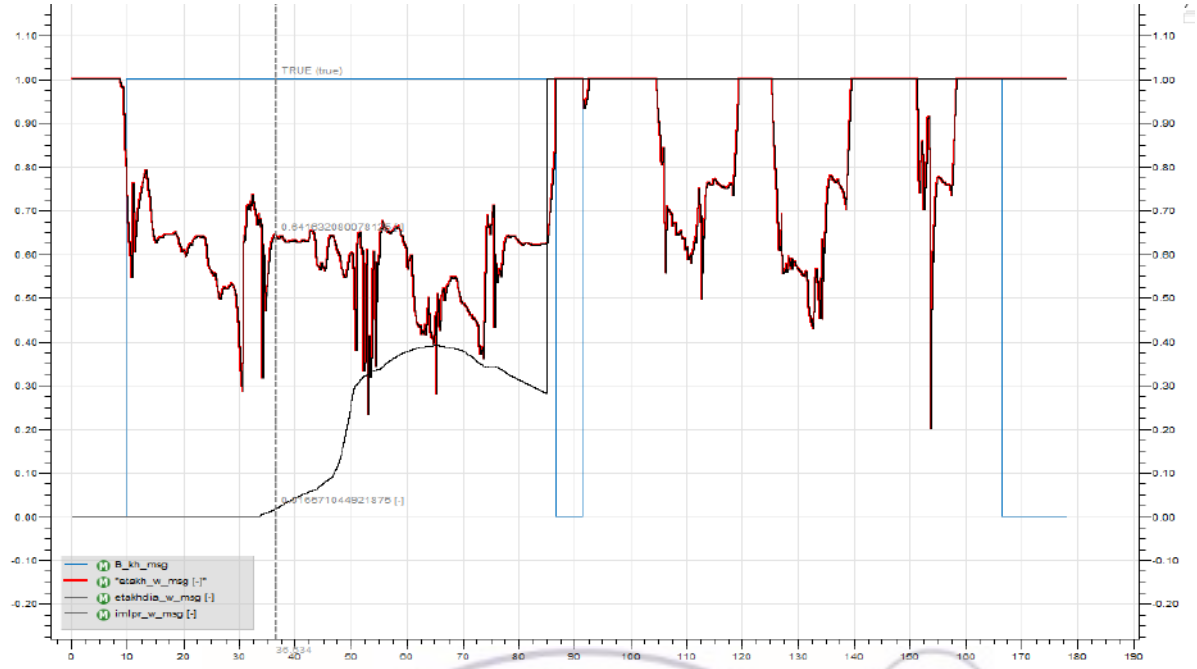

Figure 6.13. Graph Output for Controller for Idle Speed

The figure 6.13 shows the engine speed and the selection of the maximum idle speed for the worsening of the engine efficiency with the late spark ignition timing. If ignition is sparked lately then there is a sufficient amount of air is injected into the combustion chamber so that the lambda value is varied within it's range of 0.9 to 1.1

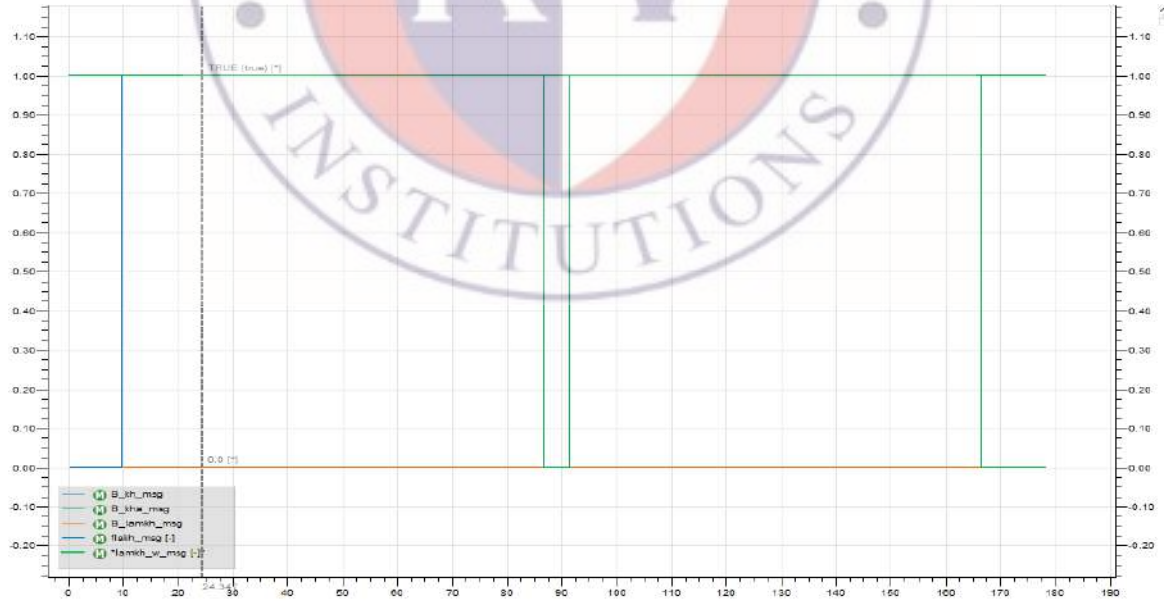

Figure 6.14. Graph Output for Controller for Lambda Coordination

The figure 6.14 shows the variation of air to fuel ratio that is lambda value. The lambda value is vary within its range of 0.9 to 1.1. The lambda value is set to its rich value during secondary air injection is not available. The lambda value is set to its lean value during the secondary a injection is not available.

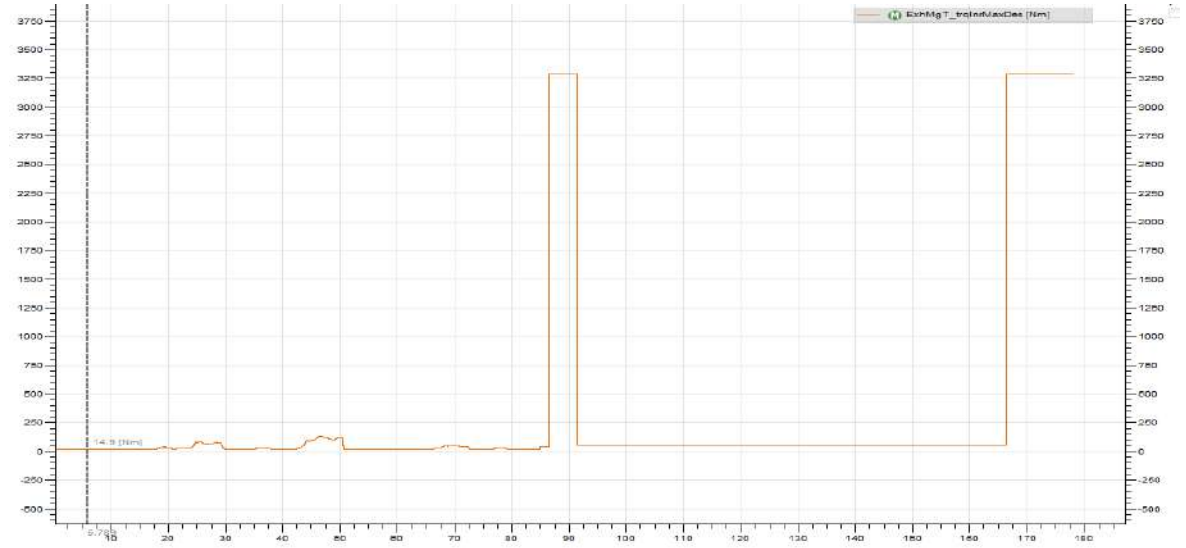

Figure 6.15. Graph Output for Controller for Setting Maximum Torque During Idle Speed

The figure 6.15 shows the torque value that is set during the maximum idle speed the torque is selected in such a way that the torque should be equal to the torques of the friction, torque that is randomly generated from the driver and the torques generated from the other moving parts of the engine.

6.3 Summary

The simulation analysis with prototype of designed model are explained in this chapter. This chapter also explains about results and discussions with output graphs of each of the controllers employed for thermal management of catalytic converter are explained in this chapter.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

This chapter summarises the conclusion and findings about each of the strategy implemented for thermal management and discusses the potential for further improvement that are implemented for futuristic two wheeler gasoline based engine vehicles.

7.1 Conclusion

Due to the risks that car emissions pose to the environment and human health, strict emission regulatory rules have been put in place. Over the past ten years, India has implemented a number of policies to reduce emissions from the fleet of vehicles. For the engines running normally, a significant reduction in exhaust pollution has already been realised conditions. The important engine-out emissions and poor catalyst performance caused by the low cylinder and exhaust temperatures mean that such emissions during cold start and warm up are nevertheless still considerable. The temperature of the exhaust gas has become a crucial factor in evaluating whether an engine is performing well. In order to reduce cold start and warm up emissions and component protection methods for automotive emission reduction, this project studied thermal management approaches for quick catalyst light-off. By preheating the catalytic converter, thermal management, in contrast to other approaches previously used, resolves the trade-off between energy use and emission reduction.

Emission control is significantly aided by electronic engine control. Modern engines are not able to attain the low emissions levels they do without computerised regulation.

- The engine control system delivers the required amount of air, fuel, and EGR at the required temperature in the required time with the required pressure as per its objective in terms of emissions. Over the course of the engine's lifetime, this control is used to offset the wear and degradation of the engine.
- The engine control management system is a mixed-signal embedded system and communicates with the engine via a variety of sensors and actuators. It organizes all of the engine's requirements, prioritizes them, and eventually implements them.
- The control techniques are designed for air-fuel ratio management, ignition control, electronic throttle control, idle speed control, accelerator pedal position control, and other applications. The control system's successful design and execution results in higher engine output in terms of control of emissions in proper way in order to reduce them.

- Catalyst temperature is selected based on maximum temperature available. Lambda value is brought into its range 0.9 to 1.1. Camshaft valve angle varies optimally in order to allow the desired value of air and fuel into the combustion chamber.
- A thorough analysis of the many functional parts of the exhaust temperature management package was conducted, and a few of these parts are updated to comply with customer-required emission standards.

The electronic control system works in conjunction with the fuel and fuel system, the engine and its combustion system, sensors, and the design and placement of the catalyst and filter to reduce emissions as much as possible. Thus, creating an optimal system enhances engine exhaust emissions for greater compliance with various exhaust legislation, improving the environment and providing health benefits.

7.2 Future Scope.

In the age of hybrid electric vehicles, the gasoline based vehicles are atleast be implemented as part of power trains. So the gasoline based vehicles are to be improvised for their working and functionality.

- Future of gasoline vehicles is tending towards reduction of emission to meet the emission standards that are going to be introduced in 2025 specially to reduce the carbon dioxide and unburnt hydrocarbons in order to reduce the environmental emissions.
- In order to meet emission standards of future the engine control unit, exhaust gas recirculation system, needs to be improvised for its functionality.
- Carbon-neutral combustion engine is a pipe dream. The idea is related to synthetic fuels, sometimes known as carbon-neutral fuels, whose production process absorbs CO_2.
- As a result, the greenhouse gas is transformed into a raw material and power generated from renewable sources are going to be used to make gasoline, diesel, and replacement natural gas.
- By about 2025, this is soon going to become a reality that synthetic fuels rendering vehicles fuelled by gasoline and diesel carbon-neutral that significantly reduces global warming.

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APPENDIX

Design And Implementation of Thermal Management System for Gasoline Based Engine Exhaust System

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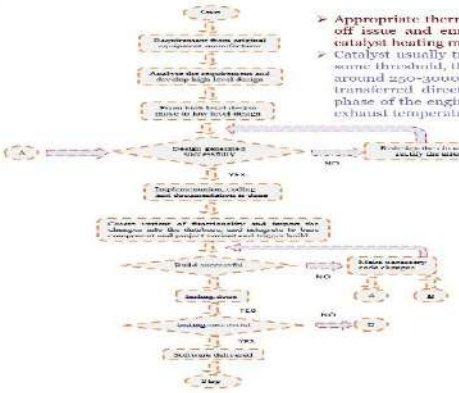
OBJECTIVE

The main objectives of the project are:
Design and simulate a system which minimizes the exhaust emission by implementing an exhaust temperature management and to validate the designed system for enhanced functionality with TPT software.

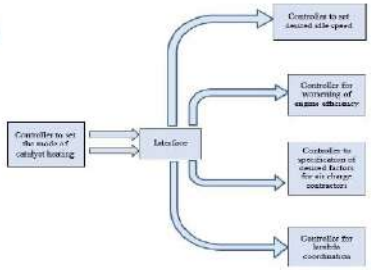
Project Methodology

Catalyst usually transforms harmful emissions when their temperature reaches some threshold, the so-called light-off temperature. For two wheelers this temperature is around 250-3000C. The methodology for maintaining the high temperature in catalytic converter for emission reduction involves certain measures are followed they are maintaining maximum idle speed, increasing the air mass flow through camshaft valve thereby worsening of engine efficiency, lambda coordination.



Methodology

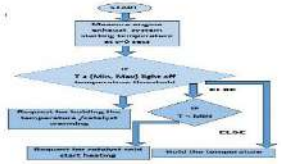
- Appropriate thermal management of catalyst can significantly reduce the light-off issue and emission concentration. This can be achieved through proper catalyst heating methods.
- Catalyst usually transforms harmful emissions when their temperature reaches some threshold, the so-called light-off temperature. For TWC this temperature is around 250-3000C. Thus, at low exhaust temperature the harmful emissions are transferred directly into the atmosphere. During the cold-start or warm-up phase of the engine the catalyst is not fully operational due to the deficiency in exhaust temperature.



Block diagram

Block diagram

- Controller to set the mode of catalyst heating: The thermal management for catalyst heating is used to heat up a cold exhaust gas system, by sending the signal to further functionalities to keep the system warm, to desulfurize the NOx storage catalyst or to trigger a short trip at the end of the production line.



- This functionality is to request catalyst heating when the engine is started with the catalyst temperature too low to reach the light-off temperature. The FC will enhance catalyst heating as fast as possible. During the start phase since the measured catalyst temperature is not available and the modelled temperature is inaccurate, the catalyst heating is calculated in dependence on the engine temperature, intake air temperature, shut off time and altitude.

Algorithm for setting temperature

The degradation of the engine efficiency can occur during the catalyst heating by a cold start, during catalyst warm-up. An effective measure that can be adopted for engine efficiency is choosing a late spark timing. Additionally a bigger air mass that that is necessary for the conversion of the optimum moment that is pre-controlled in the motronic over the air path. The spark must be pulled later for the torque reserve.

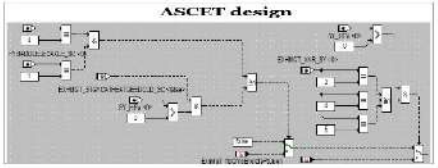
Algorithm for worsening of engine efficiency and ignition retardation

Algorithm for controller for idle speed and camshaft adjustment

Controller to specification of desired factors for air charge contractors: It exports different factors which are used to increase or reduce the cold start heating measurements gradually: factor for the lambda value, factor for the cam shaft inlet valve and for the cam shaft outlet valve and factor for the swirl control.

Simulation analysis Results and Discussions

ASCET design

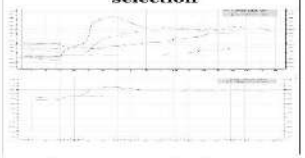


Code generated from ASCET

The temperature management package in exhaust system for the emission regulation was designed using ASCET simulation tool. The code is generated automatically based on the design This code is then compiled using motor industry standard MISRA 2012 to ensure safety. This code generation process is adopted for the development of all the FC's analysed in this project.

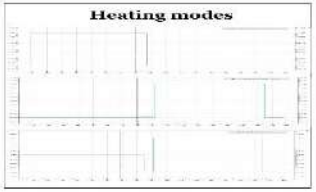
- For TPT testing, DLL of the corresponding FC needs to be generated. The input to the TPT software include sample test cases, test scheduler and actual code.
- For each modified functionalities test cases are written and are tested. For each of these test cases test reports are also generated

Max temperatures and selection

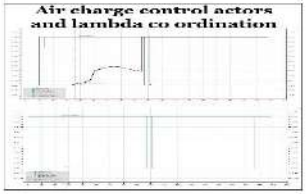


- Temperature for catalyst heating is selected among available catalyst temperatures of bricks of catalyst bank 1 and 2
- Heating mode i.e. cold start , catalyst warming is selected based on the timing of engine operation and maximum temperatures available.
- Heating mode is selected as cold start when light off temperature is not reached. Heating mode is catalyst warming when the temperature is in the range of light off temperature

Heating modes

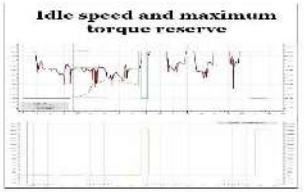


Air charge control actors and lambda co ordination



- A loss in torque caused by thermal heating measure can be compensated by increasing the quantity of air and fuel. Increasing the air charge while shifting the ignition to retard to compensate for the additional air can compensate the torque loss.
- At engine idle condition, the ECU is intended to operate the engine at a fixed RPM regardless of load. It does this by regulating mass air flow with the throttle command from the driver.

Idle speed and maximum torque reserve



Conclusions

- Exhaust gas temperature is a parameter that has become essentially important in determining the functioning of an engine. This project reviewed the thermal management methods for fast catalyst light-off, for the purpose of decreasing cold start and warm up emissions and component protection techniques for automobile emission reduction.
- Electronic engine control plays a significant role in emission control. From the emission perspective, goal of an engine control system is to provide the demanded quantity of air, fuel and EGR at the required temperature in the required time with required pressure.
- The fuel and fuel system, the engine and its combustion system, sensors and the design and location of the catalyst and filter combine with the electronic control system to give the maximum emission reduction.
- Thus developing an optimized system will improve the reduction of engine exhaust emissions for better adaptation to different exhaust legislation, thereby promoting better environment conditions.

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- I deeply express my sincere gratitude to my guide Dr. J.N Hemalatha, Associate professor, Dept. of EEE, RVCE, Principal and HOD, Dept. of EEE, RVCE and Panel members for their patience and valuable guidance throughout this project.
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Methods of Thermal Management of Catalytic Converters in Gasoline-Based Engine Exhaust Systems

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Abstract : Controlling exhaust emissions from internal combustion engines has emerged as one of the most pressing issues. Breathing difficulties, headaches, persistently impaired lung function, eye discomfort, lack of appetite, and corroded teeth are all possible side effects. It can have an indirect impact on humans by harming the ecosystems on which they rely in the sea and on land. The Indian government amended European regulations considering environmental concerns and health risks. To fulfil the impending pollution standards, existing engine technology must be modified, and a better system developed. Exhaust temperature management is the most effective approach to controlling emissions. The temperature in the exhaust system has a significant impact on emissions since exhaust gas treatment equipment like catalysts, oxygen sensors, and storage catalysts operate only within a narrow temperature range. Thus, by efficiently managing the exhaust system temperature, we can reduce emissions to a given level. The main criterion for accomplishing all of these requirements is engine torque. Catalytic converters reduce the emissions of carbon monoxide, hydrocarbons, nitrogen oxides, and particulate matter from internal combustion engines, allowing them to satisfy increasingly rigorous emission laws. Catalytic converters, on the other hand, have light-off troubles during cold start and warm-up. This work evaluates the literature on catalyst thermal management, with the goal of drastically reducing light-off time and emission concentrations using optimal heating methods. Methods based on engine parameter control, in particular, are simple to apply since they do not necessitate the use of additional heating equipment. They do well in terms of reducing catalyst light-off time.

Index Terms **- Light off temperature, Catalytic converter, Thermal management, Internal combustion engines, Spark ignited engines, Catalyst, Exhaust emissions.**

I. INTRODUCTION

This Automobiles are increasingly widely utilized since mobility improves living conditions. The ever-increasing transportation of people and things across numerous locations has a significant impact on economic progress. India, the world's second most populous country, has a diverse economy, with transportation being a key component. According to statistics, the number of automobiles in our nation has increased by more than 240 percent in the last decade. This is predicted to continue increasing at a similar rate over the next 20 years. This high car rate has negative consequences. These include severe environmental risks such as climate change, pollution, global warming, poorer agricultural yields, and threats to living creatures as a result of increased dependency on fossil fuels and increased pollution emissions, which may finally result in total ecological imbalance.

Major automotive emissions from internal combustion engines include traditional pollutants such as carbon monoxide (CO), nitrogen oxides (NOx), particulate matter (PM), and hydrocarbons (HC), as well as greenhouse gases such as carbon dioxide (CO2), methane (CH4), and others. The implementation of Bharat V/VI standards across the country may reduce automotive emissions by 86 percent. It is very advised to create engine control systems in order to attain high performance and minimal exhaust emissions. The engine management system is a mixed-signal embedded system that communicates with the engine via a variety of sensors and actuators. It organizes all of the engine's requirements, prioritizes them, and eventually implements them. The control techniques are designed for air-fuel ratio management, ignition control, electronic throttle control, idle speed control, accelerator pedal position control, and other applications. The control system's successful design and execution results in higher engine output.

To fulfil the impending pollution standards, existing engine technology must be modified, and a better system developed. Exhaust temperature management is the most effective approach to control emissions. The temperature in the exhaust system has a significant impact on emissions since exhaust gas treatment equipment like as catalysts, oxygen sensors, and storage catalysts operate only within a narrow temperature range. Thus, by efficiently managing the exhaust system temperature, emissions may be reduced to a specific level. The primary criterion for implementing all of the requirements is engine torque. This paper provides an overview of approaches for improving pollution control in vehicles by regulating exhaust temperature.

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II. Thermal Management

Internal combustion (IC) engines for vehicle propulsion have significant hurdles due to their relatively high emissions and limited efficiency. Nonetheless, popular estimates imply that IC engines will continue to be widely utilized for a relatively long time [1][2], at least as components of hybrid electric powertrains. As a result, the automobile industry is making major efforts to minimize IC engine emissions, such as carbon monoxide (CO), hydrocarbon (HC), nitrogen oxides (NOx), and particulate matter (PM) [3]. After-treatment systems, such as three-way catalysts (TWCs) [4], diesel oxidation catalysts (DOCs) [5], selective catalytic reduction systems [6], and diesel particulate matter filters (DPFs) [7] have been effectively applied in spark ignition (SI) and compression ignition (CI) engines for this purpose.

However, as most of the after-treatment systems are catalytic converters, their functionality deteriorates at low temperatures, e.g., during engine cold start and warm-up [8]. In fact, catalysts usually convert harmful emissions only when their temperature reaches certain thresholds, i.e., the so-called light-off temperature, which is normally around 250–300 °C for TWCs [9]. Hence, high levels of exhaust emissions are transferred into the atmosphere while the exhaust temperature is low, during the engine cold start or warm-up phases, in which the catalyst is not fully operational.

In addition, during cold-start, a considerable amount of gas-phase HC condenses on the surface of the tailpipe and catalyst, and partially volatilizes to the atmosphere without catalytic oxidation during the following warm-up phase The thermal management of catalytic converters is a timely topic. In fact, in the current context of the automotive sector, hybrid electric vehicles (HEVs) play an increasingly important role. HEVs allow IC engines to operate more efficiently, and partially recuperate their kinetic energy during braking [10]. However, HEVs still face the challenge of cold-start emissions, as HEV engines are usually switched off at low speed and wheel torque, when the brake specific fuel consumption is particularly high. This may reduce the exhaust temperature, and thus the catalyst efficiency. Therefore, the thermal management of the catalyst is important for both conventional vehicles and HEVs. Therefore, the thermal management of the catalyst is important for both conventional vehicles and HEVs.

A significant amount of study has been conducted to examine catalyst properties and enhance catalyst light-off performance through proper heat management. Nonetheless, the literature lacks a thorough examination of the thermal management of catalytic converters in order to reduce exhaust emissions during engine cold start and warm up.

III. Exhaust Emissions During Cold Start and Warm Up Phases

Reference [11] performed a thorough examination of cold start emissions. Several studies, including Refs. [12] and [13], indicate experimentally observed high CO and HC emissions for both gasoline and diesel engines when started cold. Maximum CO and HC values in the publications studied varied from 950 ppm to 8400 ppm and from 220 ppm to 28,000 ppm, respectively [13][14]. Poor cylinder combustion and catalyst efficiency are to blame for such high emissions. The particle number concentration does not fluctuate considerably during cold start, but it is highly dependent on engine speed and load [15]. Because of the low cylinder temperature, less elemental carbon develops under cold start circumstances, but substantially more gas-phase HC transforms to liquid-phase particles. As a result, the fall in HC content contributes to a decrease in PM under cold start circumstances. High NOx emissions were also recorded in ref. [16], owing mostly to inadequate catalyst efficiency. The exhaust temperature of some vehicles, such as airport shuttle buses, sightseeing buses, and urban buses, can be permanently below the catalyst light-off threshold.

According to Gong et al. [17], in ultra-low emission vehicles (ULEVs), 80-90 percent of tailpipe HC emission occurred during the first test cycle in the federal test procedure (FTP), and these numbers can increase in super ULEVs. Given these facts, actions were taken or considered to minimize emissions during warm-up by enhancing I combustion and/or (ii) catalyst efficiency. For example, in relation to an adequate heat storage or supplementary heat source can boost the temperature of the lubricant [18] or coolant [19] before the engine begins, thus raising the cylinder temperature and reducing CO and HC generation. Intake air heating [20] and fuel heating [21] can also help with combustion. In terms of (ii), standard procedures alter the operating engine parameters, such as adjusting the valve timing, enriching the air/fuel mixture, and adjusting the commencement of combustion. Although such solutions can significantly reduce the catalyst light-off time, IC engine emissions continue to worsen prior to the catalyst light-off. As a result, a pre-catalyst device might heat the exhaust to expedite light-off. Among the several strategies for efficiently reducing cold start and warm up emissions, this paper mainly shows overview about thermal management of the catalytic converters.

When the engine is started with the catalyst temperature too low to reach the light-off temperature, this functionality will ask for catalyst heating. Catalyst heating will be accelerated as much as possible by the FC. The catalyst heating is computed during the start phase in dependency on the engine temperature, intake air temperature, shut off time, and altitude because the measured catalyst temperature is unavailable and the modelled temperature is erroneous.

The ambient temperature, intake air temperature, and engine start temperature are approximately equal when the engine is first chilly. When the cold start heating request is set, the catalyst's light-off temperature is then gradually attained based on the catalyst ageing factor. In the meantime, a ratio between the required value for integrated air mass and the integrated air mass quality at engine start is determined. The catalyst heating is started once this ratio exceeds a predetermined threshold, failing which the catalyst heating for cold start scenarios is stopped.

In order to heat up the catalyst during long coasting phases, GPF regeneration requests, and when dew point end is not reached, catalyst heating is necessary. Figure 1 illustrates the algorithm for the controller's operation for catalyst heating owing to cold start and catalyst warming.

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Long coasting conditions could be challenging for a vehicle to handle. Therefore, using an engine dyno, which can replicate a very long coasting phase, is advised. Here, we must check to make sure there are no defects caused by engine temperature. The catalyst is warmed as soon as the catalyst heating request is set to true and all necessary operating parameters are satisfied. Time should be provided to the car in the event that the dew point is high enough to soak, as a cold start is necessary and there shouldn't be any engine temperature or air pressure-related issues.

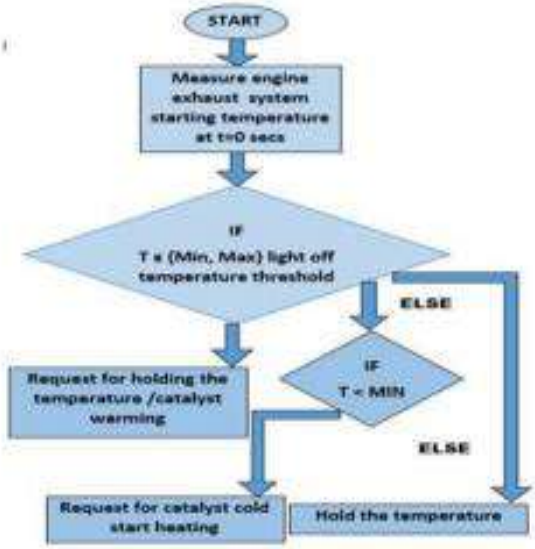

Fig.1 Algorithm for operation of controller for catalyst heating due to cold start and catalyst heating

IV. Methods of Thermal Management in Gasoline Based Engine Vehicles

The purpose of thermal management is to reach a sufficiently high temperature of the catalysts as fast as possible and maintain in order to assure an optimal conversion of exhaust emissions.

Depending on the specific system configuration, boundary conditions/restrictions and specific calibration of the heat up strategy a number of different heat up measures are possible. Some main heat up measures are described below:

- Late ignition timing to increase the exhaust temperature and exhaust mass flow
- Request heat up operation mode with adapted injection pattern
- Increased idle speed to increase the exhaust mass flow over the catalyst
- Rich combustion lambda set point in combination with secondary air to enable exotherm reaction on catalyst
- Request cylinder lambda split strategy (e.g. 2 cylinder rich / 2 cylinder lean) to enable exotherm reaction on catalyst
- Disable fuel cut-off in case of low temperatures to avoid further cooling down.

The heating strategy determines the heating demand and takes into account technical/physical restrictions as well as optimization criteria among different emission components. In case of insufficient catalyst temperatures e.g. cooling out or interrupted heating, a reactivation of the heat up measures has to be assured. The thermal state of the exhaust catalysts directly influences exhaust emissions and indirectly fuel consumption/ CO2 emission.

Adjusting the operational engine settings can quickly reach high exhaust temperatures, but it causes the engine to diverge from ideal operating conditions. The subsections explains the each of the strategies for thermal management.

4.1 Ignition Retardation

Retarded ignition time is a typical and successful way to raise exhaust temperature without the need of additional technologies [63]. However, it limits constant volume combustion and results in more unburned fuel in the exhaust pipe, resulting in decreased engine power and efficiency. When ignition occurs earlier in the cycle, more amount of heat is released around the top dead center. Thus, advanced ignition timings will result in higher peak cylinder pressure and temperature. With increase in combustion temperature NOx formation will also increase. Thus, results higher NO emissions with advanced ignition timing. Knock and engine damage problem can also occur. Whereas if the ignition timing is retarded more burning takes place during the expansion stroke that results in lower peak combustion pressure. But the exhaust gas temperature increases which reduces the engine efficiency. Also, higher oxidation rate of HC and CO are obtained with higher exhaust temperature through retarded ignition timing. Thus, low HC emissions are obtained with retarded ignition timings. Figure 2 depicts the algorithm for the controller's work flow for the worsening of engine efficiency and ignition retardation.

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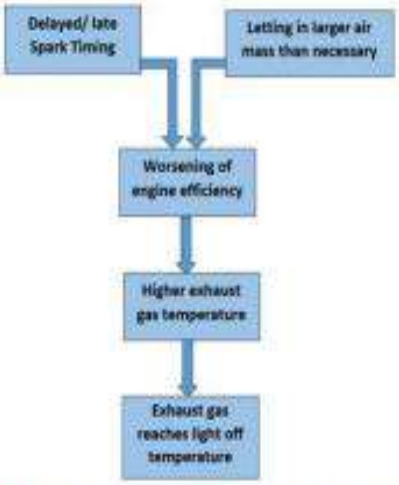

Fig 2. Algorithm for work flow for controller for worsening of engine efficiency and ignition retardation.

4.2 Multiple Injection

The multiple injection approach is used in another way for boosting the exhaust gas temperature. The combustion properties of successive injection operations raise the temperature of the exhaust gas, resulting in a totally homogenous operation. The split injection system also improves ignition stability and allows for a certain late ignition angle to heat the catalytic converter.

A complete fuel quantity that is to be given to the cylinder throughout an operating cycle is provided to the combustion chamber in at least two injection phases in multiple injection operation. Initially, a homogeneous injection occurs during the intake stroke of the cylinder, resulting in virtually homogenous distribution of the injected fuel quantity in the combustion chamber at a later ignition time. Then, during a subsequent combustion stroke, a second late injection called stratified injection is done, resulting in the so-called stratified charge, in which the injected fuel is concentrated in the cylinder in the region near the spark plug.

A multiple injection operation is a hybrid of stratified charging and homogeneous charge. The combustion properties of these operations cause an increase in exhaust gas temperature as compared to a strictly homogeneous operation, allowing for a later ignition angle. Because of the rich mixture around the spark plug, a reliable ignition for lean lambda summing is possible. As a result, both ignition retardation and multiple injection can be usefully coupled.

4.3 Lambda Split

Another heating method is to alter the air-fuel ratio of different cylinders in opposing directions, a technique known as lambda split. Several cylinders in this approach are run with a mixture richer than the total lambda, while others are operated with a leaner mixture. In comparison to lean mode, combustion in the cylinder operating in rich mode is incomplete. The non-combusted components are subsequently exothermally transformed in the downstream catalytic converter with the leftover oxygen fraction of the lean operating cylinder, heating the catalytic converter.

With this lambda split method, a large amount of chemical energy can be introduced into the catalytic converter system, heating up the catalytic converter through exothermal catalytic conversion of the exhaust gas components that were not converted during the engine's non-stoichiometric combustion process. As a result, during the heat up phase, the lambda value should preferably be controlled to at least a stoichiometric value of =1. If a catalytic converter positioned far from the engine has to be heated fast, this approach of lambda detuning is useful.

4.4 Torque Reserve

Torque loss due by thermal heating may be compensated for by increasing the amount of air and fuel. Increasing the air charge while changing the ignition to retard to compensate for the extra air can compensate for torque loss. Torque control is separated into two categories: air system torque and ignition system torque. Torque reserve is a feature that ensures a torque range that may be modified by ignition timing without affecting real torque. As a result, the torque reserve is applied to the air system necessary torque rather than the ignition system required torque.

4.5 Increase in Idle Speed for Catalyst Heating

Idle functioning of an automobile engine necessitates particular care. In idle mode, there is no throttle input from the driver via the accelerator pedal. To maintain a constant idle angular speed, the engine must provide exactly the torque necessary to balance all applied load torques from the gearbox and any accessories, as well as internal friction and pumping torques. Certain load torques are caused by driver activity. Certain additional load torques, however, occur in the absence of a direct driving order. The mass flow rate of intake air determines the torque generated by the engine at idle, as it does in all engine operating phases. While the engine is completely warmed, the electronic fuel control regulates fuel flow to maintain stoichiometry and may momentarily

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regulate fuel to slightly richer than stoichiometry during cold starts. Normally, when the engine is idle, the ECU is designed to keep the engine running at a constant RPM regardless of load. This is accomplished by modulating mass air flow in response to the driver's throttle order. The air flow necessary to maintain the correct idle RPM must enter the engine through the throttle assembly at a slight but non-zero angle.

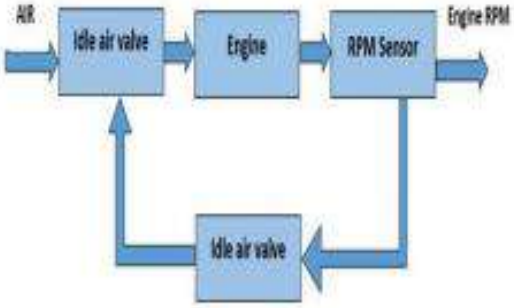

Fig.3 Algorithm for controller for idle speed and camshaft adjustment

Alternatively, some engines have an air tunnel that bypasses the throttle plate. An actuator is necessary for either way to allow the electronic engine control system to manage the idle mass air flow.

4.6 Exhaust Camshaft Adjustment

Exhaust camshaft modification can contribute to increased heat flow even further. The procedure of opening the exhaust valve as soon as feasible pauses the delayed combustion and thereby reduces the mechanical effort created even further. The corresponding amount of energy is accessible as heat in the exhaust gas.

The automobile industry has commonly used variable valve timing (VVT) to increase engine performance. VVT is another option for increasing exhaust temperature during cold start. In reality, late intake valve opening (IVO) allows less new air into the cylinders, resulting in a richer air/fuel combination in combustion engines, whereas early exhaust valve opening (EVO) limits exhaust expansion and raises exhaust temperature. These two actions result in post-oxidation and rapid catalyst light-off. Figure 3 depicts the controller's algorithm for controlling idle speed and camshaft adjustment.

Thus, executing this technique while taking these parameters into account can increase the catalyst heating characteristics efficiently, resulting in a reduction in exhaust emissions.

V. WORK ENVIRONMENT

Advanced Simulation and Control Engineering Tool is referred to as ASCET. It is a multifaceted and adaptable product family that offers an original approach to the functional and software design of contemporary automotive embedded systems. With a fresh take on modelling, code generation, and simulation, ASCET supports each step of the development process, enabling improved quality, quicker innovation cycles, and lower costs. Working of ASCET is depicted in Figure 4.

A tool for creating software for embedded systems that uses both graphical models and textual programming notations is called ETAS ASCET. The proposed function models will be converted into extremely efficient and secure embedded C-Code for AUTOSAR (Automotive Open System Architecture) applications by the ASCET Code Generator. The ASCET has been created primarily to handle the difficulties in software development for sectors where goods must be produced in large quantities, at a low cost, in compliance with industry standards, and without any flaws.

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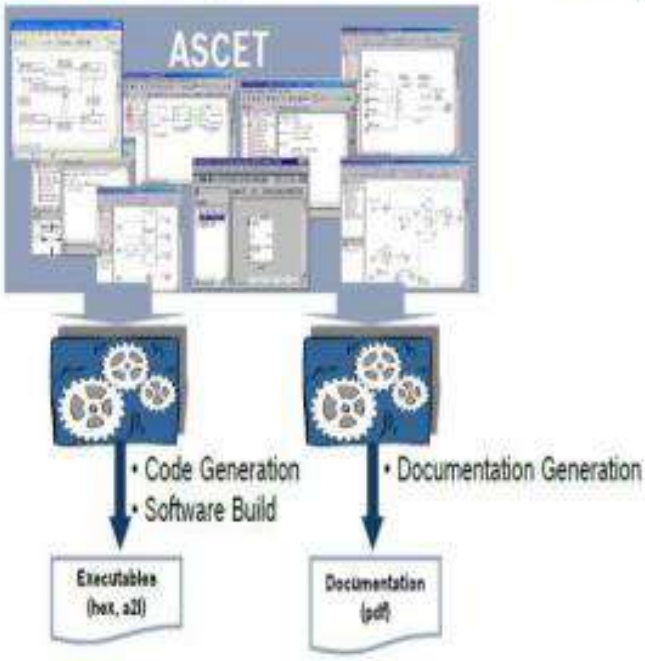

Fig.4 Working of ASCET tool

The ASCET tool enables software developers to create embedded software that is high performing, low overhead, simple to maintain, secure, and safe. High levels of automation enable productive and safe workplaces.

The ASCET tool for Automotive Software Development has the following features:

- Safe - Automatic introduction of defensive code, TUV-certified code generation using ISO26262 and IEC61508, and MISRA-C:2012 compliance
- Used for powertrain, driver assistance, battery management, brake systems (such ABS, ESP). ASCET-generated code powers the 450+ million ECUs in use today.
- The 450+ million ECUs in use today are powered by ASCET-generated code, which is used for brake systems (such as ABS, ESP), driver assistance, battery management, and powertrain.
- Quick and effective - Real-time static analysis for immediate feedback, quicker code generation
- A variety of testing alternatives, including unit testing, PC-based open-loop simulation, closed-loop simulation, and rapid prototyping
- Embedded Software Development Language (ESDL), which has an abstract data type, easy-to-understand syntax, and object-oriented encapsulation

Testing is an examination that aims to reveal details regarding a software product's quality. Executing a software system or component is part of testing. Depending on the level of code knowledge, or when the code is known and when it is unknown, there are many forms of testing.

In addition, there are many types of testing based on the complexity of the testing code, including system testing, which involves testing multiple functional components, and integrity testing, which is done whenever a new component is added to the system. When a hardware component is incorporated in the testing process, we use hardware testing. When we test software components, we use software testing. TPT is a tool for model-based testing that is used for automated embedded system testing, particularly for testing control systems. Applications include:

- PC based testing
- Open and closed loop tests
- Test in vehicle

TPT is certified to do automated tests in vehicles in accordance with ISO 26262 standards. Signal time intervals are used by TPT. The following four test activities are covered by TPT:

- Case modelling
- Execution in different environments
- Result analysis
- Documentation

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Test cases for TPT are built independent of how it runs. Due to the so-called Virtual Machine concept, the test cases can be run in nearly any environment. TPT is a comprehensive tool that may be used for all testing phases of development, including system testing, regression testing, integration testing, and unit test.

The exhaust system was initially designed as a simple duct system with the intention to safe route the toxic exhaust gas emissions from our car into harmless gases to the environment at the same time providing attenuation of noise made by the engine during combustion. Today, over the years the responsibility of exhaust system has grown. Modern exhaust systems are an integral part of combustion and pollution control thereby reducing noise, minimize harmful emissions and even give assistance in increasing fuel economy, power and hence the overall drivability. The primary components of the exhaust system work together to expel exhaust, reduce noise and assist smoother running of the operating parts. Although the emission control systems may vary based on the manufacturers and the vehicles, they all are designed to meet the same goal and they work on the same principle. The primary design consideration of an exhaust system include:

- Minimizing the gas flow resistance and confine it to specified range depending on the engine model to achieve maximum efficiency.
- Suppressing the exhaust noise to meet the automobile regulations and requirements.
- Providing sufficient clearance between exhaust system components and engine components so as to minimize the impact of high exhaust temperature.
- Ensuring that the system does not overstress engine components with excess weight as overstressing can shorten the component life.
- Ensuring that the exhaust components are able to reject heat energy as intended.

VI. RESULTS AND DISCUSSION

The TPT report provides a summary of all tests carried out. It also shows which test cases fail. The signal viewer allows to view each signal as it is displayed in the figures below. Figure 5 shows a graph of an engine in operation. Figure 6 displays a graph of time as a function of engine speed. Figure 7 depicts a graph of time versus catalyst brick temperatures. Figure 8 depicts a graph of time versus the catalyst's maximum temperature. Figure 9 shows a graph in which time is plotted against the catalyst's maximum temperature. Figure 10 displays a graph of the time v/s signal for catalyst heating brought on by a cold start. A graph displaying the catalyst heating's time v/s signal Figure 11 depicts the graph of catalyst warming. Figure 12 depicts the graph of time versus heating mode, Figure 13 depicts the graph of controller output for air charge control actors, Figure 14 depicts the graph of controller output for idle speed, and Figure 15 depicts the graph of controller output for lambda coordination. Figure 16 displays the output graph for the controller used to set the maximum torque during idle speed.

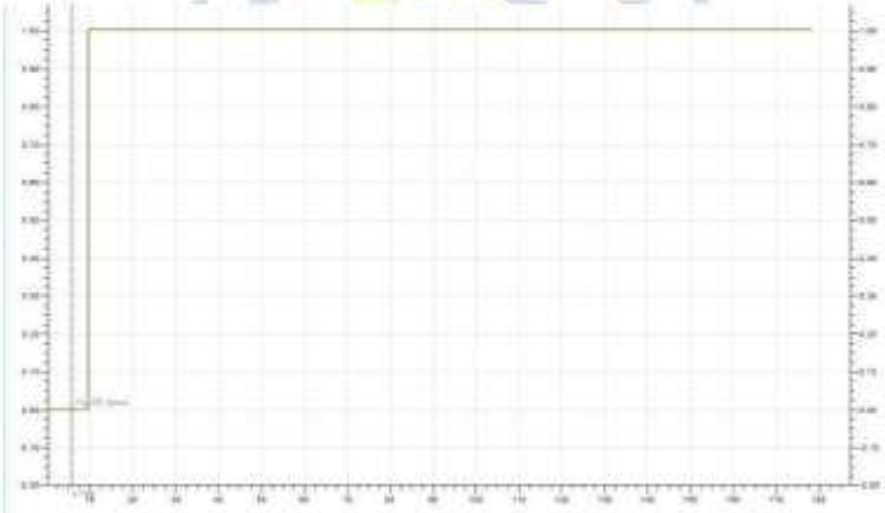

Fig.5 Graph showing engine in running mode

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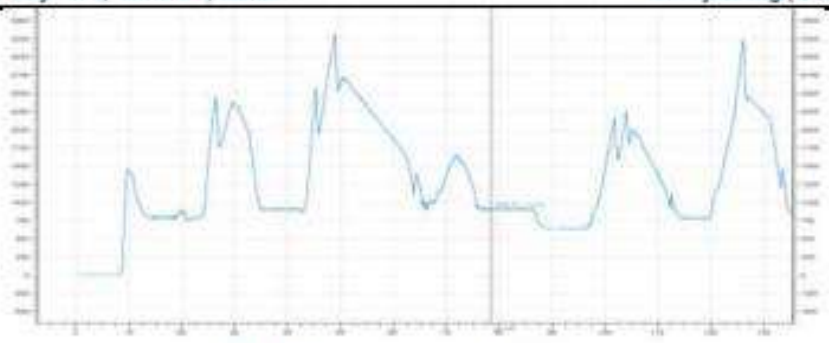

Fig.6 Graph showing time v/s engine speed

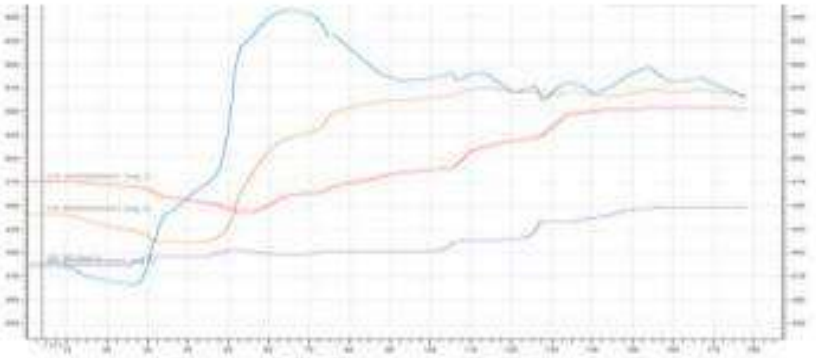

Fig.7 Graph showing time v/s catalyst brick temperatures

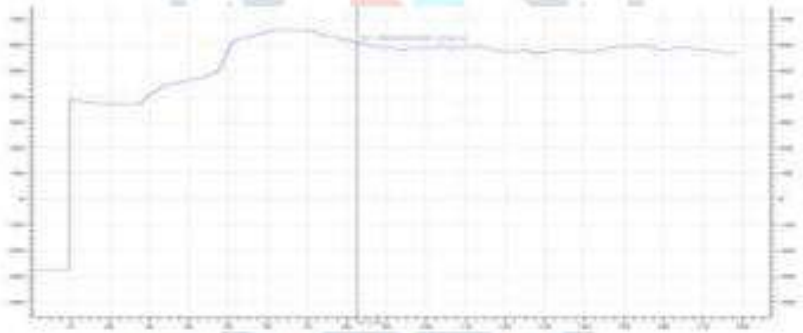

Fig.8 Graph showing time v/s maximum temperature of catalyst

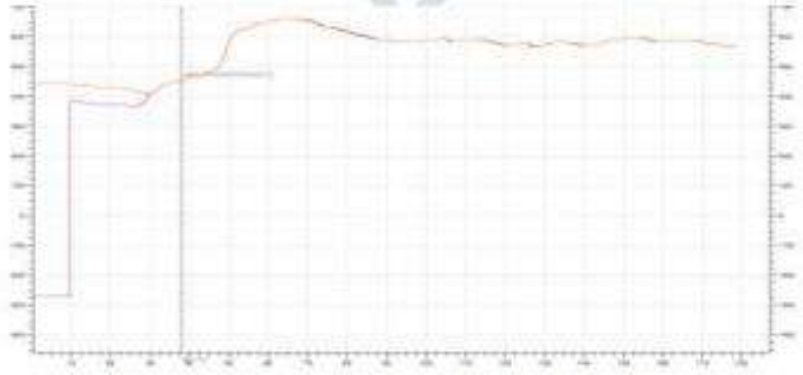

Fig.9 Graph showing time v/s selection of maximum temperature of catalyst

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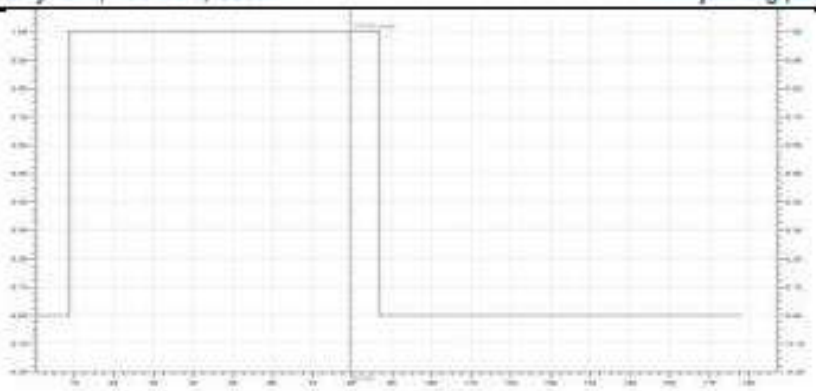

Fig.10 Graph showing time v/s signal for catalyst heating due to cold start

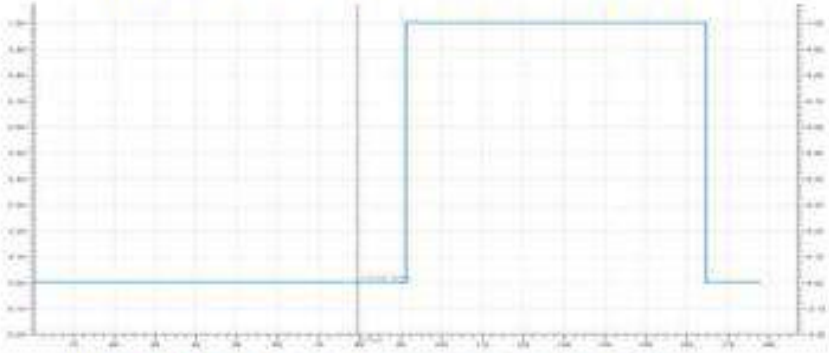

Fig.11 Graph showing time v/s signal for catalyst heating due to catalyst warming

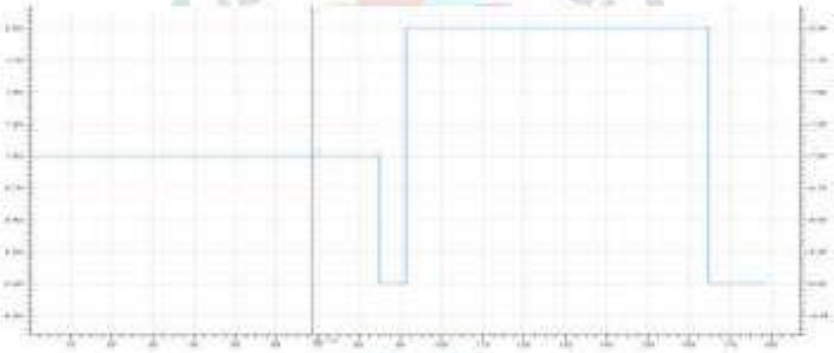

Fig.12 Graph showing time v/s heating mode

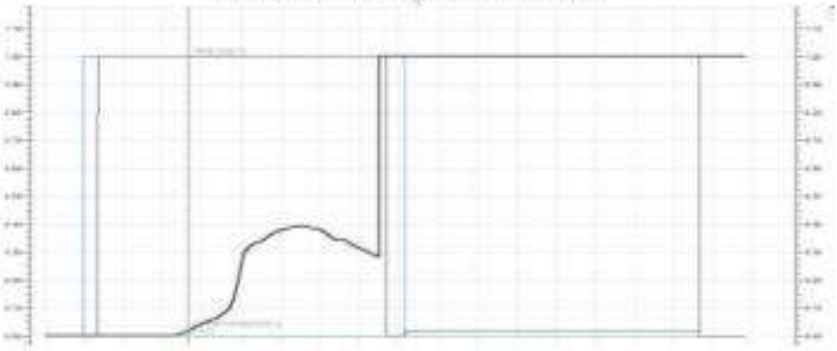

Fig.13 Graph output for controller for air charge control actors

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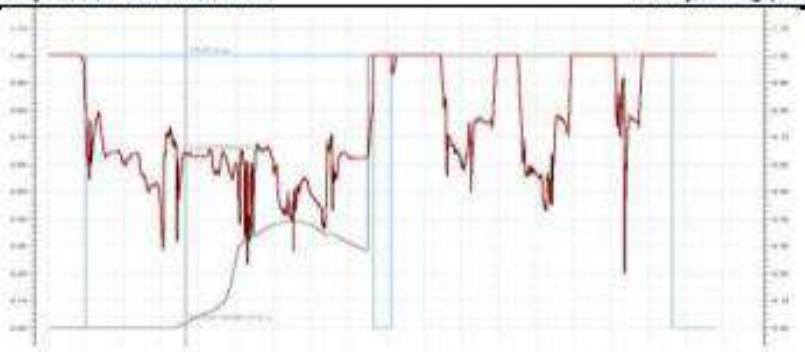

Fig.14 Graph output for controller for idle speed

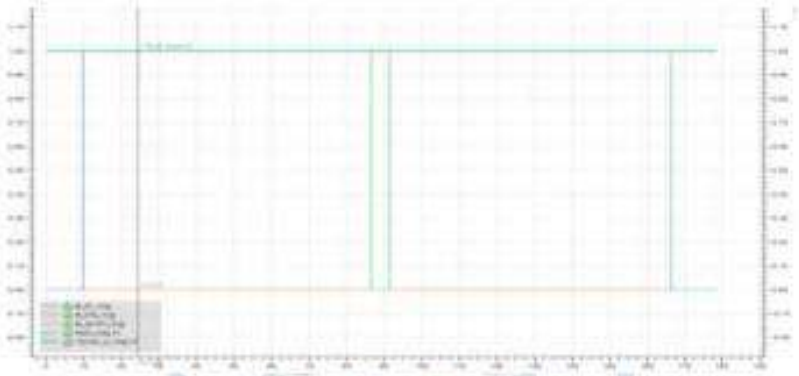

Fig.15 Graph output for controller for lambda coordination

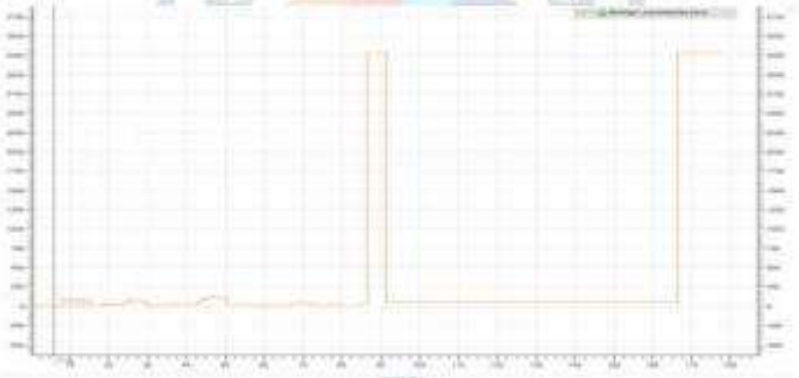

Fig.16 Graph output for controller for setting maximum torque during idle speed

VII. CONCLUSION

Automobile emissions are linked to environmental and health risks, prompting the establishment of severe emission regulating regulations. Over the last decade, our country has taken a variety of steps to reduce emissions from our automobile fleet. For engines functioning normally, significant reductions in exhaust emissions have already been realized. However, such emissions are still considerable during cold start and warm up due to important engine-out emissions and poor catalyst efficiency due to low cylinder and exhaust temperatures.

Exhaust gas temperature is a characteristic that has proven crucial in determining engine performance. This study examined thermal management strategies for quick catalyst light-off in order to reduce cold stat and warm up emissions, as well as component protection approaches for automotive emission reduction. Thermal management, in contrast to earlier techniques, resolves the trade-off between energy consumption and pollution reduction by preheating the catalytic converter.

Electronic engine control is important in emission control. The minimal emissions achieved by current engines would not be achievable without electronic control. The purpose of an engine management system in terms of emissions is to supply the needed quantity of air, fuel, and EGR at the required temperature and pressure in the required time. This control is carried out throughout the engine's lifespan, correcting for wear and degradation.

A thorough examination of the different functional components of the exhaust temperature management package was conducted, and a few functional components were adjusted to fulfil the emission limits specified by the client. The fuel and fuel system, the engine and its combustion system, sensors, and the design and position of the catalyst and filter all work together with the electronic control system to reduce emissions to the greatest extent possible. Developing an optimal system will therefore improve engine exhaust emissions for better adaptability to various exhaust laws, encouraging improved environmental circumstances and health advantages.

Until recently, a carbon-neutral combustion engine was the stuff of science fiction. The principle is found in synthetic fuels, often known as carbon-neutral fuels, whose manufacturing process collects CO2. As a result, greenhouse gases become a raw material from which gasoline, diesel, and other fuels are produced and replacement natural gas may be produced using sustainable energy sources. Synthetic fuels will make gasoline and diesel vehicles carbon-neutral, and therefore a substantial contribution to preventing global warming. This might soon become a reality around the year 2025.

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CHAPTER 1 INTRODUCTION Nowadays, people utilise cars a lot because they have more mobility, which raises their standard of living. Economic growth is significantly impacted by the constant transportation of more and more people and things between different locations. India, the second-largest nation in the world by population, has a diverse economy, one of which is dominated by the transportation industry. According to statistics, the number of vehicles in our nation has increased by more than 240 percent in the last ten years. Over the next 20 years, it is anticipated that this will continue to grow at a similar rate. There are adverse consequences associated with this massive pace of automobiles. These include severe environmental risks like climate change, pollution, global warming, decreased crop yields, and threats to living things as a result of an increased dependency on fossil fuels and increased pollution emissions, which may eventually lead to an overall ecological imbalance [1]–[4]. All societal growth sectors will have better socioeconomic opportunities thanks to increased mobility. Therefore, it is crucial to direct this increase in a way that would reduce the negative effects of automotive pollution. As a result, pollution regulations for cars are put up. In India, the initial emission rules went into effect in 1989. The mass emission restrictions for both gasoline and diesel automobiles during the 1990s eventually took the place of these idle emission limitations. The national adoption of these emission limits and deployment of the best emission control techniques will have a substantial influence on the environment, the global economy, global warming, and public health. Conventional pollutants like Carbon Monoxide (CO), Nitrogen Oxides (NOx), Particulate Matter (PM), Hydrocarbons (HC), and other greenhouse gases like Carbon Dioxide (CO2), Methane (CH4), and others make up the majority of vehicular emissions from Internal Combustion engines. The national adoption of Bharat V/VI standards has the potential to drastically reduce vehicle emissions by 86 percent. Thus, without even mentioning the terrible load of air pollution, the nation is able to fully benefit from the fuel savings provided by the diesel technology [5]-[9]. To obtain high performance and minimal exhaust emissions, it is strongly advised to create engine control systems. An embedded mixed signal system called the engine management system communicates with the engine via a variety of sensors and actuators. It organises, prioritises, and then puts all the needs for the engine into practise. The control strategies are meant to regulate the air-fuel ratio, the ignition, the electronic throttle, the idle speed, the location of the accelerator, etc. By carefully planning and implementing the control system, the engine can produce more power [10]–[14]. There is a lot of money invested in the

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Major Project: Phase-II Report

on

"DEVELOPMENT OF PLC LOGIC & SCADA SYSTEM FOR CHILLER PLANT AUTOMATION"

18MPE41

Submitted by
MEGHNA SANGEWAR
USN: 1RV20EPE06

Under the Guidance

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Submitted in partial fulfillment for the award of degree

of

MASTER OF TECHNOLOGY

in

POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

2021-22

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Certified that the project work titled **"Development of PLC Logic & SCADA System for Chiller Plant Automation"** carried out by **Meghna Sangewar, USN: 1RV20EPE06**, a bonafide student, submitted in partial fulfillment for the award of **Master of Technology** in **Power Electronics** of **RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi,** during the year **2021-22**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

Dr. Rudranna Nandihalli Professor and HOD (Retd.), Department of Electrical & Electronics Engineering, RVCE, Bengaluru –59	**Dr. S G Srivani** Head of Department, Department of Electrical & Electronics Engineering, RVCE, Bengaluru–59	**Dr. K. N. Subramanya** Principal, RVCE, Bengaluru–59

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DECLARATION

I, Meghna Sangewar, student of fourth semester M.Tech in **Power Electronics, Department of Electrical & Electronics Engineering,** RV College of Engineering®, Bengaluru, declare that the project titled **"Development of PLC Logic & SCADA System for Chiller Plant Automation",** has been carried out by me. It has been submitted in partial fulfilment for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

Date of Submission: 18/07/2022

Meghna.

Signature of the Student

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This is to certify that **MEGHNA SANGEWAR – 1RV20EPE06** student of **RV College of Engineering, Bengaluru**, has completed the project work entitled **"Development of PLC Logic & SCADA System for Chiller Plant Automation"** under the guidance of Mr. Ragavendiran. L, Operations Manager, Closoft Technologies Pvt. Ltd. from September, 2021 to June, 2022.

During the period of her internship programme with us she was found Punctual, Hardworking and Inquisitive.

We wish her every Success in Life.

For, **CLOSOFT TECHNOLOGIES PVT. LTD.**

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DIRECTOR

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I would like to express my sincere gratitude to my guide, **Dr. Rudranna Nandihalli**, Professor and Head of Department (Retired), department of Electrical & Electronics Engineering, for all his guidance and valuable advice throughout the progress. He has stimulated interest and inspired for doing the major project.

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ABSTRACT

Today, PLC applications have a significant impact on process engineering. PLC has entered this field because of its software and hardware security, internal security and programming language solutions. One such application of PLC based automation is in the field of Heating, Ventilation, and Air Conditioning (HVAC) systems. HVAC systems frequently consume the most energy in commercial buildings. More than 60% of the energy used in a typical office building is produced by the HVAC system. In both commercial and home settings, chiller units have become a necessity. A typical chiller plant consists of a number of coolers, cooling towers, water pumps, and other related components. It is a sizable, intricate, and interconnected system. Therefore, it is crucial to increase the energy efficiency of the fans, compressors, and pumps in the HVAC system, this is possible to achieve by a variety of methods. In the past and even now, chiller plant operations have been frequently governed by rules. For instance, the coolant supply temperature is constant, and there are only as many active chillers as necessary to provide the cooling requirements. The relationship between the chiller cooling load and the chiller/condenser supply temperature is nonlinear. Due to the chillers' poor effectiveness at maintaining a steady supply temperature, energy is squandered, and occasionally two chillers use less energy than one. Therefore, chiller plant optimization is required for energy savings.

The optimization and control of chiller plant requires adjustments of multiple set points, primarily temperatures, and flow rates. In this work, PLC and SCADA have been used to monitor and operate the Chiller Plant for a building's more noticeable operation. The IEC standard, enables the programmer to use multiple programming languages in the same PLC, it is the main benefit of using PLC-based automation because it eliminates the need for proprietary implementation and allows different tasks to be implemented effectively using the most appropriate language. Hence for recommissioning, troubleshooting and rescheduling is no challenge.

PLC has been utilized as hardware at the remote end to monitor and read field instruments for the predefined temperatures, and other parameters as well as to control the Chiller equipment in accordance with predetermined instructions. The many chiller units in the plant have been monitored and controlled remotely using the ladder logic created for programming PLC S7-400H. By creating Graphical User Interfaces (GUI) utilizing TIA portal software, SCADA/HMI are operated remotely.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Meghna S, Dr. Rudranna N, and Omkaraiah H M, "Development of PLC Logic and SCADA System for Chiller Plant Automation", *Journal of Emerging Technologies and Innovative Research (JETIR),* Volume 9, Issue 6, June 2022

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GLOSSARY

CPM	:	Chiller Plant Manager
DDC	:	Direct Digital Control
FBD	:	Function Block Diagram
GUI	:	Graphical User Interface
HVAC	:	Heating Ventilation Air Conditioning
IEC	:	International Electrotechnical Commission
IL	:	Instruction List
LD	:	Ladder Diagram
PLC	:	Programmable Logic Controllers
RLL	:	Relay Ladder Logic
SCADA	:	Supervisory Control and Data Acquisition
ST	:	Structured Text
TIA	:	Totally Integrated Application
UPS	:	Uninterruptable Power Supply
VFD	:	Variable Frequency Drive

Chapter 1

INTRODUCTION

Buildings are responsible for over 40% of the nation's electricity consumption and 30% of the nation's greenhouse gas emissions. Commercial real estate has always been classified as a designated consumers and it is imperative for estate operators to adhere minimum building energy consumption norms. Energy used in buildings is used for lighting, comfort-fanning/air circulation, conditioning space cooling and heating, elevators, and water pumps [1]-[2].

Heating, Ventilation, and Air Conditioning (HVAC) systems frequently consume the most energy in commercial buildings. More than 60% of the energy used in a typical office building is produced by the HVAC system [2]. In both household and commercial settings, air conditioners have become a crucial necessity. The current air conditioning system utilised in colleges and businesses uses more electricity. Each individual air conditioner in a building at a school or company needs a fan, a compressor, and refrigerant gas. Each block needs to have each of these components installed separately, this increases power consumption and causes maintenance issues. These drawbacks were overcome by using chiller plant, in both commercial and home settings, chiller units have become a necessity. Automating it is possible using Programable Logic Controller (PLC) and Supervisory Control and Data Acquisition (SCADA) [3]-[10].

The chiller plant element of HVAC systems is a central air-conditioning system for a building or group of buildings. Chiller plants are composed of numerous mechanical components. Through the distribution system, chilled air from the chiller is distributed throughout the entire structure. An air duct and fan make up the distribution system, that transports air to its location. The chiller plant system, comprises of chillers, pumps, cooling towers, and other electromechanical equipment, is the component that consumes the most energy [10]-[23].

Different kinds of control strategies are available to manage, control and monitor these chiller plants. PLC and SCADA are easily used as automation tool in Chiller plant. The HVAC control system uses a variety of instruments and sensors to collect data from the plant, such as temperature and pressure, and transmit it as an input to the controller. The controller then outputs a digital or analogue signal via a PLC based on predetermined control logic [24]-[33]. In order to direct and manage the necessary cooling area, PLC is finally used as hardware.

1.1 Overview

Air conditioners and Chiller Units have become an essential requirement in industrial and domestic environments. Industrial automation tools, on the other hand, offer a wide range of applications for controlling and monitoring machinery, power systems, vehicles, telecommunications systems, etc. By initiating an automation process, it improves the benefits by managing and controlling those plants [9].

PLC and SCADA are common automation tools in the HVAC industry. The IEC standard, enables the programmer to use multiple programming languages in the same PLC, is the primary benefit of using PLC-based automation because it eliminates the need for proprietary implementation and allows for the efficient implementation of various tasks using the most appropriate language. Hence for recommissioning, troubleshooting and rescheduling is no challenge [10].

In this work, PLC and SCADA are used to monitor and manage the Chiller Plant for a building's more noticeable operation. PLC is utilised as hardware at the remote end to monitor and read field instruments for the predetermined temperatures, pressures, and other parameters as well as to control the Chiller equipment in accordance with predetermined instructions. The ladder logic created for PLC S7 400H programming is deployed for remote monitoring and control of the plant's numerous chiller units. By creating Graphical User Interfaces (GUI) utilising TIA portal software, SCADA/HMI may be operated remotely.

1.2 Specific Details

Air Cooled Chillers are used for the CPM, chillers are allocated on the roof of the building and the pumps room. Plants produce and supply 5.5 ℃ chilled water to the connected buildings and the design return temperature of the chilled water is 12.2 ℃. Air Cooled Chillers plant classified with the 15 Chillers, 11 Primary pumps, 5 Secondary pumps, BTU meter, Modulating valve, Pressurization Unit, and Chemical treatment unit.

The Simatic S7-400H controller has been used to automate the process with the rated supply of 24V DC, achieved by implementation of SMPS for the input voltage of 230V. The input output configuration pins available are 140 AI, 101 DI, 37 AO, and 31 DO. The IO points is connected to the controller through additional remote IO modules. The communication has been established between electrical panel with controller and the local SCADA i.e., HMI using 2 Ethernet switch.

1.3 Literature Review

All businesses and sectors are embracing the global trend of industrial automation. Numerous technologies are used in automation, including wireless applications, robots, telemetry, process calibration, sensors, control systems, and professional systems. Control systems are used in automation to operate many devices with little or no human involvement [1]-[4].

LabVIEW, PLC, Python, and other development tools are frequently used in automation. Because it is dependable, simple to use, and more affordable than other types of automation, the PLC is employed in the majority of applications [4].

The concept of PLC originated over a hundred years that transformed the industrial sector. The application of PLC is not just restricted to industries but also in different segments such as metro automation, including inputs from systems such as HVAC, Lifts Escalators, UPS and Fire Alarm and Detection System etc. this has been also set at Taipei City Mass Rapid Transit [5]-[12].

It is suggested that PLCs be used to manage the energy used by different loads in residential and commercial facilities. The increased use of electrical appliances and technological systems in modern homes and businesses necessitates more controls. The entire distributed control system has a hierarchical architecture, and PLCs use common building automation communication protocols to communicate with the energy system and controls [13].

A typical chiller plant consists of a number of coolers, cooling towers, water pumps, and additional components. It is a big, intricate, and linked system (e.g., refrigerator containing a condenser, evaporator, and compressor, etc.). Through efficient refrigeration compression cycles, chiller plants cool buildings [14]. Compressors, pumps, and fans are only a few of the chillers' motor-driven HVAC system components. Therefore, it is crucial to increase the energy efficiency of the fans, compressors, and pumps in the HVAC system, that is achieved in a variety of ways [15].

In the past, chiller plant operations were frequently governed by rules. For instance, the coolant supply temperature is constant, and there are only as many active chillers as necessary to provide the cooling requirements. The relationship between the chiller cooling load and the chiller/condenser supply temperature is nonlinear. Due to the chillers' poor effectiveness at maintaining a steady supply temperature, energy is squandered, and occasionally two chillers use less energy than one. Consequently, optimising the chiller plant is essential for energy savings [14].

Multiple set points, primarily temperatures and flow rates, are adjusted for the chiller plant to be optimised and controlled. It is necessary to comprehend specific system components (pumps, control valves, etc.), use sensors (temperature, flow, differential pressure, etc.), and use appropriate control algorithms to measure, verify, and control the operation of the chiller plant. [14]-[17].

Today, these set points are kept unchanged or applied by simple rules of reset. This usually happens using a PLC. The whole process of this framework is such as opening and closing the valve, improving the VFD-cantered chiller plants and compressor motor and the level of fluid that regulates the tank using sensors [18]-[20]. In [23] all the hardware components being used are discussed and its control in the system are shown, as well as a program for Siemens PLC has been developed using TIA portal.

A supervisory MPC technique that incorporates the closed loop dynamics of the heating and ventilation subsystems is developed [21] in order to further enhance control performance and building energy efficiency. Another method is optimising a building that is already in use by changing the information in the existing controller's Building Information Model (BIM), has been used to construct control methods for the performance [22].

PLC logic design has been covered in [24]-[33] for different process applications. Studying documents like the Control Philosophy, Logic Flow Chart, IO list, specification, and architecture is the first step in the process. According to the aforementioned documents, the creation of the PLC process starts. After then, the evaluation of the controller's performance and verification of its safety standards starts with the inspection and authorization. A Similar approach has been used for automation of a chiller and ladder logic have been developed for controlling the pumps and heat exchanger system. Based on this methodology this project work has been carried out.

1.4 Motivation

Modern architecture is a multi-vector power system with observable outcomes, numerous challenges, and operational/control objectives. Control issues are a serious issue in the real estate sector. Due to the low efficiency of the chillers, energy is lost, and occasionally, the energy consumption of two chillers is less than that of one chiller. Therefore, optimising the chiller plant is essential for energy savings, and doing so is made easier by automating the procedure using PLCs.

Hence the main motivation is to maximize the process efficiency, optimize, avoiding the operator alienation and keep the plant safe through automated system with PLC logic and HMI/SCADA screen to monitor and control the process.

1.5 Problem Definition

In accordance with the motivation the problem statement of the project is to design system architecture and develop PLC Logic & SCADA system for chiller plant automation.

1.6 Objectives

The main objective of the project is,

- To efficiently automate the Chiller system of the building by designing system architecture.
- To develop PLC logic for the control of different functional parts of chiller system.
- To develop SCADA/HMI graphics as per the control philosophy.
- To develop PLC & SCADA, using TIA portal and WinCC software- Siemens.

1.7 Organization of Report

The report is organised in the chapter wise as mentioned:

Chapter 1: Introduction

Chapter 1 deals with the introduction of the project and relevant literature survey. It also includes objectives of the project, motivation, problem statement and organization of the report.

Chapter 2: Chiller Plant Automation

Discusses basic concepts of Control system and automaton of CPM, Programmable logic converters, Siemens S7 400H PLC and HMI TP1500

Chapter 3: Methodology and Block Diagram

This chapter consists of the methodology and the basic block diagram that is adopted in the automation of Chiller Plant**.**

Chapter 4: Specification and Design

Explains in detail the selection of controller, Inputs/Outputs used to configure the controller and I/O Modules. The specification of the Controller, IO Module is provided in the chapter along with System Architecture.

Chapter 5: Simulation Analysis and Hardware Implementation

Provides the Algorithm, IO Mapping, HW Configuration and Ladder Logic program developed for automation of Chiller Plant. The details of hardware implementation are also discussed.

Chapter 6: Results and Discussions

Discusses about the HMI results of the controller operation and hardware results for the same.

Chapter 7: Conclusion and Future Scope

Includes the overall conclusion drawn from the project and the future works that are possible to carried out, Followed by References consisting of list of papers referred for understanding and analyzing the project work.

Chapter 2

CHILLER PLANT AUTOMATION

The chapter explains about the Chiller Plants and its components, control system involved in Chiller Plant automation, Programmable logic controller, its basic system architecture and operation, and overview on SCADA/HMI.

2.1 Chiller Plant

Systems for heating, ventilation, and air conditioning control the comfort levels in a variety of indoor spaces. As a part of the HVAC system, a chiller unit is a centralised system that cools the air in a building or group of buildings and provides air conditioning. Over 35% of structures larger than 100,000 square feet use chillers, according to the Energy Star website of the federal government [6].

Despite the fact that chillers, or condensing units, perform the majority of the air-conditioning work, chiller plants are made up of several mechanical devices. In order to deliver chilled water to cool buildings through heat transfer, the chiller plant includes chillers, cooling towers, and primary as well as secondary pump subsystems, as depicted in Figure 2.1.

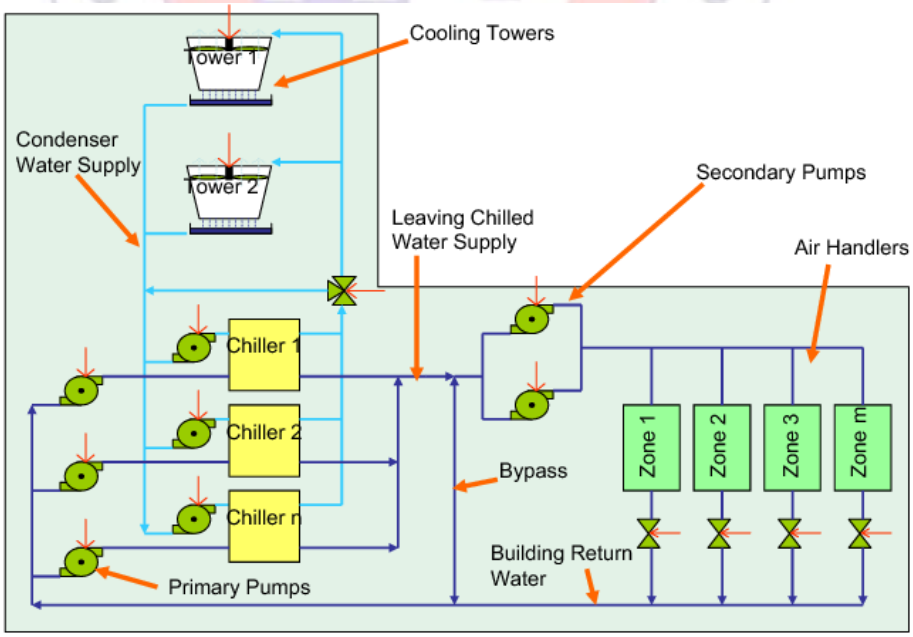


Figure 2.1 General diagram of Chiller Plant (HVAC System)

A distribution system distributes chilled air from the chiller throughout the entire structure. A metal duct that guides the air to its destination and a fan that blasts air make up the distribution

system. Today, many chiller units also have VFDs, this offer better control than simply switching a number of condensing units on and off. To minimise temperature disparities, cooling towers are also employed to cool the air before it enters the chiller.

2.2 General Control System in Chiller Plant

The control system for the chiller plant is made up of a variety of tools and sensors that gather information from the chiller plant, such as temperature and humidity, and feed it into the controller, then it produces a digital or analogue signal depending on established control logic. The plant contains temperature sensors and manually operated duct dampers for controlling the flow of air entering and exiting the building. Fresh air is brought into the plant by the supply air duct, hot air is collected by the return air duct, and hot air is sent outside by the outside duct. An air-cooling system consists of mechanical components like an exhaust fan, a cooling tower, and an air handling device. To maintain the proper temperature and humidity in the building, PLC controls plant equipment [5],[11]. Figure 2.2 depicts this system, it uses sensors placed area-by-area to read process parameters for monitoring.

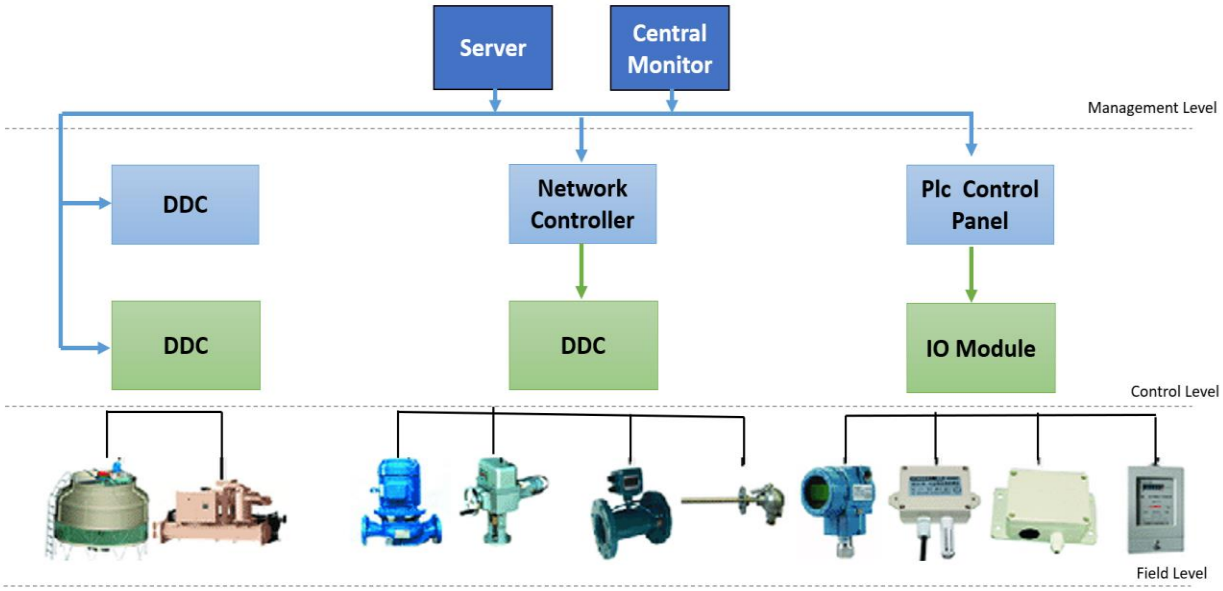


Figure 2.2 Control System in Chiller Plant

The term DDC (Direct Digital Control) refers to the automatic conception of reading sensory data, processing data on a digital domain, and intelligently managing actuators. DDC is a microcontroller-based system as a result; all components are located on a single chip and are digitally controlled via multiplexers and analog-to-digital data converters, as evidenced by the statistics. To modify the system using its own control language, various DDC architectural

developers have created a patented software. DDC technology presents a number of difficulties for the use, organisation, and coding of administrators [1].

A PLC is a small piece of hardware. It's made up of logic gates, a microcontroller, a basic CPU, and analog and digital interfaces. Each element is coded in any IEC languages, such as LD, ST, IL, or FBD, or a combination of languages. The fundamental benefit of the IEC standard for PLCs is that it allows programmers to utilise numerous programming languages in the same PLC, allowing diverse jobs to be implemented quickly using the most appropriate language. As a result, PLC-based control is appropriate for the project.

2.3 Programmable Logic Controllers

A Programmable Logic Controller, or PLC, is a robust computer used in industrial automation. PLCs are tools because they act as systems that store and execute control instructions when provided the necessary power [2]. For instance, the software might use logical arguments like "if button is pressed, open valve of pipe," etc.

The input interface, CPU, memory unit, and outgoing interface are the four fundamental parts of the PLC architecture depicted in Figure 2.3.

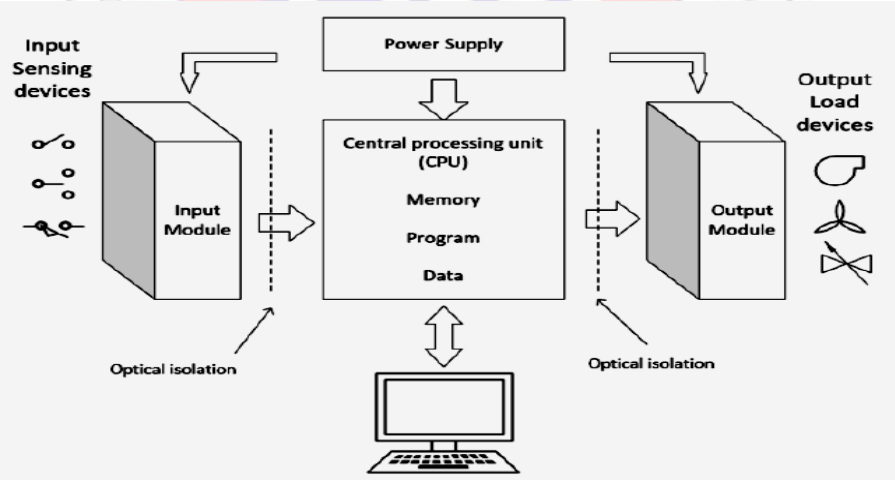


Figure 2.3 Structure of PLC

Depending on the inputs and outputs, a PLC monitors and record run-time data such as machine productivity or operating temperature, initiate and terminate processes automatically, generate alarms in the event of a machine failure, and do much more [8]. Practically any application benefits from the flexibility and dependability of PLCs as a control system.

PLCs have various features that set them apart from industrial PCs, microcontrollers, and other devices [3][4].

- I/O- The I/O module connects the PLC to the rest of the system, the CPU stores and executes programme data. These I/O modules feeds information to the CPU and cause specific outcomes. I/O is modules are digital and analogue. Sensors are one type of input device. Relays, lamps, valves, and actuators are examples of outputs in addition to switches and metres. PLC I/O are mixed and matched by users to create the ideal configuration for the application.
- Communications - Connections to various kinds of systems may be necessary in addition to PLC input and output devices. Users exports application data produced by a PLC, for instance, to a SCADA system that manages numerous connected devices.
- HMI - To communicate with the PLC in real time, need an HMI, or human machine interface. These operator interfaces are either big touch panels that resemble consumer electronics or straightforward text-based displays and keypads, but in both situations, users may view and input data into a PLC in real time.

Typically, PLC programmes are created on a computer before being downloaded to the controller. Ladder Logic or "C" programming is supported by the majority of PLC programming software [11]. A conventional programming language is ladder logic. uses logical "steps" that are read from left to right to simulate a design. Starting with a succession of inputs (contacts) leading to an input or output, each stage represents a distinct activity controlled by the PLC (coil). Ladder Logic is simpler to implement than many other programming languages due of its visual character.

2.3.1 Input/Output Module

Each PLC reads inputs from physical sensors like switches and encoders, interpret those signals, and operate physical controls like solenoids, valves, and motors.

An I/O or I/O function is the common name for this. Whereas modular (rack) PLCs employ external circuit boards or cards to provide programmable I/O capabilities, monolithic (brick) PLCs have a fixed number of built-in I/O functions. Both monolithic and modular PLCs are depicted in Figure 2.4.

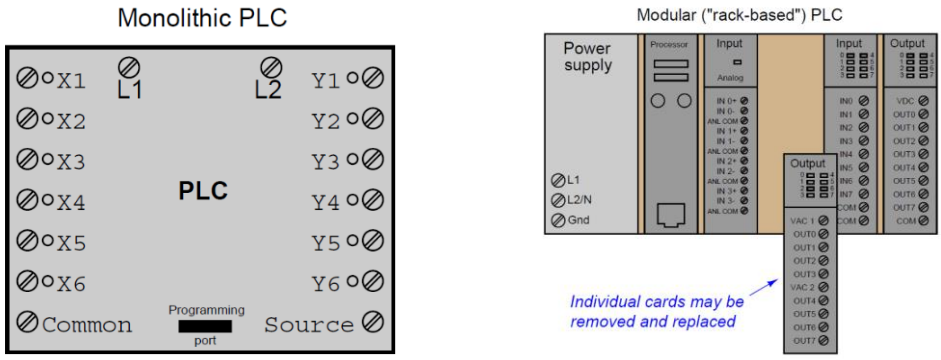


Figure 2.4 Monolithic and Modular PLC

Instead of monolithic PLC designs, pluggable I/O boards have a number of benefits. First and foremost, replacing individual I/O boards rather than the complete PLC is simple in the event of a breakdown. For customised applications, particular I/O boards are used, such as discrete cards for uses involving lots of on/off inputs and outputs or analogue cards for uses involving lots of 4 to 20 mA signals, etc.

A specific digital network, like the one in Figure 2.5, is typically used to connect the host PLC to remote I/O racks since it may physically traverse a considerable distance.

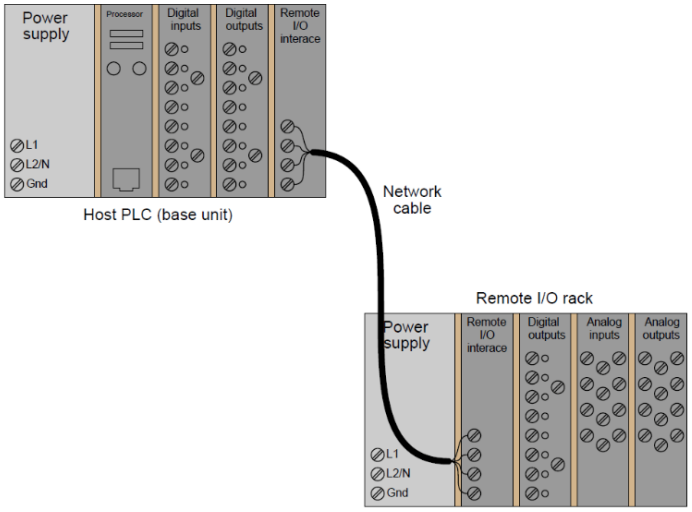


Figure 2.5 PLC and I/O Rack Network

I/O modules are positioned close to field devices in PLC systems, as depicted in Figure 2.6, to reduce the amount of wires needed. Through the communication module, the processor transmits the signal to the output module after receiving it from the remote input module [34].

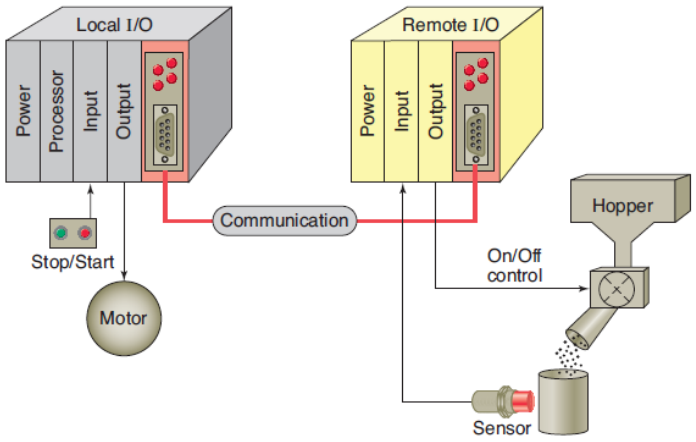


Figure 2.6 Remote I/O Rack

Connecting several PLCs together is another approach to expand the system; each PLC has a separate CPU and rack. One PLC is set up to read data from and/or write data to another via communication standards, by employing the other PLC as an extension of its I/O.

The classification of PLC I/O modules is based on signal type, Figure 2.7. There are two types of signals: separate and continuous. The I/O module is divided into two main parts depending on the signal.

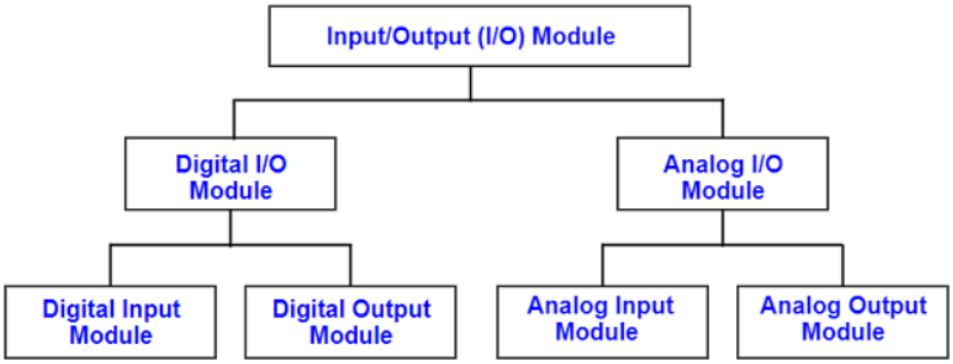


Figure 2.7 Classification of I/O Modules

An input interface module takes a signal from a machine or process device (such as 220V AC) and converts it into a signal that are used by the controller (such as 5V DC), or a processor output interface module converts a signal from the controller. Alternatively, connect the processor (eg 5VDC) with an external signal (e.g. 220VAC) used to control a machine also the process.

Figure 2.8 displays a condensed block diagram of the input module. In a PLC system, input modules carry out four key functions [34].

- Recognize when a signal is received at the machine input from the sensor.
- On the PLC, convert the input voltage to the appropriate voltage level.
- Protect the PLC from input signal voltage or current variations.
- Finally, it sends a signal to the PLC.

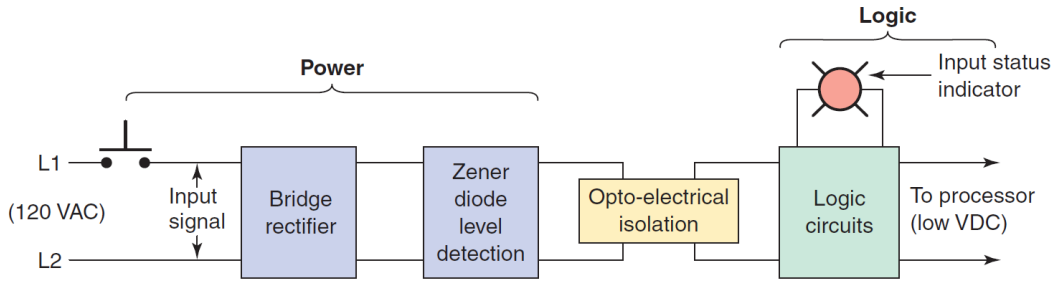


Figure 2.8 Discrete AC Input Module

The output module serves the same purposes as the input module, with the exception that it communicates with the output load in the opposite order. The block diagram of the output module is shown in Figure 2.9. Two portions are present. two power sections and one part of logic.

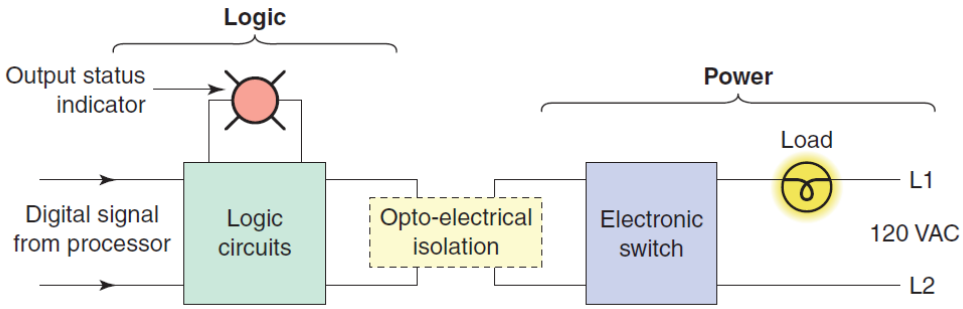


Figure 2.9 Discrete AC Output Module

2.3.2 Central Processing Unit (CPU)

A PLC CPU is comparable to the CPU of a personal computer, that manages all of the computer's operations. from receiving signals to sending them, or performing control and logic operations. Similar to that, the PLC CPU manages all of the PLC's operations and circuits. The PLC's primary component is this. The central processor unit and memory make up the CPU. The processor is in charge of carrying out all required tasks, including calculations and data analysis, by taking inputs and producing the necessary outputs [34]. Random-access memory (RAM) and read-only memory make up the majority of memory (ROM). Sections of a PLC processor are shown in Figure 2.10.

The CPU is integrated into a single fixed unit. Modular rack types frequently employ PLC and rack type modules. Different manufacturers use the words CPU, Controller, and Processor to refer to the same module, all of it serve roughly the same purposes.

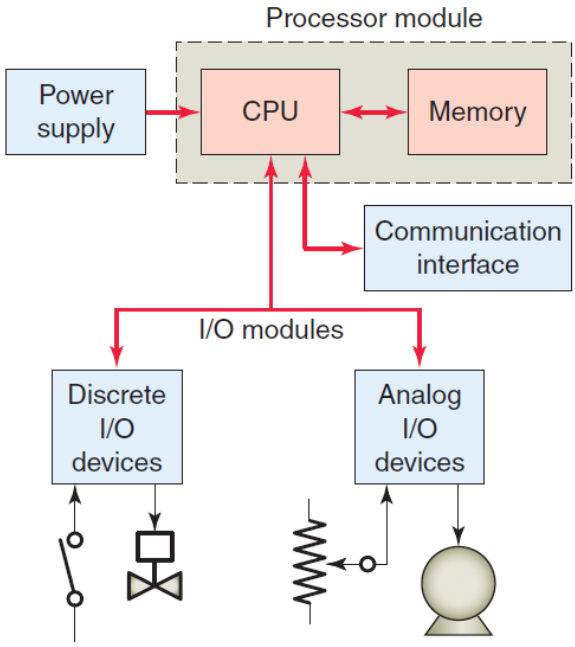


Figure 2.10 Sections of PLC Processor

2.3.3 Power Supply

The input and output units are connected to the back plane of the frame by the PLC controller power supply, this also supplies the CPU with a sizable amount of power (often 5V DC). There are various types of energy sources. The power source transforms 230V AC or 115V AC into active voltage (direct current) for input and output power circuits, memory, and processors.

PLC electrical appliances are usually built to withstand temporary power outages without interrupting the PLC process. The amount of time PLC tolerates power loss is called the holdup time and usually ranges from 10 milliseconds to 3 seconds.

Other modules attached to the rack get DC power from the power supply, as shown in Figure 2.11. Power supplies typically do not power field devices in large PLC systems. An external current (AC) or direct current (DC) current is used to power field equipment in large systems. Field devices are powered by power supplies in some PLC sub-systems. PLCs, transfer modules, sensors, proximity switches, solenoid sensors, thermal sensors, load sensors, and HMI supply are all be enabled by SMPS [8].

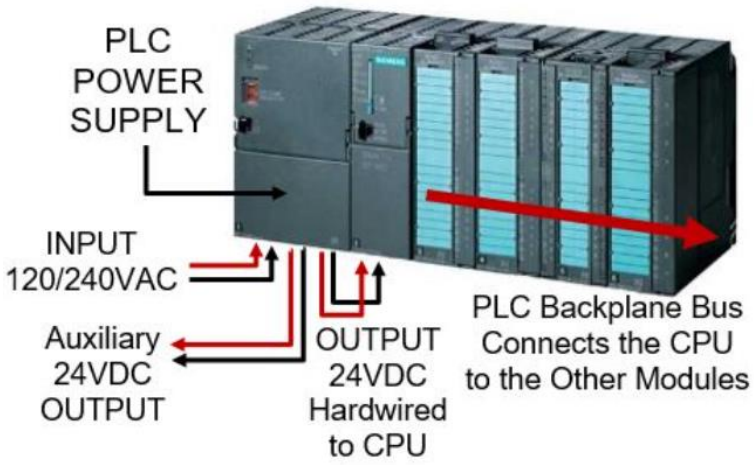


Figure 2.11 PLC Power Supply – Siemens S7-300

2.3.4 Operation of PLC

The PLC's operation is briefly illustrated in Figure 2.12, where the processor reads all inputs, calculates values from them, and then energises or de-energizes the outputs in accordance with the user programme. The programme scan cycle is the name of this procedure [34].

The PLC receives info from connected sensors or input devices, looking at the inputs and outputs. PLC stands out for its application in industries for its robustness, and flexibility to operate in any environment with the Human-machine interface interconnected for Supervisory control from remote stations. The Programmable Logic Controller accepts the inputs from field devices connected to control the operation of particular applications such as sensors, motors, starters, Variable Frequency Drives, and feedback movements from cylinders or pushbuttons.

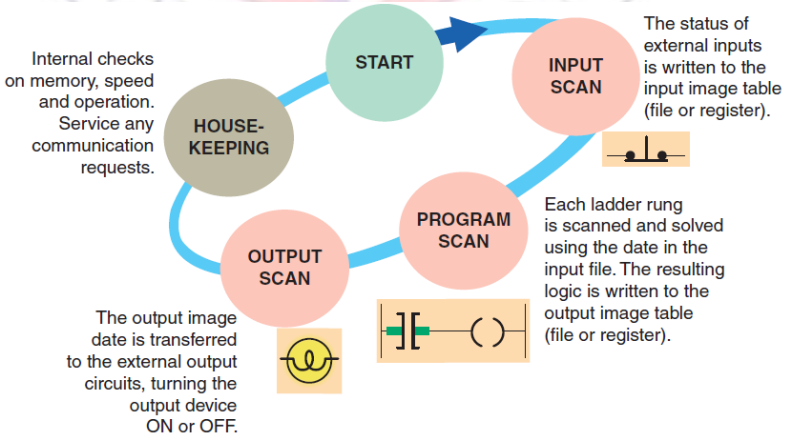


Figure 2.12 PLC Program Scan Cycle

The Input addressing is created in the memory of the controller for each feedback from the field devices. Tags are provided for each input and output to configure the controller for the implementation. In each scan cycle, the input is read and forwarded to the controller.

Programming languages available like structured text, ladder logic, basic C, and Ladder logic is opted to program due to its simplicity. The program is run based on the input feedback and output is generated to run the interfaced application. The communication is established between the graphical interface and PLC panel using the Ethernet switch or RS232 cable based on the distance of communication.

The output is displayed on the graphical interface screens developed and designed in the Human-machine interface system. The manual corrections are made through these screens and task is made simpler by providing easy access.

2.4 SCADA/HMI Overview

Supervisory Control and Data Acquisition, or SCADA systems are used to monitor and manage industrial facilities or machinery, including those for transportation, water and waste management, power, and oil and gas refining. These systems comprise a central host and terminal operators, as well as data transfer between a number of Remote Terminal Units (RTUs) and/or PLCs and a central SCADA computer [7]. The SCADA system gathers data (such as a pipe leak), transmits it back to the central location, and notifies the home channel that it is leaking simultaneously carrying out the required analysis and control, such as determining the importance of the leak and organising the data logically and in an orderly fashion.

SCADA is used for remote operation by creating a Graphical User Interface (GUI) for selecting devices such as chillers and pumps and monitoring. HMI are designed just like that; the connection between user and machine. However, HMI is more focused on production systems and control processes. Real-time data acquisition and a visual representation of the control system are provided by HMI.

2.5 Summary

This chapter provided an overview on control systems in chiller plant application and it has been explained that PLC based control is better than DDC. A brief explanation on parts of PLC, operation of PLC, SCADA and the HMI was also discussed.

Chapter 3

METHODOLOGY AND BLOCK DIAGRAM

According to the methods now employed by the automation industry, this chapter discusses methodology and block diagram for the proposed scheme. This procedure is explained in detail in this chapter. The methodology helps to understand design flow of PLC logic development. And the block diagram provides a clear idea on the working process of a chiller plant.

3.1 Methodology

Figure 3.1 shows the flow diagram of the proposed scheme with various modules: I) Literature Survey; II) Design & Selection of Components; III) PLC & HMI Logic Development; IV) Simulation Analysis; V) Hardware Implementation; and VI) Performance Analysis. The operation of these modules and the overall proposed method is described in Figure 3.1.

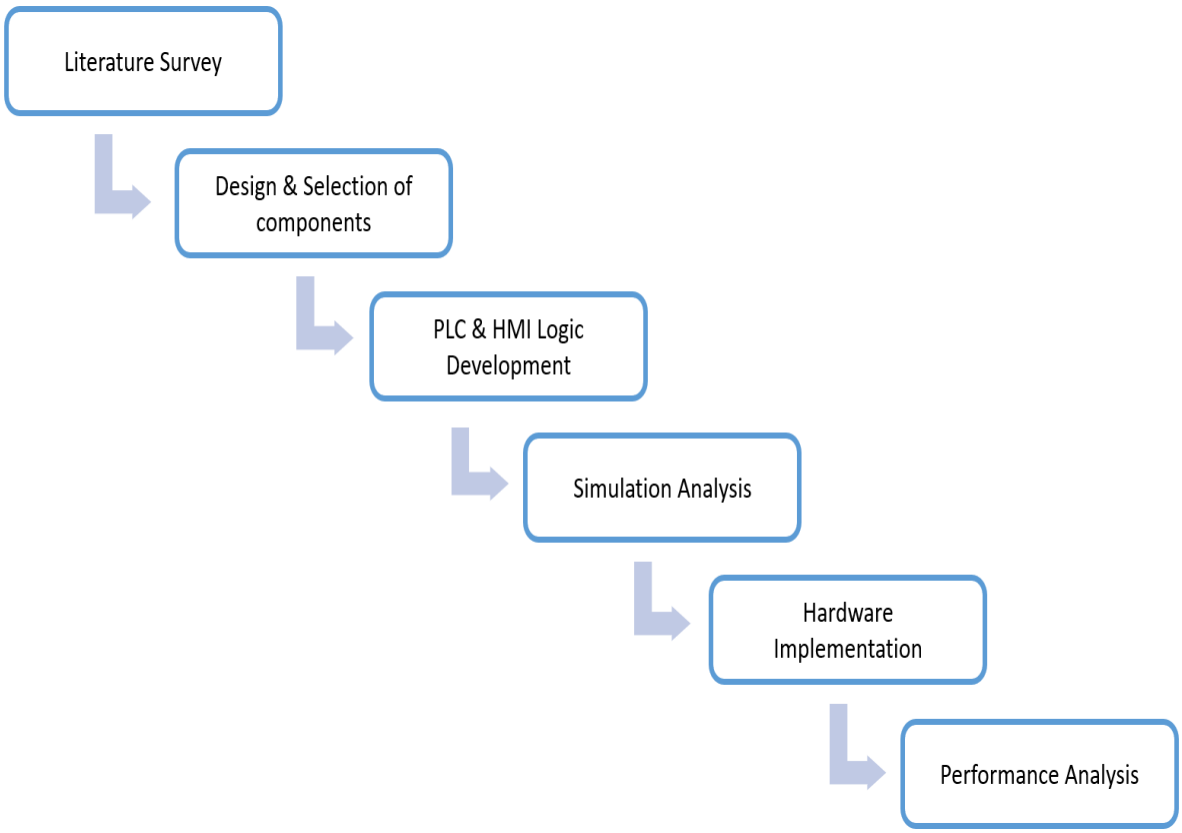


Figure 3.1 Methodology in General

The proposed technique requires Literature Survey, Module-I is carried out for understanding the control process and working of chiller plants for HVAC application, selection of components for electrical panel design and programmable logic controller selection.

Module-II (Design & Selection of Components), Documents like the Control Philosophy paper, Logical Flow Chart, IO list, specification, and structure form the basis of the PLC design process. According to the aforementioned documents, the creation of the PLC process starts. To determine the specifics of the PLC, the control philosophy becomes a useful document. Piping and Instrumentation Diagram (P&ID) is used by HVAC engineers to determine control philosophy. P&ID is an AutoCAD plant-based layout that succinctly identifies the location, label, and total number of tools. With reference to the design guidelines for HVAC and P&ID, the engineer suggests a regulation philosophical document. P&ID describes a concept of the Panel area and cable line. The input output (IO) list is created using the control philosophy.

In module-III (PLC & HMI Logic Development), Engineers begin working on the Logic Flow Chart once the control philosophy has been finished and finalised. Ladder logic is based on a document called a logic flow chart. On the basis of a logic flow chart, PLC application developers create a wide variety of control logic.

In module-IV (Simulation Analysis), Based on the Logic flow chart ladder logic program is written and the code is developed and same is analysed for any coding errors. After the simulation analysis has proper results it moves to next module-V.

In module-V (Hardware implementation), After each document mentioned in module II has been approved, PLC panel manufacture begin. The next phase, known as testing and commissioning of module-VI, is initiated after all components have been successfully installed and assembled in the PLC box's cabinet.

In Module VI (Performance Analysis), thereafter inspections and authorizations are assessed for operational suitability and to ensure safety requirements. Initially verification engineers look at security-related parameters and then evaluate the performance of the PLC panel.

The PLC design flow is shown in Figure 3.2. The relevant diagram and description of the suggested methodology are used to explain a portion of this section.

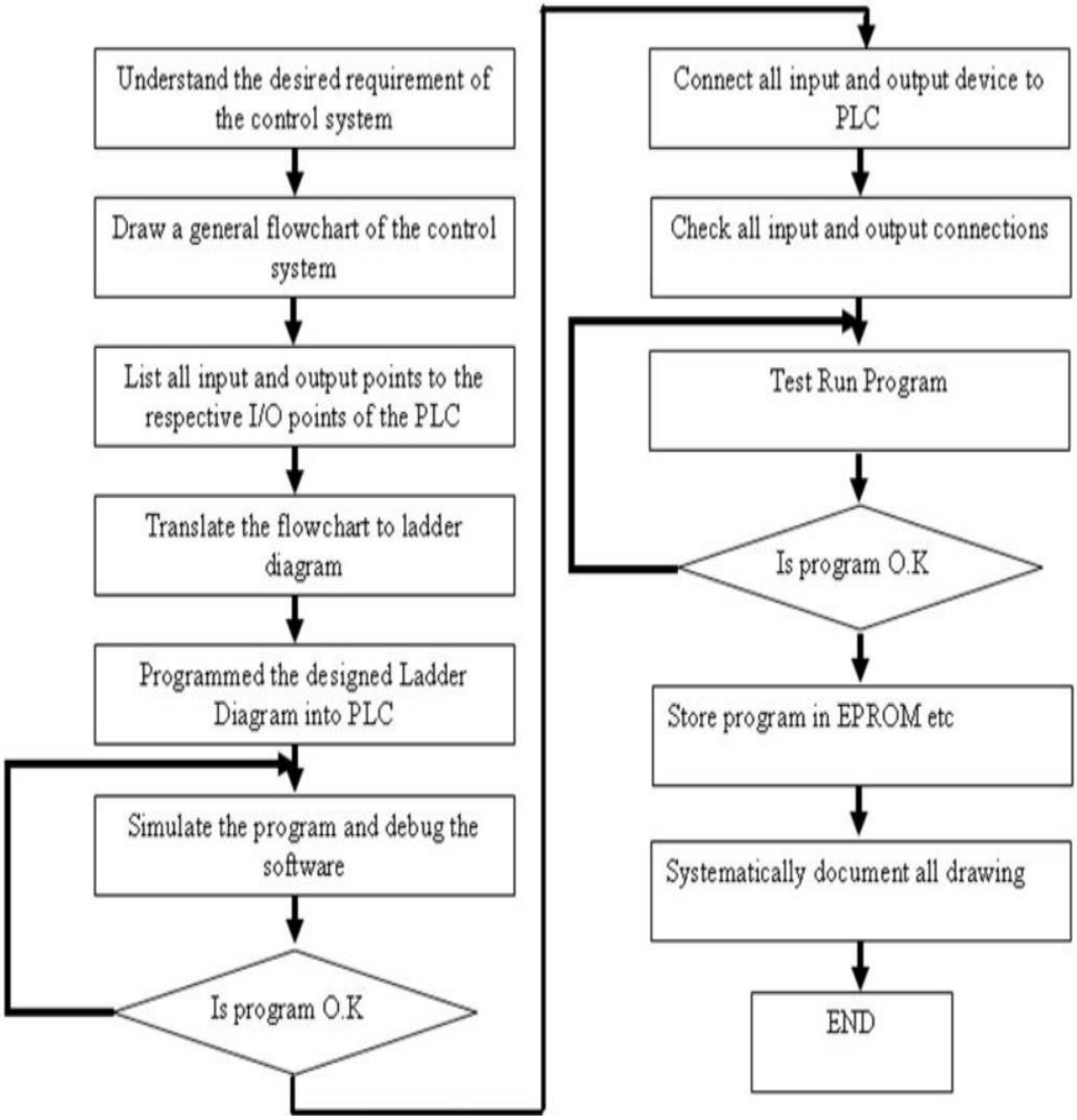


Figure 3.2 PLC Logic Design Process

3.2 Block Diagram

Figure 3.3. shows the flow chart of the working operation of the chiller plant, based on this sequence of operation the logic flow chart for the plc is developed.

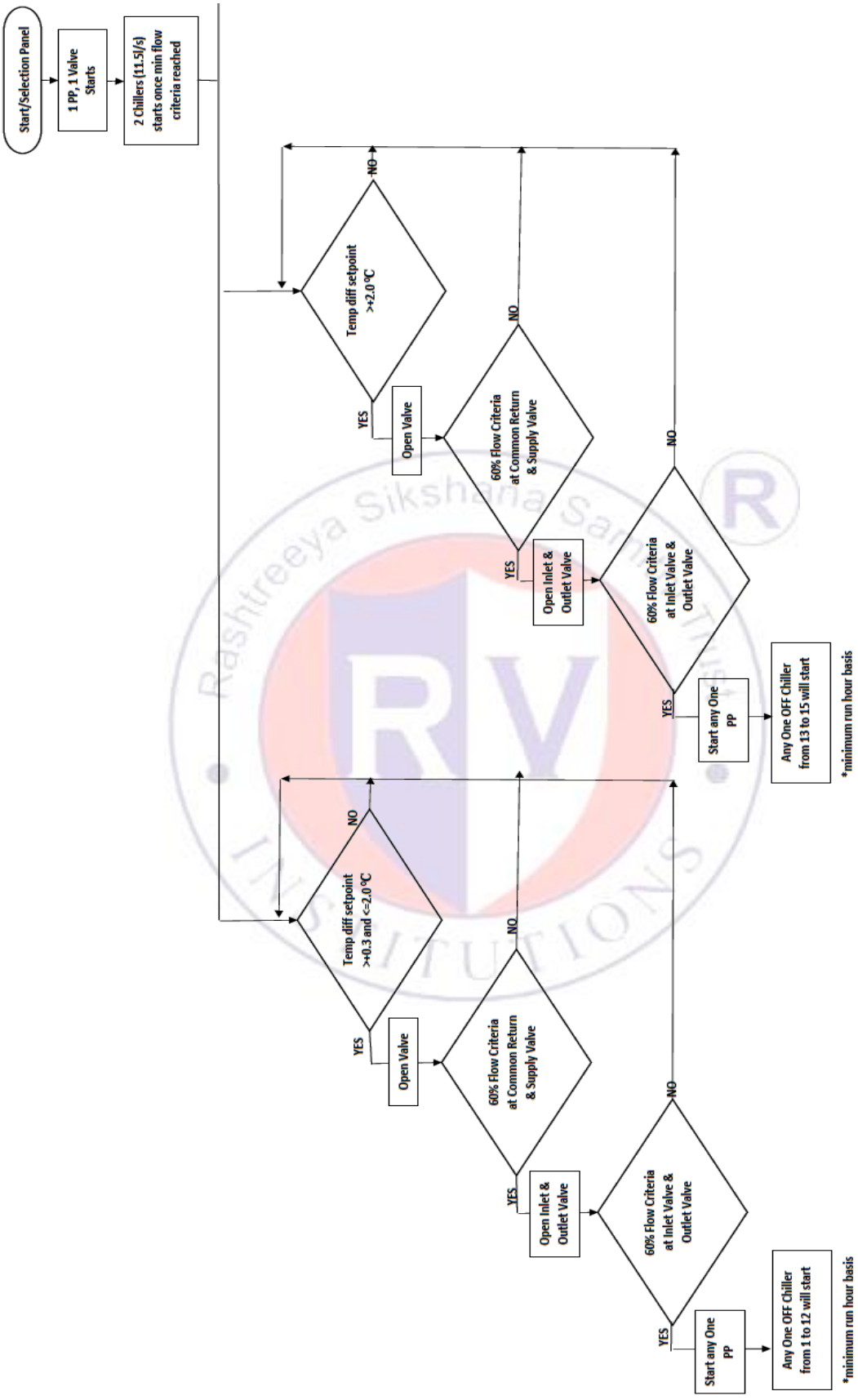


Figure 3.3 Chiller Plant Operational Flow Chart for Starting

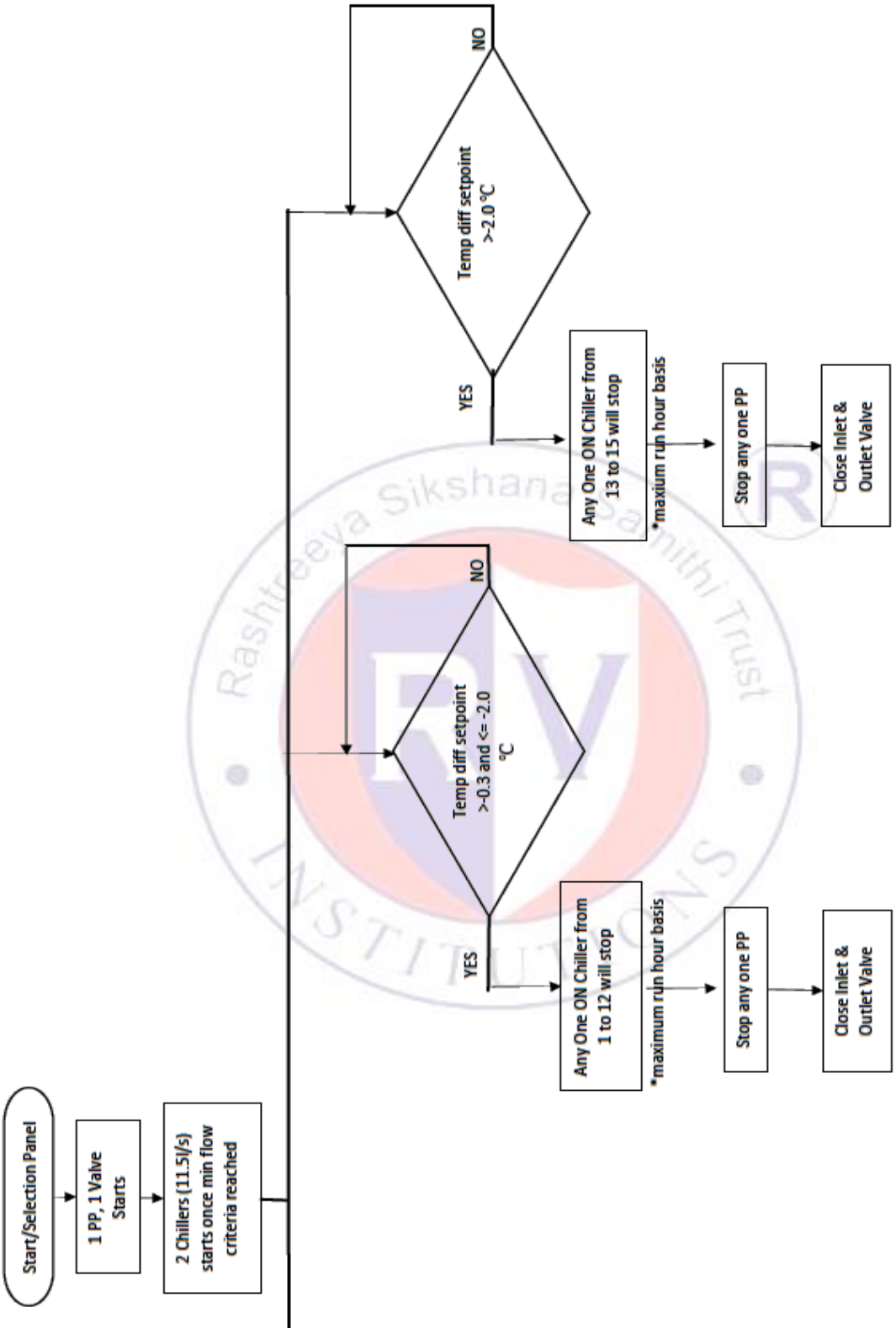


Figure 3.4 Chiller Plant Operational Flow Chart for Stopping

The operation of sequence of chillers generates idea for the control philosophy. Chiller equipment is controlled and monitored from the plant control system that is PLC and HMI. The sequence is as, first select the pump, chillers and valve, are to operate. Always 2 chillers, 1 primary pump, 1 secondary pump (anyone turned off chiller from many is started), on the minimum run hour basis, runs to maintain the temperature of the building, every 48 hrs pump and chiller then changes the duty. Then temperature is measured between the set point and return line, if the difference is high any one pump is started and after that inlet valve and return valve are opened. Again, the temperature difference is measured and if high any 1 chiller is started and if low then chiller is stopped, the difference in temperature is measured continuously. If the temperature difference at the first stage is low that meaning temperature is continuously decreasing then any one chiller is shut off and after it is stable the pumps and valve are closed. In case of any emergency or at time the chiller is unhealthy, emergency stop is provided.

The block diagram for the project application is shown in Figure 3.4.

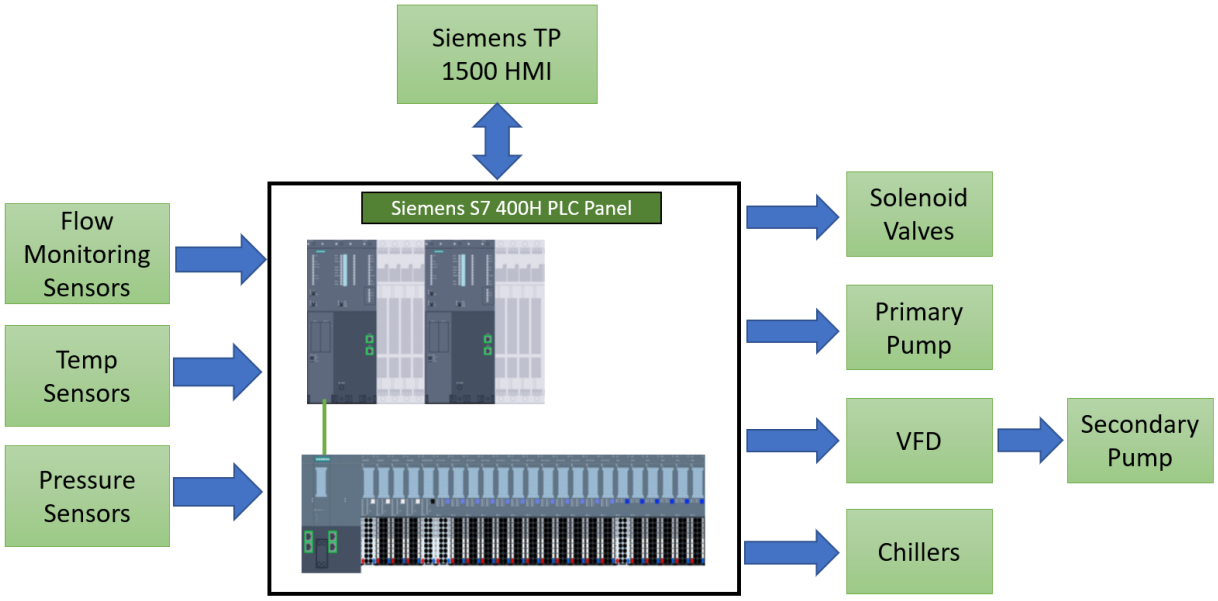


Figure 3.5 Control Block Diagram

PLCs are computers that are especially made to function dependably in challenging industrial environments, such as hot, damp, dry, and/or dusty circumstances. PLCs are utilised to automate industrial processes like the production line of a manufacturing facility, a metal processing plant, or a wastewater treatment plant. According to the kind of production and industry, Programmable Logic Controllers continuously monitor input values from various input sensors and generate compatible output.

SCADA systems are used in a variety of applications to monitor and manage distant devices and processes. The PLC is used as a process controller in SCADA systems so that its connected to them via networks. By creating Graphical User Interface (GUI) for the selection of equipment like chillers and pumps as well as for monitoring, SCADA is utilised to operate remotely [7].

Chiller plants use a lot of energy and could experience disastrous catastrophes. To guard against destruction and human casualties, reliable and cutting-edge security measures are crucial. Although safety is the first priority, having an Emergency Shutdown (ESD) system that is intended for availability is crucial in today's climate. Hence for this purpose Siemens S7-400H PLC is used, because of its powerful, fault tolerant and failsafe automation control. For more safety a redundant architecture is designed Redundancy is essential for ESD systems and it is not considered only for CPU. Based on the specification of ESD systems, redundancy existed on power supply, communication module, network, and IO modules.

The PLC system's power requirements are met by the power supply module. the necessary CPU and I/O module from the available AC power to the requisite DC power. Usually, a 24V DC source is used to power the PLC. Several PLCs only utilise one power supply. Reading the sensor input data, processing it, and then sending the command to the control devices in this manner the CPU works [34].

Input devices like chiller, valves, relays, pumps, start/stop buttons, switches, etc. Through the use of a microprocessor, the I/O module supports input and output devices. The PLC output module functions similarly to the input module, with the exception of the retrieval phase. It combines the processor and output load.

3.3 Summary

In this chapter the methodology employed for the project was discussed along with the block diagram for chiller plant process, that would be helpful to design logic flow chart and control philosophy. Network block diagram was also been discussed, for the control Process, with Simatic S7 400H control system, local SCADA.

Chapter 4

SPECIFICATIONS AND DESIGN

The chapter provides the specification of S7-400 controller, IO modules, SMPS and selection of components. The design details of IO mapping, controller configuration in TIA Portal and SMPS is also explained.

4.1 Selection of Components

The design of programmable logic controllers takes into account many input and output settings, a wide temperature range, protection from electrical noise, and protection from vibration and impact. System programmers are often used to control and utilize battery-backed or fixed memory to store equipment and production process equipment. System discharge is an example of a real-time system because it is controlled by PLC in terms of input. Thus, PLC are digital computers designed to control the machine [8].

It is designed for industrial application, unlike personal computers, and is available with unique input/output interfaces and a control programming language. There are a number of fundamental factors to take into account when choosing the PLC to utilize for automation tasks, including the PLC's make, size, number of I/O channels, memory, scan time, and cost.

4.1.1 Simatic Controller

Different PLC Make available in the market are, Siemens, Rockwell, Schneider, Omron, Emerson Electric, Keyence, ABB, Bosch, Hitachi.

Siemens SIMATIC controllers provide more than just powerful hardware for controlling various machines and plants. SIMATIC controllers' capability is constantly being supplemented with new features. Since many years, PLCs have dramatically changed. Today's PLCs are light years ahead of its predecessors in terms of everything from graphical user interface to wireless networking to machine learning. PLCs are now customised by engineers to match the requirements of specific applications [32].

SIMATIC controllers are therefore the ideal foundation of innovative solution and essentials component of totally integrated automation approach.

SIMATIC modular PLCs are optimized for control tasks and is adapted to meet application requirements by adding modules. Siemens various controllers are,

- SIMATIC S7-300
- SIMATIC S7-400
- SIMATIC S7-1200
- SIMATIC S7-1500
- SIMATIC ET-200 with integrated CPU.

4.1.2 Simatic S7- 400 PLC

The SIMATIC S7-400H contains solutions for usage in challenging environmental conditions and is intended for system solutions in the sectors of production and process automation. For data-intensive operations, that is particularly prevalent in the process industry, this process controller is suitable. Figure 4.1 shows the S7-400H controller. It provides a fault-tolerant automation system that minimizes the potential for production downtime to nearly 0%. Therefore, these devices play an important role in achieving maximum productivity and are expensive [33].

Figure 4.1 Simatic S7-400H PLC

The SIMATIC S7-400H is: Powerful, Fault tolerant, Failsafe. The following parts make up the SIMATIC S7-400H:

- Two distinct UR1/UR2 central controllers or two sections on a single divided central controller for the central controllers (UR2-H).
- Sync modules for connecting each central controller to the other device using fibre optic cable.

- One of each type of CPU (412-5H, 414-5H, 416-5H, or 417-5H) for each central controller.
- The central controllers' S7-400 I/O modules.
- Expansion units UR1/UR2/ER1/ER2 and/or ET 200M distributed I/O devices with I/O modules

4.1.3 TIA Portal

An engineering framework for building adaptable automation solutions across all industries and application domains is made available by the Totally Integrated Automation Portal (TIA Portal). The TIA portal helps engineers save time, money, and effort on everything from design to commissioning, operation, maintenance, and automation system updates. The basic software STEP7, WinCC, SINAMICS Startdrive, SIMOCODE ES and SIMOTION SCOUT TIA are integrated into the TIA portal. Figure 4.2 shows the scope of TIA software. The TIA portal enables smooth communication between the following automated equipment: drives, PLCs, HMIs, and PROFINET-capable devices [19].

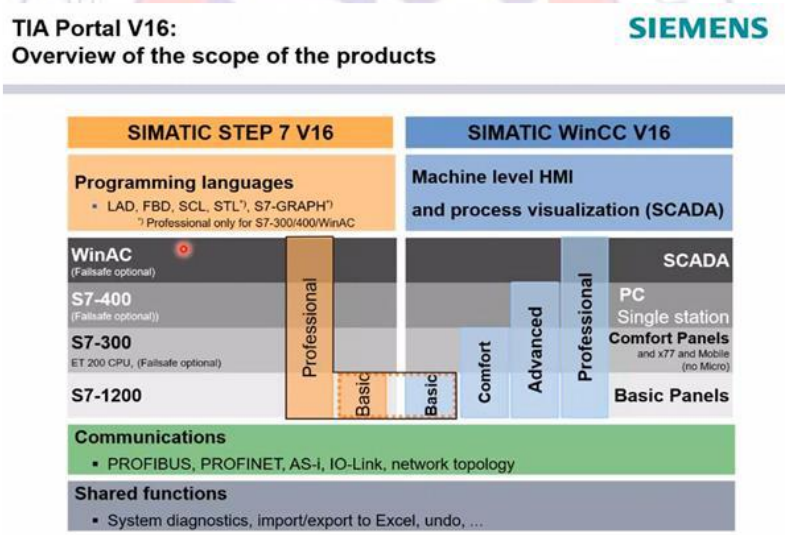


Figure 4.2 TIA Portal Product Overview

The TIA Portal's SIMATIC STEP7 software is a powerful tool for configuring, programming, testing, and diagnosing all modular and PC-based SIMATIC controllers.

4.1.4 IO Point Scheduling

I/O Point Scheduling is the important factor in the selection of controller, Simatic controllers are chosen depending on the inputs and outputs. Following Table 4.1 shows the number of inputs

and output points and the corresponding controller and I/O modules selected for the mentioned specification.

Table 4.1 IO Scheduling

SN.	EQUIPMENT SCHEDULE	INPUT		OUTPUT	
		AI	DI	AO	DO
1	CHILLER 1 TO 15	105	45	30	15
2	CHILLER COMMON POINTS	7	0	2	0
3	CHILLED WATER PUMPS 1 TO 11	11	33	0	11
4	CHILLED WATER PRESSURIZATION UNIT	6	8	0	0
5	SECONDARY CHILLED WATER PUMP 1 TO 5	11	15	5	5
TOTAL		**140**	**101**	**37**	**31**

The controller is configured based on number of inputs and output points selected according to the application requirement. Table 4.2. shows the selection of IO modules based on IO Points calculated.

Table 4.2 IO Module Selection

SN.	RIO Part	Description	Make	Qty
1	DI Cards	DI 16x24VDC ST	Siemens	8
2	DO Cards	DQ 16x24VDC/0.5A ST	Siemens	3
3	AO Cards	AQ 4xU/I ST	Siemens	12
4	AI Cards	AI 8xI 2-/4-wire BA	Siemens	16

4.1.5 HMI TP 1500 Comfort

The SIMATIC HMI Comfort Panel is designed to implement powerful visualization applications at the machine level. WinCC allows for smooth integration of these SIMATIC HMI comfort panels into the TIA interface.

4.2 Specification Details

The specifications required to carry out the project to automate the Chiller Plant with the implementation of Programmable logic controller is discussed in the following sections.

- **Controller Specification**

The S7-400H controller is chosen for the proposed work to suffice the requirement of chiller process. Table 4.3 shows the details of controller specification.

Table 4.3 Controller Specification

Controller Parameter	Specification
Rated Value DC	24V / 48V / 60V
Permissible range, lower limit (DC)	19.2V
Permissible range, upper limit (DC)	72V
Rated Value at 24V / 48V / 60V	4A / 2A / 1.6A
Current consumption (rated value)	850mA
Work memory (CPU 412-5H PN/DP) • Integrated • Integrated (for program) • Integrated (for data) • Memory Type	 1 Mbyte 512 kbyte 512 kbyte RAM
CPU processing times • for bit operations, typ. • for word operations, typ. • for fixed point arithmetic, typ. • for floating point arithmetic, typ.	 31.25 ns 31.25 ns 31.25 ns 62.5 ns
Digital channels ● Inputs 16 384 — of central 1 024 ● Outputs 16 384 — of central	 1024
MPI Protocol	Yes
Processing time for bit operation	0.085µs/operation
Hardware configuration	3 communication modules, 1 signal board, 8 signal modules
DI, DO, AI, AO	14,10,2,2
Encoder	2 wire sensors
Interface type	PROFINET

- **I/O Module Specification**

The IO module is selected based on the controller calculation and the I/O list for the particular controller. Number of I/O modules is calculated on trial-and-error method as shown in Table 4.1 and Table 4.4 shows the IO module specification.

Table 4.4 IO Module Specification

Parameter	Specification
Load voltage L+ Rated value (DC)	24V
Input current from load voltage L+ (without load), max	80mA

Digital inputs Number of DIs	16
Input delay (for rated value of input voltage) for standard inputs at "0" to "1", at "0" to "1", at "1" to "0", at "1" to "0",	min. 1.2 ms, max. 4.8 ms, min. 1.2 ms, max 4.8ms
Digital outputs Number of DOs	16
Output delay with resistive load "0" to "1", "1" to "0",	max. 100 µs, max. 500 µs
Switching frequency with resistive load, with inductive load	max. 0.5 Hz on lamp load, max. 100 Hz

- **SMPS Specification**

The specifications of the SMPS are as follows:

Input Voltage - 230 V AC
Output Voltage - 24 V DC
Output Power - 6.6 kW
Line Frequency - 50 Hz
Switching Frequency - 10 kHz

4.3 System Design

Electrical control panel is a combination of electrical devices and switchgears used to power the PLC module and communication network to control the various equipment at the chiller plant.

4.3.1 System Architecture

Figure 4.3 shows a conceptual model that describes the structure and behaviour of multiple components and network devices, hardware of a control system. It shows the connection between PLC, HMI, IO racks and field equipment and control instruments.

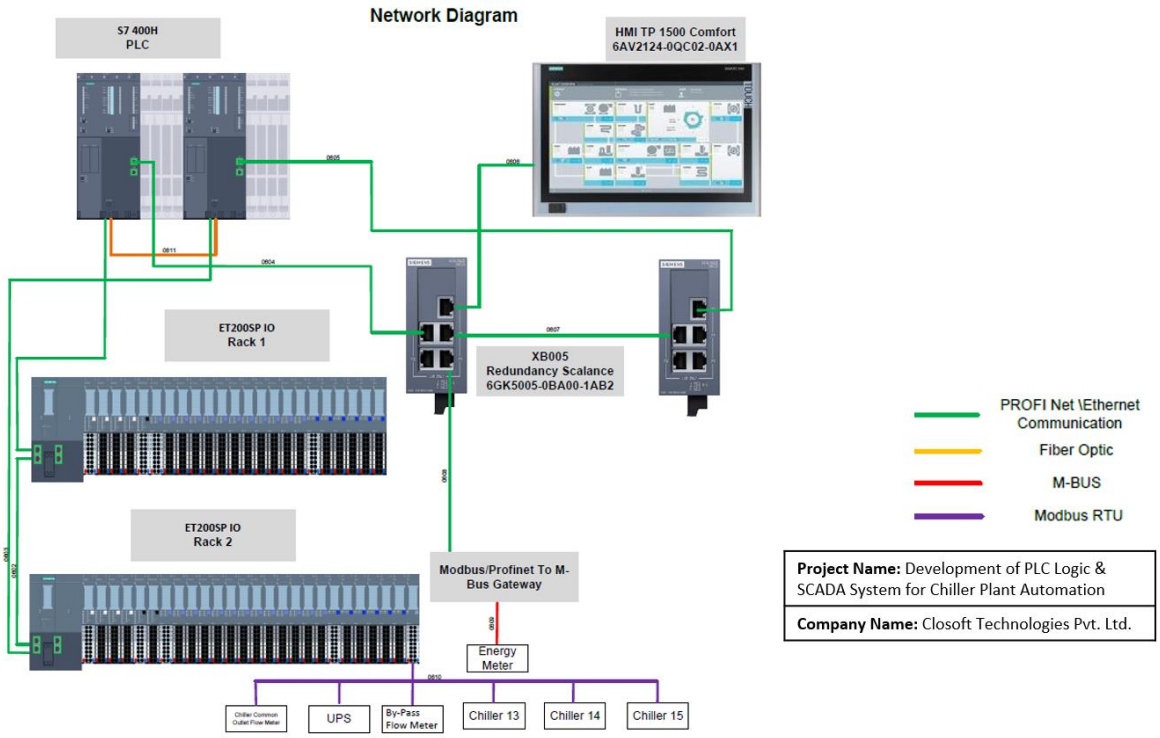


Figure 4.3 Control System Architecture

4.3.2 Panel Design

An important part of control panel design is the switchgear components. switchgear component. Switching devices help operate electrical devices in a streamlined manner and protect them from damage from overloads and short circuits. Figure 4.4 shows the connections between the panel components.

- **PLC Panel PSU**

Power supply Unit (PSU) is selected based the connected load that is PLC, IO modules, field Instruments if required. Based on Simatic PLC a 24V DC and about 5A PSU is suitable for the design.

- **Rating of MCB**

Rating of MCB is 2 times the rating of module to be protected i.e.,

For 16 Digital inputs module with 0.5A rating, I= 0.5*2*3= 3A

- **Components for DI, AO, AI module**

i. SP MCB 2A x 1 No

ii. 2.5mm^2 terminal, 2Nos for each DI = 2*101 = 202

iii. 2.5mm^2 terminal, 2Nos for each AO = 2*37 = 74

iv. 2.5mm^2 terminal, 2Nos for each AI = 2*140 = 280

v. Shielded cable are used for AO, AI wiring

- **Components for DO module**

i. SP MCB 2A x 1 No

ii. 1 x 1CO relay for each DO = 31

iii. 2.5mm^2 terminal x 2Nos for each DO = 2*31 = 62

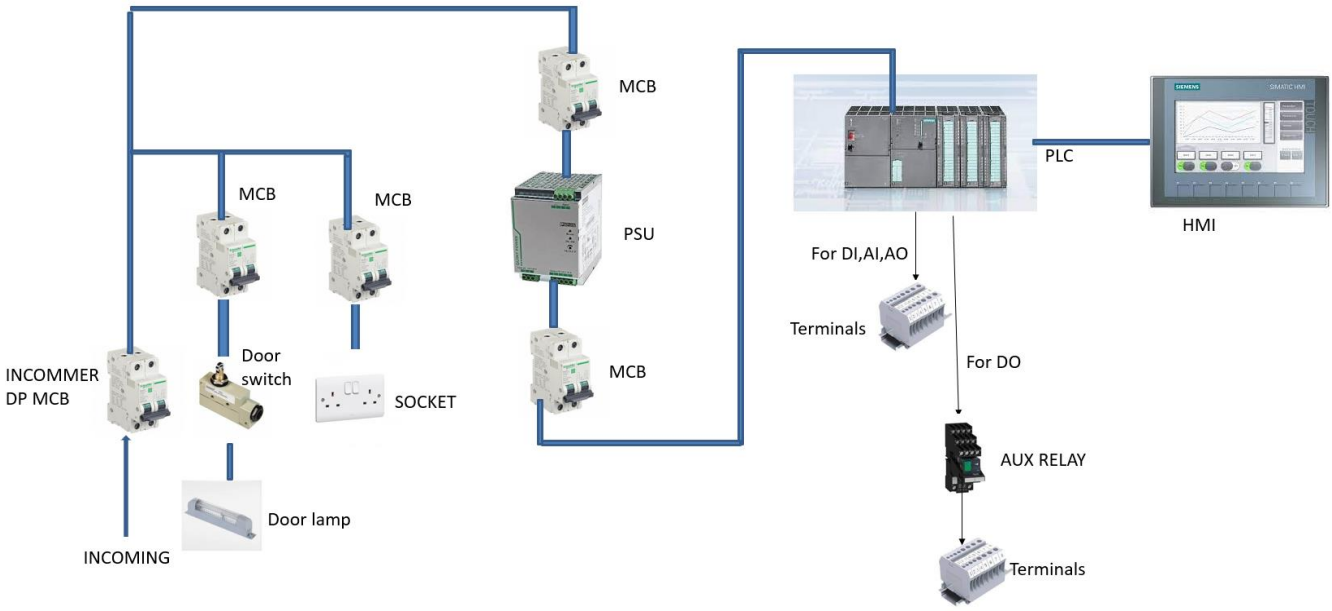


Figure 4.4 PLC Panel Switchgear Connection

4.4 Summary

The specification of the controller and input/output module was been selected based on the application requirement, the robustness of the device and IO mapping. System architecture and panel design were also discussed in the chapter.

Chapter 5

SIMULATION ANALYSIS AND HARDWARE IMPLEMENTATION

The Ladder logic program for the automation of chiller plant is developed using totally integrated automation portal. The chapter includes the algorithm used at the backend, IO address mapping and program developed for automation and also provides the selection of controller from TIA Portal for the hardware implementation in the electrical panel.

5.1 Simulations in TIA Portal

The ladder logic program is written for the controller selected i.e., 412-5 H CPU in the Siemens TIA Portal.

5.1.1 Algorithm to develop RLL

The algorithm to develop the RLL for the proposed work is as follows with initially letting the 2 chillers, 1 primary pump and 1 secondary pump in ON condition (anyone turned off chiller is started of small capacity), on the minimum run hour basis, runs to maintain the temperature of the building. 12 chillers, each capacity 11.50 l/s. operates with 6 Duty +1 standby primary pumps, each pump capacity 23 l/s, with 5 secondary pumps, each pump capacity 68 l/s to match the flow always run 2 chillers and 1 primary pump. 3 chillers each capacity of 43.85 l/s. operates with 3 Duty +1 standby primary pumps with a capacity of 44 l/s, with 5 secondary pumps, each pump capacity 68 l/s to match the flow.

If the temperature difference is + 0.3℃, between the temperature setpoint, and return line temperature, there is no action take place. And if temperature difference is > 0.3 to +2.0℃, between the temperature setpoint and return line temperature, PLC now has to check the time if the temperature same or increasing then after 10 min. The next set of chillers (Anyone turned off chiller of small capacity is started), on the minimum run hour basis, if the temperature is continuously increasing between this difference, the turned off chiller starts through the same logic. After starting a new chiller, if temperature difference >+2.0℃, between the temperature setpoint (configurable from HMI) and return line temp, PLC now again checks the time if the temperature difference is same or increasing then after 10 min. The next chillers (anyone turned

off chiller of big capacity is started), on the minimum run hour basis, if the temperature is continuously increasing between this difference, the turned off chiller starts through the same logic.

If temperature difference <=2.0℃ between the temperature setpoint and return line temperature then PLC checks if the temperature difference is same or decreasing even after 10 min. On the maximum run hour basis, one set of chillers (Any one turned on chiller of big capacity) is stopped. If the temperature is continuously decreasing between this difference, the turned-on chiller stops through the same logic. After stopped any previous chiller, if temperature difference 0.3 to +2.0℃, between the temperature setpoint and return line temperature, PLC again checks the time if the temperature difference is same or decreasing then after 10 min. The chillers (anyone turned on chiller of small capacity is stopped), on the maximum run hour basis, if the temperature is continuously decreasing between this difference, the turned-on chiller stops through the same logic. Algorithm for this comparison of temperature and sequence of operation is demonstrated in Figure 5.1, Figure 5.2 and Figure 5.3.

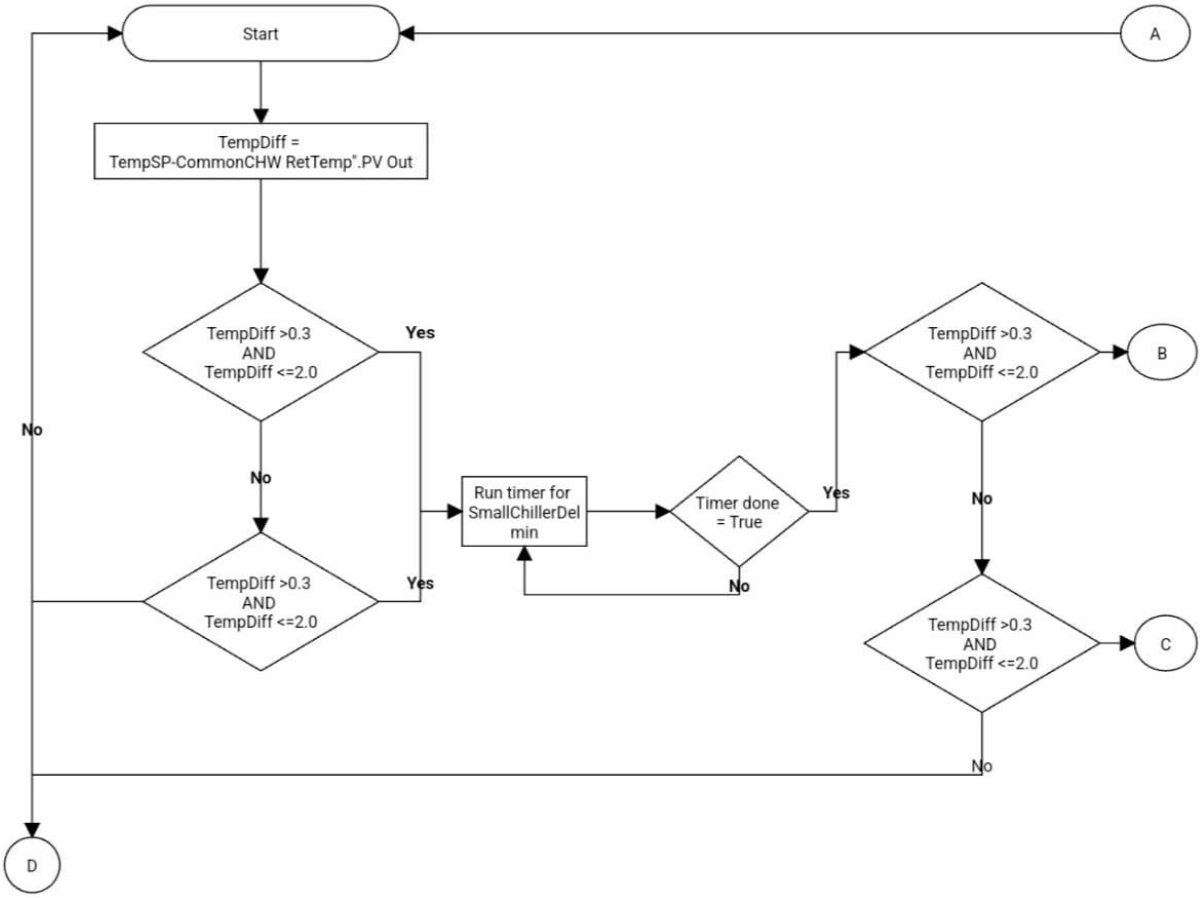


Figure 5.1 Algorithm for Temperature Comparison

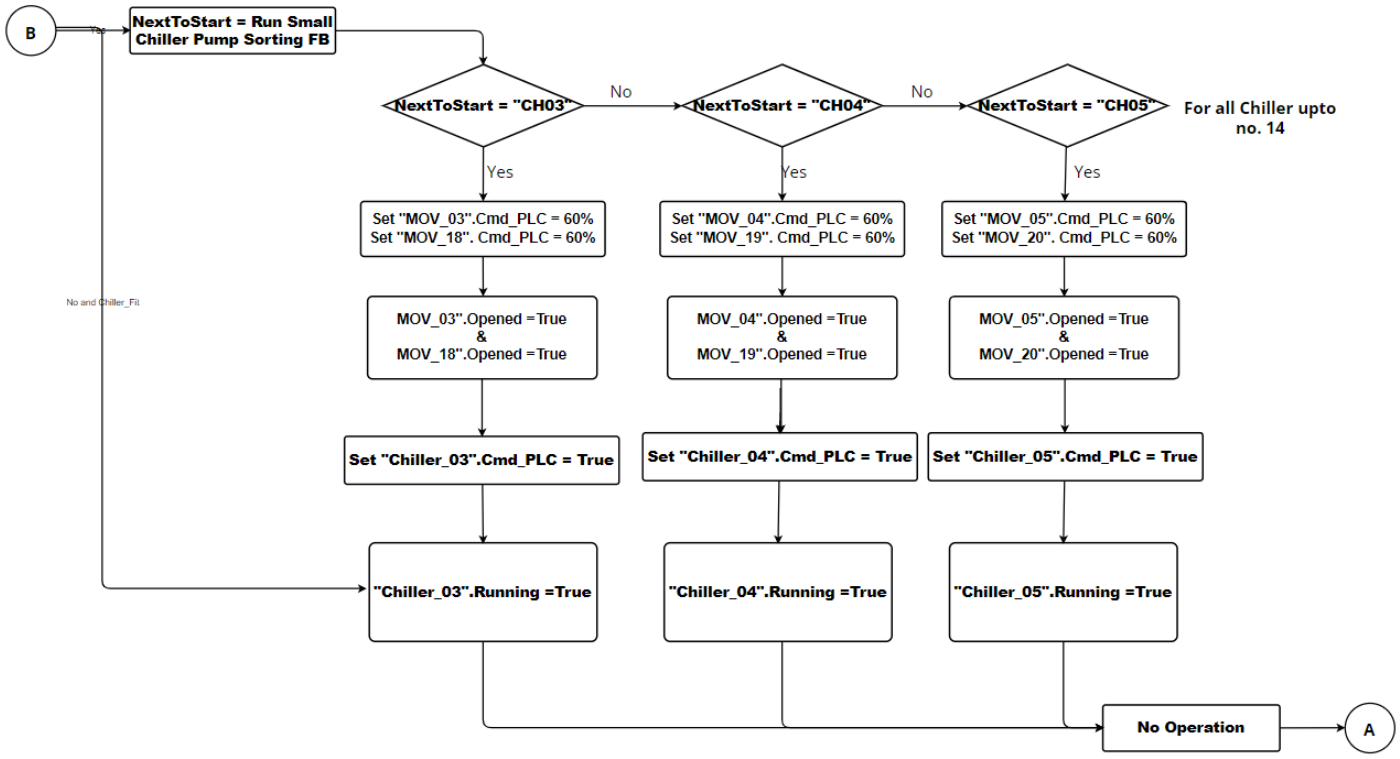


Figure 5.2 Algorithm for Starting a Chiller

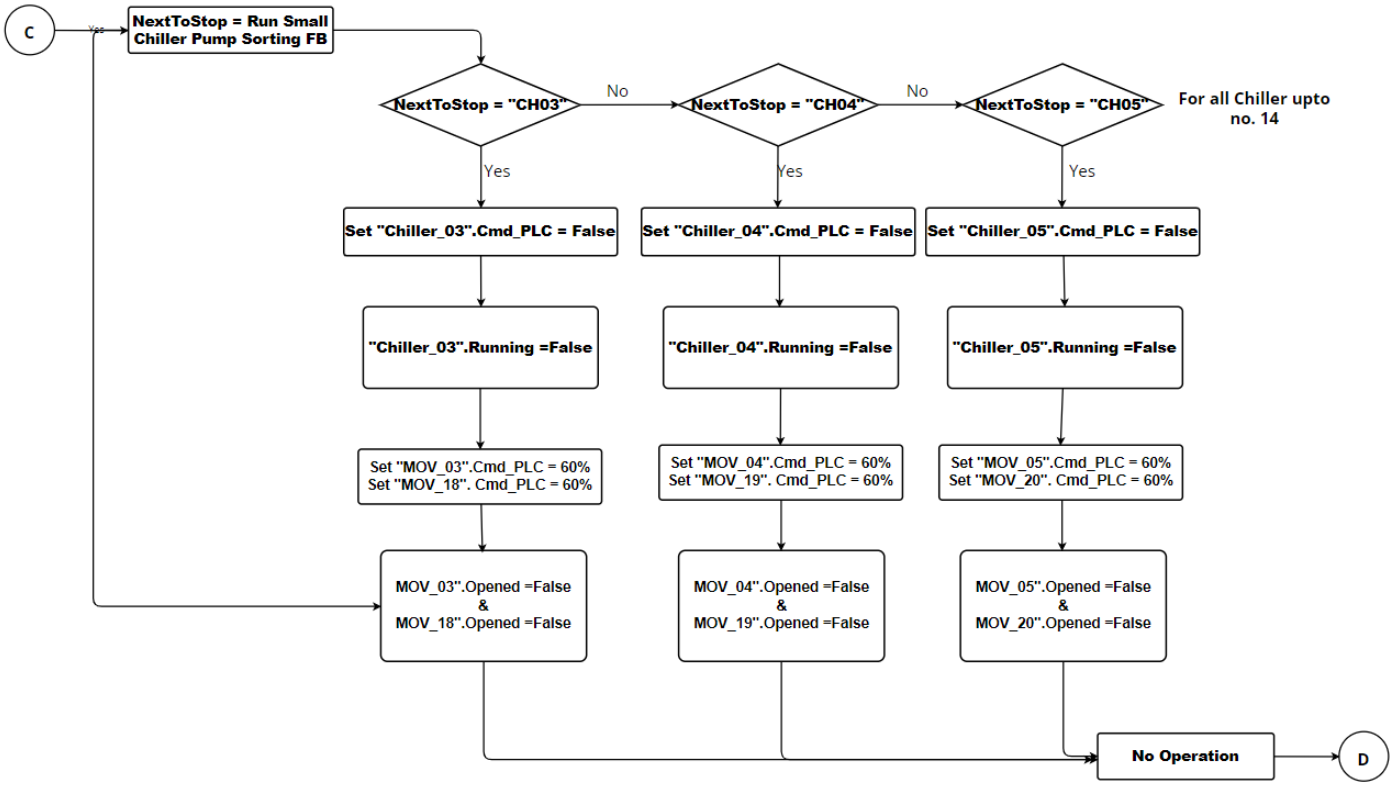


Figure 5.3 Algorithm to Stop a Chiller

5.1.2 Input/Output Mapping

In contrast to the modular design, that employs an external IO module connected to the PLC, the fixed PLC has an integrated IO configuration. The input interface module receives signals from the device or from the machine it is processing and transforms them into signals the controllers use. The PLC are usually able to identify the individual inputs and outputs. This is carried out by assigning an address to each input and output. On small PLCs, this is usually a number preceded by a letter indicating whether it is an input or an output.

IO mapping allows regular memory reads & writes to control a device. Process status information are transmitted to the system via the input interface. The IO Map, also known as the Data Table or Symbol Table, displays the addressing of memory regions set aside for user-entered applications. The Table 5.1, details the Input and Output symbol table list for the controller,

Table 5.1 IO Symbol Table

Status	Symbol	Address	Data type	Comment
	ai	VAT 2		
	ALARM_DQ	SFC 107	SFC 107	Creating Acknowledgeable Block-related Message
	CH01_RUN_STS	I 0.0	BOOL	CHILLER-01 RUN STATUS
	CH01_STR_CMD	Q 0.0	BOOL	CHILLER-01 START/STOP COMMAND
	CH01_TRP_STS1	I 0.1	BOOL	CHILLER-01 TRIP-1 STATUS
	CH01_TRP_STS2	I 0.2	BOOL	CHILLER-01 TRIP-2 STATUS
	CH02_RUN_STS	I 0.3	BOOL	CHILLER-02 RUN STATUS
	CH02_STR_CMD	Q 0.1	BOOL	CHILLER-02 START/STOP COMMAND
	CH02_TRP_STS1	I 0.4	BOOL	CHILLER-02 TRIP-1 STATUS
	CH02_TRP_STS2	I 0.5	BOOL	CHILLER-02 TRIP-2 STATUS
	CH03_RUN_STS	I 2.0	BOOL	CHILLER-03 RUN STATUS
	CH03_STR_CMD	Q 0.2	BOOL	CHILLER-03 START/STOP COMMAND
	CH03_TRP_STS1	I 2.1	BOOL	CHILLER-03 TRIP-1 STATUS
	CH03_TRP_STS2	I 2.2	BOOL	CHILLER-03 TRIP-2 STATUS
	CH04_RUN_STS	I 2.3	BOOL	CHILLER-04 RUN STATUS
	CH04_STR_CMD	Q 0.3	BOOL	CHILLER-04 START/STOP COMMAND
	CH04_TRP_STS1	I 2.4	BOOL	CHILLER-04 TRIP-1 STATUS
	CH04_TRP_STS2	I 2.5	BOOL	CHILLER-04 TRIP-2 STATUS
	CH05_RUN_STS	I 4.0	BOOL	CHILLER-05 RUN STATUS
	CH05_STR_CMD	Q 0.4	BOOL	CHILLER-05 START/STOP COMMAND
	CH05_TRP_STS1	I 4.1	BOOL	CHILLER-05 TRIP-1 STATUS
	CH05_TRP_STS2	I 4.2	BOOL	CHILLER-05 TRIP-2 STATUS
	CH06_RUN_STS	I 4.3	BOOL	CHILLER-06 RUN STATUS
	CH06_STR_CMD	Q 4.0	BOOL	CHILLER-06 START/STOP COMMAND
	CH06_TRP_STS1	I 4.4	BOOL	CHILLER-06 TRIP-1 STATUS
	CH06_TRP_STS2	I 4.5	BOOL	CHILLER-06 TRIP-2 STATUS
	CH07_RUN_STS	I 6.0	BOOL	CHILLER-07 RUN STATUS
	CH07_STR_CMD	Q 4.1	BOOL	CHILLER-07 START/STOP COMMAND
	CH07_TRP_STS1	I 6.1	BOOL	CHILLER-07 TRIP-1 STATUS
	CH07_TRP_STS2	I 6.2	BOOL	CHILLER-07 TRIP-2 STATUS
	CH08_RUN_STS	I 6.3	BOOL	CHILLER-08 RUN STATUS
	CH08_STR_CMD	Q 4.2	BOOL	CHILLER-08 START/STOP COMMAND
	CH08_TRP_STS1	I 6.4	BOOL	CHILLER-08 TRIP-1 STATUS
	CH08_TRP_STS2	I 6.5	BOOL	CHILLER-08 TRIP-2 STATUS
	CH09_RUN_STS	I 8.0	BOOL	CHILLER-09 RUN STATUS
	CH09_STR_CMD	Q 4.3	BOOL	CHILLER-09 START/STOP COMMAND
	CH09_TRP_STS1	I 8.1	BOOL	CHILLER-09 TRIP-1 STATUS
	CH09_TRP_STS2	I 8.2	BOOL	CHILLER-09 TRIP-2 STATUS
	CH10_RUN_STS	I 8.3	BOOL	CHILLER-10 RUN STATUS
	CH10_STR_CMD	Q 4.4	BOOL	CHILLER-10 START/STOP COMMAND
	CH10_TRP_STS1	I 8.4	BOOL	CHILLER-10 TRIP-1 STATUS
	CH10_TRP_STS2	I 8.5	BOOL	CHILLER-10 TRIP-2 STATUS

5.1.3 RLL for Chiller Automation

The section shows the Ladder logic for different network operation of the chillers in plant. Figure 5.4 shows the first network, it is a delay function for every cycle of operation the temperature information is collected.

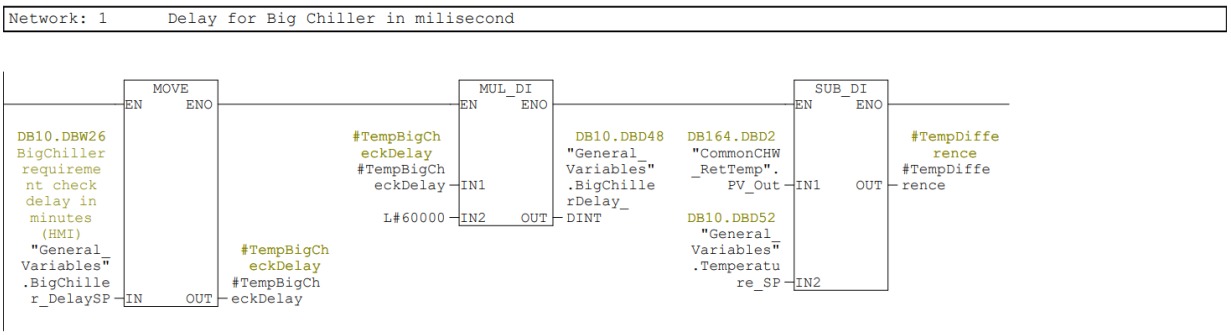


Figure 5.4 Delay for Chillers

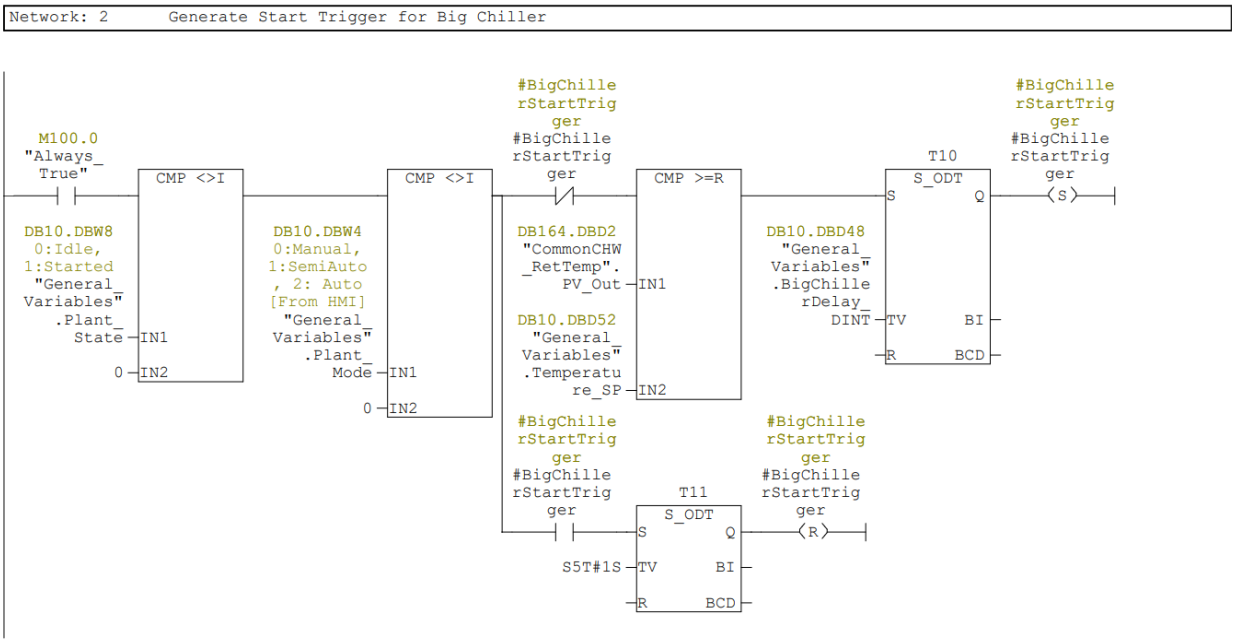


Figure 5.5 Start Trigger Generation

As the temperature related information is collected the next network as shown in Figure 5.5 generates a start trigger for the chiller based on the inputs that has been provided from the HMI panel about the operating mode and the temperature range based on the setpoint temperature. Similar action takes place for the stop trigger generation as shown in Figure 5.6.

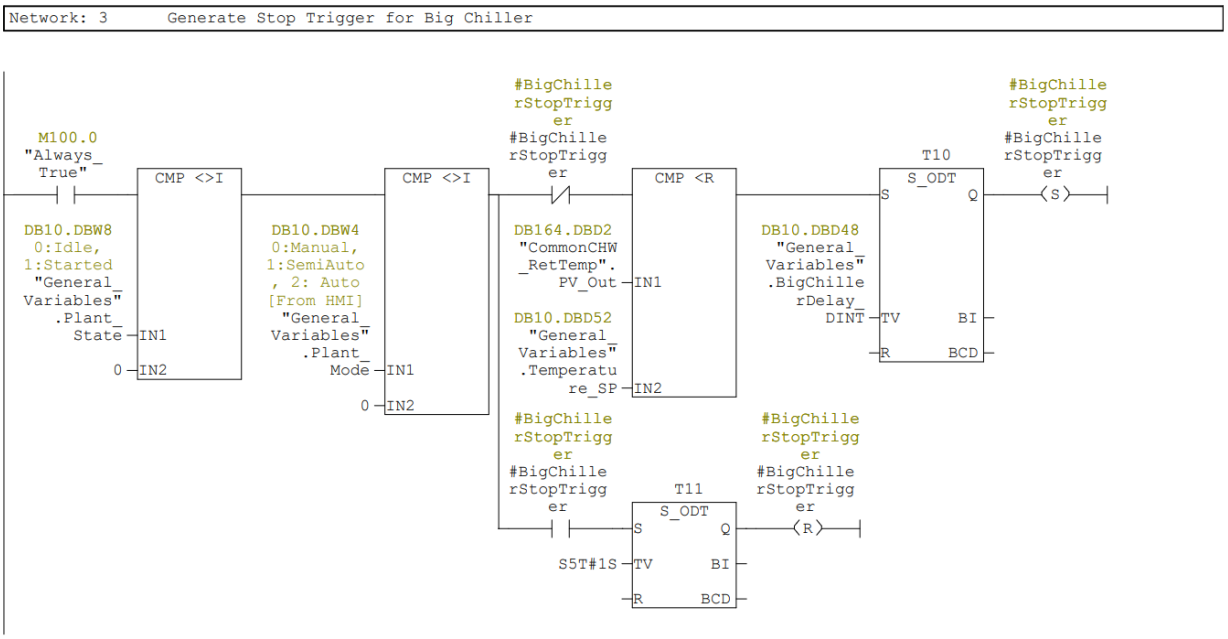


Figure 5.6 Stop Trigger Generation

Based on start or stop trigger, chiller sorting function is called and accordingly the command to start or stop the sorted chiller, as shown in Figure 5.7, 5.8, and 5.9.

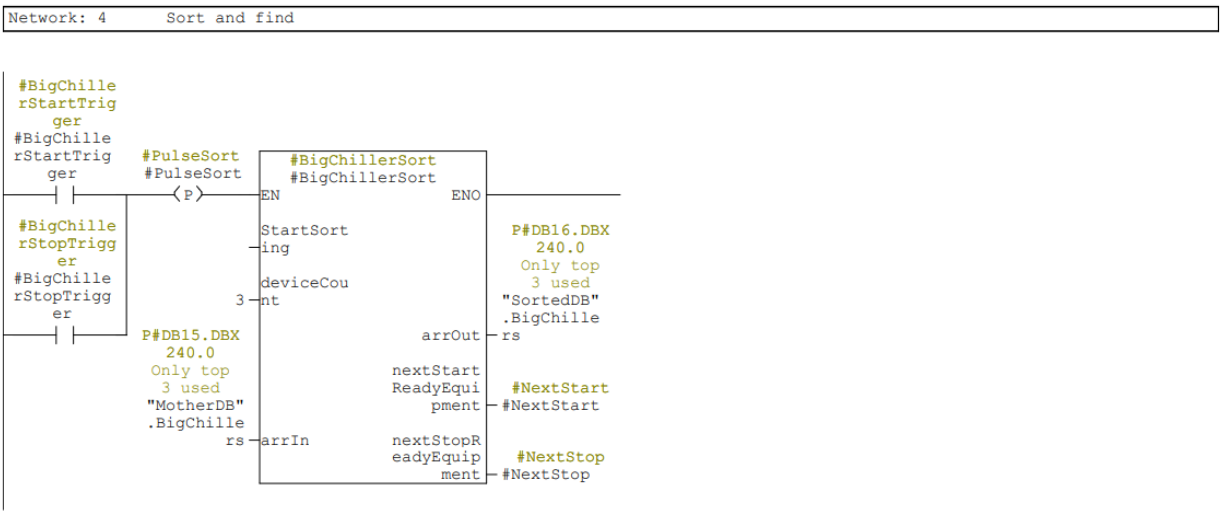
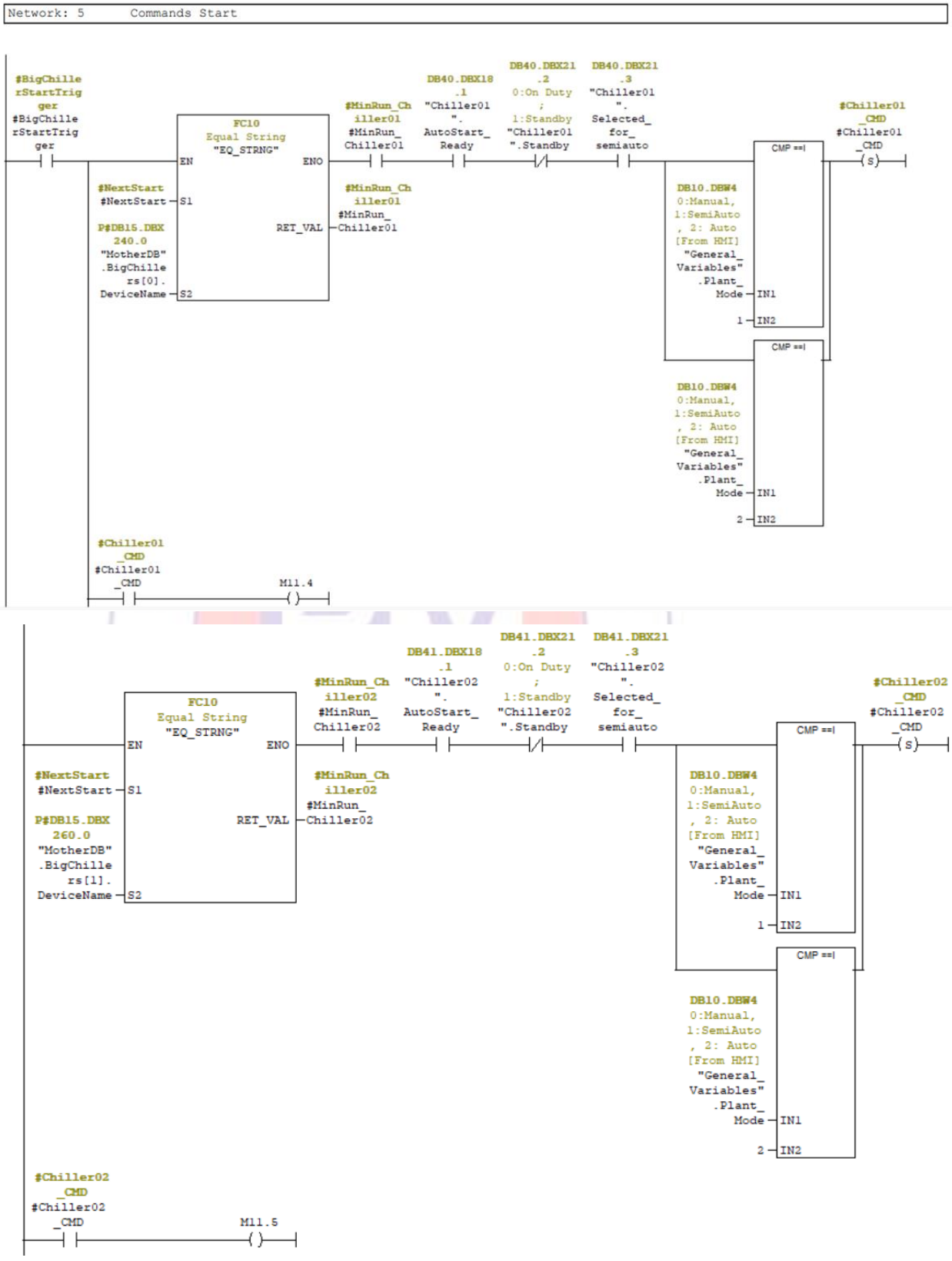


Figure 5.7 Sorting Chillers


Network: 5 Commands Start
#BigChilleStartTrigger
#BigChilleStartTrigger
FC10
Equal String
"EQ_STRNG"
EN
ENO
#NextStart
#NextStart
S1
P#DB15.DBX 240.0
"MotherDB".BigChillers[0].DeviceName
S2
RET_VAL
#MinRun_Chiller01
#MinRun_Chiller01
DB40.DBX18.1
"Chiller01".AutoStart_Ready
DB40.DBX21.2
0:On Duty; 1:Standby
"Chiller01".Standby
DB40.DBX21.3
"Chiller01".Selected_for_semiauto
CMP ==I
DB10.DBW4
0:Manual, 1:SemiAuto, 2: Auto [From HMI]
"General_Variables".Plant_Mode
IN1
1
IN2
#Chiller01_CMD
#Chiller01_CMD
(s)
#Chiller01_CMD
#Chiller01_CMD
M11.4
#MinRun_Chiller02
#MinRun_Chiller02
DB41.DBX18.1
"Chiller02".AutoStart_Ready
DB41.DBX21.2
0:On Duty; 1:Standby
"Chiller02".Standby
DB41.DBX21.3
"Chiller02".Selected_for_semiauto
#Chiller02_CMD
#Chiller02_CMD
(s)
#Chiller02_CMD
#Chiller02_CMD
M11.5

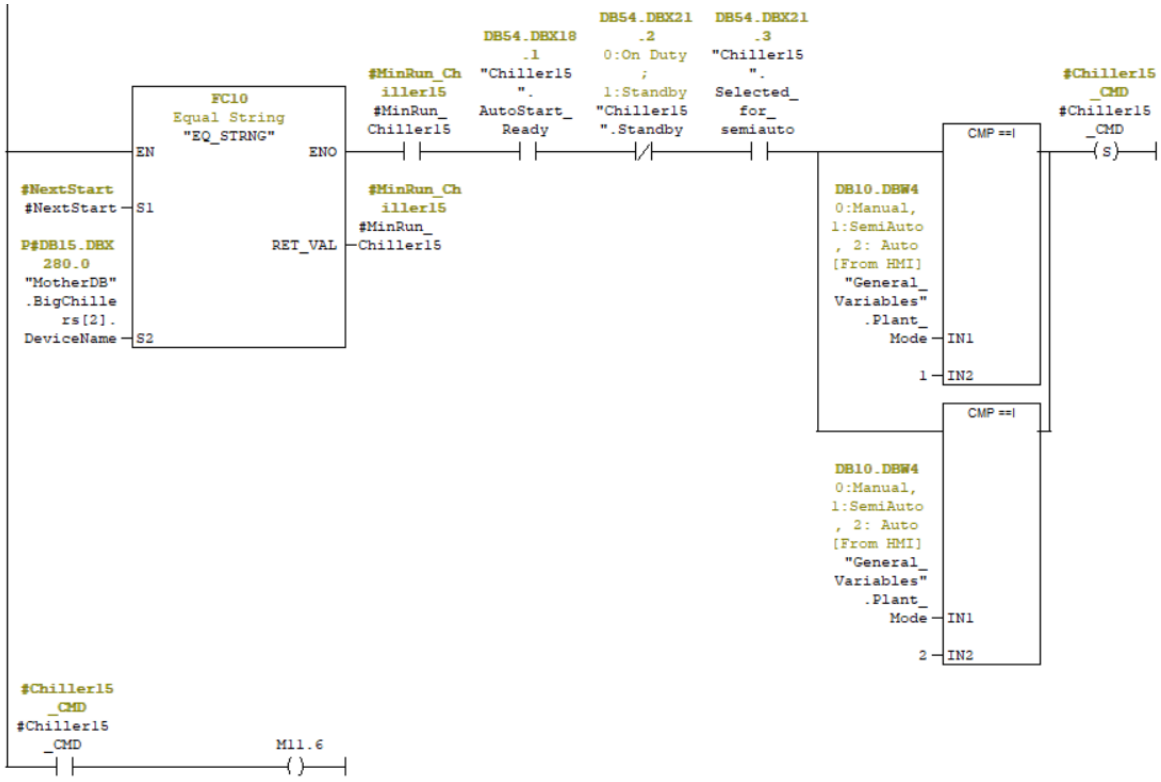


Figure 5.8 Start Command

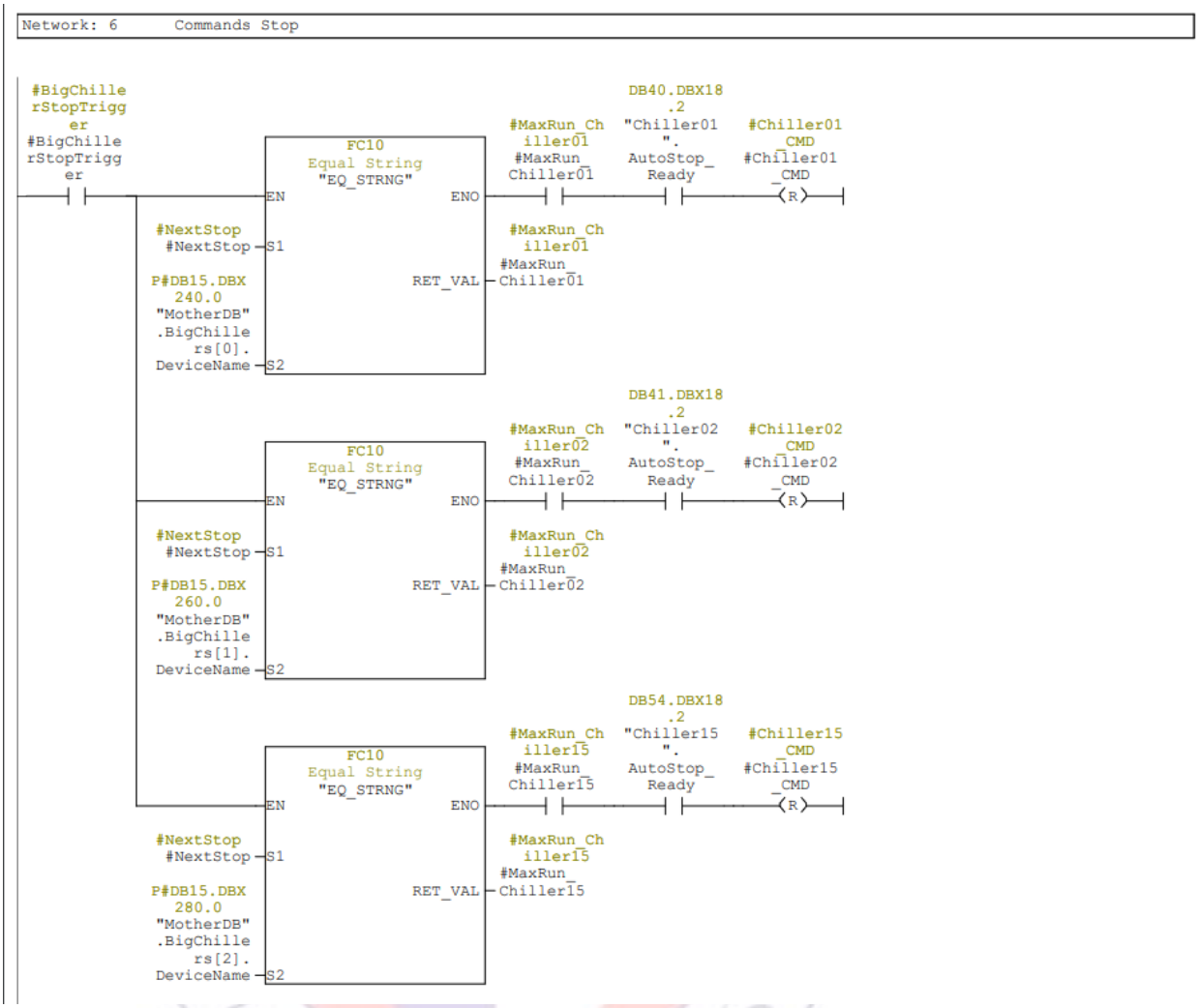


Figure 5.9 Stop Command

5.1.4 Configuration of controller in TIA

The controller selected i.e., S7-400H is simulated in TIA portal with the IO modules configured as per the requirement of the project, were Inputs are 241 and Outputs are 68. The steps involved in selection of controller is as shown in Figure 5.10, 5.11, and 5.12

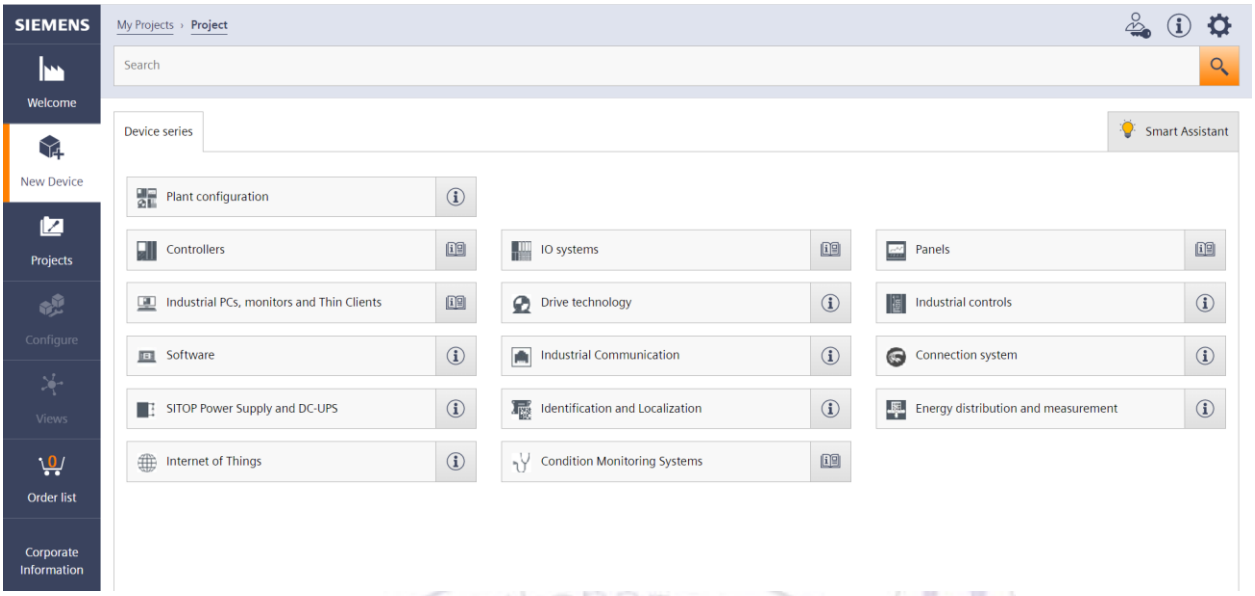


Figure 5.10 TIA Software Components Selection Screen

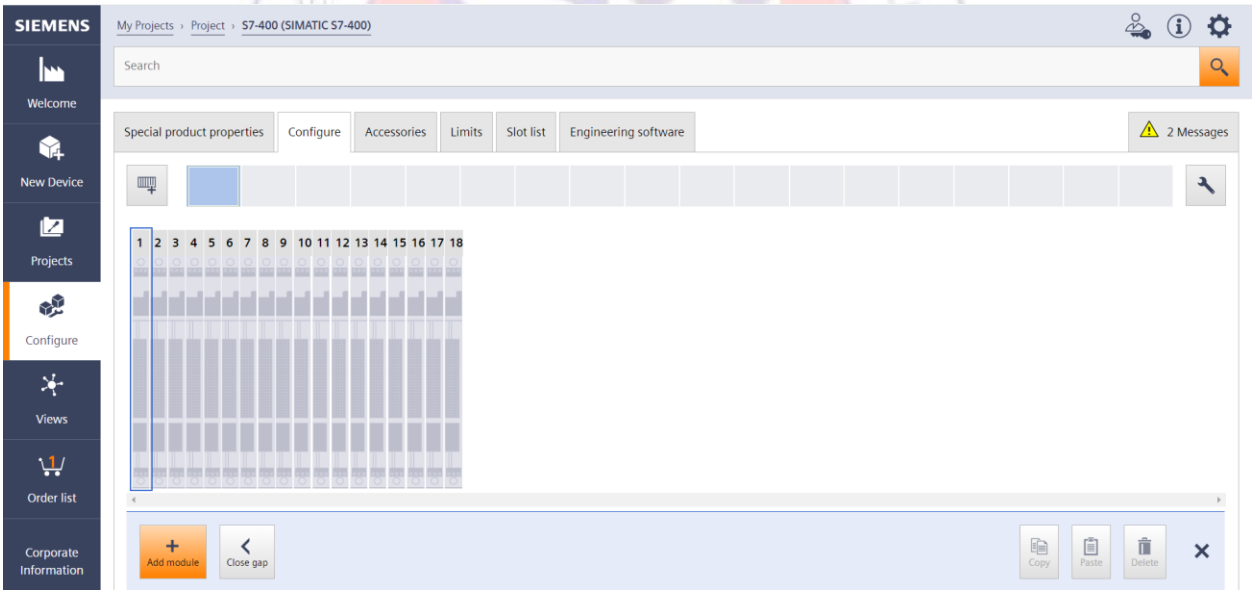


Figure 5.11 Controller Selection Screen

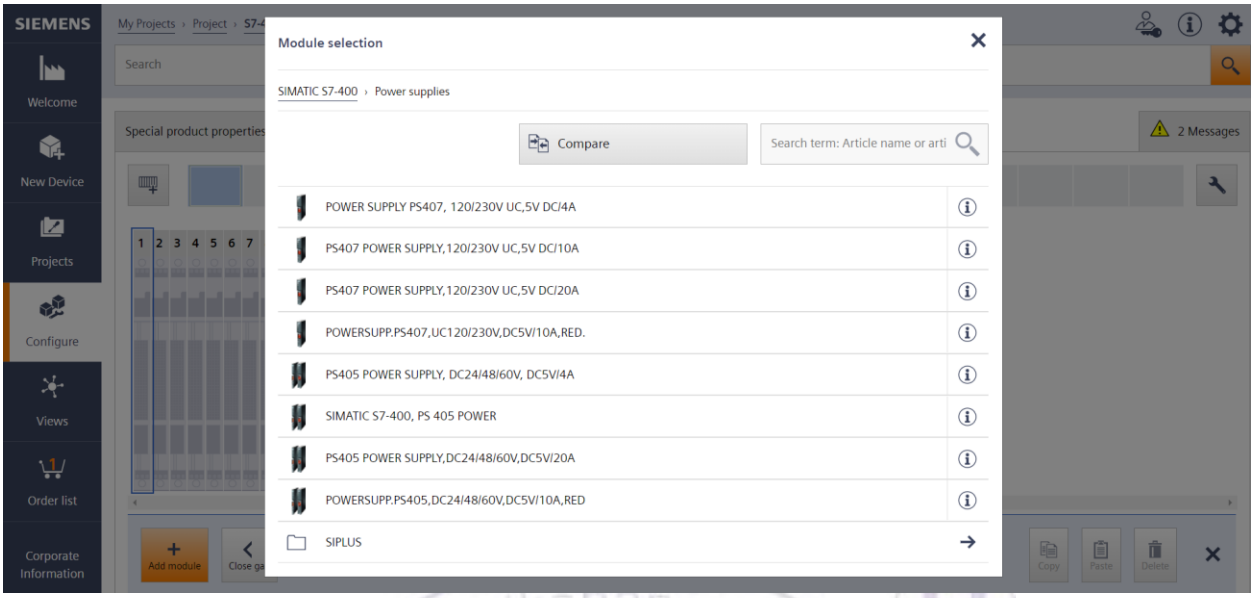


Figure 5.12 Power Supply Module Selection Screen

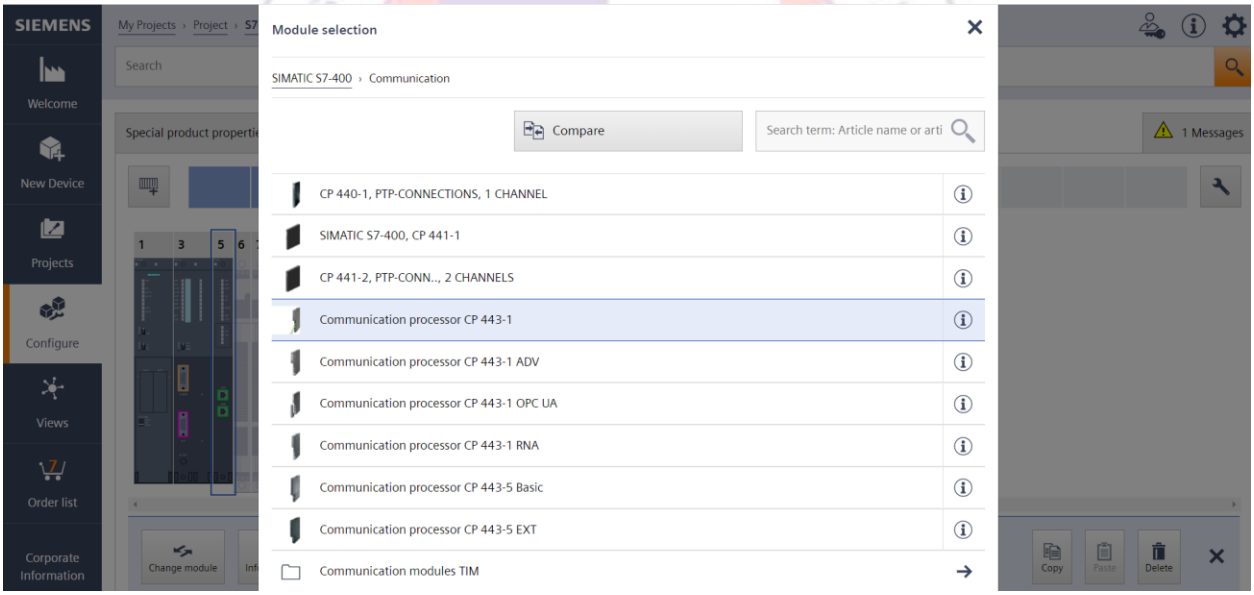


Figure 5.13 Communication Module Selection Screen

Figure 5.13 shows the controller simulated with the respective communication modules and shows the controller and IO modules configured is economical and satisfies space requirement.

5.2 Hardware Implementation

The hardware implementation of automated chiller plant has been carried out by configuring the controller in TIA portal for the calculated IO Points. The electrical panel components are selected based on the design calculations.

5.2.1 Process Block Diagram with PLC

For hardware implementations, communication between process levels, operator interfaces, and local control rooms i.e., SCADA established via a communication port and an Ethernet switch. PLCs with IO modules are configured in terms of digital and analog inputs and outputs available from field devices. Figure 5.14 shows the overall representation of the wiring.

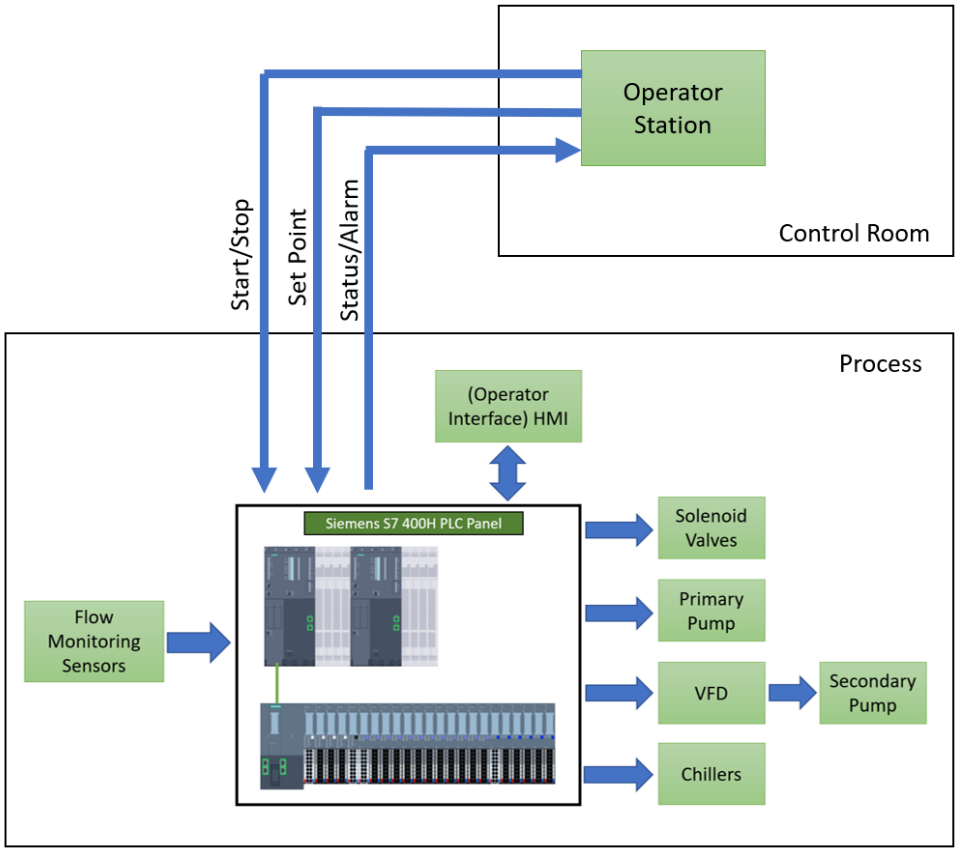


Figure 5.14 CPM Overall Representation

5.2.2 Control Panel Building

The hardware implementation of automated control of chiller and its testing is carried out by configuring the controller in TIA portal for the calculated IO Points. The electrical and control Panel components are selected based on the design calculations and the parts of the panel are

listed in the Table 5.2 with its description. Figure 5.15 and 5.16 shows the electrical control panel setup for the control and automation of the chillers.

Table 5.2 Panel Components

Sn.	Item	Description	Qty
1	HMI	TP1500 Comfort	1
2	Interface Module	IM 155-6 PN HF/3	2
3	Adapter socket	Bus Adapter 2xRJ45	6
4	Infeed AO	BU type A0, 16 push-in, 2 infeed term. separate (digital/analog, max. 24VDC/10A)	9
5	Infeed AO	BU type A0, 16 push-in, 2 infeed term. jumpered (digital/analog, 24VDC/10A)	36
6	PLC Module	SIMATIC S7-400H, 412-5H System bundle H-system with 1 x UR2-H, without memory card, 2 x PS 405 10A, 24/48/60 V DC, 4 x sync modules up to 10 m, 2 x sync cable 1 m, 2 x CPU 412-5H, 4 x buffer batteries	1
7	Ethernet Switch	SCALANCE XB005	2
8	Power Supply	SITOP PSU6200, 1-phase, 24 V DC/20 A	2
9	UPS	SITOP RED1200, DC 48 V/2 x 20 A	1
10	DI Module	DI 16x24VDC ST	8
11	DO Module	DQ 16x24VDC/0.5A ST	3
12	AO Module	AQ 4xU/I ST	12
13	AI Module	AI 8xI 2-/4-wire BA	16
14	IO Rack	ET 200SP, AI 8xU Basic	5
15	Memory Card	SIMATIC S7, RAM Memory Card for S7-400, long design, 1 Mbyte	2
16	Communications	Communications processor CP 443-1; 2x 10/100 Mbit/s (IE switch); RJ45 ports; ISO; TCP; UDP; PROFINET IO	2
17	IE Cable	IE TP cord RJ45/RJ45, 4x2, 0.5 m	10
18	Comm. Module	CM PTP communication module for serial connection RS422, RS485	1

Figure 5.15 PLC Control Panel

Figure 5.16 HMI Screen on Control Panel

The onsite equipments/instruments communicates with the controller based on the industrial protocols like Modbus, Ethernet, Profibus, Profinet etc. For the interface HMI is provided for the local control and monitoring of the chiller plant equipments.

5.3 Summary

The PLC program was been developed for chiller plant automation using ladder logic language, control panel was build according to the design calculations of IO points. The count of validated components in TIA portal configurations is carried out. The real time set up of automated machine, electrical panel and HMI integration was represented in the chapter.

Figure 6.2 Simulation Monitor Screen

Figure 6.1 shows the RLL network simulated for the validation of the automation from the inputs provided from monitor screen in Figure 6.2. The input selection and output command monitoring is also performed through the HMI screen as shown in Figure 6.3 to provide manual and automatic command for equipment mode selection. There are two modes for the equipment for the shown ladder logic that is Remote mode and Local mode. As the Remote mode is high, HMI input decides if in Manual mode or Auto mode, if Auto mode selected then HMI follows PLC command.

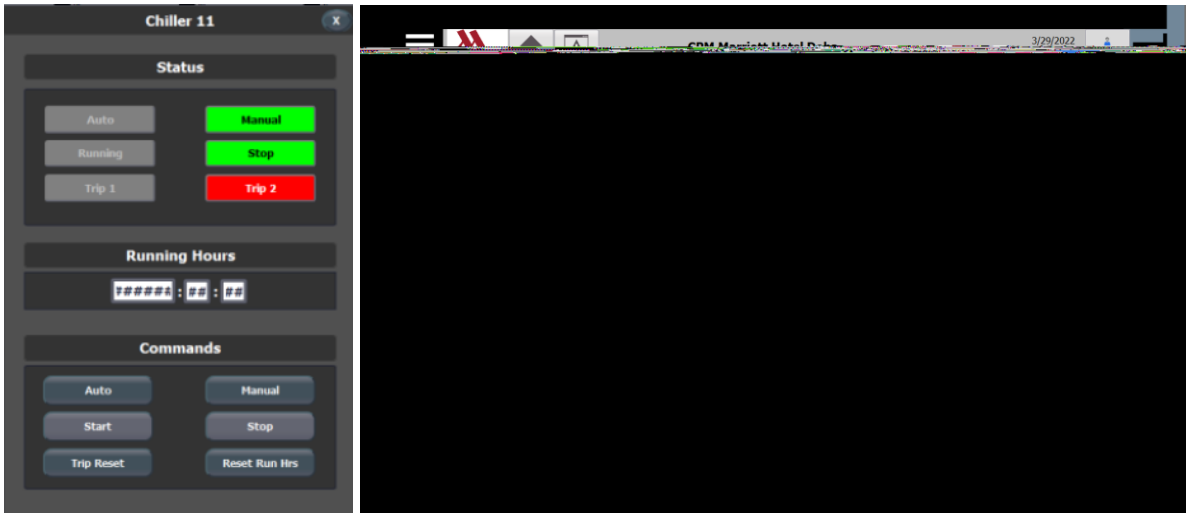


Figure 6.3 HMI Screen & Faceplate for Mode Selection

Following are the results for the simulation,

- The Simatic S7-400H controller is used to automate the process with the input output configuration pins available are 140 AI, 101 DI, 37 AO, and 31 DO.
- Based on the plant state 0 (i.e., Idle) or 1 (i.e., Start) and simultaneously the input selected from HMI screen for mode selection sets the rung energised (0=Manual mode, 1=Auto mode)
- Variable Set temperature has been considered as 12℃, based on this temperature difference is found.
- For variable temp diff between 0.3℃ and 2℃, start trigger has been set to 1 (high) for a preset delay of 1min and following respective pump, MOVs and chillers commands are set to 1 (high).
- Similar to the simulation for mode selection all other section of the program is simulated and tested by configuring it to the HMI.
- Similarly for variable temp diff between -0.3℃ and -2℃, stop trigger has been set to 1 (high) for a preset delay of 1min and following respective chiller, pump and MOVs are set to 0.

6.2 Summary

Based on the ladder logic developed for chiller plant automation, HMI Screens output was developed to configure the input status, feedback and output command to have manual and

automated access to the operation. The final testing was conducted, the PLC programming in ladder logic, results obtained after are indicated.

Chapter 7

CONCLUSION AND FUTURE SCOPE

In both commercial and home settings, chiller units have become a necessity. Contrarily, industrial automation tools offer a wide range of applications for controlling and monitoring machinery, power, etc. The advantages for monitoring and controlling chiller plants are improved by starting an automation process. HVAC businesses may simply automate using PLC and SCADA.

In this work, PLC and SCADA have been used to monitor and operate the chiller plant for a building's more noticeable operation. PLC is utilised as hardware at the remote end to monitor and read field instruments for the predetermined temperatures, pressures, and other parameters as well as to control the chiller equipment in accordance with predetermined instructions. The ladder logic created for PLC S7 400H programming is deployed for remote monitoring and control of the plant's numerous chiller units. By creating Graphical User Interfaces (GUI) utilising TIA portal software, SCADA/HMI may be operated remotely.

7.1 Conclusion

Following conclusions were drawn from the proposed project,

- The logic developed has been validated through the simulation in Siemens Simatic Manager Software.
- Also validated and confirmed through interfacing the HMI screens input using Siemens TIA Portal and WinCC Software.
- For the control strategy the PLC program is developed, it observed that automation helps optimize the process as well as helps reduce energy consumption.
- For the same plant working under normal strategy (manual mode) compared to auto mode based on programmed control strategy, about 25% less energy consumption is indicated (actual data during site commissioning).

7.2 Future Scope

The project can be implemented with add on technology to operate, control and monitor the chiller plant. Plant equipment and machines can be optimized using the operation data from

energy systems to modify the existing controller's information, Building Information Modelling (BIM) will be used to design control strategies. Following are some ways to carry out the same:

- A low-code programming for such event-driven applications is possible to develop using tool such as NODE-RED.
- Integration of SAP/ERP to the process for continuous report generation and data logging at the field, automation and management system level.
- A collaborative data system, and the BIM data is pushed to the cloud server, by developing building as a service (BaaS) model to provide a fully virtualized environment for services implementation, control, maintenance and usage.

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JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

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Development of PLC Logic and SCADA System for Chiller Plant Automation

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Abstract : Today, PLC applications are having a major impact on process engineering. PLC has entered this field with software and hardware for fail-safe, intrinsically safe, and process language-speaking solutions. Controls the entire system. The installation cost is not low, but it is possible to operate efficiently for a long period of time. Reduce operating costs and energy consumption. Chiller Units have become an essential requirement in industrial and domestic environments. On the other hand, industrial automation tools provide many applications to control and monitor equipment, power etc. By initiating an automation process, it improves the benefits of managing and controlling chiller plants. PLC and SCADA are easiest automation tool in HVAC industries. The Simatic S7-400H controller is used to automate the process with the rated supply of 24V DC, achieved by implementation of SMPS for the input voltage of 230V.

Index Terms **- PLC, Chillers, Automation, SCADA, HVAC, Simatic, SMPS**

I. INTRODUCTION

Heating, Ventilation, and Air Conditioning (HVAC) systems frequently consume the most energy in commercial buildings. More than 60% of the energy used in a typical office building is produced by the HVAC system [1].

In both commercial and home settings, chiller units have become a necessity. A typical chiller plant consists of a number of coolers, cooling towers, water pumps, and other related components. It is a sizable, intricate, and interconnected system [2]. Compressors, pumps, and fans are only a few of the chillers' motor-driven HVAC system components. Therefore, it is crucial to increase the energy efficiency of the fans, compressors, and pumps in the HVAC system, this is possible to achieve by a variety of methods [3].

However, there are numerous applications for industrial automation tools to control and monitor equipment, power, vehicle, telecommunications systems etc. By initiating an automation process, it improves the benefits compared to managing and controlling those plants manually [4]. PLC and SCADA are easy to use for automation in HVAC industries. The IEC standard, enables the programmer to use multiple programming languages in the same PLC, it is the main benefit of using PLC-based automation because it eliminates the need for proprietary implementation and allows different tasks to be implemented effectively using the most appropriate language. Hence for recommissioning, troubleshooting and rescheduling is no challenge [5].

In the past and even now, chiller plant operations have been frequently governed by rules. For instance, the coolant supply temperature is constant, and there are only as many active chillers as necessary to provide the cooling requirements. The relationship between the chiller cooling load and the chiller/condenser supply temperature is nonlinear. Due to the chillers' poor effectiveness at maintaining a steady supply temperature, energy is squandered, and occasionally two chillers use less energy than one. Therefore, chiller plant optimization is required for energy savings [6].

The optimization and control of chiller plant requires adjustments of multiple set points, primarily temperatures, and flow rates. In this work, PLC and SCADA have been used to monitor and operate the Chiller Plant for a building's more noticeable operation.

PLC has been utilized as hardware at the remote end to monitor and read field instruments for the predefined temperatures, pressures, and other parameters as well as to control the Chiller equipment in accordance with predetermined instructions. The many chiller units in the plant have been monitored and controlled remotely using the ladder logic created for programming PLC S7 400H. By creating Graphical User Interfaces (GUI) utilizing TIA portal software, SCADA/HMI are operated remotely.

II. CONTROL AND OPERATION USING PLC

2.1 Programmable Logic Controller (PLC)

A Programmable Logic Controller, or PLC, is a ruggedized computer used in industrial automation. PLCs are devices that allow control logic and instructions to be stored as programmes and executed by running the PLC with power that is supplied [4]. The programme, for instance, uses logical justifications such "if button is pressed, open valve," etc. Depending on the inputs and outputs, a PLC monitor and records run-time data such as machine productivity or operating temperature, initiate and terminate

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processes automatically, generate alarms in the event of a machine failure, and do much more [7]. The input interface, CPU, memory unit, and output interface are the four fundamental parts that make up a PLC's structure, Fig. 1.

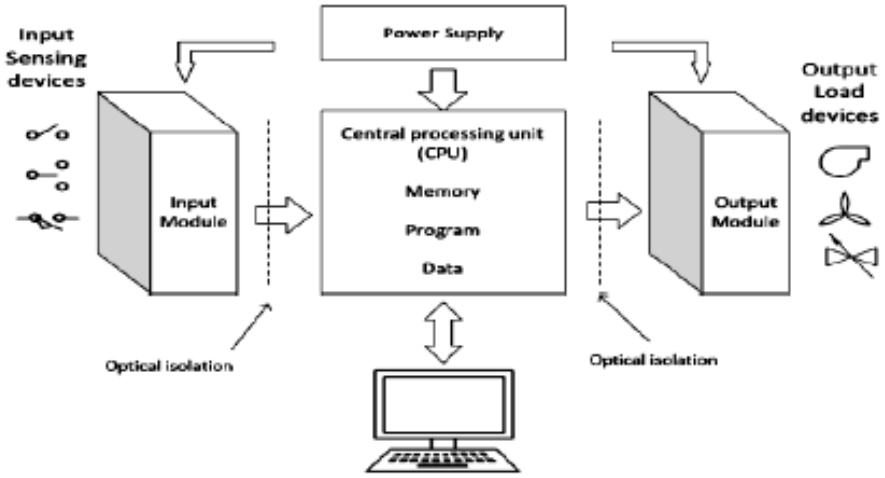

Fig.1. Components of PLC

Typically, PLC programs are created on a computer before being downloaded to the controller. Ladder Logic or "C" programming is supported by the majority of PLC programming software [6]. A classic programming language often used is called Ladder Logic.

2.2 SCADA & HMI Overview

Supervisory Control and Data Acquisition, or SCADA. In sectors like telecommunications, water and waste management, power, oil and gas refining, and transportation, SCADA systems are used to monitor and manage equipment or plants. These systems cover the data transfer between a SCADA central host computer and several Remote Terminal Units (RTUs) or PLCs, as well as between the central host and the operator terminals[8]. A SCADA system collects data (such as a pipeline starts to leak), sends the data back to a central location, and then notifies the control station that a leak has occurred. At this point, the control station starts the necessary analysis and control, such as by determining whether the leak is critical and presenting the data logically and efficiently.

By creating Graphical User Interface (GUI) for the selection of equipment like chillers and pumps as well as for monitoring, SCADA is utilised to operate remotely. HMIs are made specifically to act as a user-machine interface. An HMI, on the other hand, is a lot more tailored to industrial and process control systems. An HMI delivers real-time data of the site's instruments and equipment as well as a visual depiction of a control system.

2.3 Block Diagram

Figure 2 shows a conceptual block diagram that describes the structure and behavior of multiple components and network devices, hardware of a control system. It shows the connection between PLC, HMI, IO racks and field equipment and control instruments.

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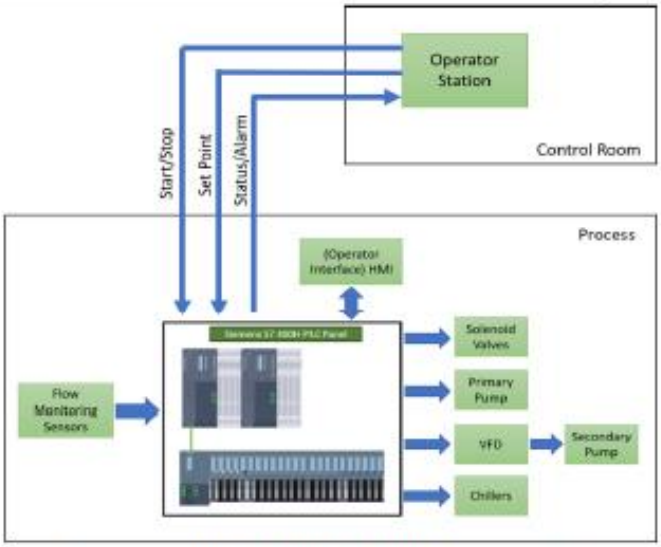

Fig.2. Control Block Diagram

III. Hardware Structure And Network Establishment

All of the hardware that has been used in the system is described in this section. The network diagram in Fig. 3 displays the components.

- Siemens PLC S7-400H
- HMI TP 1500 Comfort
- IO Racks.
- Ethernet Switch
- Field equipment like chiller, pumps and valves
- Control Instruments like temperature sensors, pressure transmitter etc.

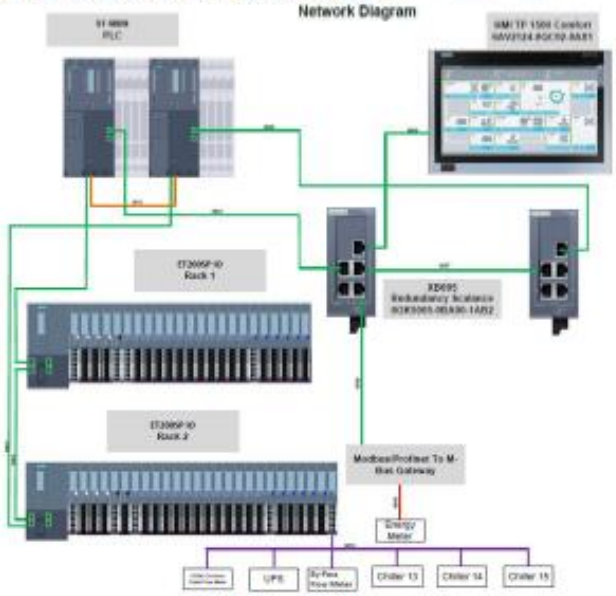

Fig.3. Network Diagram

3.1 IO Point Scheduling

I/O Point Scheduling is the important factor in the selection of controller, Simatic controllers are chosen depending on the inputs and outputs. Based on the load calculation and equipment scheduling, the input output configuration pins available are 140 AI, 101 DI, 37 AO, and 31 DO. The IO points is connected to the controller through additional remote IO modules.

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3.2 Control Panel Design

Electrical control panel is a combination of electrical devices and switchgears used to power the PLC module and communication network to control the various equipment at the chiller plant.

Power Supply Unit (PSU) has been selected based on the connected load that is PLC, IO modules, Field Instruments if required. Based on Simatic PLC a 24V DC and about 5A PSU is suitable for the design. Rating of MCB is 2 times the rating of module to be protected i.e., For 16 Digital inputs module with 0.5A rating, I= 0.5*2*3= 3A. In similar manner MCB, terminals and relays are calculate based on number of DI, AO, AI and DO module.

IV. Software Structure

The Ladder Logic Program for the automation of Chiller Plant has been developed using Totally Integrated Automation Portal. The ladder logic program is written for the controller selected i.e., 412-5 H CPU in the Siemens TIA Portal.

4.1 The Algorithm

The overall algorithm is depicted in the Fig. 4 ,5 and 6. The algorithm demonstrates the behavior of the controller it consists of the following:

- Check the mode of operation selected by operator
- Checking the temperature difference of the inlet and outlet pipe
- ON and OFF of the modulating Valve
- Start and Stop of the pumps and chillers
- Maintaining the process for the run cycle

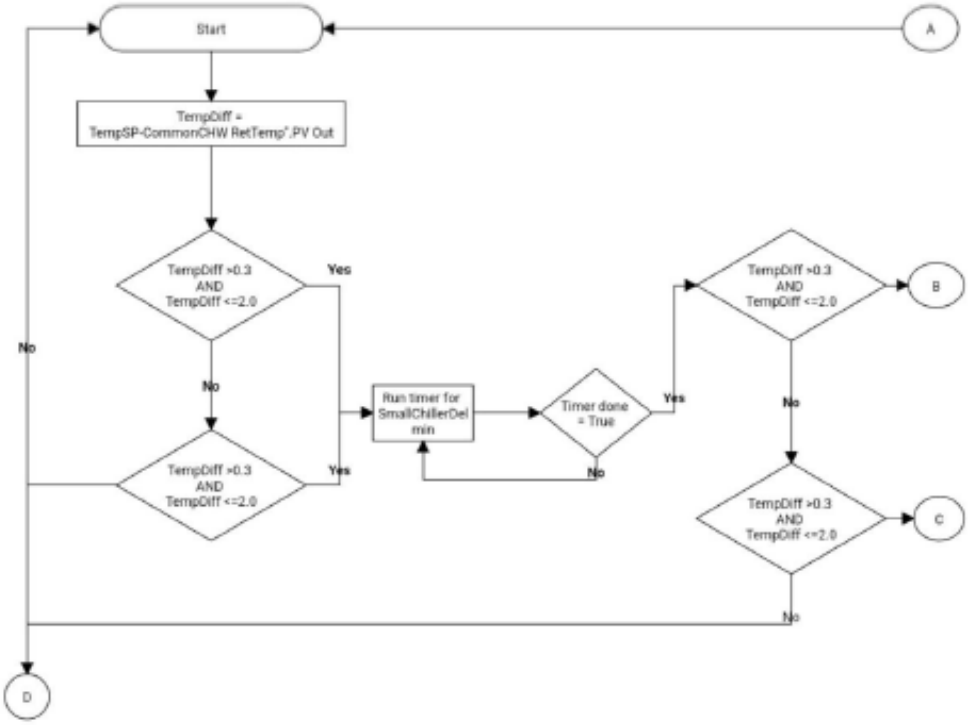

Fig.4. Comparison of Temperature Difference

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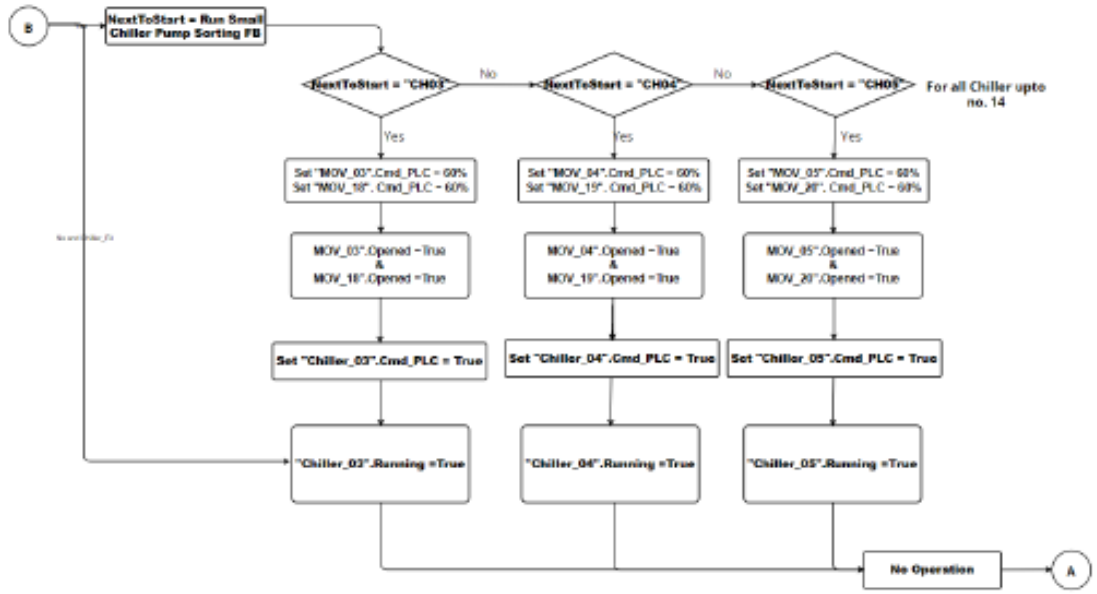

Fig. 5. Starting of a Chiller

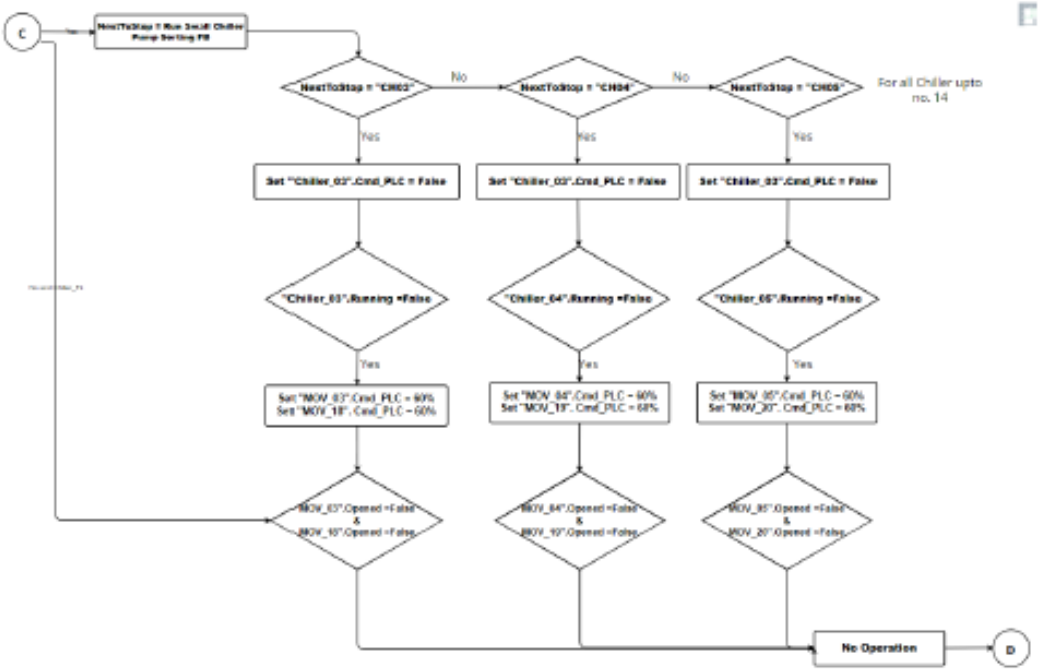

Fig. 6. Stopping of a Chiller

4.2 PLC Program

The controller selected i.e., S7-400H has been simulated in TIA portal with the IO modules configured as per the requirement of the project, here Inputs are 241 and Outputs are 68. The steps involved in selection of controller is as shown in Fig. 7 and Fig. 8.

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Fig. 7. Controller Configuration

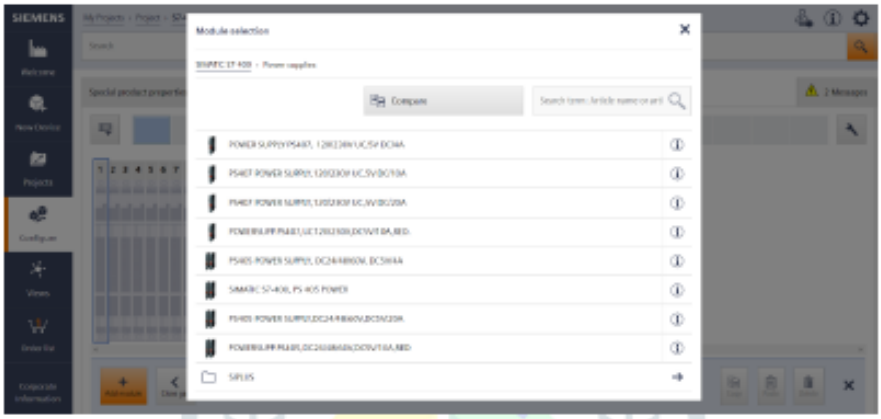

Fig. 8. Component Selection

The S7-400H PLC has been used and programmed to carry out all automation activities, including automated mode operation, as illustrated in Fig. 9, and manual control mode is also depicted. TIA Portal V15 is used for programming purposes.

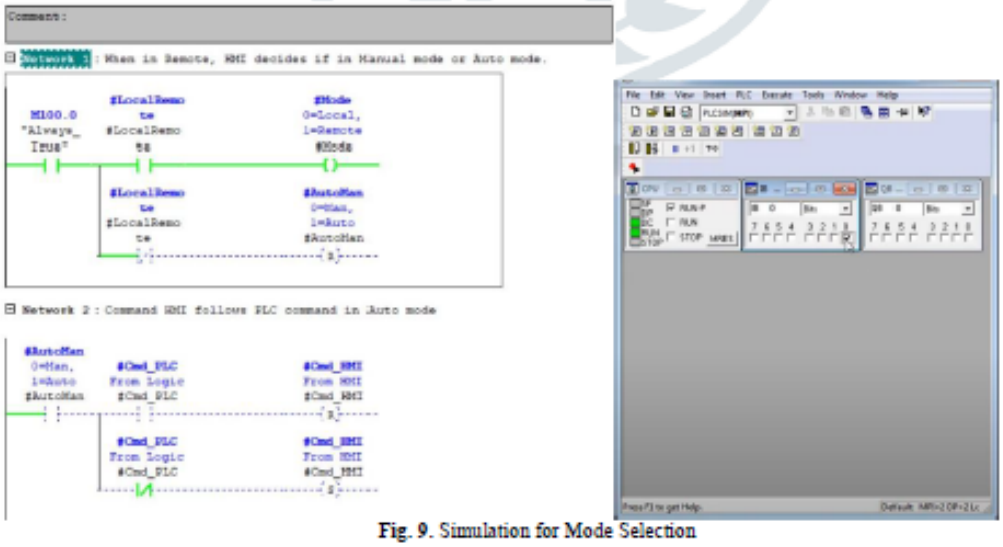

Fig. 9. Simulation for Mode Selection

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4.2 HMI Implementation

The input selection and output command monitoring is carried through the HMI screen as shown in Fig. 10 to give manual and automatic command for equipment mode selection. For the equipment used in the displayed ladder logic, there are two operating modes: remote mode and local mode. Depending on whether Manual mode or Auto mode is selected by the HMI input as the Remote mode is high, the HMI has to execute PLC commands.

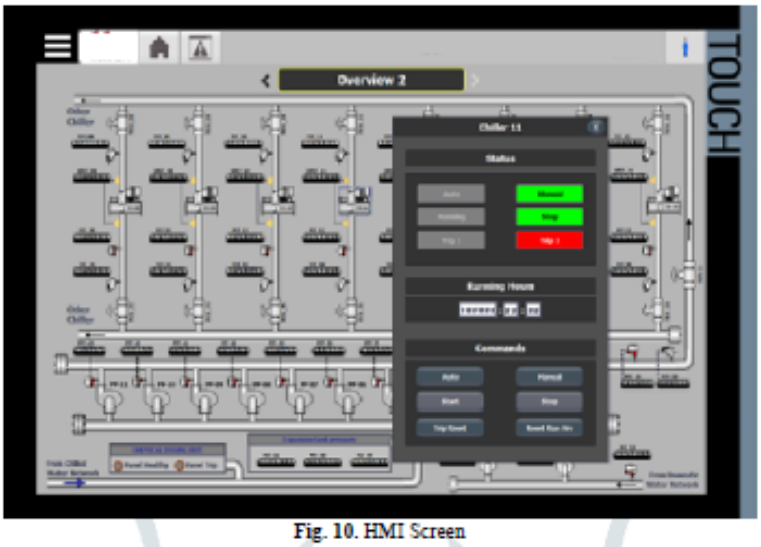

Fig. 10. HMI Screen

V. Results

The Simatic S7-400H controller has been used to automate the process with the input output configuration pins available are 140 AI, 101 DI, 37 AO, and 31 DO. Based on the plant state 0 (i.e., Idle) or 1 (i.e., Start) and simultaneously the input selected from HMI screen for Mode selection sets the rung energized (0=Manual mode, 1=Auto mode). Variable Set temperature is at 12℃, based on it the temperature difference is found.

For variable Temp Diff between 0.3℃ and 2℃, Start Trigger is set to 1 (high) for a preset delay of 1min and following respective pump, MOVs and chillers commands were set to 1 (high). Similar to the simulation for mode selection all other section of the program is simulated and tested by configuring it to the HMI. Similarly for variable TempDiff between -0.3℃ and -2℃, Stop Trigger is set to 1 (high) for a preset delay of 1min and following respective Chiller, Pump and MOVs were set to 0.

VI. Conclusion

In this work, PLC and SCADA have been used to monitor and manage the Chiller Plant for a building's more noticeable operation. PLC is utilized as hardware at the remote end to monitor and read field instruments for the predetermined temperatures, pressures, and other parameters as well as to regulate the chiller equipment in accordance with predetermined instructions.

The Simatic S7-400H controller is used to automate the process with the rated supply of 24V DC, achieved by implementation of SMPS for the input voltage of 230V. The input output configuration pins available are 140 AI, 101 DI, 37 AO, and 31 DO. The IO points is connected to the controller through additional remote IO modules. The communication is established between electrical panel with controller and the local SCADA i.e., HMI using 2 Ethernet switch. The PLC program that has been developed for the control philosophy, it observed that automation helps optimize the process as well as helps reduce energy consumption.

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Major Project: Phase-II Report

on

DESIGN AND IMPLEMENTATION OF SPEED CONTROL OF SWITCHED RELUCTANCE MOTOR

Submitted by

KAVANA E

USN: 1RV20EPE04

Under the Guidance of

Dr. Rudranna Nandihalli / Dr. Anitha G S,
Professor and HOD (Retd.) / Associate Professor,
Department of EEE,
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Bengaluru – 560059

Dr. Narasimha M V
Chief of Advance Engineering
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Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY
in
POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

2021-2022

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Bengaluru– 560059

CERTIFICATE

Certified that the project work titled **"Design and Implementation of Speed Control of Switched Reluctance Motor"** carried out by **Kavana E, USN: 1RV20EPE04**, a bonafide student of **RV College of Engineering®, Bengaluru** submitted in partial fulfilment for the award of **Master of Technology** in **Power Electronics** of **RV College of Engineering®, Bengaluru affiliated to Visvesvaraya Technological University, Belagavi** during the year **2021-22**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

Dr. Rudranna Nandihalli / Dr. Anitha G S	**Dr. S G Srivani**	**Dr. K. N. Subramanya**
Professor and HoD (Retd.) / Associate Professor	Head of Department,	Principal,
Department of EEE,	Department of EEE	RVCE, Bengaluru–59
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DECLARATION

I, **Kavana E**, student of fourth semester **M.Tech** in **Power Electronics**, **Department of Electrical and Electronics Engineering**, RV College of Engineering®, Bengaluru declare that the project titled **"Design and Implementation of Speed Control of Switched Reluctance Motor"** has been carried out by me. It has been submitted in partial fulfilment of the course requirements for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering®, Bengaluru affiliated to Visvesvaraya Technological University, Belagavi during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

Date of Submission: 18/07/2022

Kavana E.

Signature of the Student

Student Name: Kavana E

USN: 1RV20EPE04

Department of Electrical and Electronics Engineering

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TO WHOMSOEVER IT MAY CONCERN

This certificate is being awarded to Ms. Kavana E (**USN:** 1RV20EPE04), a student pursuing an M.Tech in Power Electronics from **R.V. College of Engineering** has done her internship with our Research and Development Department, Bangalore from the 1st of September 2021 to the 30th of June 2022.

Her Project Title is "Design and Implementation of Speed Control of Switched Reluctance Motor" and has completed the project under the guidance of Dr. Narasimha MV, R&D.

During the tenure of the internship at Ampere, her conduct, character, and interest to learn were found good.

We wish her all the best in her future endeavors.

Thanks & regards,

Vithal Acharya
Head – Human Resources
Greaves Electric Mobility Pvt Ltd

ACKNOWLEDGEMENT

Any achievement, be it scholastic or otherwise does not depend solely on the individual efforts but on the guidance, encouragement and cooperation of intellectuals, elders and friends. A number of personalities, in their own capacities have helped me in carrying out this project titled, **"Design and implementation of speed control of Switched Reluctance Motor**". I would like to take this opportunity to thank them all.

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ABSTRACT

Currently, many electrical applications use brushless DC motors (BLDCs) and DC motors. SRM, generally known as doubly salient variable reluctance machine, gained the attention of researchers and industries from the past few decades because of its rugged and simple construction, high torque to inertia ratio, thermal robustness, etc. They are widely used in variable speed drives due to its several advantages. SRM provides opportunity to explore the performance studies with structural modification, converter structure and controller design. For the Alternating current or the direct current drives, it is the customer's first choice due to its easy maintenance.

An asymmetric bridge with single phase bridge rectifier was used to keep the output voltage regulated. An asymmetric bridge mainly consisted of IGBT based semiconductor diode was used that operates at a frequency of 15 kHz. The gating pulse for IGBT was provided from the DSP controller. The SRM was an 8 stator slots and 6 rotor slots that consists of inbuilt hall sensors. Hall sensors were mainly used for detecting the speed and position of rotor. The actual speed was compared to the reference speed. An error generated that was supplied to the PID controller that was varied and the pulse width modulation generator that generates the pulses and was directly supplied to the IGBT asymmetric bridge and the generated pulses was supplied to the SRM. An error signal that was generated was sent to the controller block, the error detector compared the reference speed with the actual speed. In accordance with the error signal, the controller sends the converter the suitable control signal. Through appropriate excitation of the corresponding windings in the stator, the converter regulates the motor's speed.

The speed control of SRM was performed using MATLAB/SIMULINK software by varying the values of P, PI and PID controller. The simulation for speed control of SRM was simulated for 1500rpm and the obtained speed was 1500rpm. The hardware for the speed control of SRM was tested. The hardware for the speed control for open loop with the reference speed was 1500rpm but obtained speed was 1420rpm and for open loop with the reference speed of 1500rpm but obtained speed was 1460rpm. The proposed speed control of SRM was tested for both no-load and full-load condition with reference speed of 1500rpm and the obtained speed at no-load was 1644rpm and at full-load was 1180rpm respectively.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Kavana E, Dr. Rudranna Nandihalli, "Speed Control of Switched Reluctance Motor", *In Journal of Emerging Technologies and Innovative Research (JETIR)*, pp 266-270, Vol. No. 9, Issue No. 6, June 2022.

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GLOSSARY

ADITC	Advanced Direct Instantaneous Torque Control
DITC	Direct Instantaneous Torque Control
DSP	Digital Signal Processor
SMPS	Switch Mode Power Supplies
SRM	Switched Reluctance Motor
TSF	Torque Sharing Function
UPS	Uninterruptible Power Supply

Chapter 1

INTRODUCTION

A Switched Reluctance Motor (SRM) is also called as variable reluctance motor. They work on the principle of variable reluctance is singly excited and doubly salient machine. The SRM is being used from the year 1838. The SRM is used up-to its maximum potential after the invention of power electronic components [1]-[3]. SRM is a motor that runs by using reluctance torque and so it is also called as variable reluctance motors. The working and construction of SRM is same as some of the conventional motors like induction motor, synchronous motor and other types of motors that operates in all the four quadrants [4]. It consists of many features like that of motors Induction motor drives, DC motor drives and permanent magnet brushless DC motor. SRM is rugged, simple to construct, fault tolerant capability and economical compared to other motors like induction and synchronous motor. Since they possess high peak torque to inertia ratio, high speed applications and in various industries [5]-[9].

SRMs are used in industrial application, servo, electric propulsion applications. Construction of SRM is simple, it includes some of the features like concentrated winding that is comparatively less on the rotor [10]-[13]. The functional characteristics of SRM is that they lend to programming of speed and torque profiles. The converter includes lesser number of Insulated Gate Bipolar Transistor (IGBT) or Metal Oxide Semiconductor Field Effect Transistor (MOSFET) the switching devices as compared to induction motor or any other conventional motors. So, due to these reasons the drive system of SRM is highly simple to construct, reliable and economical [14]-[19].

The presence of nonlinear behaviour of SRM makes it very difficult and complex to control. SRM is suitable for high-speed applications mainly due to its robust nature. The salient poles include concentrated windings on rotor and stator [20]-[23]. Windings are not present on the rotor. The stator and rotor both contain salient poles but only stator support windings. The rotor laminations of the motor are made of steel to get required number of poles on the rotor. The rotor does not consist of rotor windings or squirrel cage bars or either permanent magnet. The number of stator slots and the number of rotor poles may be different [24]-[29].

1.1 Overview

Nowadays, SRMs are more appealing because of their straightforward design. It not only includes features of a salient pole stator including the concentrated coils, but also allow

earlier winding and shorter end returns compared to other types of motors, but also features a salient pole rotor, absence of conductors or magnet [1]. As a result, SRM is one of the important options for many applications since it is highly dependable, less expensive, has a high-speed capacity, and has a high torque to inertia ratio.

The 8/6 SRM consists of built-in hall sensors with loading. An asymmetric bridge including 4 phase bridge rectifier is used to keep the output voltage regulated. An asymmetric bridge is mainly of Insulated Gate Bipolar Transistor (IGBT) based semiconductor diode is used that operates at a frequency of 15 kHz. The gating pulse for IGBT is provided from the DSP controller. An asymmetric bridge consists of 4 phases [4] [5]. The SRM is an 8 stator slots and 6 rotor slots that consists of inbuilt hall sensors. Hall sensors are mainly used for detecting the speed and position of rotor. The speed of the motor is measured using hall sensor, so the actual speed of motor is measured. The actual speed is compared to the reference speed. An error is generated that is supplied to the PID controller [7] [8]. The pulses are varied based on the error signals. The pulse width modulation generator generates the gating pulses and is directly supplied to the SRM through IGBT asymmetric bridge converter [10].

1.2 Specific Details

There are different number of stator slots and number of rotor poles like 6/4 or 8/6 or 10/8. The number of stator slots and the number of rotor slots are not same. Here 8 stator slots and 6 rotor poles is used. The 8/6 SRM consists of built-in hall sensors with loading. An asymmetric bridge with 4 phase bridge rectifier is used to keep the output voltage regulated [2]-[6]. An asymmetric bridge is mainly of Insulated Gate Bipolar Transistor (IGBT) based semiconductor diode is used that operates at a frequency of 15 kHz. The gating pulse for IGBT is provided from the DSP controller. An asymmetric bridge is that mainly consists of 4 phases namely phase A, phase B, phase C and phase D respectively [8].

MATLAB/SIMULINK software is used to simulate the speed control of the SRM. 240V DC is used as the supply voltage in the circuit. For the speed ranges, the turn on and turn off angles supplied to the converter are 45° and 75°, respectively. The hysteresis band is selected to be 10A, and the reference current is 200A [6]. Applying the step reference to the regulator input initiates the SRM. The properties of the load affect the acceleration rate. A very light load is chosen to reduce the starting time.

The motor runs in 3 stages:

Initiation Sequence 1: Phases B, C and D are energized.

Initiation Sequence 2: Phases C and D are de energized and only phase B is energized to align the motor.

Commutation Sequence: The motor after previous phase is commutated in either clockwise or anti clockwise by energizing the phase A, B, C and D in either sequence.

The PWM Generator generates necessary PWM for the IGBTs. The entire programming is performed by using Simulink Embedded Coder and the C2000 Simulink blocks that directly program the TMS320F28379D controller used [9].

Hardware for speed control of SRM is performed for 8/6 SRM with 8 stator poles and 6 rotor poles for 1 kW motor [12]. The hardware is implemented for both open loop and closed loop condition. Under open loop condition the reference speed is maintained at 1500 rpm and the measured value is 1428rpm at 200VAC. Under closed loop condition, here also the reference speed is maintained at 1500rpm, the measured speed is 1460rpm for 210VAC.

1.3 Literature Review

The simulation of speed control motors for SRM using MATLAB/ Simulink. Controllers P, PI, and PID is used for simulation and after correcting the correct trial and error, the PID controller provided the best solution in terms of reducing resolution time, eliminating solid error and reduce speed overshoots [1]-[4].

An 8/6 pole, 4-phase and 75kW SRM drive based 32-bit digital signal processor (DSP) TMS320F2812 is designed. The controller design, its details and analysis are discussed. In addition, it is intended to solve the nonlinear problems of the SRM by Fuzzy-PI hybrid algorithm is used to speed control of the motor and the phase current. Test results show that the software and hardware design of the SRM drive system are reasonable, and the Fuzzy-PI double closed loop control strategy is correct and feasible [5]-[9].

The adaptive speed control of SRM is defined and implemented using DSP. The design of controller is based on PWM control scheme that is used for the current controller of SRM. To see the speed controller, the speed reference is calculated as the function of the current machine. From test results show that all modified speed controls provide transient and steady state results [10]-[14].

The demand for SRM is gradually increasing due to its similar benefits like less weight, low cost, increased efficiency, high initial torque as well construction is rugged compared to other conventional motors. Complete reduction of SRM drive costs is made at least switching devices on the power converter. The AC split supply converter is an alternative for an asymmetric bridge converter. This paper is about the functionality of the AC split converter as well an asymmetric bridge converter with 8/6 SRM motor used MATLAB simulation. The parameter of the 8/6 SRM motor is determined by Ansys / Rmxprt. So, split AC the delivery converter at lower cost and better performance [14]-[19].

SRM drive includes an amazing feature, that makes it attractive at high speeds at low voltage application. A new driving circuit is introduced from the bridge family using a resonant circuit during discharge. The new topology provides a faster rate of current releases. In the new circuit, the capacitor is connected to the series by motor windings. This capacitor is charged directly through the use of motor phase phases during phase closure times. In addition, the power supply circuit creates a trapped power in the resonant capacitor to be obtained by a single quadrant chopper consisting of a transistor, capacitor and diode. This topology provides the fastest fall rate of the current phase, that allows the engine to operate at high speeds [19]-[25].

Currently, most power systems use brushless DC motors (BLDCs) and DC motors. Recently, SRM is the best alternative for traditional motors and BLDC motors due to increased efficiency, error tolerance, reduced cost and exceptional speed. Motors with switching resistance SRMs are used in many industries such as automation and aerospace as they own high torque. It includes no windings on the rotor side. For current switch drives or direct current drives, it is the customer's choice due to easy maintenance. The advantages of motors are the flexibility and simple construction [26]-[30].

1.4 Motivation

The motivation of the project is

- SRMs are the most appropriate motors for various applications, due to robust construction, cost is less, high-speed capability, great efficiency, and dependability over a broad speed range.
- The SRM is more advantageous as compared to the induction motor and permanent magnet synchronous motor (PMSM) because of absence of magnet and rotor structure is robust that allows operations of motor at high speed and fault tolerant.

- PID controller includes some of the features like settling time is less, control is faster, and low-cost application, to eliminate steady-state error and reduction of speed overshoot.

1.5 Problem Statement

The problem statement of the project is

- All motors are preferred to operate in
  - wide range of speed
  - desired speed based on the application
- To control the speed of the motor, suitable speed control techniques are analysed and selected.
- PID controller is chosen because it provides many features like settling time is less, control is faster, and low-cost application, to reduce speed overshoot and remove steady-state inaccuracy.

1.6 Objectives

The main objective of the project is to

- Design a 4phase asymmetric bridge converter using PSIM.
- Design a 3phase bridge rectifier using MATLAB/Simulink.
- Closed loop simulation of speed control of SRM by using P, PI and PID controller using MATLAB/Simulink software.
- Develop the hardware for speed control of SRM for no-load and full load for open loop condition.
- Comparison of simulation and hardware results.

1.7 Organization of Report

The project work is organized in seven chapters.

Chapter 1: Introduction

This chapter consists of literature, problem definition, objectives, motivation behind carrying out this project and the methodology.

Chapter 2: Switched Reluctance Motor drives

This chapter consists of basics of SRM drives. The operation and the converters of SRM drives, its control is discussed.

Chapter 3: Block diagram and methodology

This chapter consists of the proposed converter block diagram with explanation of working and methodology.

Chapter 4: Specification and design details

This chapter represents the design details of forward converter and protection circuits.

Chapter 5: Simulation and hardware implementation

This chapter consists of simulation of SRM for speed control using MATLAB/SIMULINK software and Hardware Implementation of the circuit

Chapter 6: Results and discussion

This chapter consists of the simulation and hardware of the proposed speed control of SRM.

Chapter 7: Conclusion and future scope

This chapter consists of overall conclusion drawn from the project and the future works that can be carried out.

References include the list of references referred in the successful completion of the project.

Chapter 2

SWITCHED RELUCTANCE MOTOR DRIVES

The chapter explains in detail about the Switched reluctance motor, its construction, and working of converters used in SRM drives, various control techniques, advantages, disadvantages, and applications.

2.1 Switched Reluctance Motor

SRM, also known as a variable-reluctance motor, is used in wind energy systems and industrial applications. It inherits the capacity to function at extremely high speeds because of its hardy behaviour and straightforward architecture. It is very less sensitive temperature changes and fault tolerant capability is remarkable. SRM are used extensively in various applications like phonograph turntables and clocks earlier but now-a-days, amidst of rising high importance on energy efficiency, SRM is taking more value in industrial, commercial appliances etc., In this chapter an overview of SRM, its operation, applications, and differences from other motors is discussed.

To understand SRM in a better way, the detailed definition and information of each and every word used with SRM is discussed.

- **Switched**: It describes the location of magnetic field of the rotor. The rotor location continuously spins from current location to the adjacent next location after it is switched.
- **Reluctance:** It is an engineering term that refers to the presence of electromagnetic field. The steel part located close to field remains reluctant and un-aligned to the field provided. Electromagnetic field (EMF) exerts a strong force onto to the steel part nearer to its alignment inducing invisible magnetic field.
- **Switched Reluctance (SR) motor**: It is an electromagnetic rotating device. The ability of an object to move to a location that depends on the inductance of the exciting coil is the way torque is created. The exciting winding's inductance is at its highest level. Manufacturers of SRMs assert that the products outperform normal induction motors and other adjustable speed motors in terms of performance, dependability, affordability, and efficiency.

2.2 Construction of SRM

Stator windings of SRM consists of wound field coils as in case of a DC motor. Permanent magnets or coils are not present in the rotor. It consists of a salient pole rotor that is solid

and is made up of laminated steel that is soft magnetic material. The magnetic poles are either projected or extended. The stator winding receives power. A force that attempts to align the rotor pole with the closest stator pole is produced by the magnetic reluctance of the rotor. The magnetic field causes the stator to lead the rotor forward, and in order to provide continuous rotation, the electronic control system continuously switches the windings on successive stator poles. SRM employs a position sensor to determine the angle between the rotor and the stator to create continuously variable pulses rather than the mechanical commutator to switch the winding current [3]. This is completely different from other types of motors that energize the winding at a particular sequence. In SRM magnetization of rotor is stationary salient North Pole retains so the induction motor rotates at a comparatively lesser speed of motor, so the slip obtained is less. SRM in the absence of slip makes it is easier to notice the position of rotor, the motor to be stepped arbitrarily slowly.

The construction of the SRM is shown in Fig 2.1. This motor consists of 6 stator slots and 4 rotor poles. The design of the stator is made up of steel stampings using silicon inside projected or extended poles. The poles in stator are either an odd number or an even number. Most of the electric motor's possess an even number of poles within the stator that own field coils.

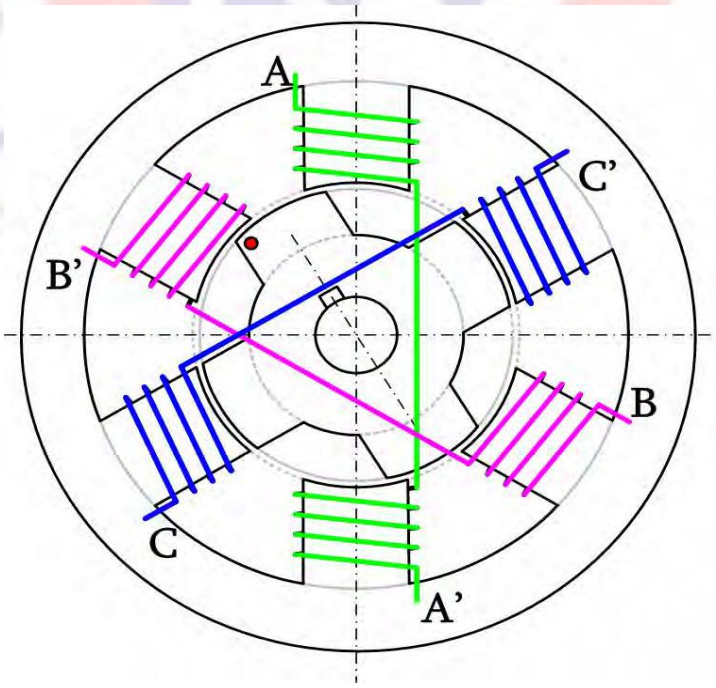


Fig 2.1: Construction of SRM

The poles that are opposite to the field coils are connected in series. So, the magneto-motive forces are additive that are called phase windings. Set of coils or a single coil to comprise

phase windings. Each winding is connected to the motor terminal, and these are properly connected toward the output terminals of a switching circuitry of power semiconductor. The input is a DC supply [6]. The rotor design is performed by using Silicon (Si) steel stampings. The rotor stampings poles are externally projected. It is different from stator poles. In most of the available existing motors, the poles of the rotor are 4 otherwise 6. The number of stator poles are either 6 or 8 [6]. The standard number of stator and rotor poles is either 6/4 or 8/6. 10/8 is used very rarely. The number of poles is selected either based on the rating of the motor required or based on the specific applications. The rotor shaft holds firmly on to position sensor. Entire power semiconductor circuit is operated and mainly controlled by the signals attained from this sensor [7].

In SRM both stator and rotor include an extended or projected pole and is designed with soft iron and as well as Si stampings. Stampings reduces hysteresis loss. The stator includes field winding and rotor doesn't contain any field winding. In the stator, each and every winding is connected in series through the opposite poles. It increases magneto-motive force (MMF) of the circuit.

The advantages of SRM are:

- Construction is robust and simple
- Absence of windings on rotor
- Absence of brushes and slip rings results in lesser maintenance
- Absence of permanent magnet (PM) in both stator and rotor
- Ventilating system is very simple so motor cools effectively
- Switching circuit is simple due to the use of Power semiconductor devices
- Torque developed doesn't depends on the polarity of current.

The disadvantages of SRM are:

- Windings of stator is capable of carrying magnetizing current, results in setting up of flux in the air gap
- At high-speed operations, the torque developed includes undesirable ripples
- For high speeds, current waveform consists of undesirable harmonics
- Large size of capacitor is required
- Size of motor is more as compared to the size of induction motor

In SRM applications cost, energy and efficiency plays an integral role. SRM motors of power ratings that varies from 5 to 22 kW are commercially available for many applications. Applications are as follows:

- Domestic appliances include fans, washing machines, and vacuum cleaners
- Machine tools: drill machines and lathes
- General equipment, including pumps, fans, and compressors
- Food-mixing equipment
- Conveyors, lifts, and winches are lifting devices
- Wind turbine rotor blade load control for power generation equipment
- Machines for paper mills
- Rolling mills for metal
- Equipment for wrapping and unwinding coils

2.3 Control Techniques

The various control techniques available for SRM drive are,

- Torque control
- Current control

2.3.1 Torque Control Method

Current Control, Angle Control, Direct Instantaneous Torque Control (DITC), Torque Sharing Function (TSF), and Advanced Direct Instantaneous Torque Control (ADITC) are some of the control techniques for SRM. The control methods are used for various purposes since torque ripple is less, noise is low, simpler model and higher efficiency.

TSF is primarily used to divide the total torque among all the motor's phases; the reference torque or supplied torque is equal to the sum of the torque in each of the phase's separate components. Since numerous functions meet the Torque Ripple Minimization (TRM) criteria, the selection of TSF is not particularly uncommon [5]. The commonly used control method is TSF because different types of waveforms like linear, cubic, sinusoidal, exponential curves signals are analysed. Modified TSF is preferred for the optimal implementation in SRM drive, so that it provides the minimum rate of change of flux linkage to reduce square RMS current [11]. The typical profile of the modified sinusoidal TSF is as shown in Fig 2.2. The modified sinusoidal TSF depends on switch-off angle (θ_{off}), switch-on angle (θ_{on}) and over-lap angle (θ_{ov})as follows,

$TSF\ (\theta) = 0, (0 \leq \theta \leq \theta_{on})$……(2.1)

$$TSF\ (\theta) = \frac{T_e}{2} - \frac{T_e}{2}\cos\frac{\pi}{\theta_{ov}} * (\theta - \theta_{on}),\ (\theta_{on} \le \theta \le \theta_{on} + \theta_{ov}) \quad \text{.....(2.2)}$$

$$TSF\ (\theta) = T_e,\ (\theta_{on} + \theta_{ov} \le \theta \le \theta_{off}) \quad \text{.....(2.3)}$$

$$TSF\ (\theta) = \frac{T_e}{2} + \frac{T_e}{2}\cos\frac{\pi}{\theta_{ov}} * (\theta - \theta_{off}),\ (\theta_{off} \le \theta \le \theta_{off} + \theta_{ov}) \quad \text{.....(2.4)}$$

$$TSF\ (\theta) = 0,\ (\theta_{off} + \theta_{ov} \le \theta \le \theta_p) \quad \text{.....(2.5)}$$

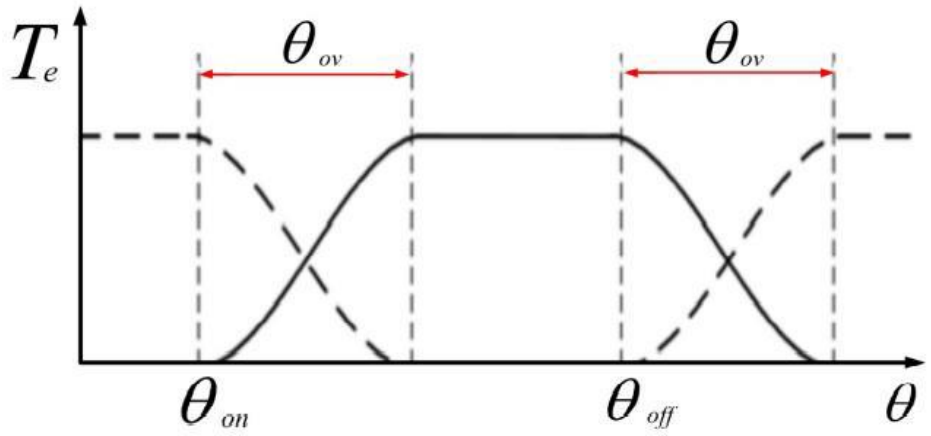


Fig 2.2: Variation of Torque with Respect to Angle (θ)

The overlap angle (θ_{ov}) is related to rotor period (θ_p) as follows:

$$\theta_{ov} \le \frac{1}{2}\theta_p - \theta_{off} \quad \text{.....(2.6)}$$

Fig 2.3 explains the torque controller block diagram with TSF for 3 phase SRM drive.

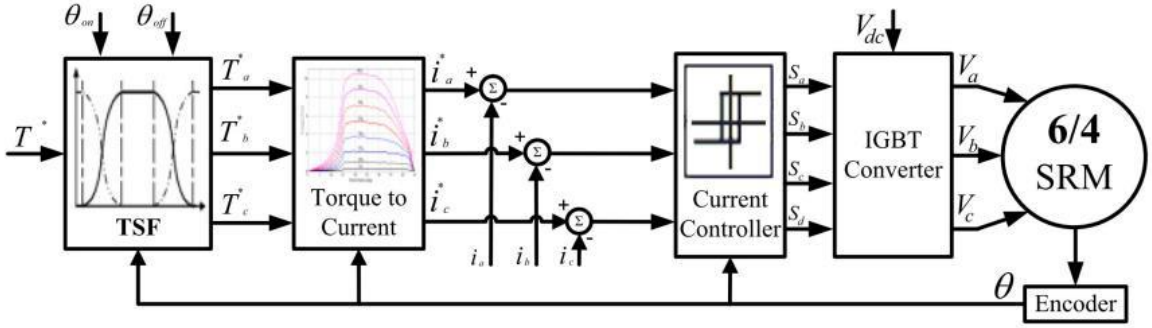


Fig 2.3: Torque Controller Block Diagram with TSF for Three-Phase SRM Drive

2.3.2 Current Control Method

Constant voltage is supplied to the controller. Due to back EMF, position of rotor is varied by varying the value of inductance. Current controller is mostly required for each phase. The block diagram of current controller is as depicted in Fig 2.4. The cascade control of

current is possible in the inner loop and outer loop. It helps in the control of speed. There is a decision block that determines the position of the rotor during the conduction of current.

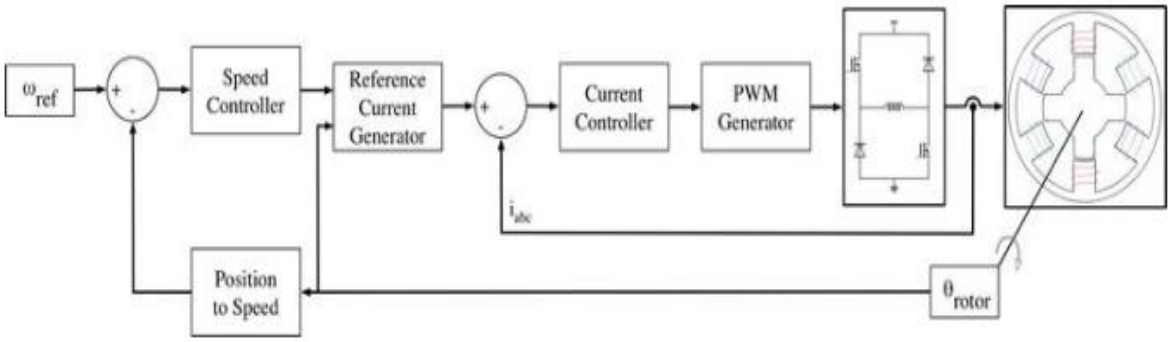


Fig2.4 Block Diagram of Speed Control Based on Current Control

The torque characteristics not only depends on current but also on the current constant even then it doesn't make the required torque constant. So, improvement of current control technique is required to use some more functions like exponential and cosine.

2.4 Converters used for SRM

The converter is often powered by an AC/DC converter-established fixed voltage DC link or straight from a battery bank. The performance and needs of the SRM application determine the best converter and control strategy to use [3], [9]. Before choosing the types of converters to be utilised, the operational characteristics of SRM are highlighted.

The following characteristics are condensed into three tasks [5]:

- During the positive gradient phase of the inductance profile, the current is provided to the phase.
- The torque of the motor is maximised during the phase energising stage, and this is accomplished by modifying phase current. The rise time is increased, and the fall time is decreased.
- During the commutation phase, the magnetic energy is stored and either returned or freewheeled to the dc source.

2.4.1 H-bridge Soft-Switched Converter

In soft-switched H-bridge converter, two phases always carry current. The advantage of this converter is that it decreases components size and cost. Only one diode and one switch operate per phase. The main disadvantage of the converter is that it prevents independent

control of phases, the number of phases is always a multiple of four. Fig 2.5 depicts the H-bridge soft-switched converter.

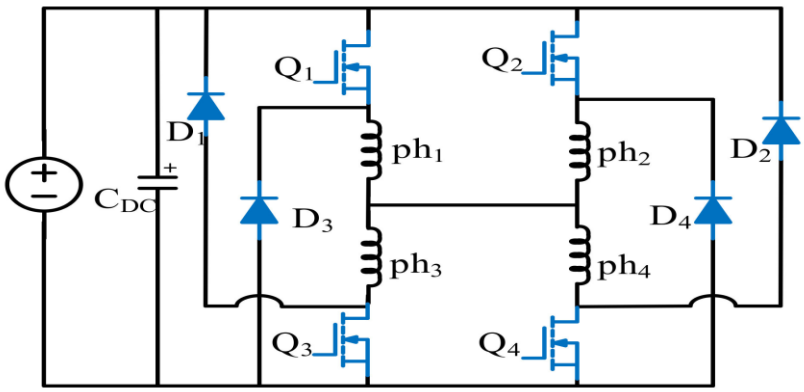


Fig 2.5 H-Bridge Soft Switched Converter

2.4.2. R-Dump Converter

R-dump converter is as depicted in Fig. 2.6. One of the variants uses one transistor and one switch (i.e., diode) for each phase. Power dissipation and switch voltage are determined by the resistor's value. The value of R is modified to produce an appropriate current fall time (that increases with lower R) and switch stress that is tolerable (increases with higher R). During switch T1 is switched off, current flows freely via the diode D1, builds up across the capacitor Cs, and then passes through the external resistor R. The stored energy is partially released by the resistor during the powered period [10], [11].

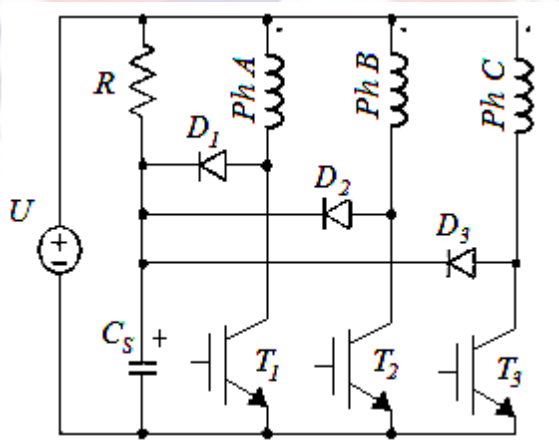


Fig 2.6. R-Dump Converter

The rating of the switch T1 includes design factors such the turn-off transient voltage. Negative torque is generated by the current in the region of the phase inductance with a negative slope, that lowers the average torque of the motor. The drawback of converter is

that current in any phase doesn't take as long to discharge as it does to recharge. The overall efficiency of the motor drive is decreased by the energy lost in the resistor [10].

2.4.3. C-Dump Converter

Since an auxiliary voltage supply receives the demagnetization energy of a phase, the C-dump converter is regarded as a converter of auxiliary voltage supply [1]. To recover the direct energising current from the intermediate subsequent phase, a dump capacitor is employed in the circuit. Fig. 2.7 depicts this converter circuit. Assume that T1 is turned on to activate the Phase A in that converter. If phase current (ia) rises over the reference level, T1 is turned off, enabling diode D1, that is then forward biased. In order to achieve rapid demagnetization as an asymmetric converter, the current route through the dump capacitor Cd is blocked and the voltage across the capacitor is increased. The dump switch Tr is then activated, transferring the extra energy from the dump capacitor to the DC source through the inductor Lr. To apply (U) across the outgoing phase for faster demagnetization, the capacitor's voltage is adjusted and kept at twice the supply voltage (2U). The switching pulses [12, 13] are operated at a frequency lower than the dump switch Tr.

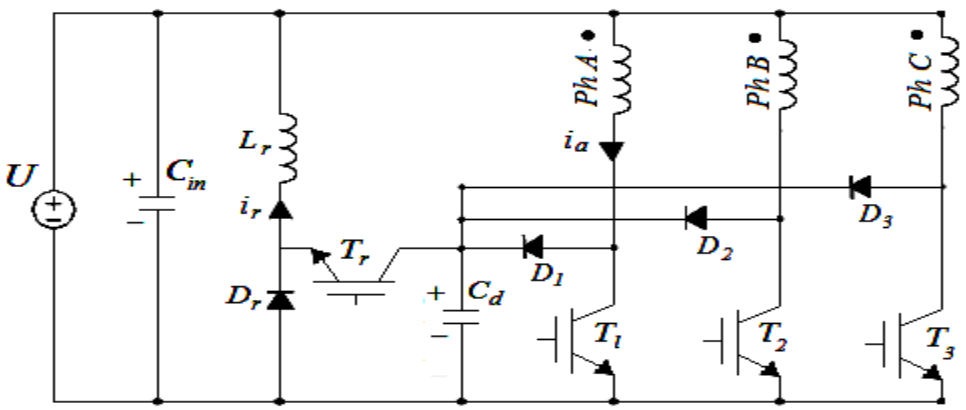


Fig2.7. C-Dump Converter

The C-dump converter provides the benefits of using fewer switching devices, independent phase-by-phase current management, complete regeneration capabilities, faster demagnetization during commutation, and phase commutation. The use of larger capacitor and inductors in the dump circuit makes the circuit bulky, the voltage rating of the devices is double that of the dc link voltage, capacitor voltage is maintained at 2U mainly to allow for faster demagnetization, and the converter does not allow freewheeling [1], [10]. These are the main drawbacks of C-dump converters. Because the power switches and diodes are turned on and off if the voltages and currents are not zero, the C-dump SRM converters

adhere to hard switching topologies. Additionally, the energy flowing between the dc link and Cd causes extra machine losses, lowering the motor's efficiency [14].

2.4.4 Asymmetric, Classic, or Conventional Converter

Asymmetric converter is used for fast built-up of the excitation current. The switching voltage is high. The H-bridge topology, an asymmetric bridge converter, is employed. The circuit for an asymmetric bridge converter utilised in a three-phase SRM drive is shown in Fig. 2.8. Figure 2.9 depicts the device current with a modified switching frequency. Two power switches and two diodes per phase are used in a converter to implement the unipolar switching method. The lower switch is utilised to control commutation during each phase during the upper switch controls PWM switching. Each stage is independently managed. the magnetization, freewheeling, and demagnetization modes of operation of current [3]. In the inner current control loop of the drive system, utilising a unipolar switching technique result in reduction of current ripple and frequency response is good [17], [18]. The SRM of an asymmetric converter is typically under either voltage or current control. The primary advantage of current control over voltage control is the ability to precisely manage the phase current, results in appropriate torque control and the ability to reduce torque ripple or noise. The phase current is compared with the current reference value in the SRM drive system to enforce the current reference value. It is assumed that the current error is handled by a hysteresis controller using the current window of the value (Δi). If the current error is beyond the value (–Δi), the phase switches are turned-off simultaneously. So, during that time the phase diodes, the path is complete through dc source [19], [20].

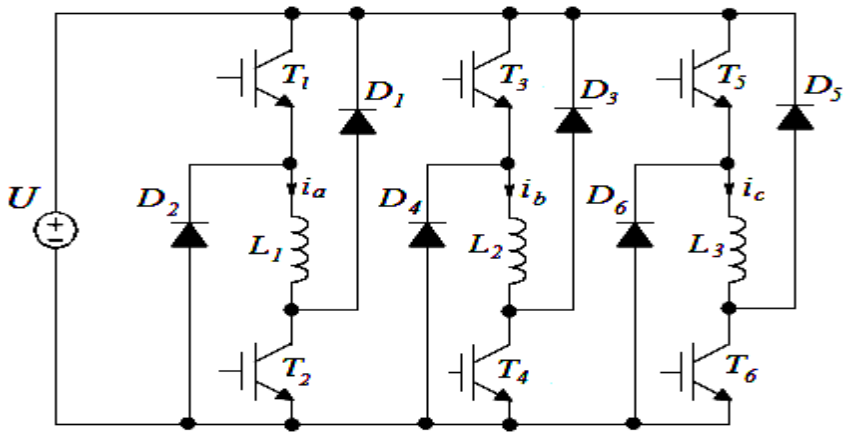


Fig 2.8 Asymmetric Bridge Converter

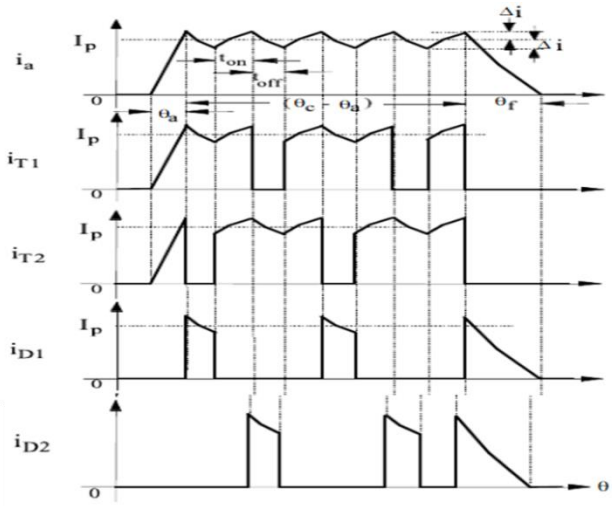


Fig 2.9 Device Current with Modification of Switching Frequency

The benefits of a traditional converter include higher flexibility in controlling the machine current due to the converter's ability to apply the values of supply voltages (U, -U, and 0); independent control of each phase, that is crucial for extremely high-speed operation; fault tolerance capability; and voltage stresses is reduced across the switching components if one switch is damaged. One switch being permanently in the current-conduction route more converter losses and necessitates a larger heat sink for cooling are drawbacks. This further reduces the effectiveness of the system. Since a 3-ph SRM drive includes three switches and three diodes, two devices are constantly connected to the motor winding in series, increasing conduction loss as well as drive size and cost. Operating at high speeds, this converter generates a comparatively modest demagnetizing voltage. [10], [19], [22], [23].

2.4.5. Comparison of Converters used for SRM

Table 2.1 provides the comparison of converters used for SRM.

Table2.1: Comparison of Converters Used for SRM

Features	R-dump converter	C-dump converter	Asymmetric converter
Phase Independence	complete	partial	complete
Freewheeling	allowed	allowed	allowed
No. of devices	low (N)	low (N+1)	high (2N)
Performance	fair	very good	very good
Control	simple	complex	simple
Efficiency	low	high	high
Torque per ampere	low	high	medium
Fault tolerance	low	low	high

2.5 Single-Phase Bridge Rectifier

To replace the diodes with controlled switches, mainly thyristors (SCRs), is a flexible way to regulate the output of a full-wave rectifier. The output voltage is variable over a narrow range by regulating the delay angle for each SCR, that controls output.

In Fig. 4-10, controlled full-wave rectifiers are depicted. SCRs S1 and S2 in the bridge rectifier becomes forward-biased even though the source is now positive, but they do not conduct till gate signals are supplied. Switches S2, S3 and S4 also undergo forward biassing, that causes the source to become negative, but they do not conduct till gate signals are supplied. Switches S1 and S2 are forward-biased for the center-tapped transformer rectifier although Vs is positive and negative, respectively, but neither conducts till gate signal is supplied. The angle formed by the forward biassing of the SCR and the application of the gate signal is known as the delay angle. The rectifiers perform exactly like uncontrolled rectifiers with diodes if the delay angle is zero. Both bridge rectifiers and center-tapped rectifiers is generally covered in the material that follows. Figure 2.10 shows a single-phase full bridge rectifier diagram; Figures 2.11 and 2.12 show the output for a resistive load and continuous current, respectively.

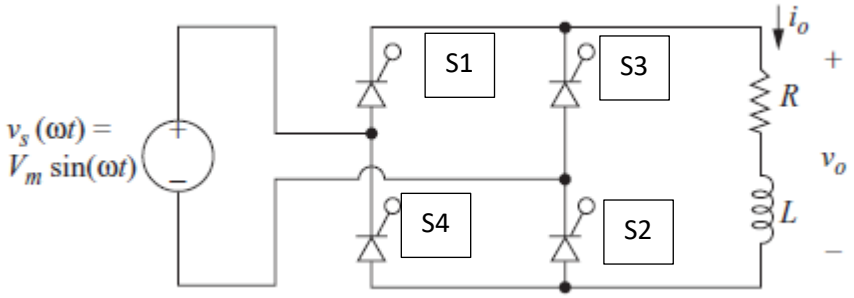


Fig 2.10 Single-Phase Full-Bridge Rectifier

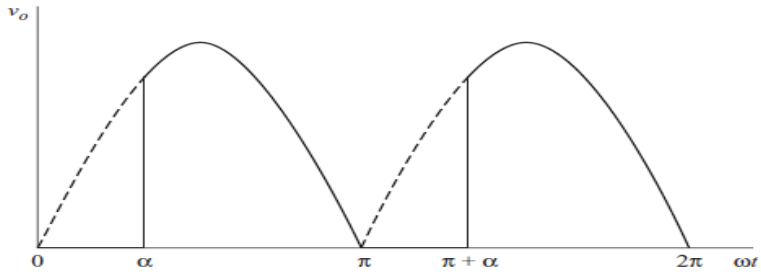


Fig 2.11 Output for a Resistive Load

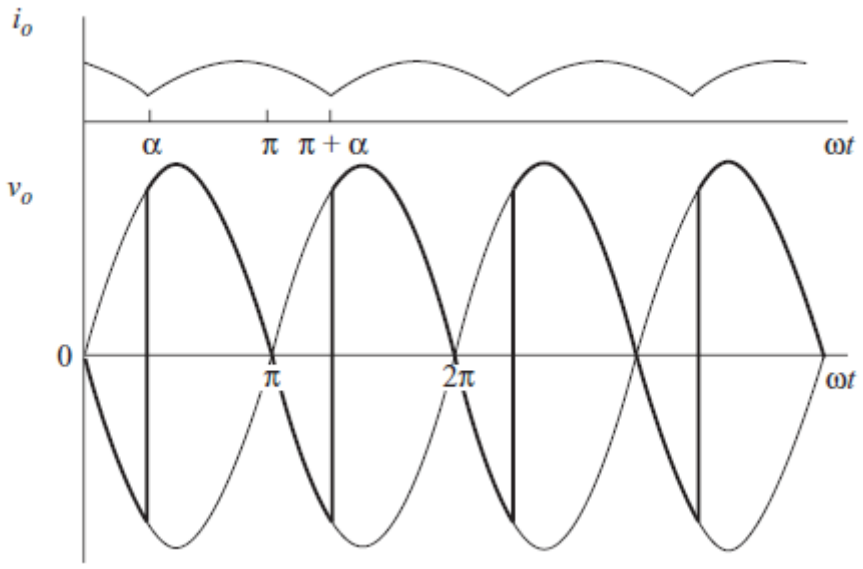


Fig 2.12 Continuous Current

2.6 Summary

The asymmetric converter topology was found to be suitable for high-speed operation because of the quick current rise and fall times and negligible shot through faults after all the converters had been analysed. Because there is no resistance commutation circuit or additional coil added to the converter topology, there are no significant heat or copper losses in the asymmetric bridge converter.

Chapter 3

BLOCK DIAGRAM AND METHODOLGY

The chapter includes the brief explanation on methodology of SRM for speed control is employed in the project. The chapter also briefly explains the working of the asymmetric bridge converter circuit and process flow for the simulation and hardware implementation and it also contains the explanation of block diagram of the project.

3.1 Block Diagram

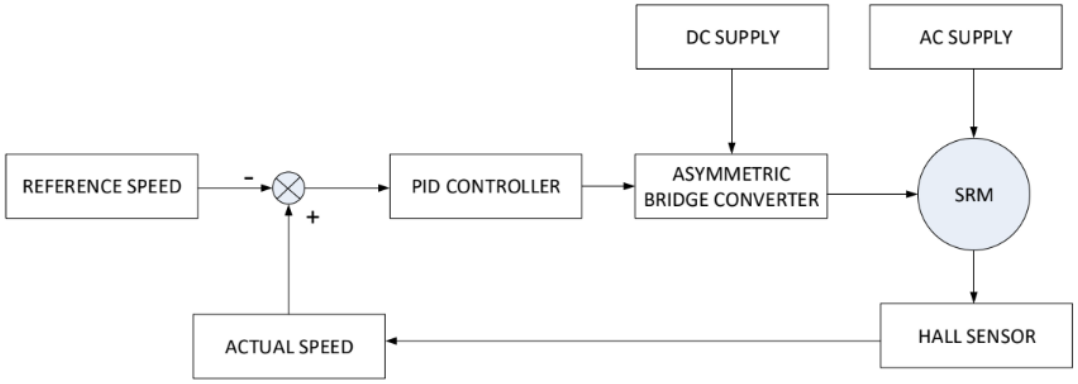


Fig 3.1 Block Diagram of Speed Control of SRM

The block diagram of SRM for speed control is as depicted in the Fig 3.1. There are different number of stator slots and number of rotor slots like 6/4 or 8/6 or 10/8 respectively. The number of stator slots and the number of rotor slots need not be same. Here 8 stator slots and 6 rotor poles is used for hardware implementation and for simulation 6 stator slots and 4 rotor slots. The 8/6 SRM consists of built-in hall sensors with loading. An asymmetric bridge with 4 phase bridge rectifier is used to keep the output voltage regulated. An asymmetric bridge is mainly of Insulated Gate Bipolar Transistor (IGBT) based semiconductor diode is used that operates at a frequency of 15 kHz. The gating pulse for IGBT is provided from the DSP controller [3], [9]. An asymmetric bridge is that mainly consists of 4 phases namely phase A, phase B, phase C and phase D respectively.

The SRM is an 8 stator slots and 6 rotor slots that consists of inbuilt hall sensors. Hall sensors are mainly used for detecting the speed and position of rotor. The speed of the motor is measured using hall sensor so the actual speed of motor is measured. The actual speed is compared to the reference speed. An error is generated that is supplied to the PID controller is varied and the pulse width modulation generator that generates the pulses and

is directly supplied to the IGBT asymmetric bridge and the generated pulses is supplied to the SRM.

The rotor position sensor detects the position of the rotor and sends the related output to the error detector. To generate an error signal that is sent to the controller block, the error detector compares the reference speed with the actual speed. In accordance with the error signal, the controller sends the converter the suitable control signal. Through appropriate excitation of the corresponding windings in the stator, the converter regulates the motor's speed.

3.2 Methodology

The methodology involved in developing the work is as depicted in Figure 3.2

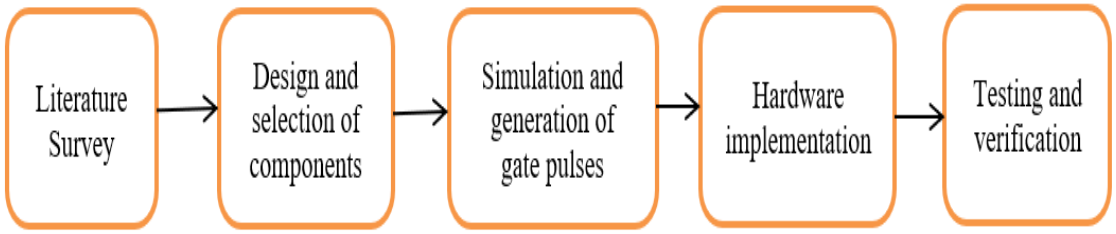


Fig 3.2 Methodology for Speed Control of SRM

- **Planning**

Efficient converter topology for speed control of SRM is selected by comparing with various topologies. The selected topology in this project is IGBT based asymmetric bridge converter [1]. The 3ph bridge rectifier is selected based on the designed values [4].

- **Design and selection of components**

An asymmetric bridge converter is designed. The designing of the converter involves selection of transformer, switching devices IGBT, and selection of diode and design of filter components like capacitor [2]. The tools used for schematics and simulations are MATLAB/SIMULINK.

- **Simulation Analysis**

The asymmetric converter is simulated using PSIM software. The feedback is provided with PI controller circuit [4]. The overall simulation of the entire system with motor, controller and converter circuit is simulated using MATLAB/Simulink [4].

- **Hardware Implementation.**

The assembled system with SRM motor [7], DSP controller [11] with control signals is checked and the test setup is made for the analysis and testing purposes.

- **Testing and verification.**

The implemented converter, rectifier along with DSP module is analysed and the performance of motor is tested under various input conditions.

3.3 Flow Chart

The flow chart of speed control of SRM for open loop is as mentioned in Fig 3.3. Initially the hall sensors read the position of motor. Now, the initiation sequence 1 here the phases B, C and D are energised. In the initiation sequence 2 here the phases B is energised, phases C and D are de-energised.

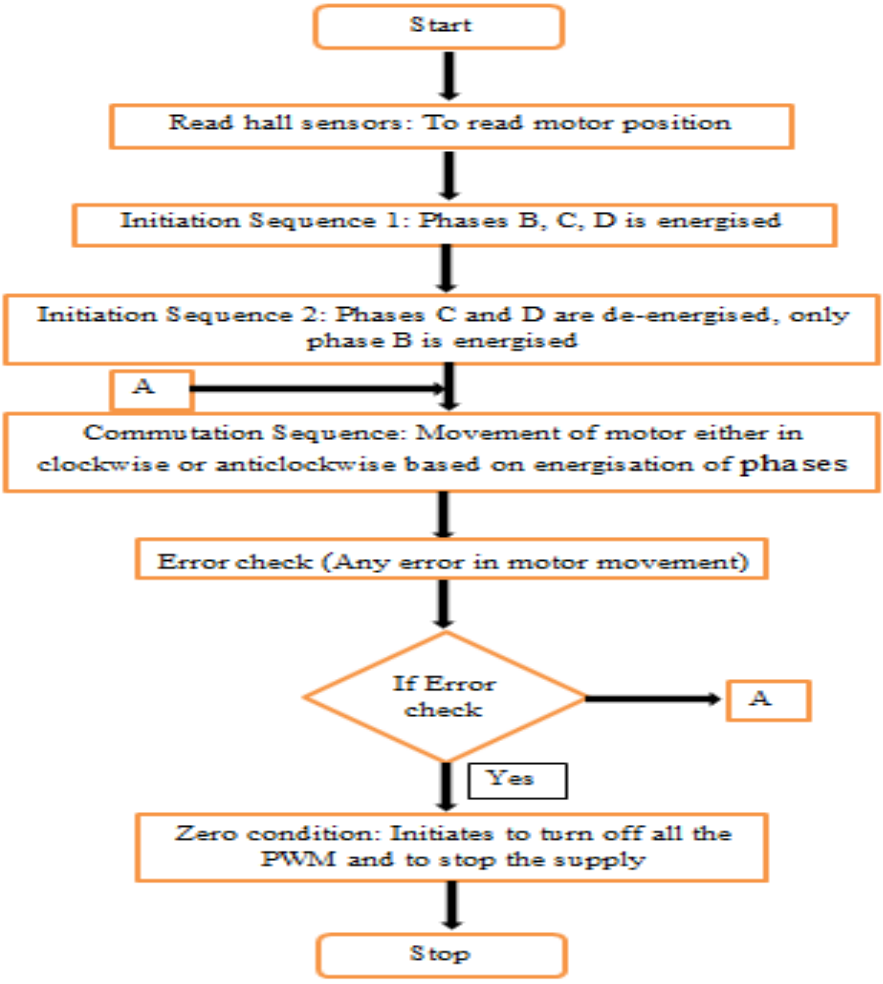


Fig 3.3 Flow Chart for Speed Control of SRM for Open Loop

In the commutation sequence the movement of motor is either in clockwise or anti-clockwise based on the energisation of phases. Error check is performed if there is any error in the rotor movement then zero condition is initiated to stop the supply and turn-off all PWM.

The flow chart of speed control of SRM for closed loop is as shown in Fig 3.4. Initially the hall sensors read the position of motor. Now, the initiation sequence 1 here the phases B, C and D are energised. In the initiation sequence 2 here the phases B is energised, phases C and D are de-energised. In the commutation sequence based on any one feedback of hall sensor speed is calculated. Any deviation from reference speed is encountered by duty cycle of PWM. Error check is performed if there is any error in the rotor movement then zero condition is initiated to stop the supply and turn-off all PWM.

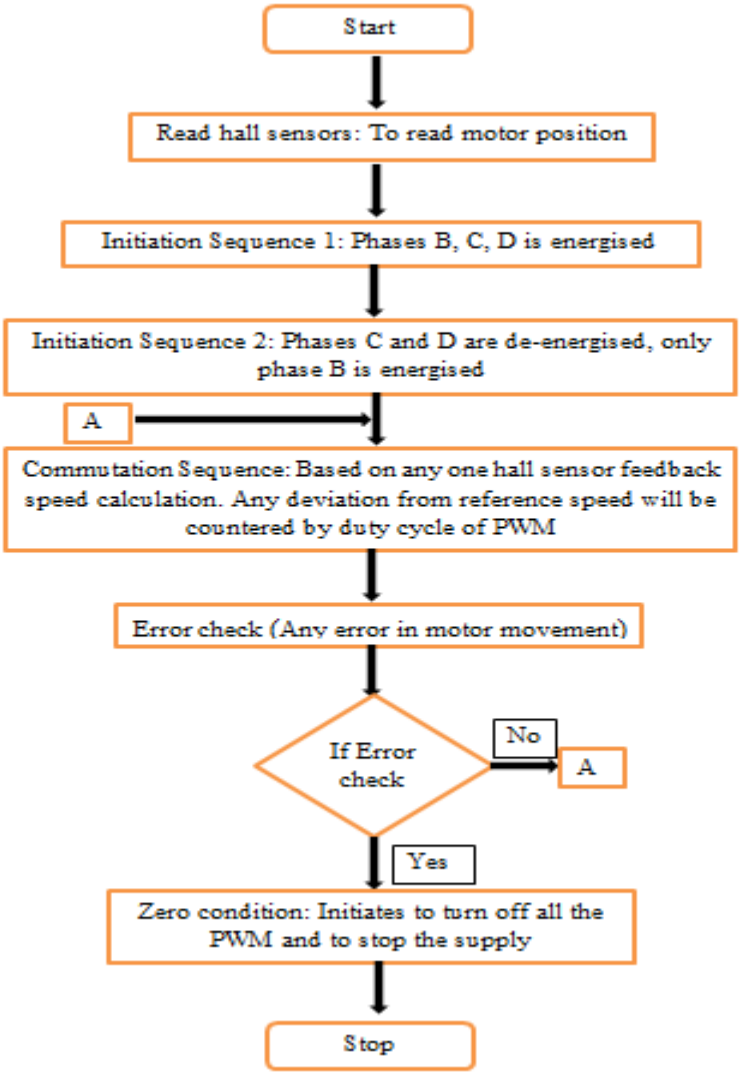


Fig 3.4 Flow Chart for Speed Control of SRM for Closed Loop

3.4 Summary

This chapter consisted block diagram and methodology for speed control of SRM. It consisted of planning, design for selection of components, selected suitable simulation tool namely PSIM and MATLAB/SIMULINK. Finally, methodology for the hardware implementation, testing and verification.

Chapter 4
SPECIFICATION AND DESIGN DETAILS

This chapter consists of specifications for speed control of SRM. Hardware components selected for the implementation are also discussed.

4.1 Specifications of the motor

The specifications of three phase having 6 stator slots and 4 rotor poles for SRM simulation is as represented in Table 4.1.

Table 4.1: Parameters of Three Phase 6/4 Poles SRM for Simulation

Motor parameters	**Values**
Rated Power	60kW
Number of phases	3
Number of stator poles	6
Number of rotor poles	4
Aligned phase inductance	23.6mH
Unaligned phase inductance	0.67mH
Inertia	0.05kg.m
Stator resistance	0.05Ω
DC Voltage supply	240 V
Inductor	1mH

4.2 Asymmetric Bridge Converter Design

The design parameters for Asymmetric converter are as follows as shown in Fig. 2.10 and Fig. 2.11.

- Switch rms current is supplied by

$$I_{T1} = \left(\frac{1}{\theta rp}\left\{\left(I_p + \Delta i\right)\left(I_p + \Delta i\right) * \frac{\theta_a}{3} + \left\{I_p^2 + \frac{7}{3}(\Delta i^2)\right\}\frac{\theta_c - \theta_a}{2} * (1\text{-}\Delta i1)\right)\right. \quad \text{(4.1)}$$

- θrp in terms of rotor poles

$$\theta rp = \frac{2\pi}{P_r} \quad \text{(4.2)}$$

- The average current in the diode is

$$I_{D1(avg)} = \frac{I_p}{\theta rp} * (1 - d1) * \frac{\theta_c - \theta_a}{2} + \frac{\theta_f}{2} \quad \text{(4.3)}$$

- θf is the current fall angle

- The average duty cycle in region $(\theta_c - \theta_a)$ may be derived as:

$$d_1 = \frac{I_p*(R_s+\omega_m)}{V_{dc}} \text{.....(4.4)}$$

- Output voltage is supplied by = $\frac{V_{in} - V_{sw}}{d(1-d)}$ = 50V.....(4.5)

- Inductor = L = 1mH

4.2.1 IGBT Switch Details

TSG40N120CE IGBT uses improved NPT technology and trench design for its design. 1200V NPT IGBT provides superior switching performances and conduction, ruggedness high avalanche, and parallel operation of the switch is easier [4], [8]. It is suited for high frequency and soft switching applications such as microwave oven, induction heating etc.,

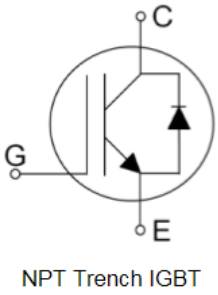


Fig 4.1 Diagram of IGBT

Features:

- 1200V NPT Technology
- Switching frequency is high
- Conduction losses are less

Selection of the IGBT switch depends on Collector-Emitter Voltage $V_{CE,}$ Gate-Emitter Voltage V_{GE} etc.,

The package and size of the IGBT is based on the losses that takes place in IGBT. The two types of losses are calculated during the selection of the IGBT.

• Conduction losses
• Switching losses

Conduction losses are calculated as per the equation. Multiplication factor of 1.4 is considered as the normalized resistance corresponding to 110 °C of junction temperatures (T_j).

- Conduction Loss (P_COND) = 1.4*Rds*(Ip_rms)^2 .....(4.5)

- Switching losses are calculated by bellow equations.

The Turn-on and Turn-off of the IGBT are depicted by the equation:

$$T_{on} = \frac{(Q\_GD * R\_GATE)}{(VGATE - VTH)} \quad \text{.....(4.6)}$$

$$T_{off} = \frac{(Q\_GD * R\_GATE)}{(VTH)} \quad \text{.....(4.7)}$$

The selected IGBT includes the following parameters are as shown in Table 4.2.

Table 4.2: Rating of IGBT

Parameters	Value
Collector-Emitter Voltage	1200V
Gate-Emitter Voltage	±20V
Continuous Current	64A
Diode Forward Current	40A
Max Power Dissipation	208W
Turn-On Delay Time	41ns
Rise Time	82ns
Turn-Off Delay Time	200ns
Fall Time	85ns
Diode Forward Voltage	2.8V

4.2.2 Details of Diode

Diodes are the protection devices and are designed for the use of inverters, switching power supplies and freewheeling diodes. Fig 4.2 represents the Diode used for hardware implementation.

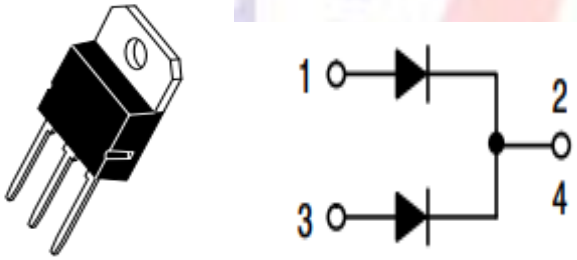


Fig 4.2 Diagram of Diode

Features

- Ultrafast recovery time (35 and 60 ns)
- Operating junction temperature (T_j) is 175°C
- It handles up to 600 V
- Forward voltage drop is less
- Derating current is specified at ambient temperatures
- Junction withstands high temperature

Ratings of diode are as shown in Table 4.3

Table 4.3 Rating of Diode

Parameters	Value
Peak Reverse Voltage	200V
Average Rectified Forward Current (Rated VR)	15 @ TC = 150°C
Peak Rectified Forward Current, Per Leg	30 @ TC = 150°C
Operating Junction and Storage Temperature	− 65 to +175°C
Maximum Thermal Resistance, Junction−to−Case Junction−to−Ambient	1.5 °C/W 40 °C/W
Maximum Reverse Recovery Time	35ns

4.3 Design of 1-Phase Rectifier

Single phase rectifier is as depicted in Fig 4.3.

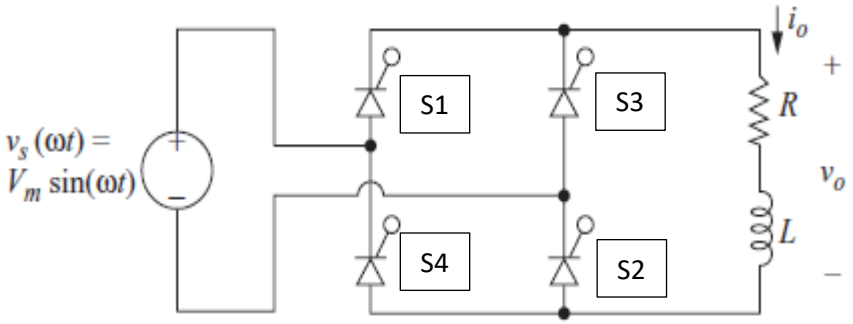


Fig 4.3 Single Phase Rectifier

$Vm = \frac{120}{\sqrt{2}} = 169.7$ V ……..(4.8)

$Z = \sqrt{R^2 + \omega XL^2} = \sqrt{10^2} + (377 * 0.02)^2 = 12.5\Omega$ ……..(4.9)

$\theta = tan - 1\frac{\omega L}{R} = tan - 1[(377 * 0.02)/10] = 0.646$ rad ……..(4.10)

$\omega r = \frac{\omega L}{R} = 0.754$ rad ……..…….(4.11)

α = 60°= 1.047 rad

Average load current $Io = \frac{\pi}{2}\int io(\omega t)d(\omega t) = 7.05$ A ……..……(4.12)

$Vo = \frac{2Vm}{\pi}\cos\theta = 296V$ …….(4.13)

4.4 Capacitor

KEMET's (ALS30/31) Series are screw terminal capacitors. It covers a greater range of voltage ratings and case sizes, featuring too long-life performance and high ripple currents. They are preferably suitable for commercial and industrial applications. It exhibits long life expectancy for high frequency converters, Switch Mode Power Supplies (SMPS) Uninterruptible Power Supply (UPS).

Fig 4.4 Capacitor

Benefits

- Compact in size
- Long life spans up to 25,000 hours at 85°C
- Less current ripple
- Voltage surge capability is good
- Optimized designs are also available

Table 4.4 Ratings of Capacitor

Parameters	Value
Capacitance Range	100 – 680,000 µF
Rated Voltage	25 – 500 VDC
Operating Temperature	−40 to +85°C
Capacitance Tolerance	±20% at 100 Hz/+20°C

4.5 Transformer

Transformer provides isolation between the input and output. It helps to regulate the output voltage to be either higher than input voltage or lower than the input voltage depending on the application. Transformers are used in a dc-dc converter to provide protection against electric shock and it reduces the hazards caused due to the fault conditions [20]. Transformers are used in applications requiring a different ground point for different parts of the circuit. For the hardware implementation of the dual input LLC converter a step-down transformer is used. Fig 4.5 shows a step-down transformer. The rating of transformer is 230V/14V, 2A.

Fig 4.5 Step-Down Transformer

The transformer includes the following parameter values:

➢ Input Voltage: 230V AC
➢ Output Voltage: 14V and 0V
➢ Output Current: 2 Amp
➢ Winding: Copper
➢ Mounting: Vertical mount type

4.6 Hall Effect Sensor

The magnetic field is measured using the Hall Effect, and the Hall Effect sensor is the one that monitors presence. The Hall sensor's output voltage is inversely proportional to the magnetic field intensity.

Positioning, speed detection, proximity sensing, and current sensing are just a few of the applications that typically depend on hall sensors. A binary switch is produced at the same time a hall sensor is coupled with the detection of threshold values. Computer printers that detect missing paper and open covers during operation, as well as 3D printers to measure the filament thickness, are frequently employed in industrial applications. Hall sensor is as depicted in Fig 4.6 and pin configuration is as shown in Table 4.5.

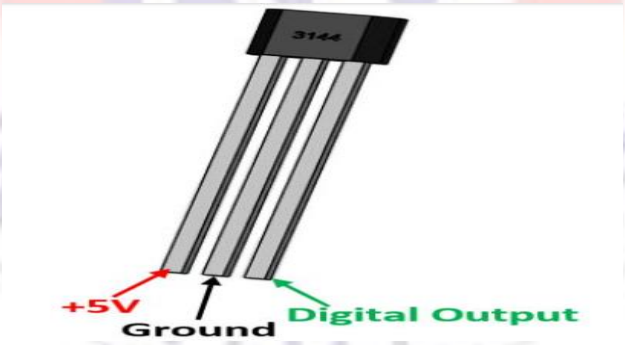


Fig 4.6 Hall Sensor

Table 4.5 Pin Configuration of Hall Sensor

Pin Name	Description
+5V (Vcc)	Used to power the hall sensor, typically +5V is used
Ground	Connect to the ground of the circuit
Output	This pin is high, if magnet is detected. Output voltage is equal to Operating voltage.

4.6.1 Specifications of Hall-Effect Sensor

- Hall-effect sensor's output is digital
- Operating voltage ranges from 2.5 V to 30 V (typically 5 V)
- Output current is 20 mA
- Used to detect the magnets
- Output voltage is normally equal to the operating voltage
- Operating temperature ranges from -30°C to 85°C
- Turn-on and turn-off time is 1us
- In-built protection
- Appropriate for use in industrial and automotive applications

4.6.2 Use of Hall-Effect Sensor

There are two types of hall effect sensors: the first produces an analogue output, the second produces a digital output. A3144 is a hall sensor with a digital output. The output is low or logic zero if a magnetic field is detected; otherwise, the output is high or logic one. In order to maintain the output at logic low as soon as a magnet is detected, it is advised to utilise a pull-up resistor as illustrated in circuit Fig. 4.7. The pull-up resistor R1 (10K) and filter capacitor C1 (0.1uF) in the circuit help to reduce noise that combines with the digital output.

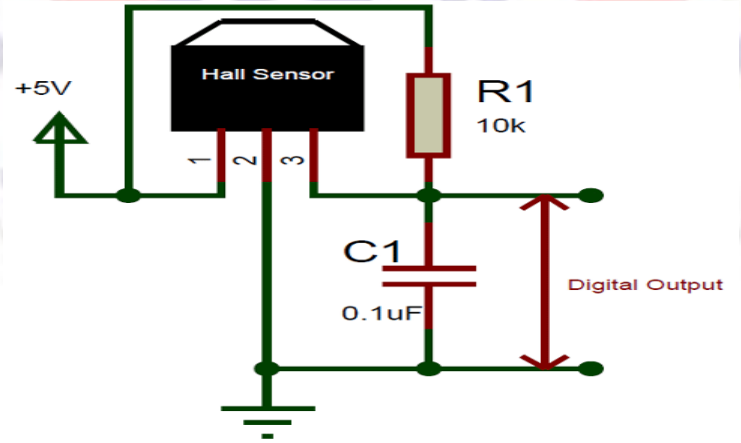


Fig 4.7 A3144 Hall Sensor

Application

- Used to detect magnetic objects
- Used in magnetic alarm door system
- Measures speed in automobiles
- Detect the pole of magnets in SRM, BLDC motors

4.7 Evaluation Board

The launchpad F28379D is as shown in the Fig 4.8.

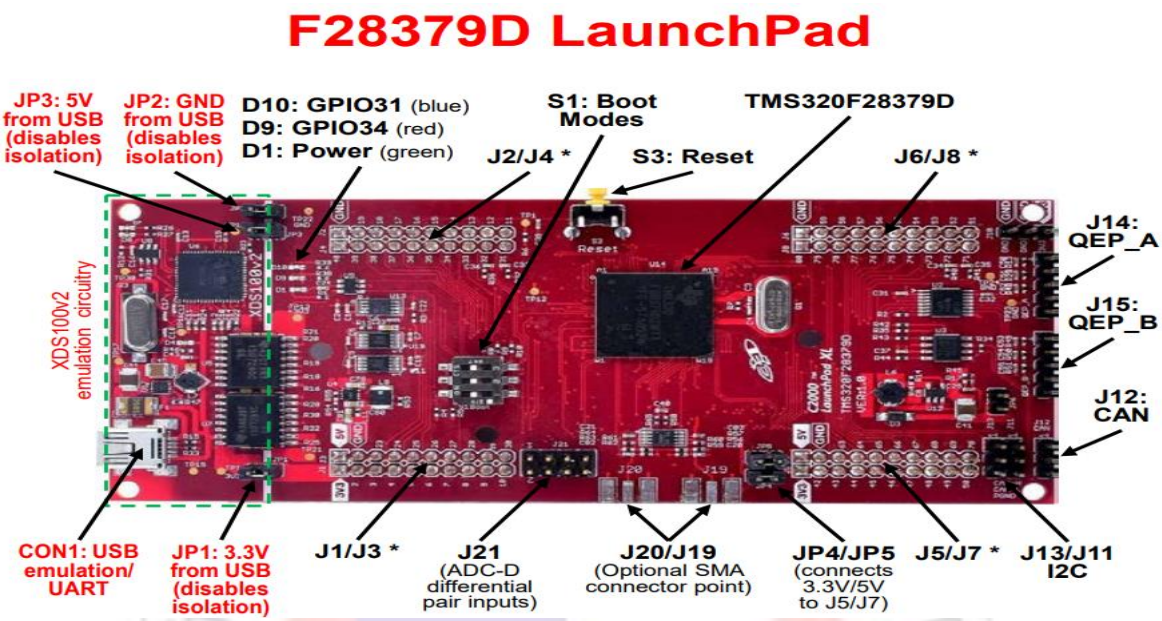


Fig 4.8 F28379D Launchpad

4.7.1 Pinouts of F28379D

The F28379D consists of 11 connectors for external interface and the pin details are as listed. Out of 11 connectors only 4 connectors are used namely J2, J4, J8 and J7.

J2 Connector

Pin number	Description
20	GND
19	GPIO61
18	GPIO123
17	GPIO122
16	RST
15	GPIO58
14	GPIO59
13	GPIO124
12	GPIO125
11	GPIO29

J4 Connector

Pin number	Description
40	GPIO0
39	GPIO1
38	GPIO2
37	GPIO3
36	GPIO4
35	GPIO5
34	GPIO24
33	GPIO16
32	DAC1
31	DAC2

J7 Connector

Pin number	Description
70	ADCINA1
69	ADCINA4

J8 Connector

Pin number	Description
80	GPIO6
79	GPIO7

68	ADCINB4
67	ADCINC4
66	ADCINA5
65	ADCINB5
64	ADCINC5
63	ADCIN15
62	GND
61	5V

78	GPIO8
77	GPIO9
76	GPIO10
75	GPIO11
74	GPIO14
73	GPIO15
72	DAC3
71	DAC

4.7.2 TMS320F28379D DSP

The TMS320F28379D is a DSP based PID controller and a produce of Texas instrument is as depicted in Fig 4.7. It is directly connected to the PC using the USB cable. The features are as follows,

- 54 Digital Input/Output pins out of those 15 pins are used as Pulse Width Modulation outputs
- 16 pins are used for Analog Inputs (AI)
- 4 UART pins are used in serial interface
- Crystal oscillator of 16MHz
- USB connection
- It is interfaced with PC using USB cable
- Powered using a battery or AC-to-DC adapters
- Pins 34 to 40 are used to the control signals of asymmetric bridge converter 1 to 6.
- Pins 79 and 80 are used to the control signals of asymmetric bridge converter 7 and 8.

4.8 Summary

Specifications and the design of the speed control of SRM were discussed. The hardware components for the implementation to develop the proposed hardware were presented in the chapter.

Chapter 5

SIMULATION AND HARDWARE IMPLEMENTATION

The chapter discusses about the simulation of SRM for speed control is carried out using MATLAB/SIMULINK and PSIM software. The implementation to develop the proposed hardware is presented in the chapter.

5.1 Simulation Analysis

It uses a 240V DC supply power. For the speed ranges, the converter turn-on angle is 45° and turn-off angle is maintained at 75°. The hysteresis band is set to 10A with a reference current of 200A. Applying the step reference to the regulator input initiates the SRM. The properties of the load affect the acceleration rate. A very light load is chosen to reduce the starting time. The motor speed increases in accordance with the mechanical dynamics of the system because only the currents are controlled. Fig. 5.1 depicts the simulation of SRM speed control using a P controller using MATLAB/SIMULINK software.

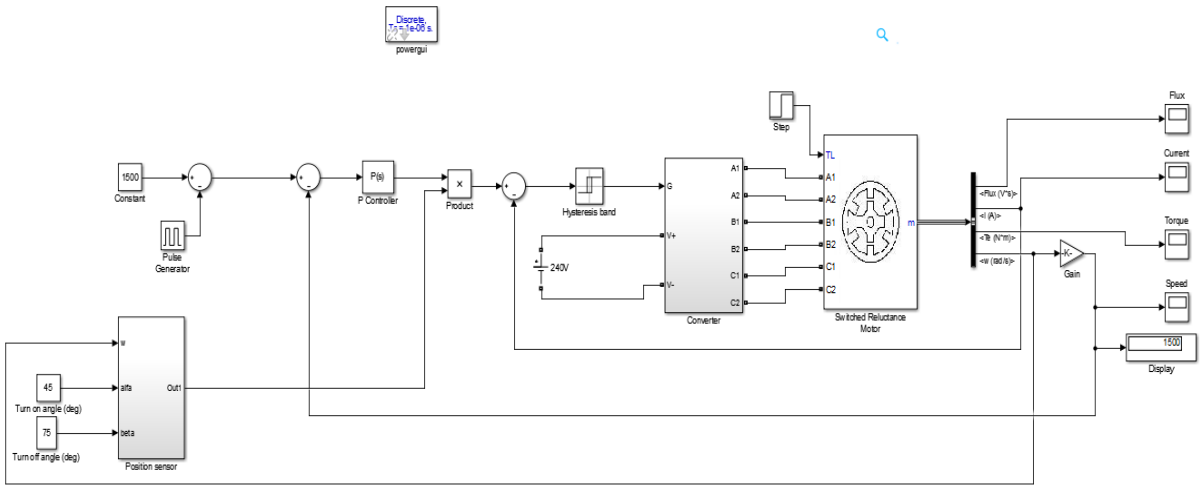


Fig 5.1 Speed Control of SRM using P Controller

A type of control system known as a proportional controller function in a linear or linear manner and serves as a correction factor between the measured value and the reference value. Comparison of the reference value and actual value is performed, an error is produced [5].

To reduce the steady state error, a large gain is necessary. A proportional controller is therefore employed. The Simulink model is created to regulate the SRM's speed using a P controller. The actuating error signal and the controller output u, possess a continuous linear relationship that is

$$u = K_P * e(t) \quad \text{.....(5.1)}$$

Here u - Output signal

e(t) - Error signal and

K_P - Gain constant

The simulation of SRM for speed control using PI controller using MATLAB/SIMULINK software is as shown in Fig 5.2.

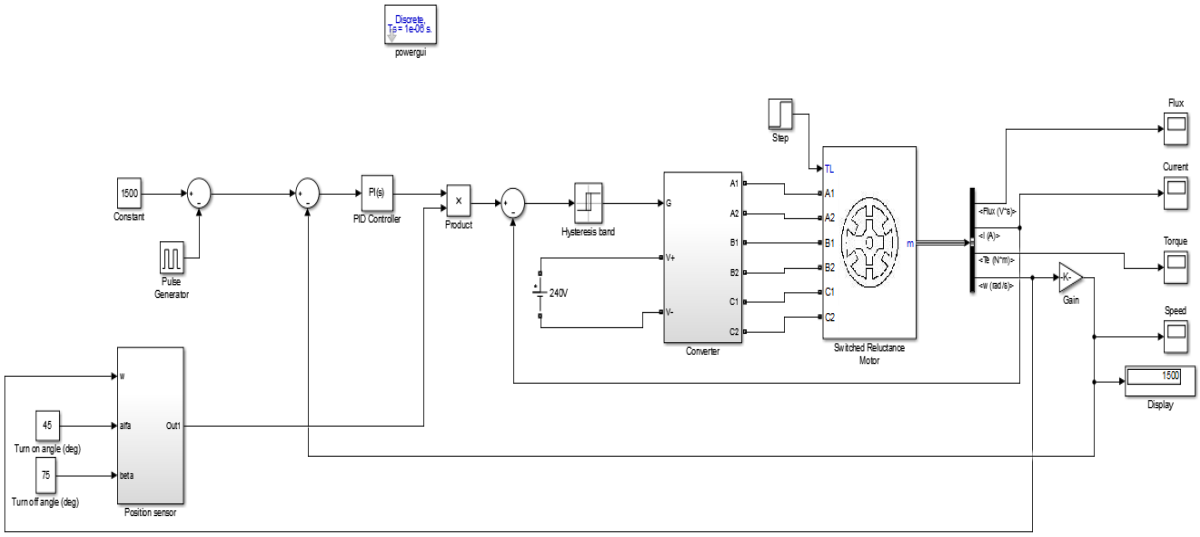


Fig 5.2 Speed Control of SRM using PI Controller

Proportional integral P_i controllers are also known as proportional in conjunction with integral control. Proportional integral is used to reduce error between the measured value and the reference value by varying the value of input supplied to the circuit. PI controller is a combination of both proportional control and the integral control. SRM for speed control using PI controller is simple, implementation is easier, low cost, less error in the steady state condition and highly robust [5].

The error input supplied to the circuit is

$$u = K_P * e(t) + K_i * \int e(t)\, dt \quad \text{.....(5.2)}$$

The values of K_p and K_i is obtained by method of tuning. The values of K_p and K_i used in the simulation circuit are 50 and 0.1 respectively. The simulation of SRM for speed control using PID controller using MATLAB/SIMULINK software is as depicted in Fig 5.3.

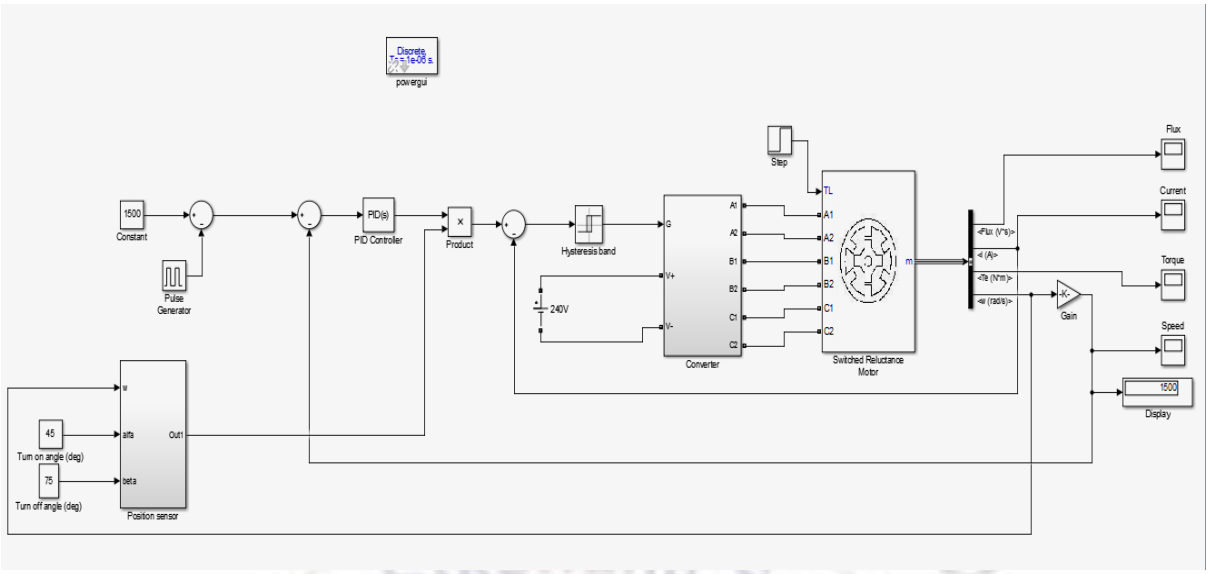


Fig 5.3 Speed Control of SRM using PID Controller

Proportional Integral Differential Controller is a closed loop system that is commonly used in most of the industrial and other applications. The error that is generated is reduced in spite of increase in gain [5]. The error input supplied to the circuit is

$$u = K_P * e(t) + K_i * \int e(t)\,dt + K_d * \frac{de(t)}{dt} \quad \text{.....(5.3)}$$

Here u is the control signal, e(t) is the error signal. The value of K_p, K_i and K_d are obtained by tuning method. The value of K_p, K_i and K_d used in the simulation circuit is 20, 0.1 and 0.05 respectively. The tuning method is used to get the values of K_p, K_i, and K_d.

K_p, K_i, and K_d values are

- Proportional term (K_p) is the proportional to the error,
- Integral term (K_i) is the proportional to the integral of the error and
- Differential term (K_d)is the proportional to the derivative of the error.

The controller's K_P, K_i, and K_d constant values depend on the system being regulated, so after proper tuning and testing to select the optimal parameters, the values of the constants utilised in this analysis are obtained as follows:

Proportional controller, $K_P = 50$

Proportional Integral controller, $K_P = 50$, $K_i = 0.1$

For Proportional Integral Differential controller, K_P is 20, K_i is 0.1, and K_d is 0.05

The comparison of gain responses of P, PI, PID controller is as displayed in Table 5.1.

Table 5.1 Comparison of Gain Response for P, PI and PID Controller

Parameter	Speed of response	Stability	Accuracy
Increasing K_p	Increases	Deteriorate	Improves
Increasing K_i	Decreases	Deteriorate	Improves
Increasing K_d	Increases	Improves	No impact

5.1.1 Power Converter

An asymmetric bridge converter shifts the current provided to the phase in accordance with the rotor position. Converter circuit is as shown in the Fig 5.4 (a), Power Converter Block is as depictef in Fig 5.4 (b) and each phase converter, showing the switching devices as depicted in Fig 5.4 (c).

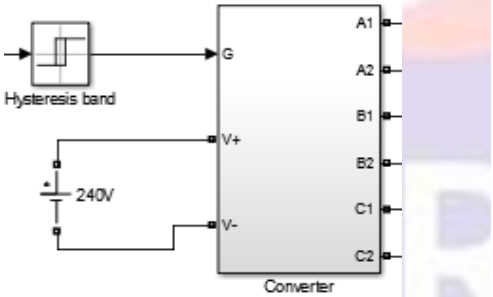


Fig 5.4 (a) Converter Circuit

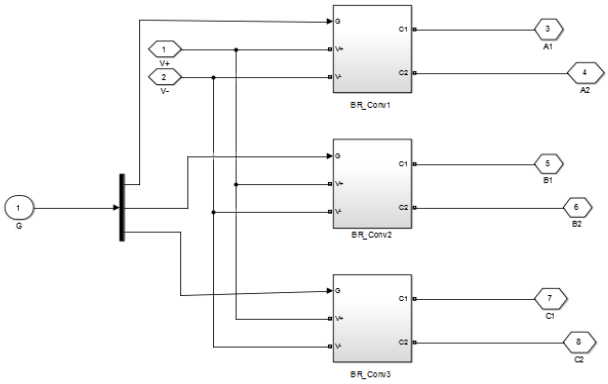


Fig 5.4 (b) Power Converter Block

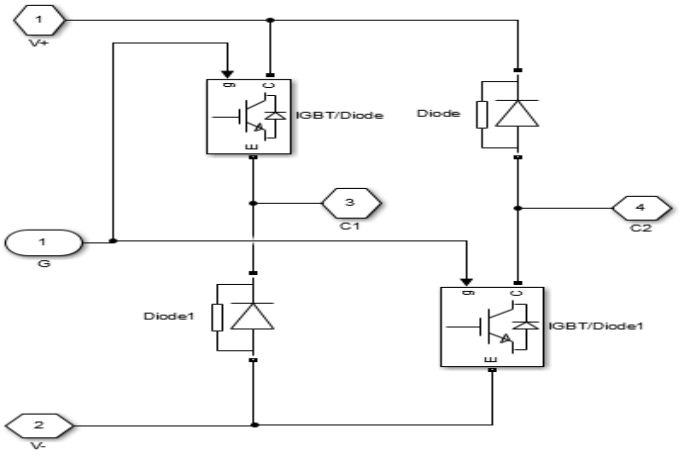
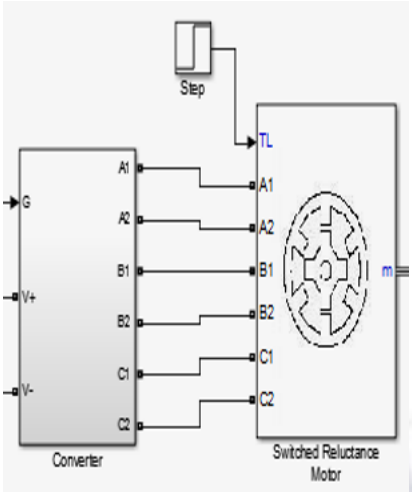


Fig 5.4 (c) Each Phase Converter

5.1.2 SRM Block

The SRM block used for the simulation is as shown in Fig 5.5. The detailed set parameters for SRM block are as mentioned in Fig 5.6.



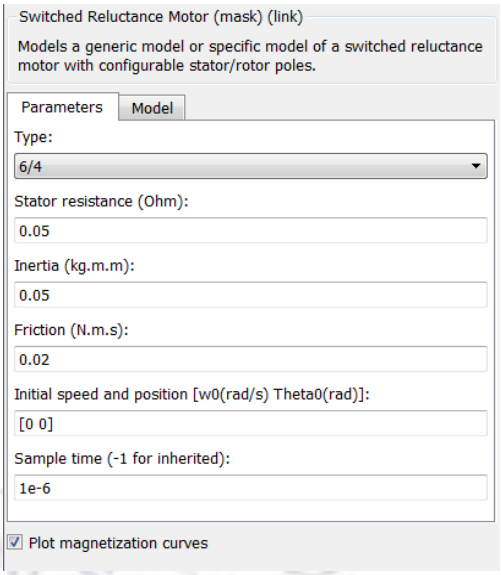


Fig 5.5. SRM Block for Simulation

Fig 5.6 Set Parameters for SRM

5.1.3 Position Sensor

The sensor is a crucial part of any measuring system because it collects information from the environment or physical parameter and converts it into an electrical signal that the system may use as input. By definition, a position sensor is a device that tracks an object's movement and transforms it into signals that may be sent, controlled, or processed. These sensors are typically used to detect the body from a reference point. As a result, it recognises the change in position and uses this output as feedback so that the control system may react appropriately. The primary functions of a position sensor are to control motion, count, and encode various activities by determining whether they exist or not. Position sensor block and its detailed simulation is as described in Fig 5.7 and Fig 5.8 respectively.

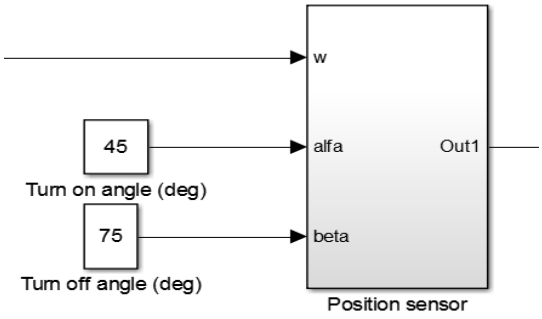


Fig 5.7 Position Sensor Block

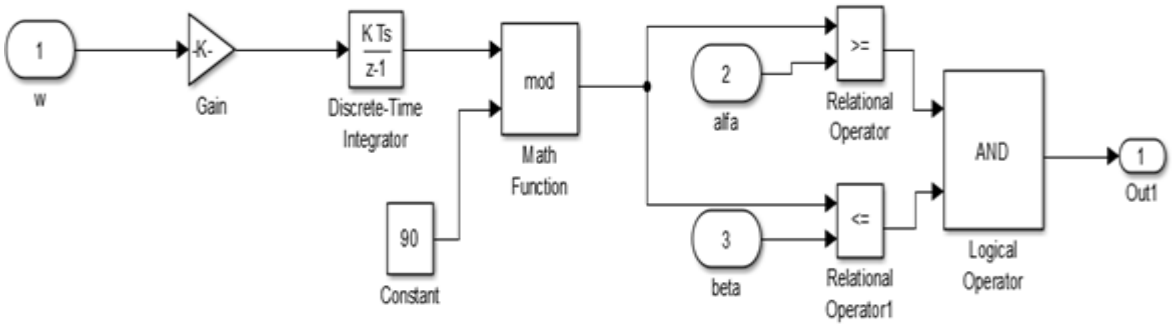


Fig 5.8 Detailed Simulation Block of Position Sensor

5.1.4 Simulation of Asymmetric bridge

The simulation of 4phase asymmetric bridge is performed using PSIM software as shown in Fig 5.9. The switching sequence of the bridge is as provided in Table 5.2. The reference signal is commutated with the commutation of the phases. Table 5.2. represents the active, reference and discharge phases for commutation in the sequence C-D-A-B-C.

Table 5.2. Commutation Sequence of Asymmetric Bridge

Step	Active phase	Discharge phase	Reference phase
1	C	D	A
2	D	A	B
3	A	B	C
4	B	C	A
1	A	B	C

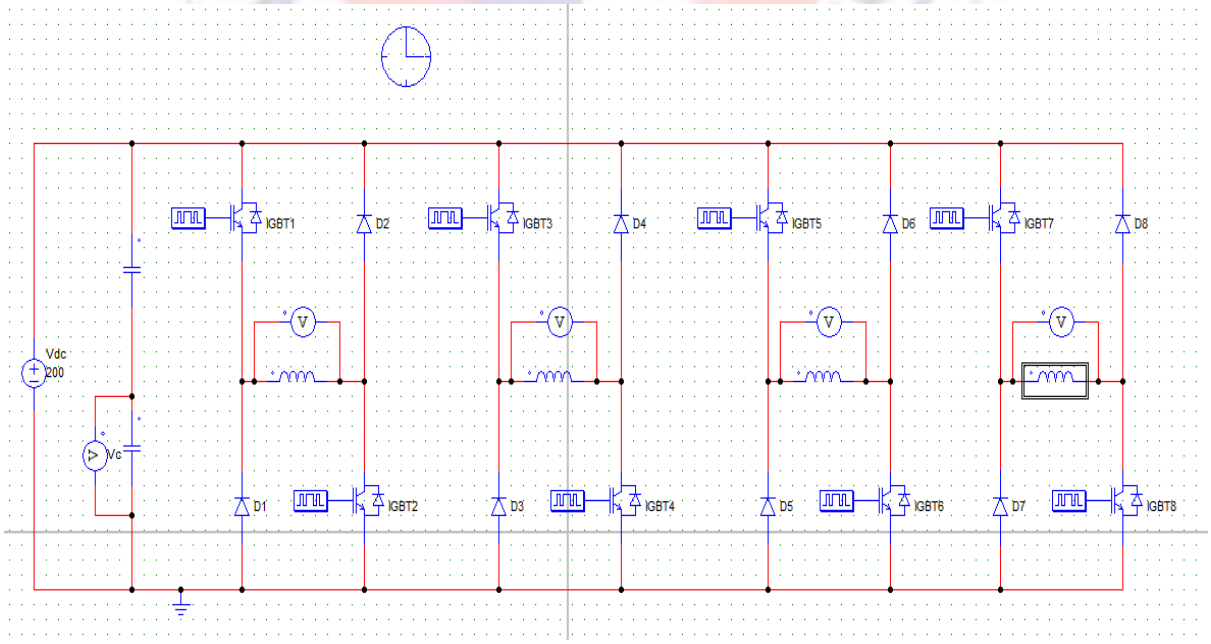


Fig 5.9. Simulation of Asymmetric Bridge

5.2 Hardware Implementation

The hardware implementation of control signals for the generation of PWM signals is as mentioned in the circuit Fig 5.10. The system takes one of the two inputs that is either the closed loop speed reference or the open loop duty cycle. Open loop duty is the ratio of set duty value to 3000 as designed in the program. The motor runs in 3 stages:

- Initiation Sequence 1: Phases B, C and D are energized.
- Initiation Sequence 2: Phases C and D are de energized and only phase B is energized to align the motor.
- Commutation Sequence: The motor after previous phase is commutated in either clockwise or anti clockwise by energizing the phase A, B, C and D in either sequence.
- Zero Condition: If there is an error this condition is initiated to turn off all PWMs and stop supply.

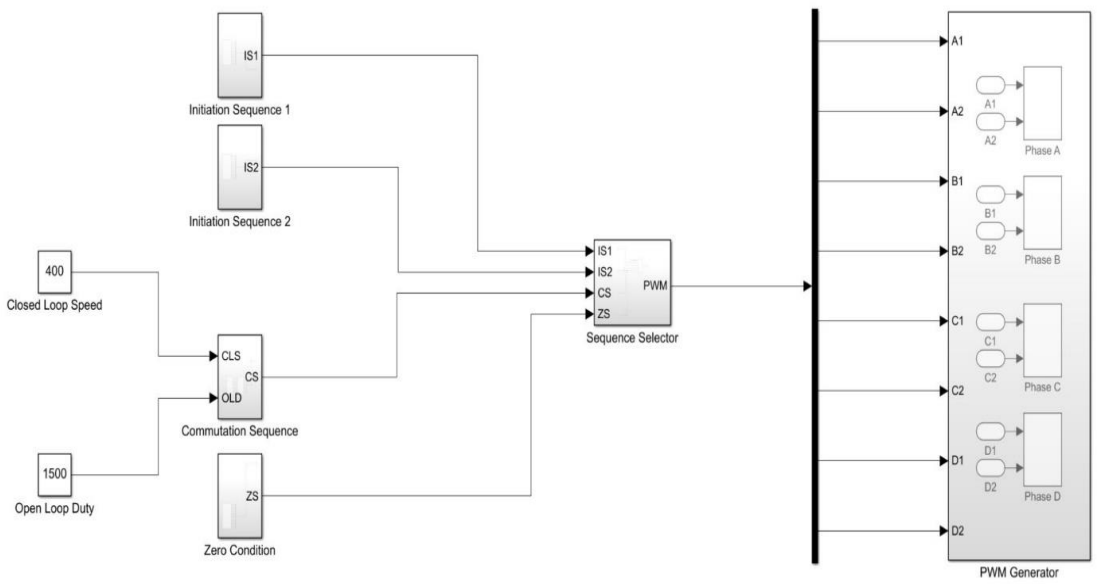


Fig 5.10 Control Block for PWM Generation

Sequence Selector is used to switch between the sequences as Initiation Sequence 1 for 1 second after start, Initiation Sequence 2 for next 1 second and switched over to Commutation Sequence for rest of motor operation.

The PWM Generator generates necessary PWM for the IGBTs. The entire programming is performed by using Simulink Embedded Coder and the C2000 Simulink blocks that is directly program the TMS320F28379D controller used. The different blocks are:

- General Purpose Input
- General Purpose Output
- Counter
- PID controller
- PWM block
- GPIO Input

GPIO block is used as shown in Fig 5.11 to read all the signals from Hall Sensors in order to commutate the motor as well as speed calculation.

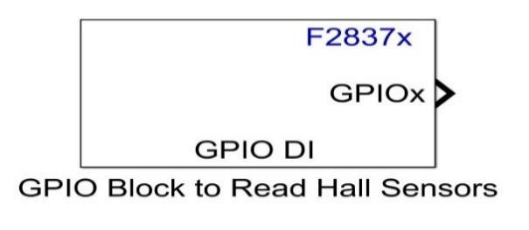


Fig 5.11 General Purpose Input Block

- Counter

The counter block as shown in Fig 5.12 is used to calculate the speed on the basis of periodicity of the hall sensors every 0.5 seconds.

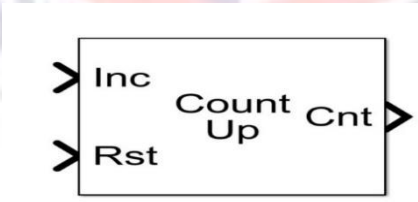


Fig 5.12 Counter Block

- PID Block

The PID block as shown in Fig 5.13 is the PID controller for the closed loop system. The values for P, I and D are tuned in real time with hardware in loop testing to get a good trade-off between settling time and overshoots.

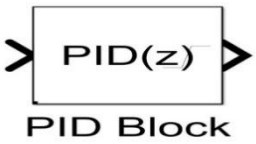


Fig 5.13 PID Block

- PWM Block

PWM block as mentioned in Fig 5.14 directly generates the PWM from the DSP controller based on excitation input. The operating frequency used is 15 kHz.

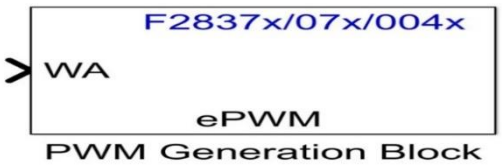


Fig 5.14 Pulse Width Modulation Block

- GPIO Output

The GPIO Output block as shown in Fig 5.15 is used to generate digital high or low output that is used for driving low side IGBTs.

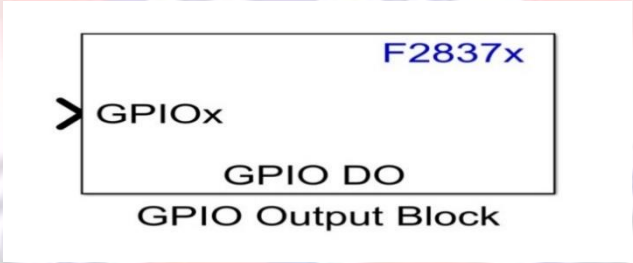


Fig 5.15 General Purpose Output Block

In the control sequence soft switching sequence is used. This basically means high side IGBTs are driven by PWM signals of 15 kHz the low side IGBTs are driven by just high or low signals.

5.3 Main Block

The main block of the system as shown in Fig 5.16. All the 4 hall sensor states are read using GPIO Input block. One hall sensor is used for speed calculator using the counter block. The controller is implemented using the PID block. The Selector is to switch between open loop and closed loop operation.

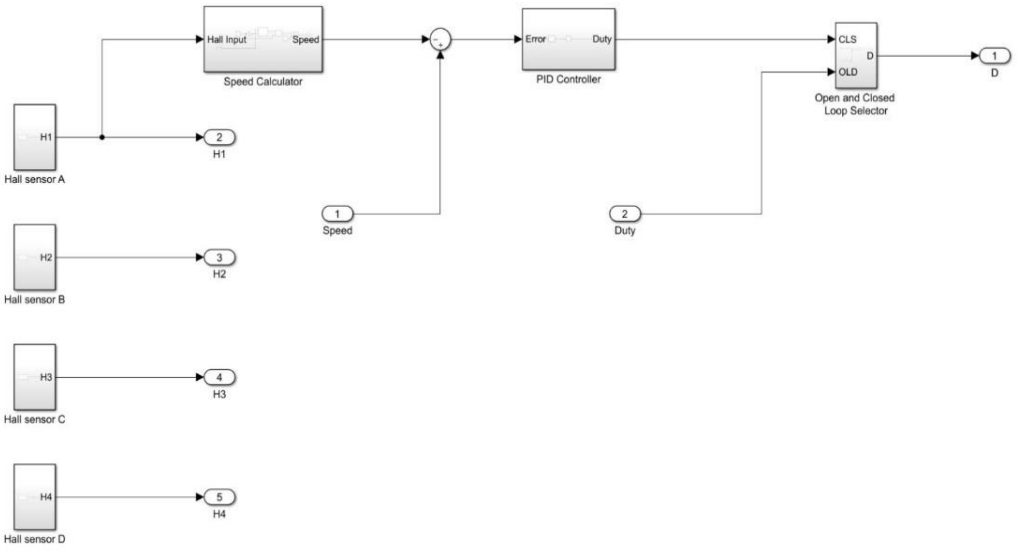


Fig 5.16 Main Block of Hardware

5.4 4-Phase Asymmetric Bridge Converter

The hardware connection of 4 phase asymmetric bridge converter is as mentioned in Fig 5.17.

- It consists of a step-down transformer with 230V/14V to drive the MOSFET circuit.
- It consists of 4 legs with 2 MOSFET with diodes in each leg.
- It consists of 2200uF capacitor with a supply voltage of 250V.
- A rectifier is used to convert 230VAC into 311VDC.
- Input to the converter is single phase, 220VAC, 50Hz and 2A.
- The voltage across the capacitor is 296VDC.

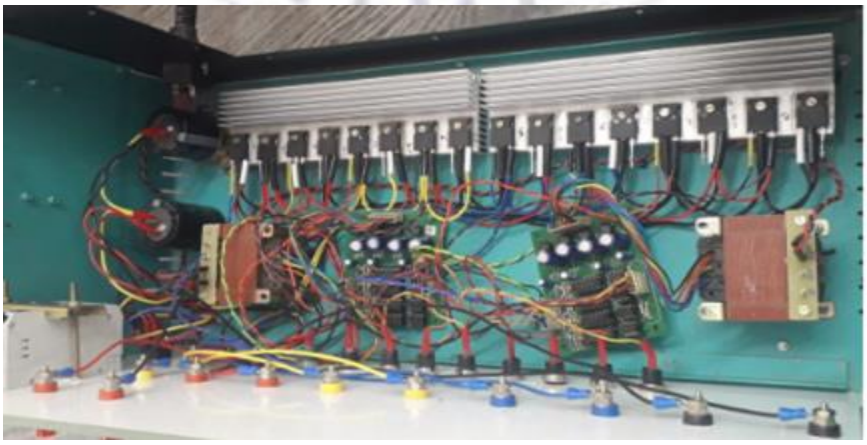


Fig 5.17 Asymmetric Bridge Converter

4-Phase Asymmetric bridge converter with gating pulses is as shown in Fig 5.18.

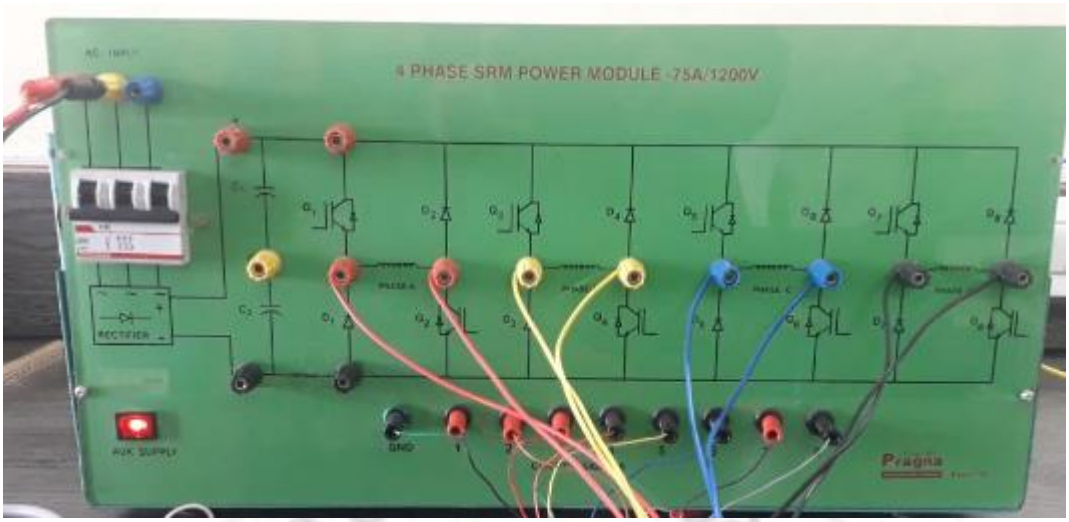


Fig 5.18 4-Phase Asymmetric Bridge Converter with Gating Pulses

The specifications of motor and its ratings are as shown in the Table 5.3

Table 5.3 Specifications of Motor

Motor parameters	**Values**
Rated Power	1kW
Speed (rated)	2500rpm
Number of stator poles	8
Number of rotor poles	6
DC Voltage supply	240 V
Inductor	1mH

The switched reluctance motor used for hardware implementation is as described in Fig 5.19.

Fig 5.19 Switched Reluctance Motor

5.5 TMS320F28379D DSP Controller Connections

The connections of gating pulses to Asymmetric bridge converter, hall sensors provided from the DSP is as shown in Fig 5.20.

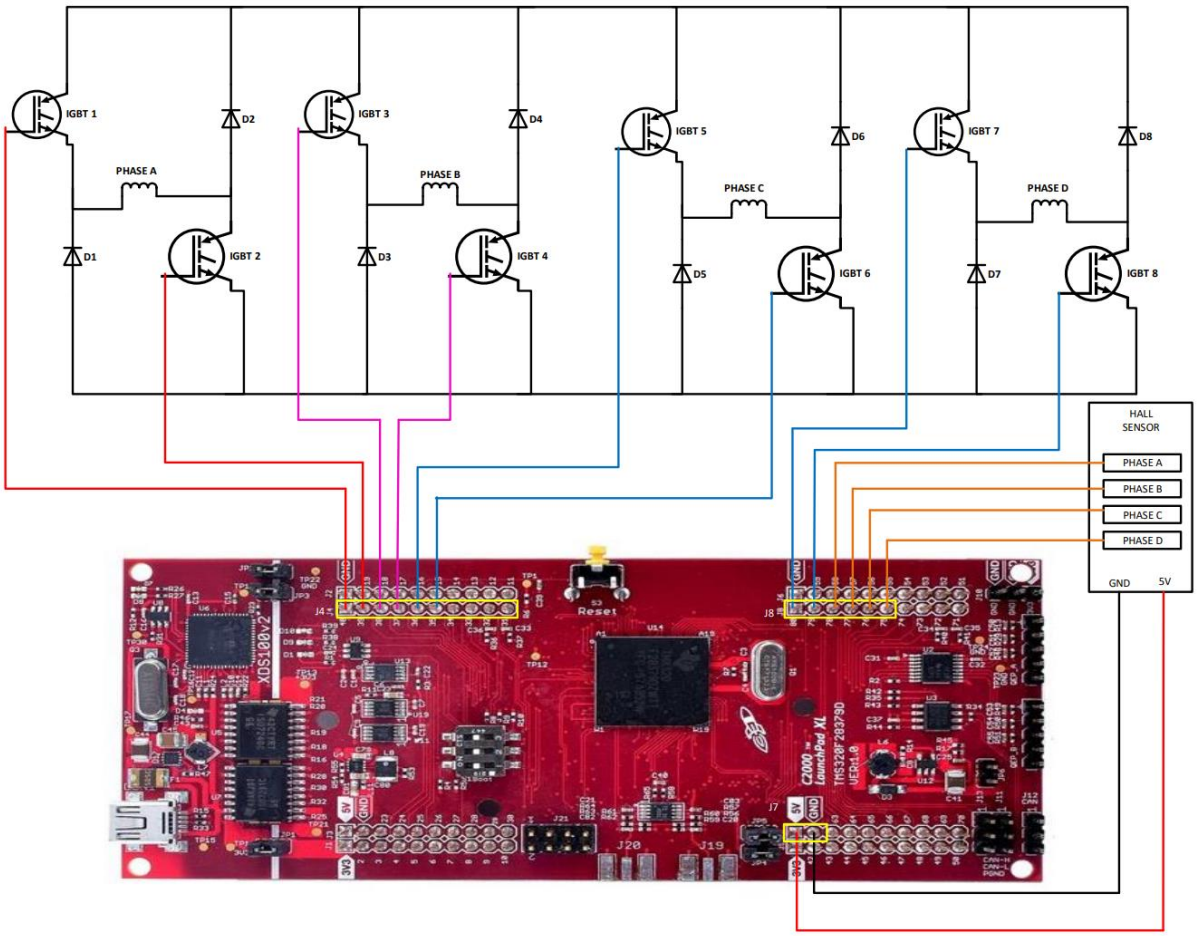


Fig 5.20 TMS320F28379D a DSP Based PID Controller Connections

5.6 Summary

This chapter includes the simulation circuit using MATLAB/SIMULINK and PSIM software, flow chart and the hardware components that are used for implementation were discussed. It also includes the connection diagram connected to the asymmetric bridge and the hall sensors.

Chapter 6

RESULTS AND DISCUSSIONS

The chapter includes the simulation results and hardware results for the speed control of SRM.

6.1 Simulation Results

Chapter 5 presented the simulation circuit for the speed control of SRM. The results observed from the circuits are explained.

The reference speed is set at 1500rpm and the obtained response is displayed in the scope. The graph depicted on the scope is speed against time with the value of K_P is 50. The reference speed used in the simulation circuit is 1500rpm and the obtained speed is also 1500rpm. A plot of speed varying with time is as shown in Fig 6.1.

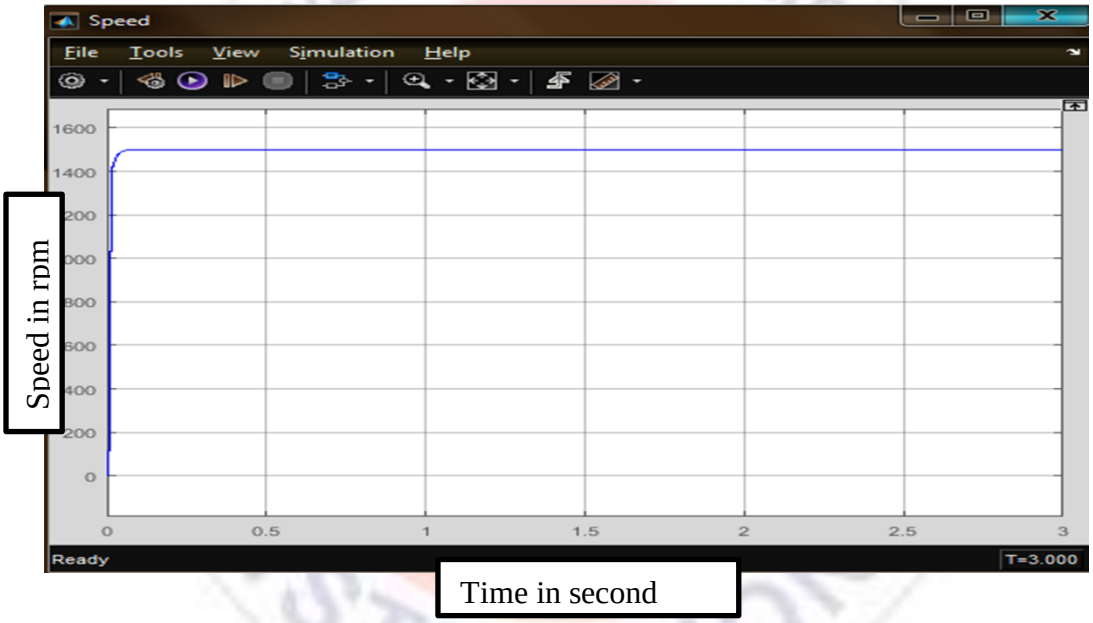


Fig 6.1 A Plot of Speed Varying Time using P Controller K_P = 50 and Reference Speed = 1500rpm

By varying the value of K_p the graph depicted on the scope is speed varying with time with the value of K_P is 40. The reference speed used in the simulation circuit is 1500rpm and the obtained speed is also 1500rpm. A plot of speed varying with time is as shown in Fig 6.2. Similarly, the value of K_P is 30 and the output speed as 1500rpm that is as mentioned in Fig 6.3.

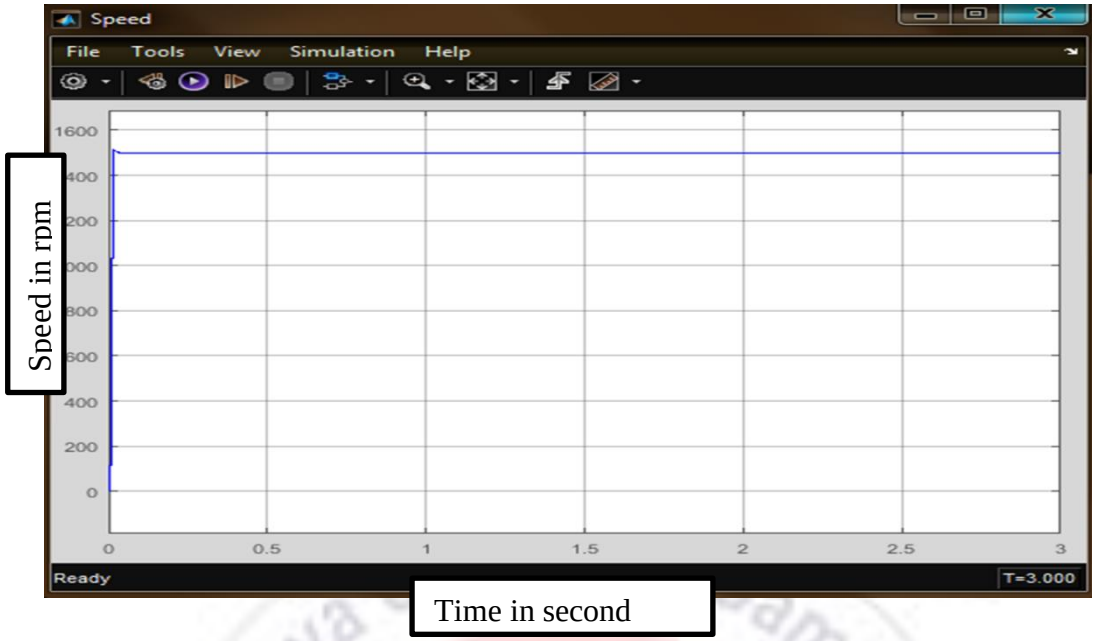


Fig 6.2 A Plot of Speed Varying Time using P Controller K_P = 40 and Reference Speed = 1500rpm

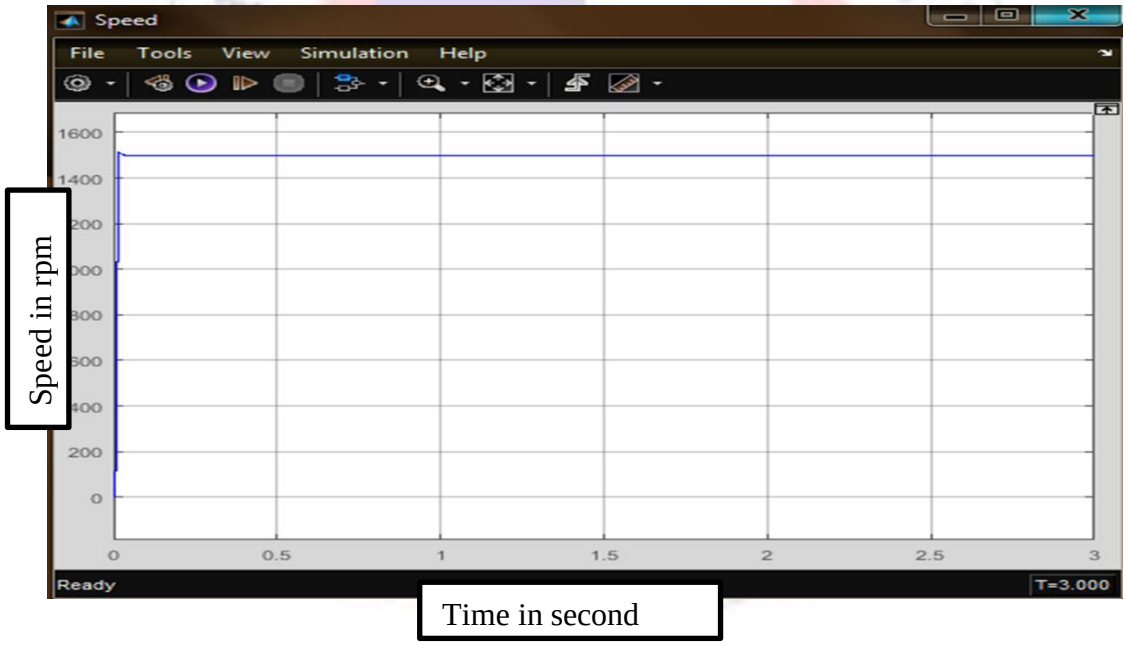


Fig 6.3 A Plot of Speed Varying Time using P Controller K_P = 30 and Reference Speed = 1500rpm

The reference speed is set at 1500rpm and the obtained response is depicted in the scope. The graph depicted on the scope is speed varying with time with the value of K_P is 50 and K_i is 0.01. The reference speed used in the simulation circuit is 1500rpm and the obtained speed is also 1500rpm. A plot of speed varying with time is as shown in Fig 6.4.

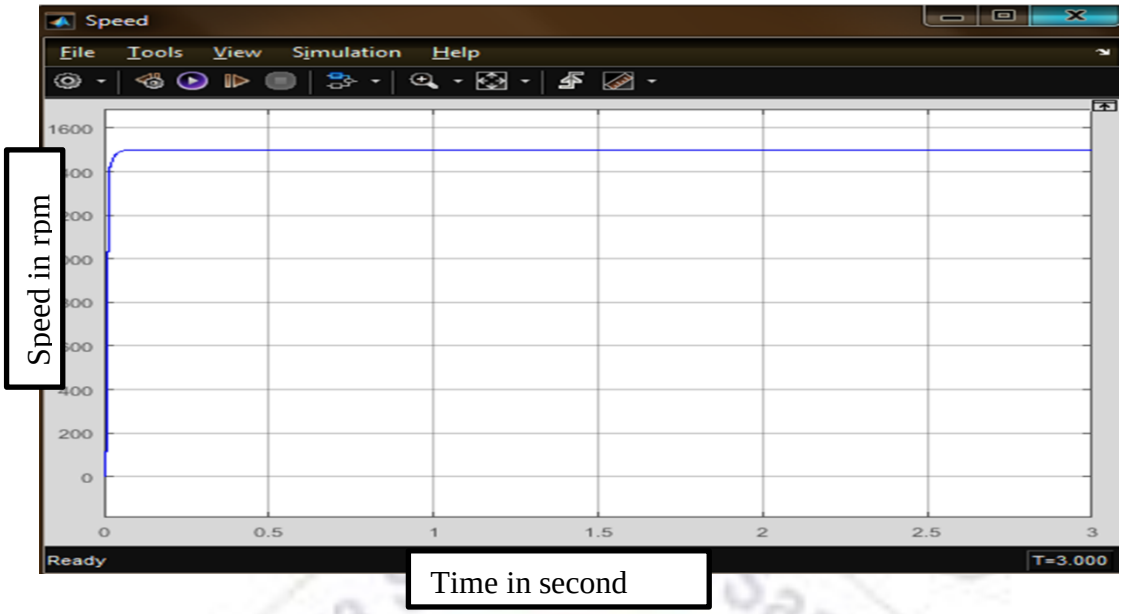


Fig 6.4 A Plot of Speed Varying Time using P Controller K_P = 50, K_i = 0.01 and Reference Speed = 1500rpm

By varying the value of K_p and K_i the graph depicted on the scope is speed varying with time with the value of K_P and K_i. Similarly, the value of K_P is 50 and K_i is 0.01 and K_P is 40 and K_i is 0.01 and the output speed as 1500rpm that is as described in Fig 6.5 and Fig 6.6 respectively.

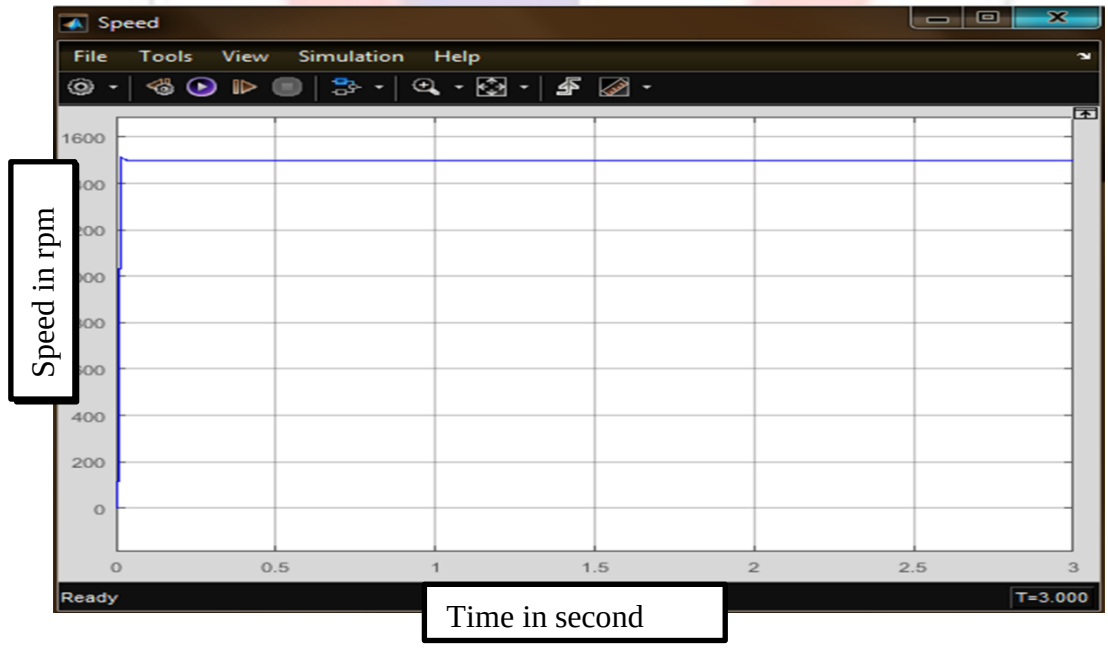


Fig 6.5 A Plot of Speed Varying Time using P Controller K_P = 40, K_i = 0.01 and Reference Speed = 1500rpm

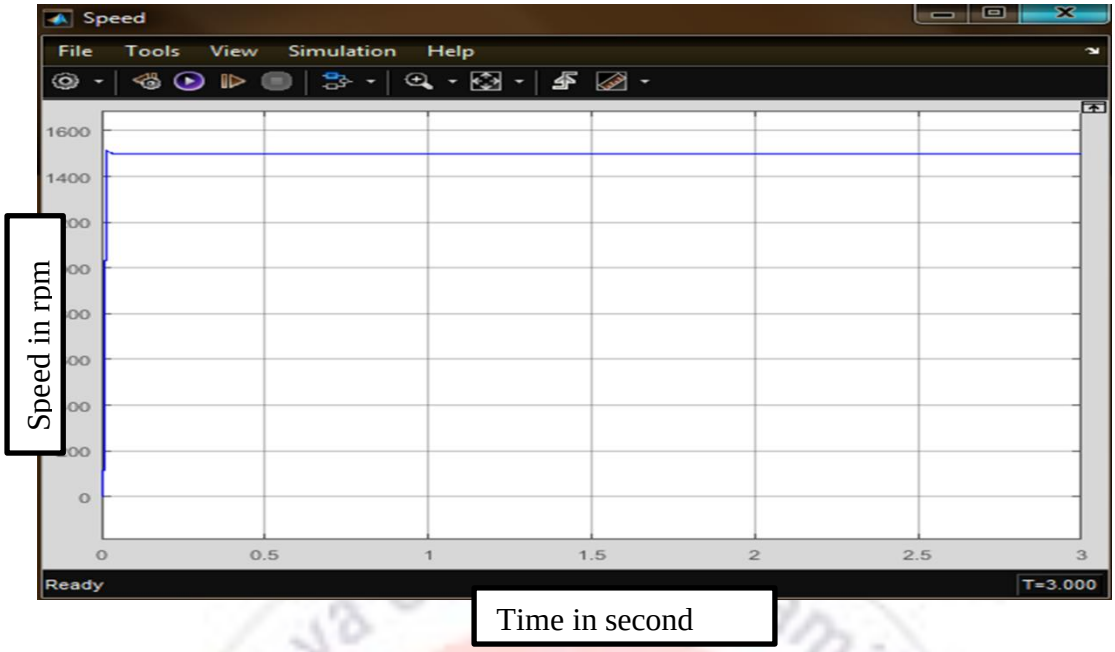


Fig 6.6 A Plot of Speed Varying Time using P Controller K_P = 30, K_i = 0.2 and Reference Speed = 1500rpm

The reference speed is set at 1500rpm and the obtained response is depicted in the scope. The graph depicted on the scope is speed varying with time with the value of K_P = 20, K_i = 0.1 and K_d = 0.05. The reference speed used in the simulation circuit is 1500rpm and the obtained speed is also 1500rpm. A plot of speed varying with time is as shown in Fig 6.7.

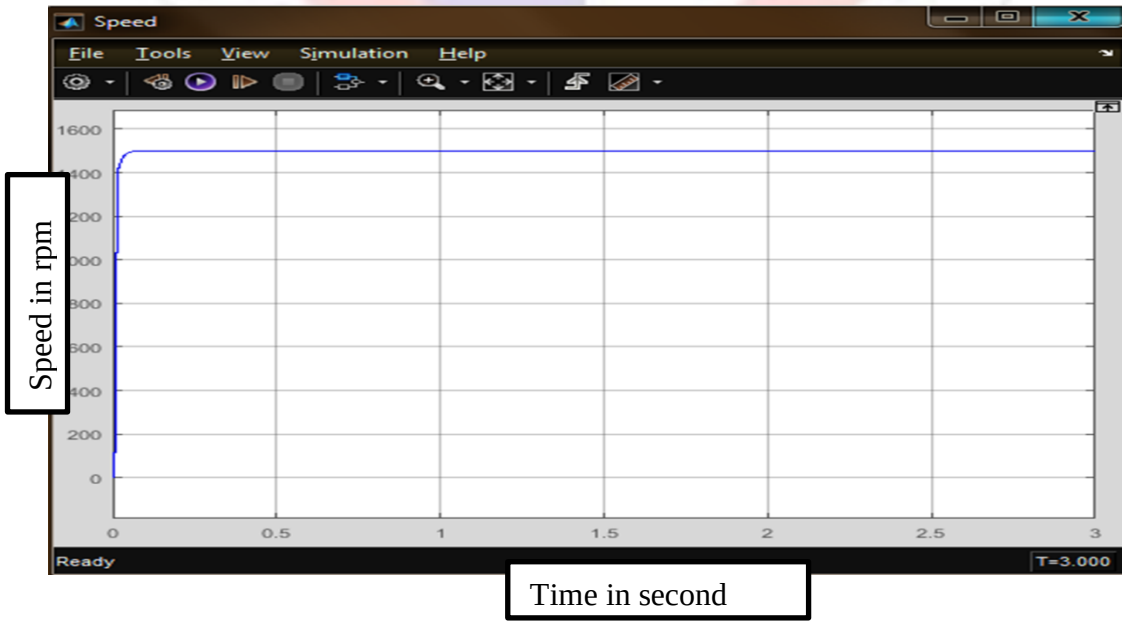


Fig 6.7 A Plot of Speed Varying Time using P Controller K_P = 20, K_i = 0.1 and K_d = 0.05, Reference Speed = 1500rpm

By varying the values of K_p, K_i and K_d the graph depicted on the scope is speed varying with time with the value of K_P and K_i. Similarly, the values of $K_P = 30$, $K_i = 0.01$ and $K_d = 0.5$ and of $K_P = 40$, $K_i = 0.2$ and $K_d = 0.04$ and the output speed as 1500rpm that is as shown in Fig 6.8 and Fig 6.9 respectively.

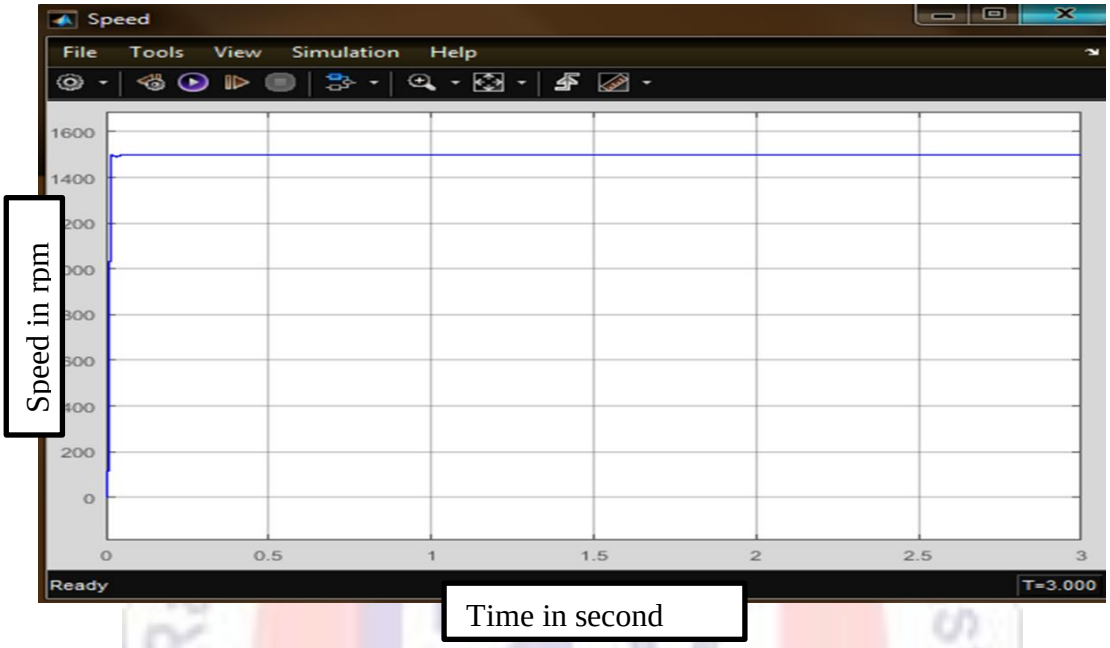


Fig 6.8 A Plot of Speed Varying Time using P Controller $K_P = 30$, Ki = 0.01 and $K_d = 0.5$, Reference Speed = 1500rpm

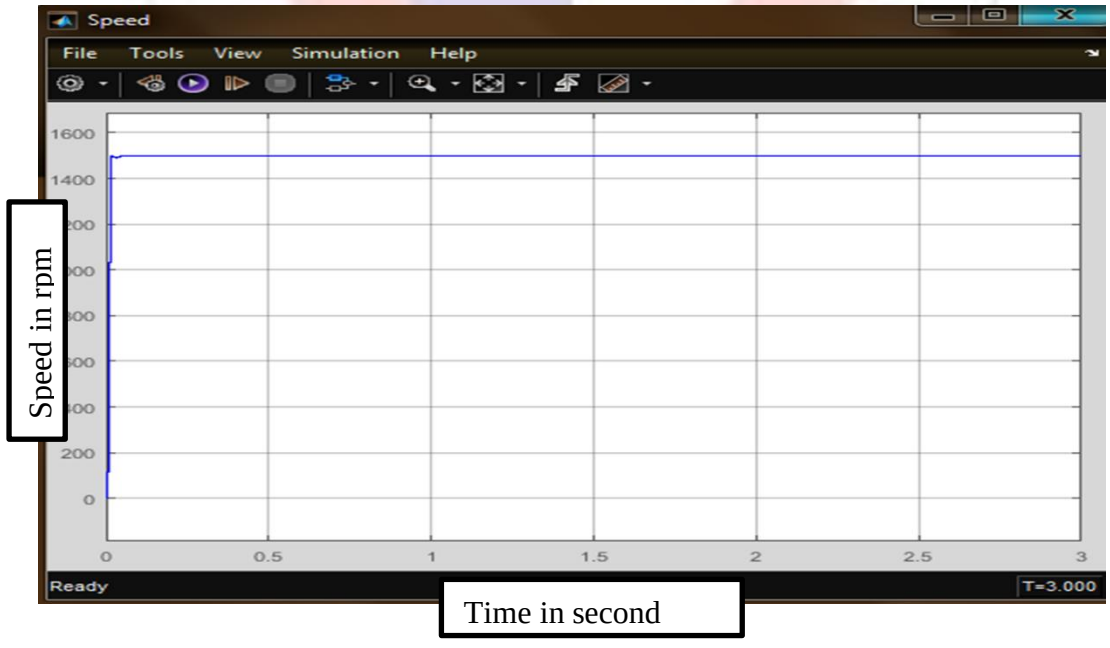


Fig 6.9 A Plot of Speed Varying Time using P Controller $K_P = 40$, $K_i = 0.2$ and $K_d = 0.04$, Reference Speed = 1500rpm

Simulation results of SRM for speed control using PID controller is as mentioned in Table 6.1.

Table 6.1 Simulation results for speed control of SRM using PID controller

		Reference speed in rpm	Actual speed in rpm
P controller	$K_p = 50$	1500	1500
	$K_p = 40$	1500	1500
	$K_p = 30$	1500	1500
PI controller	$K_p = 50, K_i = 0.01$	1500	1500
	$K_p = 40, K_i = 0.01$	1500	1500
	$K_p = 30, K_i = 0.2$	1500	1500
PID controller	$K_p = 20, K_i = 0.1, K_d = 0.05$	1500	1500
	$K_p = 30, K_i = 0.01, K_d = 0.5$	1500	1500
	$K_p = 40, K_i = 0.2, K_d = 0.04$	1500	1500

Simulation of Asymmetric Bridge is as mentioned in Fig 5.9 in Chapter 5. The output voltages across various phases V1, V2, V3 and V4 is as shown in Fig 6.10, Fig 6.11, Fig 6.12, and Fig 6.13 respectively.

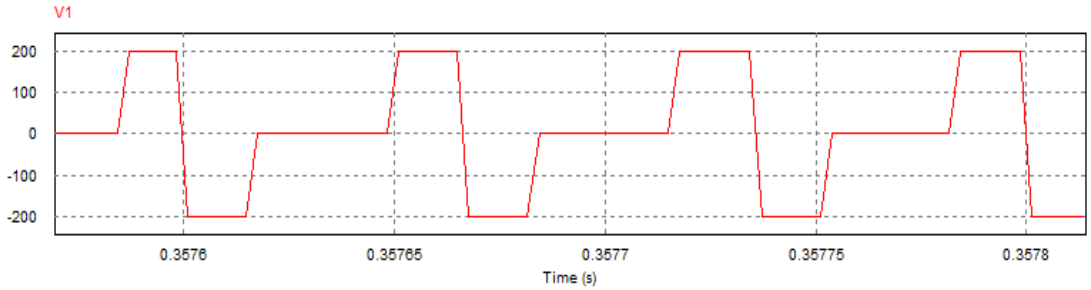


Fig 6.10. Output Voltage across Phase A (V1)

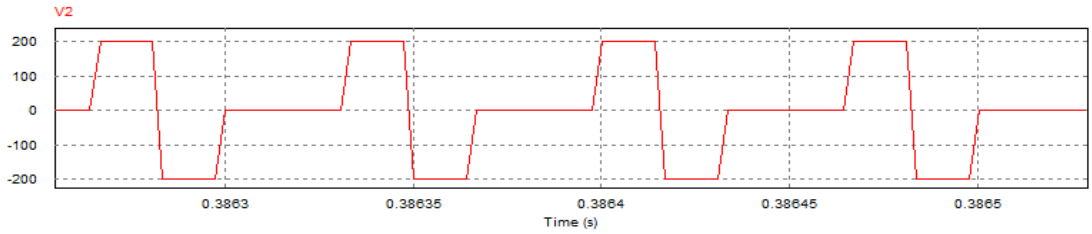


Fig 6.11. Output Voltage across Phase B (V2)

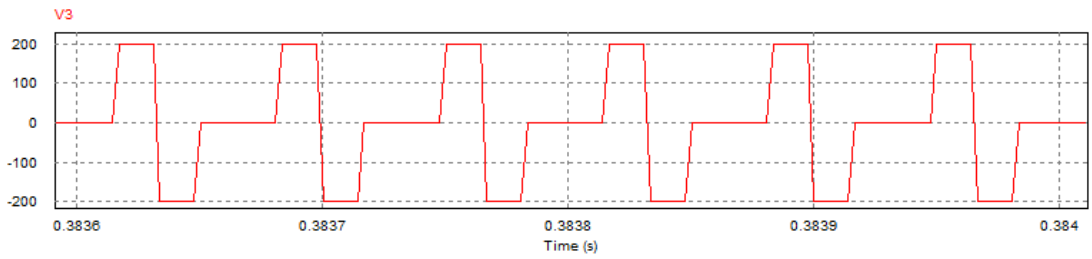


Fig 6.12. Output Voltage across Phase C (V3)

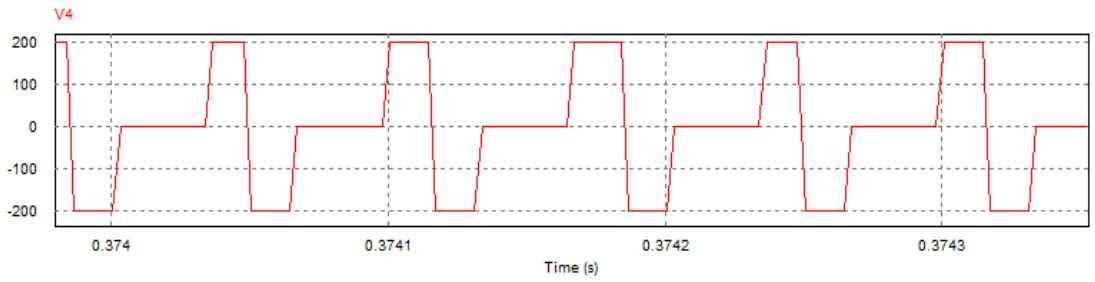


Fig 6.13. Output Voltage across Phase D (V4)

The voltage across the capacitor Vc is as shown in Fig 6.14.

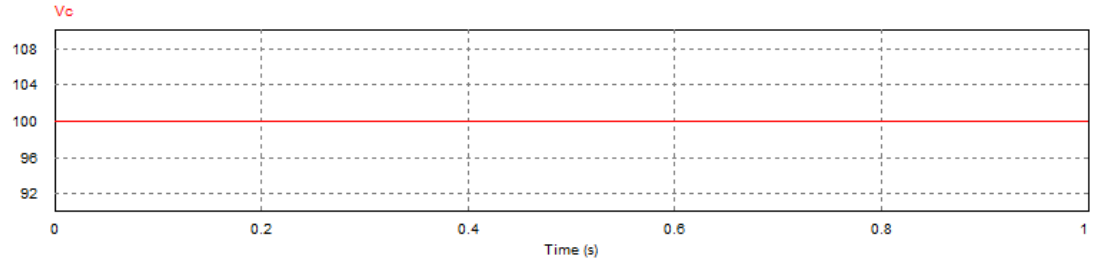


Fig 6.14. Voltage across Capacitor (Vc)

The currents through the switches IGBT 1,2,3 and 4 are as provided in Fig 6.15.

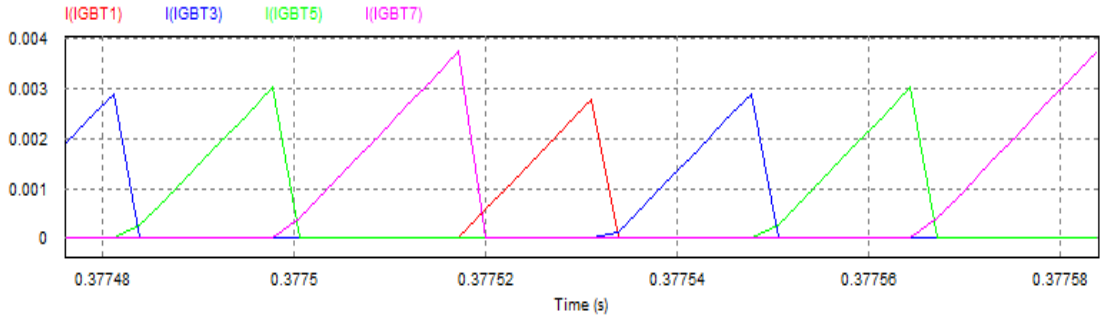


Fig 6.15. Currents Through Switches IGBT 1,3,5 and 7

The currents through diodes D1, D3, D5 and D7 are as provided in Fig 6.16.

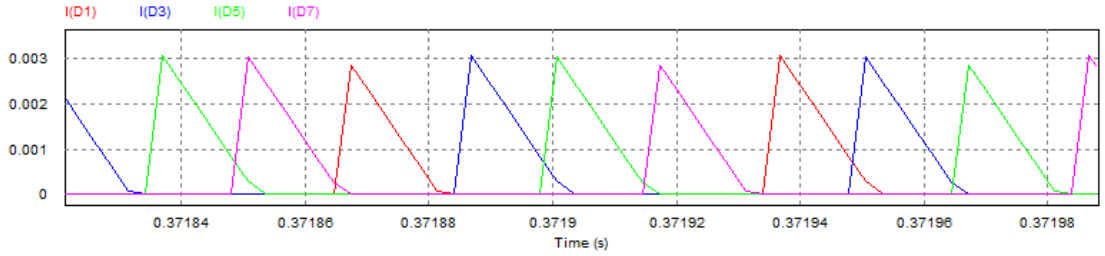


Fig 6.16 Currents Through Diodes D1, D3, D5 and D7

6.2 Hardware Results

The designed values are used for selecting various components. The overall setup of the proposed hardware is as shown in the Fig 6.17.

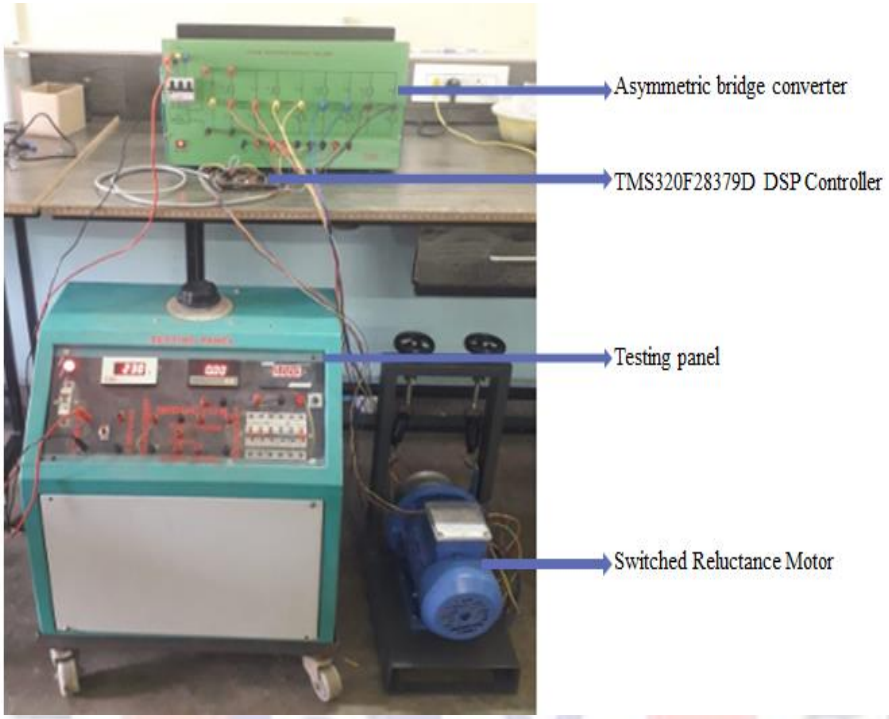


Fig 6.17 Hardware Module of SRM

The hardware module is tested for open loop and closed loop conditions. For open loop condition the supply voltage is 201.5 VDC as shown in Fig 6.18(a) and 151 VAC as shown in Fig 6.18(b) and the reference speed is kept at 1500rpm but obtained speed is 1420rpm are as shown in Fig 6.18(c).

Fig 6.18(a) DC Supply Voltage in V

Fig 6.18(b) AC Supply Voltage in V and Current in A

Fig 6.18(c) Speed in rpm for Open Loop Condition

For closed loop condition the supply voltage is 210.7 VDC as shown in Fig 6.19(a) and 151 VAC as shown in Fig 6.19(b) and the reference speed is kept at 1500rpm but obtained speed is 1420rpm are as shown in Fig 6.19(c).

Fig 6.19(a) DC Supply Voltage in V

Fig 6.19(b) AC Supply Voltage in V and Current in A

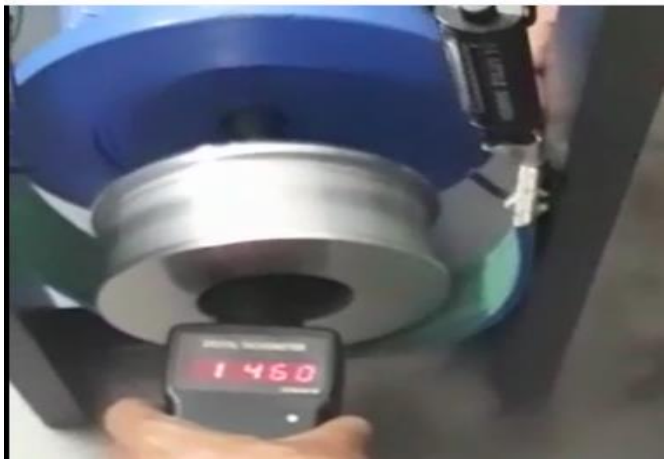


Fig 6.19(c) Speed in rpm for Closed Loop Condition

Speed of the motor during no-load and full-load condition. The reference speed is 1500rpm but obtained speed at no-load is 1644rpm is as shown in Fig 6.20(a) and at full-load is 1180rpm as shown in Fig 6.20(b) respectively.

Fig 6.20(a) Speed in rpm at No-Load Condition

Fig 6.20(b) Speed in rpm at Full-Load Condition

Hardware results of SRM for speed control is as shown in Table 6.2.

Table 6.2 Hardware results for speed control of SRM

AC voltage (V)	Reference speed (rpm)	Simulation result of speed in rpm	Measured speed (rpm) Open loop	Measures speed (rpm) Closed loop
31	1500	1500	186.1	1417
50	1500	1500	256.8	1423
70	1500	1500	402.5	1446
90	1500	1500	754	1442
110	1500	1500	987.5	1452
130	1500	1500	1287.6	1454
150	1500	1500	1428	1460

6.3 Summary

This chapter includes the simulation results that was simulated using MATLAB/SIMULINK and PSIM software. The software, hardware results were noted. Both simulation and hardware results were compared.

Chapter 7

CONCLUSION AND FUTURE SCOPE

Now a days, SRMs are more attractive due to its simple construction. SRM is highly reliable, less expensive, high-speed capacity, high torque to inertia ratio that is one of the important choices for different application. The presence of nonlinear behaviour of SRM, it is not so easy to control. SRM is suitable for high-speed applications mainly due to its robust nature, the salient poles including concentrated windings of on rotor and stator and also the absence of winding on rotor. The simplest of all the motor techniques is adopted. Speed control of SRM is simulated and implemented by using PID controller.

The 8/6 SRM consists of built-in hall sensors with loading. An asymmetric bridge including 4 phase bridge rectifier is used to keep the output voltage regulated. An asymmetric bridge is mainly of IGBT based semiconductor diode is used that operates at a frequency of 15 kHz. The gating pulse for IGBT is provided from the DSP controller. An asymmetric bridge is that mainly consists of 4 phases. The SRM is an 8 stator slots and 6 rotor slots that consists of inbuilt hall sensors. Hall sensors are mainly used for detecting the speed and position of rotor. The speed of the motor is measured using hall sensor, so the actual speed of motor is measured. The actual speed is compared with the reference speed. An error is generated that is supplied to the PID controller. The pulses are varied based on the error signals. The pulse width modulation generator generates the gating pulses and is directly supplied to the SRM through IGBT asymmetric bridge converter. A 4-phase asymmetric bridge converter is designed. The speed control of SRM is performed using MATLAB/SIMULINK software by varying the values of P, PI and PID controller. The proposed speed control of SRM is tested for both no-load and full-load condition with reference speed is 1500rpm.

7.1 Conclusion

- The 6/4 SRM is driven by an asymmetric bridge converter and construction is simple and control compared to a commutation motor.
- SRM is modelled on MATLAB/Simulink and it is simulated for best performance. PID controller is better in comparison to P and PI controller. The 4-phase asymmetric bridge converter is designed.

- The speed control of SRM is performed using MATLAB/SIMULINK software by varying the values of P, PI and PID controller.
- The hardware for the speed control of SRM is tested. The hardware for the speed control for open loop with the reference speed is 1500rpm but obtained speed is 1420rpm.
- The hardware for the speed control for open loop with the reference speed is 1500rpm but obtained speed is 1460rpm.
- The proposed speed control of SRM is tested for both no-load and full-load condition with reference speed is 1500rpm. The obtained speed at no-load is 1644rpm and at full-load is 1180rpm.

7.2 Future Scope

Following are the scope for further improvements of this project work**.**

- The issues related to SRM can be solved to provide solutions with reasonable cost and performance since the cost of SRM is very high.
- Design of the motor with speed – torque performance for applications with higher efficiency and less size.
- Controller design of SRM is more complex as compared to other motors due to the dependency of torque developed on the rotor angle.
- Elimination of mechanical position sensor that reduces size of motor and cost so the reliability of system can be improved.

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Design and implementation of speed control of Switched Reluctance Motor

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Objective

The main objective of the project is

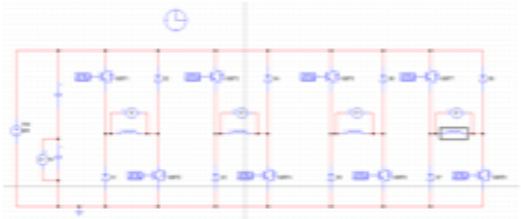
- To design 1 phase rectifier.
- To design of 4 phase asymmetric bridge converter.
- To simulate speed control of SRM using P, PI and PID controller using MATLAB/Simulink.
- To develop the hardware for speed control of SRM.

➤ To test the hardware module for open loop and closed loop condition.
➤ To test the hardware module for no-load and full-load condition.

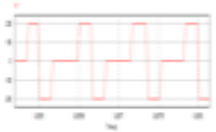
Project Methodology

When supply and necessary pulses are given 8 stator slots and 6 rotor poles Switched Reluctance Motor which gives the output speed. The motor consists of a hall sensor where the measured speed is obtained. The measured speed is compared with the reference speed where the error signal is obtained which is directly given to the PID block. The proportional controller, integral controller and the differential controller are tuned to a particular value so that the speed will not go beyond the reference speed. The duty cycles are given to the PWM block which is directly given to the IGBT asymmetric bridge converter. The variation between the reference speed and the measured. If the variation is high, the manipulated variable will get affected and it cannot stabilize higher order processes. Large gain is needed to improve the steady state error, when proportional controller is used. In each phase, the upper switch is used to perform the PWM switching control, while the lower one is used in charge of commutation. Each phase can be controlled independently.

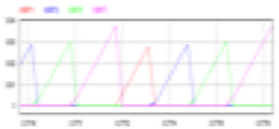
Block diagram



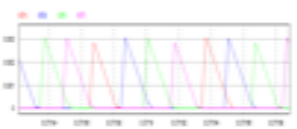
Simulation of 4-phase asymmetric bridge converter using PSIM



Output voltage in V



Current through switches in A



Current through diodes in A

Specifications

Motor parameters	Values
Rated Power	1Hp
Number of Stator Poles	8
Number of Rotor Poles	6
Speed	2500rpm
DC supply	240V
Inductor	1mH
DSP based controller	TMS320F28379D
Step down transformer	230/14V
Capacitor	2200uF, 250V
Rectifier output	296VDC

Hardware module for speed control of SRM

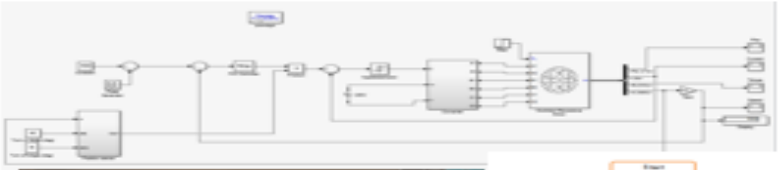
Results and Discussions

Simulation and hardware results

A DC supply voltage of 240V is used. The converter turn-on and turn-off angles are kept constant at 45deg and 75deg, respectively, over the speed ranges. The reference current is 200A and the hysteresis band is chosen as ±10A. The SRM is started by applying the step reference to the regulator input. The acceleration rate depends on the load characteristics.

The value of the constants of the controller KP, Ki and Kd is dependent on the system to be controlled, so after tuning appropriately and testing for best condition, the values of the constant used for this analysis was obtained as follows: For P controller, KP = 50; For PI controller, KP = 50, Ki = 0.1; For PID controller, KP = 20, Ki = 0.1, Kd = 0.05

For hardware, for 8 number of stator slot and 6 number of rotor slots. Speed is measured with built-in hall sensors of SRM. An error is generated which is given to PID controller. DSP based PID controller is used as the speed control of SRM is done. For a speed of 1500rpm the open loop and closed loop is done. Speed of the motor during no-load and full-load condition. The reference speed is 1500rpm but obtained speed at no-load is 1644rpm and at full-load is 1180rpm respectively.



Time in s

Hardware results

AC voltage (V)	Current (A)	Reference speed (rpm)	Measured speed (rpm) Open loop	Measured speed in rpm Closed loop
31	0.19	1500	166.1	1417
50	0.19	1500	256.0	1433
70	0.20	1500	402.5	1446
90	0.20	1500	754	1442
110	0.20	1500	907.5	1452
120	0.20	1500	1397.5	1444
128	0.20	1500	1439	1452

Flow chart

Conclusions

- The 1-phase rectifier and 4-phase asymmetric bridge converter is designed.
- The speed control of SRM is performed using MATLAB/SIMULINK software by varying the values of P, PI and PID controller.
- The hardware for speed control of SRM is done and tested.
- The hardware for the speed control for open loop and closed loop with the reference speed is 1500rpm but obtained speed is 1420rpm and 1460rpm respectively.
- The speed control of SRM is tested for both no-load and full-load condition with reference speed is 1500rpm but obtained speed at no-load is 1644rpm and at full-load is 1180rpm respectively.

Future Scope

- To solve the issues of SRM to provide solutions with reasonable cost and performance since the cost of SRM is very high.
- To design a motor with speed – torque performance for any application with less size and higher efficiency.
- Dependency of torque developed on the rotor angle makes controller design of SRM more complex compared to other motors.

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Speed Control of Switched Reluctance Motor

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Abstract – Recently Switched Reluctance Motors are suitable for replacing the other conventional motors like DC motor, Induction motor mainly because of low cost, improved efficiency of motor, and variable speeds. This paper uses MATLAB/SIMULINK to demonstrate the simulation of SRM speed control. MATLAB/SIMULINK is used to simulate the speed control of a 6/4 SRM. The 6 stator slots and 4 rotor poles are driven by an asymmetric bridge converter. Hardware implementation of SRM is performed for both open loop and closed loop condition.

Key Words: *Asymmetric bridge converter, Switched Reluctance Motor, PID controller.*

1. INTRODUCTION

Switched Reluctance Motor (SRM) is being used from the year 1938. Limited utilization of SRM is mainly due to the absence of power electronic components in the earlier days. Development of power electronic components used to boost all the motor drives [1-2]. SRM is also known as variable reluctance motor. SRM is rugged, simple to construct, economical and exhibits fault tolerant capability as compared to induction motor and synchronous motor. High peak torque to inertia ratio is exhibited by SRM. The mechanical structure of the rotor is suitable for high-speed applications, electric vehicles and in various industries [3]. Due to the non-linear behavior of SRM, it is not that easy to control. SRM is highly suitable for application that involves very high-speed operation mainly due to its robust nature. The construction of SRM is as shown in Fig.1 [1,4].

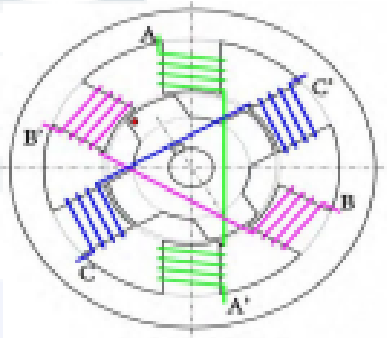

Fig.1. Construction of SRM [2]

The salient poles with concentrated windings are present on rotor and stator poles. The feature that stands SRM apart from other motors is the absence of winding on rotor [5-7]. The block diagram of speed control of SRM is as shown in the Fig.2. The number of stator slots and number of rotor slots differs based on the applications. Normally used SRMs having number of stator slots and number of rotor poles are 6/4 or 8/6 or 10/8 or 12/10 respectively. The number of stator and rotor slots is not recommended to be same. Here, 6 stator slots and 4 rotor slots are used for simulation i.e, 6/4 SRM. An asymmetric bridge with 3 phase bridge rectifier is used to keep the output voltage regulated [8-10].

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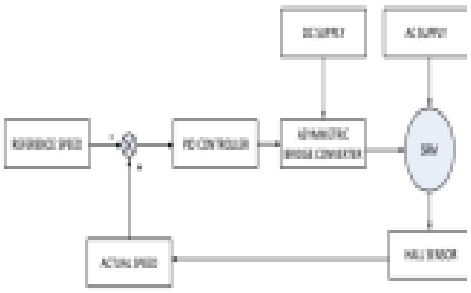

Fig.2. Block Diagram of Speed Control of SRM

2. PROPOSED CONFIGURATION

The asymmetric bridge converter is used to provide fast excitation current. So, high switching voltage is therefore necessary. Fig.3 shows the circuit diagram of asymmetric bridge converter for 3-phase drive of SRM [4]. Strategy of unipolar switching is incorporated in the converter. For each phase or leg of the converter, there are two power switches and two diodes. The upper switch is used to switch control of PWM in each phase or leg, and the bottom switches are used to charge commutation. So, every phase is controlled independently. Magnetization, freewheeling, and demagnetization modes of operation are the various operating conditions. The inner current control loop of the drive system uses the unipolar switching method to reduce current ripple and improve frequency response. Table 1 represents the parameters considered for simulation of speed control of SRM [1].

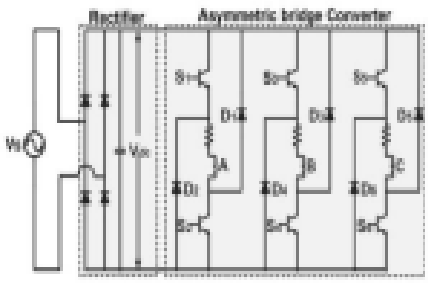

Fig.3. Asymmetric bridge converter

Table 1: Parameters considered for simulation of speed control of SRM

Motor parameters	Values
Rated Power	60kW
Number of phases	3
Number of stator poles	6
Number of rotor poles	4
Aligned phase inductance	23.6mH
Unaligned phase inductance	0.67mH
Inertia	0.05kg.m
Stator resistance	0.05Ω
DC Voltage supply	240 V
Inductor	1mH

4. SIMULATION RESULTS

The simulation of speed control of SRM is performed using MATLAB/SIMULINK software. The supply voltage that is applied to the circuit is 240VDC. The turn-on angle and turn-off angle supplied to the converter is 45° and 75° respectively. The specifications for speed control of SRM are as shown in the Table 1. The reference speed is considered as 1500rpm. The converter used for simulation is an asymmetric bridge converter. Position sensor is mainly used to gather all the physical data from the motor and converts them into electrical input signals to the system. They measure the distance of object or body from a particular position from the reference point.

Speed control using P controller:

Proportional controller is a type of control system that operates in the direction of a line or linear and acts as a correction element between the measured value and the reference value. An error is generated by the comparison of actual and the reference value [5]. The error input supplied to the circuit is

$$u = K_p * e(t)$$

For the steady state error to be improved, a large gain is necessary. A proportional controller is therefore employed. The value of K_p is used by tuning method. The value of K_p used in the simulation circuit is 50.

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Simulation of speed control of SRM for P controller is as depicted in Fig 4.

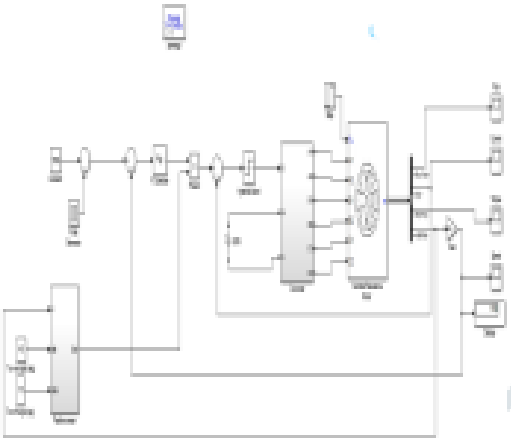

Fig.4 Speed Control of SRM using P Controller

Speed control using PI controller:

Proportional integral controllers are also known as proportional in conjunction with integral control. Proportional integral is used to reduce error between the measured value and the reference value by varying the value of input supplied to the circuit. PI controller is a combination of both proportional control and the integral control. Speed control of SRM using PI controller is simple, implementation is easier, low cost, less error in the steady state condition and highly robust [5].

The error input supplied to the circuit is

$$u = K_p * e(t) + K_i * \int e(t)\,dt$$

The tuning procedure is used to determine Kp and Ki values. The simulation circuit uses Kp and Ki values of 50 and 0.1, respectively. Fig. 5 depicts the simulation of SRM speed control for PI controller.

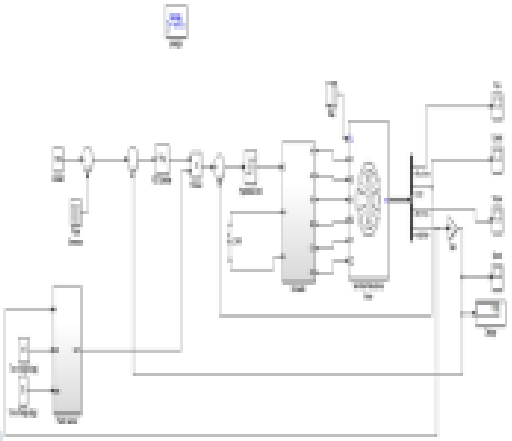

Fig.5 Speed Control of SRM using PI Controller

Speed control using PID controller:

Proportional Integral Differential Controller is a closed loop system that is commonly used in most of the industrial and other applications. The error that is generated is reduced in spite of increase in gain [5]. The error input supplied to the circuit is

$$u = K_p * e(t) + K_i * \int e(t)\,dt + K_d * \frac{de(t)}{dt}$$

The tuning procedure is used to determine the values of K_p, K_i, and K_d. The simulated circuit uses K_p, K_i, and K_d values of 20, 0.1, and 0.05, respectively. Fig. 6 depicts the simulation of SRM speed control for PID controller. The tuning method is often used to get the values of Kp, Ki, and Kd. Kp, Ki, and Kd values are

Proportional controller, $K_p = 50$

Proportional Integral controller, $K_p = 50$, $K_i = 0.1$

Proportional Integral Differential controller, $K_p = 20$, $K_i = 0.1$, $K_d = 0.05$

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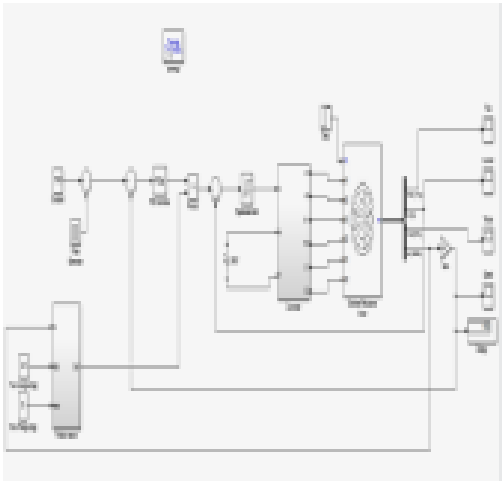

Fig.6 Speed Control of SRM using PID Controller

The simulation results for the simulation of speed control of SRM for P controller is as shown in Fig 7 and the waveform is same for PI and PID controller.

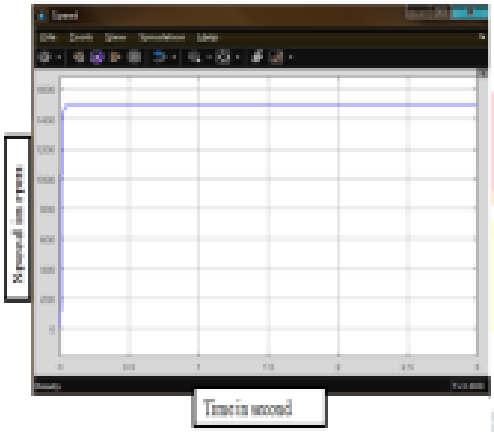

Fig.7 A plot of Speed using P controller with Kp = 50 and reference speed = 1500rpm

Simulation results for speed control of SRM using PID controller is as shown in Table 2.

Table2 Simulation results for speed control of SRM using PID controller

		Reference speed in rpm	Actual speed in rpm
P controller	Kp = 50	1500	1500
	Kp = 40	1500	1500
	Kp = 30	1500	1500
PI controller	Kp = 50, KI = 0.01	1500	1500
	Kp = 40, KI = 0.01	1500	1500
	Kp = 30, KI = 0.2	1500	1500
PID controller	Kp = 20, KI = 0.1, Kd = 0.05	1500	1500
	Kp = 30, KI = 0.01, Kd = 0.5	1500	1500
	Kp = 40, KI = 0.2, Kd = 0.04	1500	1500

The hardware for speed control of SRM is performed for 8/6 SRM with 8 stator poles and 6 rotor poles for 1 kW motor. The hardware is implemented for both open loop and closed loop condition. For open loop condition the reference speed is maintained at 1500 rpm and the measured value is 1428rpm at 200VAC. Under closed loop condition, here also the reference speed is maintained at 1500rpm and the measured speed is 1460rpm for 210VAC. Since it is under closed loop condition the PID controller provides 1460rpm as the output speed under both no-load and full load conditions. Hardware results for speed control of SRM is as shown in Table 3.

Table 3: Hardware results for speed control of SRM

AC voltage (V)	Reference speed (rpm)	Simulation result of speed in rpm	Measured speed (rpm) Open loop	Measured speed (rpm) Closed loop
31	1500	1500	186.1	1417
50	1500	1500	256.8	1423
70	1500	1500	482.5	1446
90	1500	1500	734	1442
110	1500	1500	997.5	1452
130	1500	1500	1287.8	1434
150	1500	1500	1428	1460

5. CONCLUSION

MATLAB/SIMULINK is used to simulate the speed control SRM. An asymmetric bridge converter powers the 4 rotor poles and 6 stator slots. So, the construction is simple and speed control is easy. Based on the PID values the output speed that is obtained is same as the reference speed. Hardware implementation of SRM is performed for both open loop and closed loop condition and the measured

speed is almost same as the reference speed. The future scope of the project is

- The issues related to SRM can be solved to provide solutions with reasonable cost and performance since the cost of SRM is very high.
- Design of the motor with speed – torque performance for applications with higher efficiency and less size.
- Controller design of SRM is more complex as compared to other motors due to the dependency of torque developed on the rotor angle.
- Elimination of mechanical position sensor that reduces size of motor and cost so the reliability of system can be improved.

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We appreciate your valuable contribution and wish you success in your future endeavours.
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ABSTRACT

With the extent use of internal combustion engines for driving automobiles has resulted in violation of exhaust emission standards and rise of fuel economy, increase in non-safety of vehicle users. The electromechanical system helps system control to improve fuel economy and reduce pollutant emissions resulting in increased safety and comfort of passengers. The electromechanical system involves the use of sensors and is considered as a preferable choice for signal conditioning and integration. As sensors become more sophisticated according to market requirements, it results in need of more accurate, specific and reliable sensor interfacing circuit. The use of conventional sensor interfacing circuits like Universal Sensor Interface (USI), Intelligent Sensor Interface, Universal Micro Sensor Interface results in non-optimal solution, higher power consumption and occupies larger area. The use of a flexible sensor interfacing circuit can address the issues.

The proposed work includes the design and validation of flexible sensor interfacing circuit.. The flexible sensor interface block comprised of protective devices such as common mode and differential capacitors, ESD protection devices such as ESD capacitors and ESD diodes, pull-up and pull down resistors, attenuator circuit, a RC lowpass filter and L9966 IC. The signals from the sensor interface block were processed into VRSP and VRSN pins of L9966 IC. By the comparator action located inside L9966 IC, digital rectangular pulses were generated were fed into the microcontroller. Here, basically three types of sensors such as Hall effect sensor, Inductive sensor, Push-pull type sensor were tested for functionality. The analysis was carried out using a suitable simulation tool. The verification and validation of the designed circuit was performed using Monte Carlo and Sensitivity analysis. After verification, hardware design was implemented.

The average output voltage obtained during simulation analysis was 3.3 V. The performance validation was incorporated using Monte Carlo and Sensitivity Analysis tool. The three sigma data of Monte Carlo Histogram plot verified that circuit design was 99.7% accurate considering all boundary conditions and worst case conditions. The view of Sensitivity analysis gave an idea how to optimize the circuit as per the design requirements After validation, hardware analysis was implemented. The average output voltage during hardware analysis was 5 V. The results of simulation analysis and hardware analysis were proved to be compatible.

LIST OF PUBLICATIONS

Publication Type	Publication Details
International Journal	Gangadhar Mahalingappa Akki, Dr. S G Srivani, Uma Maheswari R, "Design and Verification of a Flexible Sensor Interface Module for Engine Control Unit", *Journal of Emerging Technologies and Innovative Research (JETIR),* pp. f1-f17 Vol No 9, Issue No 6, June 2022.

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GLOSSARY

ESD	:	Electrostatic Discharge Protection
EMI	:	Electromagnetic Interference
EMC	:	Electromagnetic Compatibility
PSI5	:	Peripheral Sensor Interface 5
USI	:	Universal Sensor Interface
UMSI	:	Universal Macro Sensor interface
VRSP	:	Variable Reluctance Sensor Positive
VRSN	:	Variable Reluctance Sensor Negative
VRS_OUT	:	Variable Reluctance Sensor Output
TVS	:	Transient Voltage Suppressors

CHAPTER 1

INTRODUCTION

The growing demand for new technological solutions in automobiles has led to the replacement of mechanical system with electromechanical solutions. Over the last two decades the electronic content in automobiles and lorries has significantly increased. In contemporary cars it has reached a value of about 15–20% and it is expected to further increase to 35–40% due to legislation and environmental requirements [1]-[5]. The electromechanical system helps system controls to improve fuel economy and reduce pollutant emissions and improving the comfort and safety of vehicle users. With the recent advancement in microelectronics, many sensors are being used in wide variety of applications, particularly in automotive industries and are considered as a preferable choice for signal conditioning accuracy and integration which is increasingly used in vehicles due to their ease of application [6]-[10]. One key element in automotive electronics field is sensor and thus sensor interface circuits beside the actuators. In a contemporary car, between 70 and 150 sensors are accommodated measuring pressure, temperature, position, air flow, acceleration, yaw rates, tilt angles, humidity and speed and few other applications. Thus, sensors have become an important element in the overall automotive electronic system [11]-[15].

The sensor functioning becomes sophisticated as market trends and customer requirements increase, this leads to the requirement of more accurate and reliable sensing element [16]-[20]. Due to the central importance of such sensor systems, the development of integrated automotive sensor interface and conditioning circuits require a dedicated development, qualification and test flow to meet the very demanding requirements of automotive quality and to avoid costly call-back actions [21]-[29]. The new flexible sensor interfacing circuit can help in improving the accuracy and can be considered as the suitable choice for sensor interfacing [30]-[35].

The flexible sensor interfacing circuit is an automotive grade IC designed to be used as parameter sensing interface equipment. L9966 IC is one such type of dedicated integrated chip. The dedicated chip comprises of 15 channels available for analog sensing, resistance measurement and digital sensing (e.g. temperature, lambda, pressure, position sensors). The L9966 allows replacing the number of discrete components and it gives the possibility to change the sensors across different applications without modifying the PCB hardware.

The flexible sensor interfacing circuit is a part of an electronic control unit of an automotive

and acts as a functional block that receives the electrical signals from sensor output and processes it and compares the received signal with the reference signal. By the comparator action, rectangular pulses are generated. The generated digital pulses are fed into a microcontroller. The microcontroller drives the actuator and an alarm signal is generated. The generated alarm signal controls the engine control unit. The Monte Carlo Analysis and Sensitivity Analysis tools are implemented for circuit verification and validation.

1.1 Overview

The design of a flexible sensor interface module for is presented for providing an interface for automotive sensors [2]. A sensor interface basically receives inputs from different parts of the vehicle, depending on its function. The flexible sensor interface block comprises of protective devices such as common mode and differential capacitors for EMI/EMC protection, ESD protection devices such as ESD capacitors and ESD diodes, pull-up and pull down resistors, attenuator circuit, a RC lowpass filter and L9966 IC. A RC lowpass filter damps out undesired signals before giving it as a input to a L9966 IC. The signals from the sensor interface block is processed into VRSP and VRSN pins of L9966 IC. The difference between the VRSP and VRSN signals is known as the control signal. An internal comparator located inside an IC, compares the control signal to the reference signal and thus by the comparator action, digital rectangular pulses are generated. The generated pulses are fed into the microcontroller. Here, basically three types of sensors such as Hall effect sensor, Inductive sensor, Push-pull type sensor are interfaced to an electronic control unit. The analysis is carried out using a suitable simulation tool. The verification and validation of the designed circuit is performed using Monte Carlo and Sensitivity analysis [15]-[17]. After verification, hardware design is implemented.

1.2 Specific Details

The Flex input IC has a programmable interface for accommodating 15 inputs, 12 inputs are meant for analog signal conditioning and 3 inputs for digital signal conditioning. The circuit also contains 1 analog output channel and 4 digital output channels. Capacitors CSTvrsp and CSTvrsn of 4.7nF provide low impedance path for incoming transient ESD pulses and there by preventing the IC pins from damage. Capacitor Cvrspn of 1nF provides a low impedance path to shunt high frequency differential noise, there by providing EMC/EMI protection connected between Rpu and Rpd. Resistances RIN1,RIN2,RIN3,RIN4,Rsrup1,Rsrup2,Rsrlo1,Rsrlo2,Radj form the attenuator circuit. Capacitors Cvrsp and Cvrsn of 470pF act as common mode filters protect the VRSP and VRSN pins from EMI/EMC problem [10]-[11].

1.3 Literature Survey

The sensor interface is basically a circuit that performs signal conditioning and makes a logical decision and generates the output so that the process is controlled in a desired manner. The design environment for developing a digital interface for a given automotive sensor was presented. The concept of analog signal interfacing is not discussed [1].

The single chip solution of Universal Sensor Interface (USI) offered an advantage to be compatible with a wide set of sensors, not allowed designers to achieve optimal solution for a given sensor. The use of an USI resulted in higher power consumption and area occupation, and it offered lower performances as compared to a chip dedicated to a particular type of sensor [2]-[4].

The need to design high-performance dedicated sensor interfaces, without designing a chip from scratch in order to meet time-to-market requirements resulted in a need to develop new platform based design methodologies [5]-[8].

Single Edge Nibble Transmission (SENT) was a promising low-cost solution for communication between off-ECU sensors and a microcontroller. The sensor interface was meant for automotive applications such as vacuum measurement, clogged filter detection, industrial applications such as process monitoring, fluid pressure Consumer/Home. The task analysed the advantages of digital sensors with a special focus on position sensors. The possible integration of SENT in other application fields (such as pressure sensors) was not discussed [9]-[11]

ISIF (Intelligent Sensor Interface) platform developed by Sensor Dynamics AG was introduced. Such platform was designed to offer a wide range of software, digital, analog IPs, for fast prototyping ad hoc solutions for a particular class of sensors, in a way that from ISIF only the most suitable modules have to be picked to realize an optimum specific-sensor interface. Further more power consumption, area occupation and time-to-market were the major drawbacks identified [12]-[14]

The Universal Micro Sensor Interface (UMSI) served as a single-chip interface solution to support many low-power microsystem applications utilizing capacitance, resistance, voltage and digital output sensors. It comprises of user programmable modes and implements many useful functions. More power consumption and the non-flexibility of the UMSI were the issues identified in the work [15]-[19].

Some interesting sensor interfacing circuits were developed including an interface for capacitive and resistive readout, a mixed voltage sensor interface with self test and a mixed signal data acquisition system that combines a microcontroller and analogue readout. The use of such interfacing circuits resulted in high cost and non linearity [20]-[22].

Magnetic sensors of position, distance, and speed were reliable, precise, rugged, and durable. They were inexpensive and are suitable for defence and automotive applications. A position sensor based on the mutual inductance between two air coils is reported. The position error is 1% for 240 mm distance. This shows that the accuracy of inductive sensor was low for smaller distances [23]-[24].

The PSI5 interface was used to connect multiple sensors to electronic control units (ECUs) and was used as the primary sensor communications bus for airbags and related restraint systems. PSI5 (Peripheral Sensor Interface 5) was a digital bus interface to connect control units and sensors. The introduction of PSI5 paid the way for digital interfacing of pressure sensor. The concept of analog sensor interfacing was not dealt in the work [25]-[26].

The smart pressure sensor showed the improved reliability and greater accuracy due to its built-in temperature compensation, filtering and self-calibration capabilities. The economy of pressure sensor was high [27]-[30]. The work includes the use of a Hall Effect Sensor to control the flow of the engine cooling fluid. The use of hall effect sensor requires auxiliary supply for its operation [31]-[36].

1.4 Motivation

In the present automotive sector, as sensors become more sophisticated according to market requirements, it results in need of more accurate, specific and flexible sensor interfacing circuit [16-17]. The use of a flexinput L9966 IC, a automotive grade IC as a sensor interface block can overcome such complexity. The use of L9966 IC incorporates an advantage to be compatible with wide variety of sensors and allows designers to achieve optimal solution resulting low power consumption. Up to 15 channels are available for analog sensing, resistance measurement and digital sensing (e.g. temperature, lambda, pressure, position sensors). The L9966 allows to replace the number of discrete components and it gives the possibility to change the sensors across different applications without modifying the PCB hardware. The use of a flexinput results in increased flexibility and reduction in overall cost of the system.

1.5 Problem Statement

To design, simulate and validate the performance of a flexible sensor interface module, that can interface different sensors to an electronic control unit without modifying the PCB hardware.

1.6 Objectives and Scope

The main objectives of the proposed work include:

- To design and implement the flexible sensor interfacing circuit.
- To simulate and validate the performance of a developed circuit using Monte Carlo Worst Case Analysis and Sensitivity Analysis technique by interfacing with different sensors.
- To develop the Hardware module of flexible sensor interfacing circuit.
- To test and analyse the performance of a developed Hardware module with different sensors.

1.7 Organization of Report

The project report consists of total seven chapters. An introduction to each phase in developing the work is listed as follows.

Chapter- 1 consists of a literature survey that was carried out to understand the need of a flexible sensor interface module design. It includes the problem definition, objectives of the project, motivation behind carrying out this project.

Chapter- 2 presents the information about automotive sensors. The construction and working of hall effect sensor, inductive sensor, Push Pull type sensor are discussed. The Monte Carlo analysis, sensitivity analysis, simulation steps for monte Carlo and sensitivity analysis is also discussed.

Chapter -3 consists of the methodology adopted in the work to meet the objectives. It also consists of details about electrostatic discharge protection, attenuator circuit, RC low pass filter, flex inpu integrated circuit.

Chapter- 4 includes specifications and the design details of various components used for the simulation model of project.

Chapter-5 presents the simulation studies of the proposed system in Pspice. It also provides the hardware approach for the project. The experimental set up to test the hardware is explained in detail.

Chapter-6 presents the results of simulation analysis and hardware implementation performed. In this chapter, the waveforms of various parameters such as VRSP, VRSN, VRS_OUT are

analysed using simulation and hardware testing. The simulated results of monte carlo, sensitivity analysis are also observed.

Chapter -7 discusses the history of the various interfacing circuits adopted in the past, their demerits and a brief overview of the proposed system and its merits. It also discusses the conclusion and future scope proposed of the work.

Followed by References consisting of list of papers referred for understanding and analyzing the project work.

CHAPTER 2

ELECTRONIC CONTROL UNIT FOR AUTOMOTIVES

This chapter deals with the theory of automotive sensors, details about Hall sensor, Inductive sensor, Push Pull type sensor, monte carlo simulation and sensitivity analysis simulation.

2.1 Automotive Sensors

Automobile technology is one of the most evolved and the cars present at the moment lay bare as evidence. The result of the technological development in car manufacturing is various components serve to make driving and car maintenance a hassle-free engagement. Among the essential parts that most important is the car sensor. It plays a crucial role in the car in notifying an issue within its system. It helps to narrow down to the part with a problem and saves on time when it comes to repairs and maintenance of vehicle. There are different types of sensors used in cars. They are embedded in the engine and each of them performs a specific function. With a sensor-equipped vehicle, the assurance of efficiency on the road is guaranteed.

Sensors are essential components of automotive electronic control systems. Sensors are defined as "devices that transform (or transduce) physical quantities such as pressure or acceleration (called measurands) into output signals (usually electrical) that serve as inputs for control systems." The primary automotive sensors were discrete devices used to measure oil pressure, fuel level, coolant temperature, etc. Starting in the late 1970s, microprocessor-based automotive engine control modules were phased in to satisfy federal emissions regulations. These systems required new sensors such as MAP (manifold absolute pressure), air temperature, and exhaust-gas stoichiometric air-fuel-ratio operating point sensors. The need for sensors is evolving and is progressively growing. For example, in engine control applications, the number of sensors used will increase from approximately ten in 1995 to more than fourty, in upcoming years [2].

Automotive engineers are challenged by a multitude of stringent requirements. For example, automotive sensors typically must have combined/total error less than 3 % over the entire range of operating temperature and measurand change including all measurement errors due to nonlinearity, hysteresis, temperature sensitivity and repeatability. Moreover, even though hundreds of thousands of the sensors may be manufactured, calibrations of each sensor must be interchangeable within 1 percent. Automotive environmental operating requirements are also very severe, with temperatures of 40 to 125 C (engine compartment), vibration sweeps up to 10 g for

30 h, drops onto concrete floor (to simulate assembly mishaps), electromagnetic interference and compatibility, and so on. When purchased in high volume for automotive use, cost is always a major concern. Mature sensors (e.g., pressure types) are currently sold in large-quantities (greater than one million units annually) at a low cost of less than $3 (US) per sensor (exact cost is dependent on application constraints and sales volume), whereas more complex sensors (e.g., exhaust gas oxygen, true mass intake air flow and angular rate) are generally several times more costly. Automotive sensors must, therefore, satisfy a difficult balance between accuracy, robustness, manufacturability, interchangeability, and low cost. Important automotive sensor technology developments are micromachining and microelectromechanical systems (MEMS). MEMS manufacturing of automotive sensors began in 1981 with pressure sensors for engine control, continued in the early 1990s with accelerometers to detect crash events for air bag safety systems and in recent years has further developed with angular-rate inertial sensors for vehicle-stability chassis systems. What makes MEMS important is that it utilizes the economy of batch processing, together with miniaturization and integration of on-chip electronic intelligence. Simply stated, MEMS makes high-performance sensors available for automotive applications, at the same cost as the traditional types of limited-function sensors they replace. In other words, to provide performance equal to today's MEMS sensors, but without the benefits of MEMS technology, sensors would have to be several times more expensive if they were still made by traditional electromechanical/discrete electronics approaches [4].

As shown in Fig 2.1, the three major areas of systems application for automotive sensors are powertrain, chassis, and body. In the present systems-classification scheme, anything that isn't powertrain or chassis is included as a body system application. Fig 2.1 also identifies the main control functions of each area of application and the elements of the vehicle that are typically involved. The automotive industry has increasingly utilized sensors in recent years. The penetration of electronic systems and the associated need for sensors is summarized in Table 2.1. Powertrain applications for sensors, shown in Table 2.1, can be thought of as the "1st Wave" of increased use of automotive sensors because they led the first widespread introduction of electronic sensors. Chassis applications for sensors are considered to be the "2nd Wave" of increased use of sensors, and body applications are called the "3rd Wave." Automotive control functions and associated systems for powertrain, chassis and body areas of application are shown respectively in Fig 2.2, Fig 2.3, Fig 2.4.

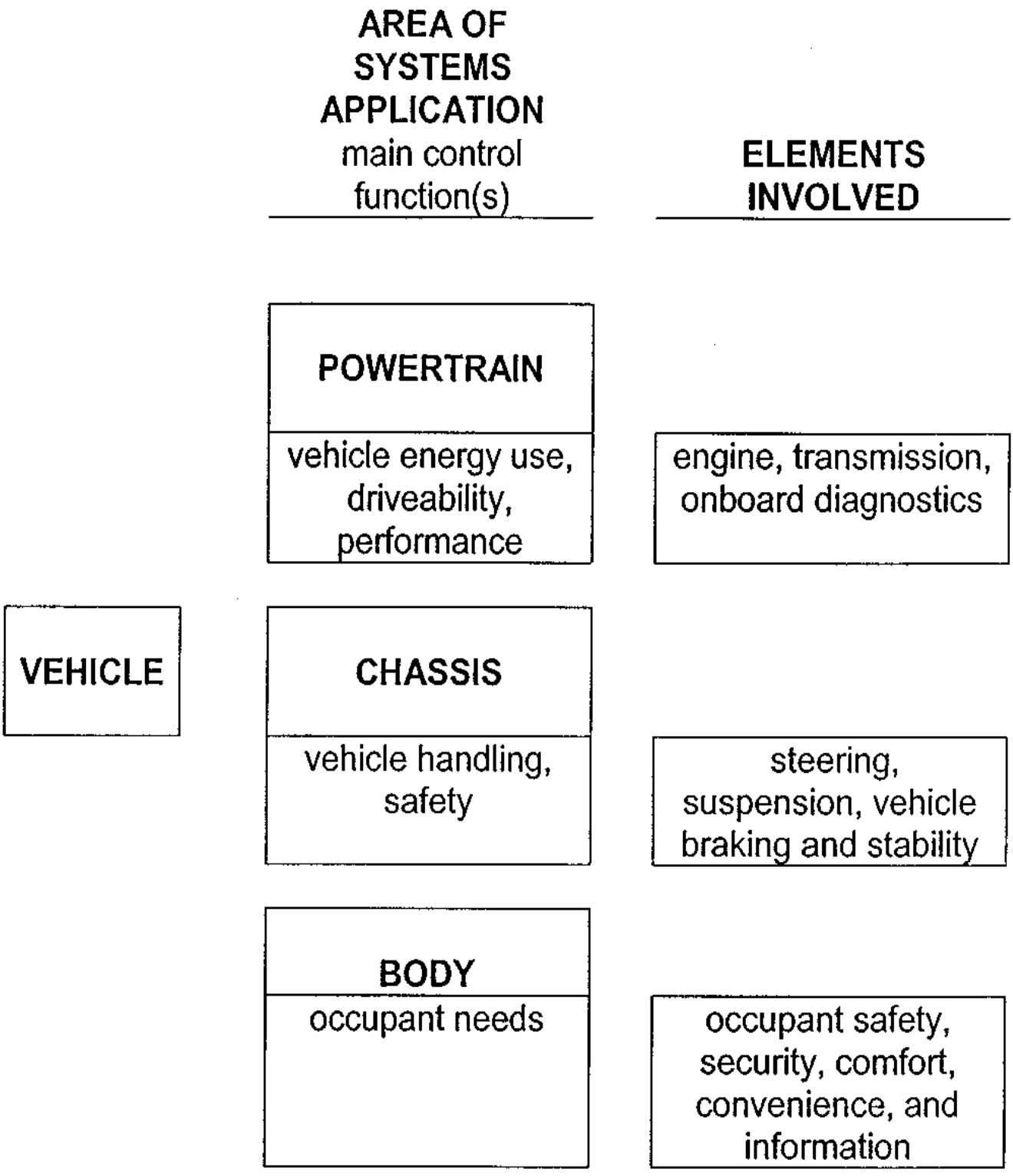

Fig 2.1 Major areas of systems application for automotive sensors [4]

Table 2.1: Driving factors leading to increased use of sensors (North American Automotive market) [4]

POWERTRAIN: "1st Wave," Continued Growth due to Legislation	
	Driving Factors: (*applications*)
1980s and 1990s:	driven by emissions, fuel economy, and onboard diagnostics (OBD-II) legislation, and added features:
	(*closed-loop air-fuel ratio control, catalyst deterioration, engine misfire, and O_2 sensor-degradation, diagnostic systems, cruise control, electronic transmission control*)
2000 and beyond:	driven by ultra-low emssions vehicle (ULEV) legislation, OBD-II added-feature requirements, and best-in-class driveability:
	(*fuel-injection common-rail pressure sensors, variable valve timing, optimized combustion-based engine control*)
CHASSIS: "2nd Wave," Steady Growth due to Demand for Performance	
1980s and 1990s:	driven by vehicle safety and comfort features:
	(*ABS braking, traction control, adaptive suspension, vehicle-stability, electric power steering, on-wheel tire pressure*)
2000 and beyond:	driven by safety, weight/cost reduction, multiplex compatibility, and impending legislation:
	(*vehicle/SUV anti-roll stability systems, fully active suspension, steer-by-wire, brake-by-wire, suspension-by-wire, etc.*)
BODY: "3rd Wave," Accelerating Growth due to Vehicle Personalization	
1980s and 1990s:	driven by safety legislation, security, comfort, convenience, and electronics advances:
	(*air-bag frontal-crash protection, air-bag side-crash protection, theft-deterrent systems, memory seats, navigation*)
2000 and beyond:	driven by safety, new legislation, and intelligent transportation system/electronics advances:
	(*advanced air-bags, rollover-crash curtain-bag protection, collision avoidance, intelligent/ radar cruise-control, real-time traffic and navigation*)

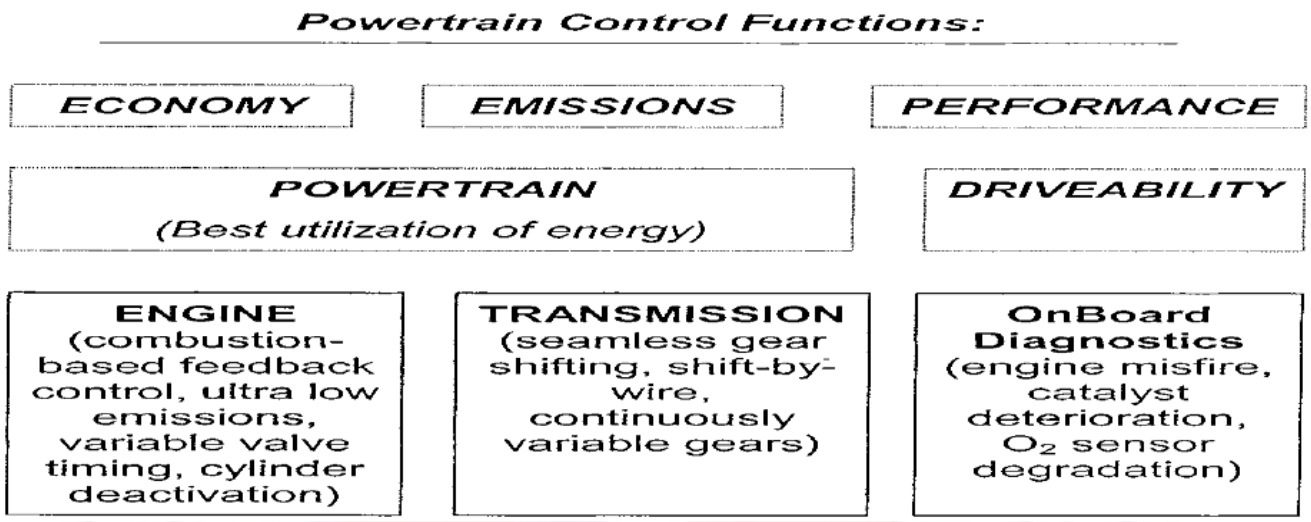

Fig 2.2 Powertrain systems, control functions and applications (Simplified diagram) [4]

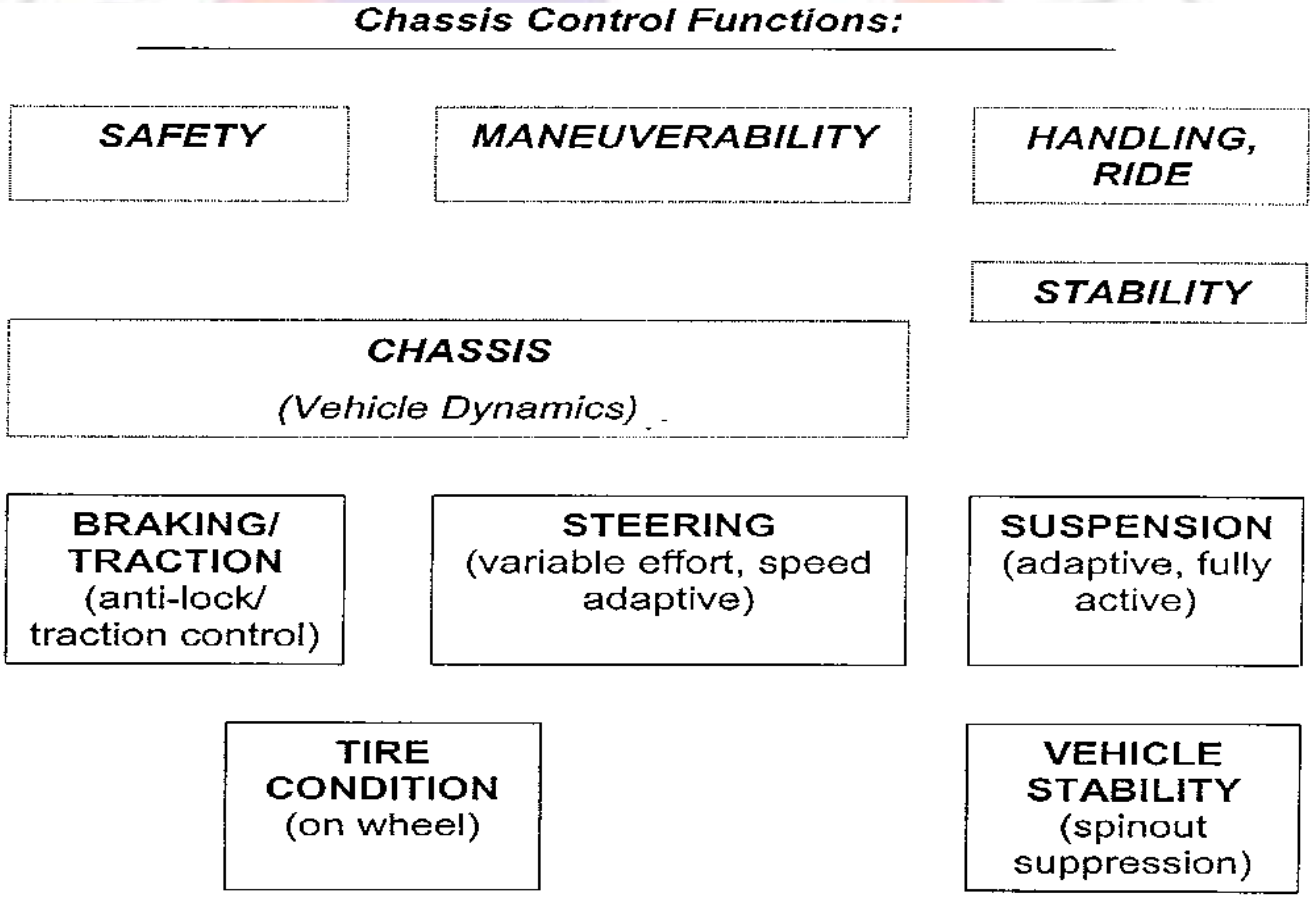

Fig 2.3 Chassis systems, control functions and applications (Simplified diagram) [8]

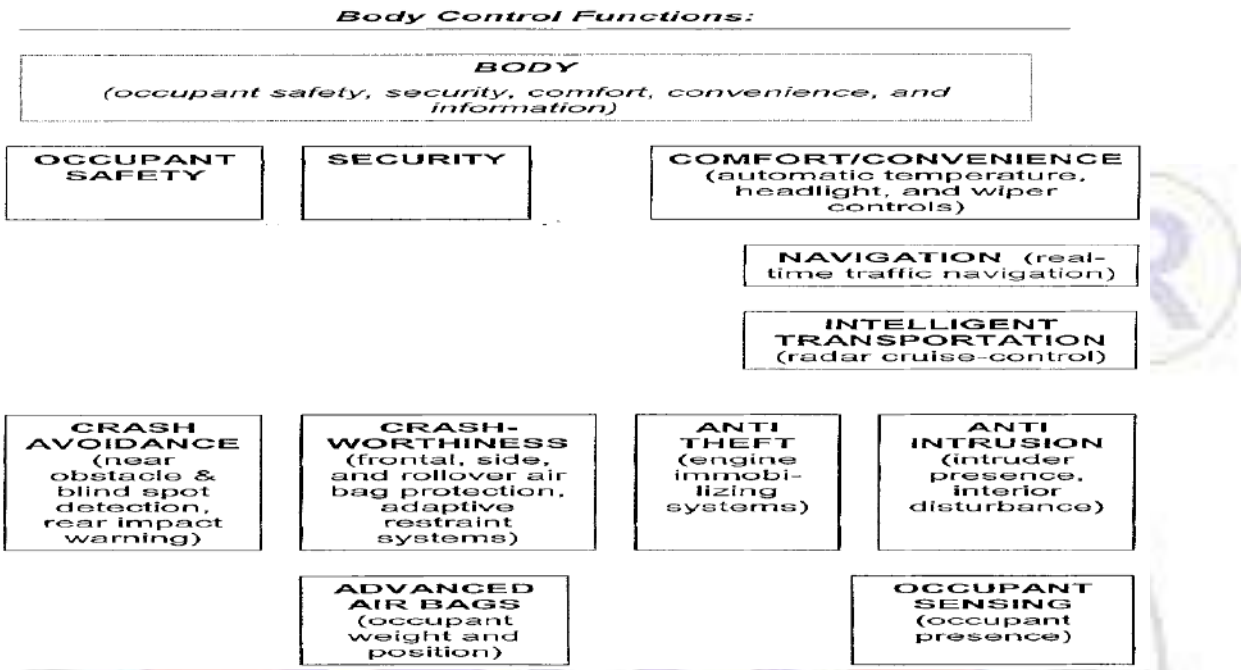

Fig 2.4 Body systems, control functions and applications (Simplified diagram) [8]

2.2 Variable Reluctance Sensor

Variable Reluctance sensors are electromagnetic devices that produce a pulse train- like voltage-output signal governed by the time-varying fluctuations of magnetic flux created by rotating motion of mechanical parts. As gear teeth, slots, or magnetized poles rotate with a shaft and pass by a sensor, flux variations are generated in the sensor's magnetic circuit via Faraday's law and the sensor generates voltage variations in its sensing coil corresponding to the derivative of magnetic flux with respect to time. Variable reluctance sensors are available with low cost, small-to-moderate size, self-generated signals, and good temperature stability. Variable reluctance sensors are used to measure position and speed of moving ferrous objects. The versatility, simplistic design and relatively low cost of manufacturability favors for use in aerospace and automotive industries where it is desired to quantify the rotational speed of engine components such as crankshafts and turbines [6].

The variable reluctance sensor consists of a permanent magnet and a ferromagnetic pole piece surrounded by a coil of wire. The sensor generates an analog voltage output signal when a ferromagnetic material passes by the tip of the pole piece. The induced voltage follows Faraday's

Law of Induction, stated by the equation as:

$$V = -N\frac{d\phi}{dt} \tag{2.1}$$

where N is the number of turns in the coil, ϕ the magnetic flux induced in the coil and t is the time elapsed during the change in magnetic flux. The magnitude of the induced voltage is therefore a direct function of the flux linkage in the coil as a function of time. The configuration of Variable Reluctance Sensor is shown in Fig 2.5.

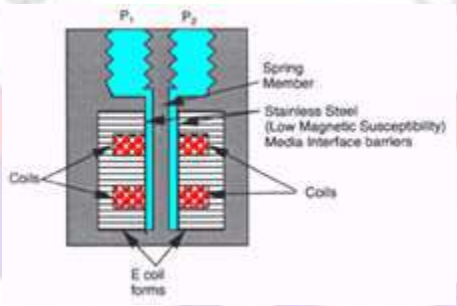

Fig 2.5 The Variable Reluctance Sensor [6]

The coils are sealed from the measurand by nonmagnetic welded stainless steel barriers. In case of the differential pressure transducer, the difference in pressure between the two sides of the spring member causes distortion of the spring member towards the magnetic pole piece on the low pressure side of the spring member resulting in modulation of the inductance of two coils. The electrical configuration of the variable reluctance sensor is that of an inductive half-bridge driven by an alternating voltage source in the range of 1 kHz to 10 kHz. The centrally disposed spring member results in an inductive push-pull arrangement causing deflection of the spring member reduces the inductance of one coil and increases the inductance of the other creating a difference in coil impedance. The variation in the magnetic reluctance produces the effective inductance modulation as a function of the parameter input.

2.2.1 Hall Effect Sensor

The Hall Effect sensor is a magnetic-field sensor that is based on the effect discovered by Edwin Hall in 1879. The electrically isolated device can be applied to sense continuous and alternating currents of typically up to hundreds of kilohertz. Due to its simple structure and compatibility with microelectronics, a Hall device can be monolithically integrated into a fully

integrated magnetic sensor and manufactured using conventional complementary metal–oxide–semiconductor (CMOS) technology [7].

When a conductor is crossed by a current and placed in a magnetic field, the voltage is perpendicular to the current and field. The principle is known as the Hall Effect. When there is no magnetic field and the current distribution is uniform, no potential difference appears at the output. When a perpendicular magnetic field is present, a Lorentz force is exerted on the current. The force causes a disturbance in the current distribution that results in a potential difference between the output terminals. The voltage is known as the Hall voltage (HV). The Hall voltage is proportional to the cross product of the current (I) and the magnetic field (B), as shown in Equation (2).

$$V_{HV} \propto I \times B \tag{2.2}$$

The yield signal for straight (analogue) sensors is taken straight forwardly from the output of the operational amplifier with the output voltage being proportional corresponding to the magnetic field going through the Hall sensor is shown in Fig 2.6. The output Hall voltage is given by Equation 2.3.

$$V_H = R_H \left(\frac{I}{t}\right) \times B \tag{2.3}$$

Where

VH is the Hall Voltage in volts;

RH is the Hall Effect coefficient;

I is the current flow through the sensor in amps;

t is the thickness of the sensor in mm;

B is the Magnetic Flux density in Tesla.

A Hall Effect device is basically a field-effect sensor. It requires an additional circuit to condition the signal and produces an output voltage usable for most applications consisting of an amplifier stage and temperature compensation. A typical Hall transducer has a limited current peak due to core saturation and limited bandwidth (<1 MHz) even though it can measure DC current. In addition, it is very sensitive to external magnetic fields. Hall Effect sensors operate

mainly in closed-loop mode to realize better accuracy and greater dynamic range. These sensors are sensitive to the polarity of the magnetic field (north and south), as in the amplified output, that provides a voltage proportional to the magnetic field to which it is exposed. Saturation occurs in the amplifier, not in the Hall element and does not damage the sensor.

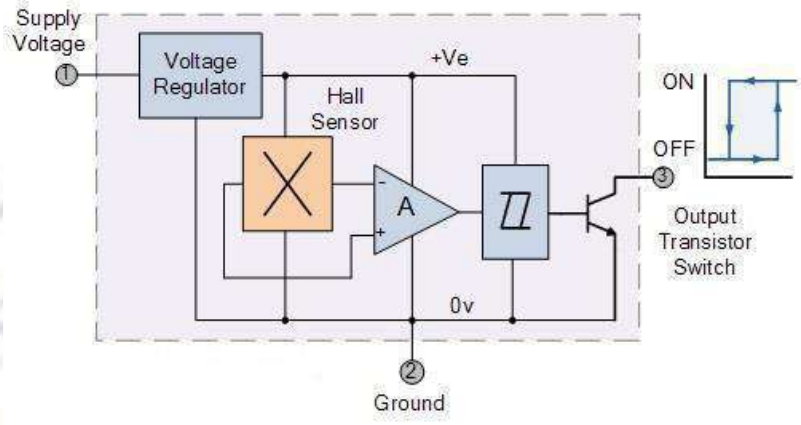

Fig 2.6 Typical Hall effect sensor circuit [7]

Hall effect sensors are solid state gadgets that are becoming more and more popular since they can be utilized in a wide range of sorts of use, for example, detecting position, speed or directional movement. They are additionally a well-known choice of sensor for the gadgets designer due to their non-contact wear free task, their low support, a strong plan and as sealed Hall Effect gadgets are insusceptible to vibration, residue and water.

2.2.2 Inductive Sensor

An inductive sensor is a device that uses the principle of electromagnetic induction to detect or measure objects. An inductor develops a magnetic field when a current flows through it alternatively, a current flows through a circuit containing an inductor when the magnetic field through it changes. The resulting current flow sets up a new magnetic field that opposes the original magnetic field. The net effect is that it changes the inductance of the coil in the inductive sensor. By measuring the inductance, the sensor can determine when a metal object has been brought near by. The effect can be used to detect metallic objects that interact with a magnetic field. Non-metallic substances such as liquids or some kinds of dirt do not interact with the magnetic field, so an inductive sensor can operate in wet or dirty conditions [7].

Inductive proximity sensors work by setting up a high frequency field. If a target nears the sensor, magnetic field induces eddy current. The current consumes power because of resistance,

so energy is in the field is lost, and the signal amplitude decreases. The detector examines filled magnitude to determine when it has decreased enough to switch.

Inductor circuit model consists of three coils, which are modelled as an inductor in series with resistor. The excitation coil is modelled as an inductor Lx in series with resistance Rx which is a transmitter. The moving element, which is resonator, is modeled as a RLC circuit with inductance Lrso, capacitance Crso and resistance Rrso. The output coils (sine and cosine) are modeled as inductors 'Lsine' and 'Lcos' which is a receiver. All these inductors are mutually coupled.

The function of the excitation coil is to provide a uniform magnetic field along the track. Kx is the coupling coefficient between excitation coil and the resonator. The resonator circuit (an RLC combination) in turn induces voltages in the receiving coils and the magnitude and phase of these voltages vary as a function of position of the resonator. The function in such spiral sensors is sine and cosine. Krsine(phi) and Krcos(phi) are the coupling coefficients between the resonator and sine and cosine coils respectively which are the function of phi (angle which relates the position of the resonator on the board). There is also coupling between the excitation coil and the receiving coils. Kxsine and Kxcos are the coupling coefficients respectively.

The response of the sensor mainly depends on the inductance values of excitation coil, sine and cosine coils and the coupling coefficient between these coils. The variation of inductance of these coils leads to change in magnetic field, which in turn changes the response of sensor. So the prediction of inductance of these coils is crucial for the design process. The spiral inductive sensor model and inductive sensor model are shown in Fig 2.7 and Fig 2.8.

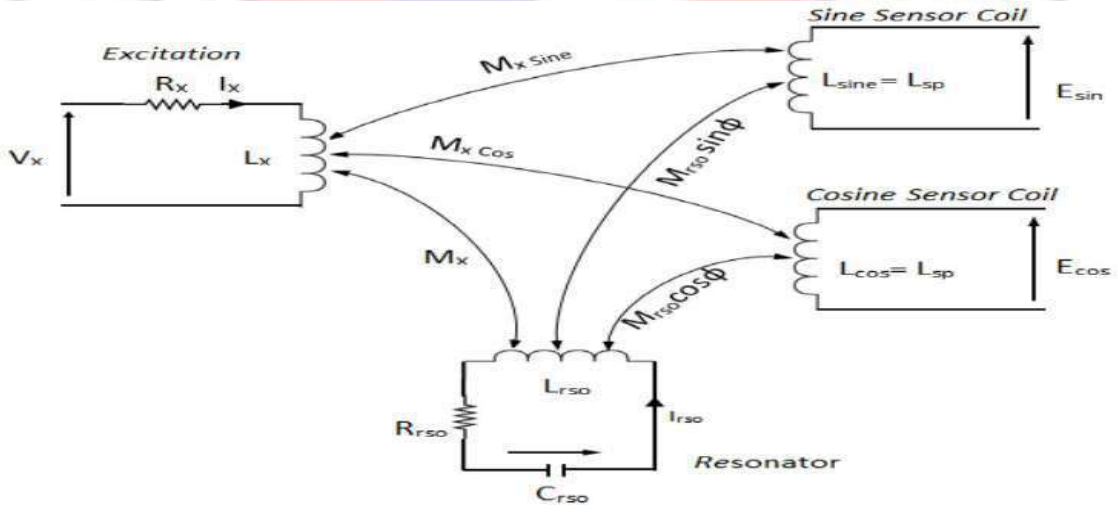

Fig 2.7 Spiral Inductive Sensor model [7]

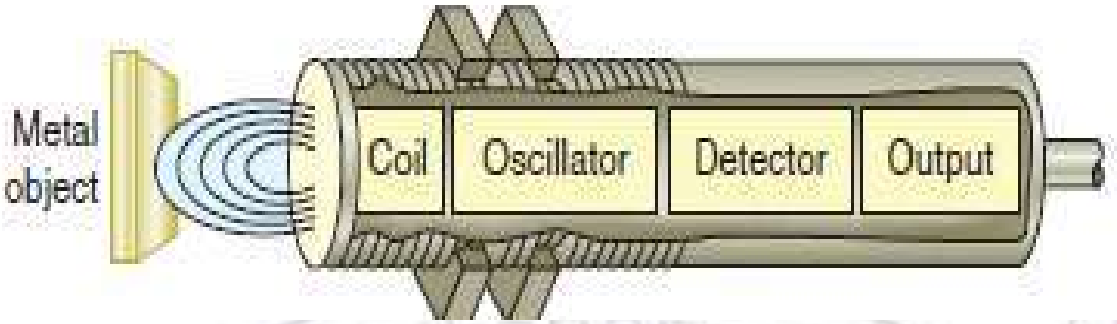

Fig 2.8 Inductive Sensor model [7]

The oscillator circuit generates a high-frequency electromagnetic field that radiates from the end of the sensor. When a metal object enters the field, eddy currents are induced in the surface of the object. The eddy currents on the object absorb some of the radiated energy from the sensor, resulting in a loss of energy and change of strength of the oscillator. The sensor's detection circuit monitors the oscillator's strength and triggers a solid-state output at a specific level. Once the metal object leaves the sensing area, the oscillator returns to its initial value.

2.2.3 Derivation of Transfer Function for the System Output Voltage

The circuit for estimating transfer function of inductive coil is shown in Fig 2.9.

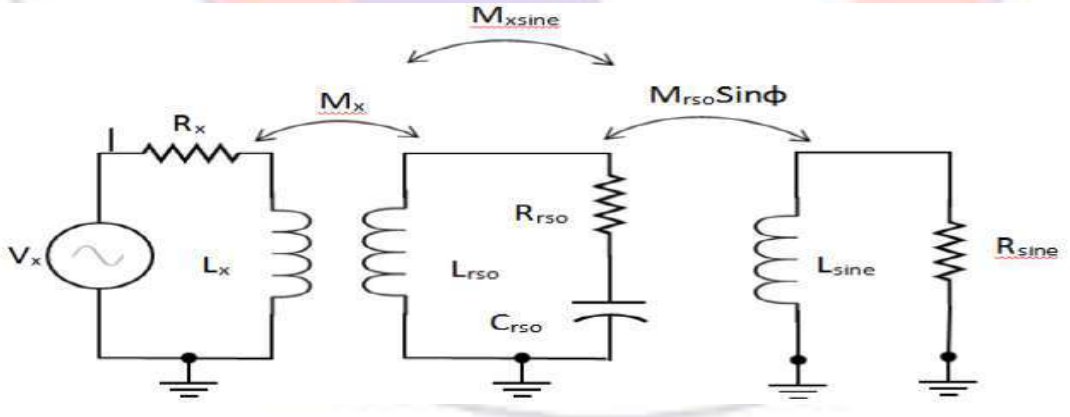

Fig 2.9 Circuit to determine transfer function of the inductive coil model [7]

Transfer function is also known as the system function. It is a mathematical representation that describes the transfer characteristics of a system that is the relationship between the input and output of a system.

For sine coil consider excitation, resonator and sine coil, for deriving transfer function of

sine coil.

$$M_x = K_x\sqrt{L_{rso}L_x} \quad (2.4)$$

$$M_{X\,\text{sine}} = K_{X\,\text{sine}}\sqrt{L_xL_{\text{sine}}} \quad (2.5)$$

$$M_{X\cos} = K_{X\cos}\sqrt{L_xL_{\cos}} \quad (2.6)$$

$$M_{rso}max = K_{rso}max\sqrt{L_xL_{\text{sine}}} \quad (2.7)$$

Apply Kirchoff's law in the above circuit and we get the following

$$V_x = I_xR_x + j\omega L_xI_x + j\omega M_xI_{rso} \quad (2.8)$$

$$0 = I_{rso}R_{rso} + j\omega L_{rso}I_{rso} - \frac{j}{\omega C_{rso}}I_{rso} + j\omega M_xI_x \quad (2.9)$$

Induced EMF on the sine and cosine coil are

$$E_{\text{sine}} = j\omega M_{X\sin}I_x + j\omega M_{rso}\sin\varphi I_{rso} \quad (2.10)$$

$$E_{\cos} = j\omega M_{X\cos}I_x + j\omega M_{rso}\cos\varphi I_{rso} \quad (2.11)$$

$$\begin{bmatrix} V_x \\ 0 \\ E_{\text{sine}} \end{bmatrix} = \begin{bmatrix} R_x + j\omega L_x & j\omega M_x & K_1 \\ j\omega M_x & R_{rso} + j\left(\omega L_{rso} - \frac{1}{\omega C_{res}}\right) & K_2 \\ j\omega M_{X\,\text{sine}} & j\omega M_{rso}\sin\varphi & K_3 \end{bmatrix} \begin{bmatrix} I_x \\ I_{rso} \\ I_{\text{sine}} = 0 \end{bmatrix}$$

From equation 2.9, calculate $Irso/I_x$

$$\frac{I_{rso}}{I_x} = \frac{-s^2M_xC_{rso}}{s^2(L_{rso}C_{rso}) + sC_{rso}R_{rso} + 1} \quad (2.12)$$

$$\text{Let } T_{f1} = \frac{-s^2M_xC_{rso}}{s^2(L_{rso}C_{rso}) + sC_{rso}R_{rso} + 1} \quad (2.13)$$

From equation 2.10

$$I_{rso} = T_{f1}(I_x) \quad (2.14)$$

For sine coil

$$E_{\text{sine}} = sM_{X\text{sine}}I_x + \left(T_{f1}(I_x)\right)\cdot sM_{rso}\sin\varphi \quad (2.15)$$

Solving we get

$$\frac{E_{\text{sine}}}{I_x} = \frac{s^3(M_{X\,\text{sine}}L_{rso}C_{rso} - M_{rso}M_xC_{rso}) + s^2M_{X\,\text{sine}}R_{rso}C_{rso} + sM_{X\,\text{sine}}}{s^2(L_{rso}C_{rso}) + sC_{rso}R_{rso} + 1} \quad (2.16)$$

Input impedance of sine coil

$$\frac{V_x}{I_x} = \frac{s^3(L_{rso}L_x - M_x^2) + s^2C_{rso}(R_xL_{rso} + R_{rso}L_x) + s(L_x + R_{rso}R_xC_{rso}) + R_x}{s^2(L_{rso}C_{rso}) + sC_{rso}R_{rso} + 1} \quad (2.17)$$

Transfer function of sine coil

$$\frac{E_{\text{sine}}}{V_x} = \frac{s^3(M_{X\text{ sine}}L_{rso}C_{rso} - M_{rso}M_xC_{rso}) + s^2M_{X\text{ sine}}R_{rso}C_{rso} + sM_{X\text{ sine}}}{s^3(L_{rso}L_x - M_x^2) + s^2C_{rso}(R_xL_{rso} + R_{rso}L_x) + s(L_x + R_{rso}R_xC_{rso}) + R_x} \quad (2.18)$$

For cosine coil

$$E_{\cos} = sM_{X\cos}I_x + \left(T_{f1}(I_x)\right) \cdot sM_{rso}\cos\,\varphi \quad (2.19)$$

Solving we get

$$\frac{E_{cos}}{I_x} = \frac{s^3(M_{X\cos}L_{rso}C_{rso} - M_{rso}M_xC_{rso}) + s^2M_{X\cos}R_{rso}C_{rso} + sM_{X\cos}}{s^2(L_{rso}C_{rso}) + sC_{rso}R_{rso} + 1} \quad (2.20)$$

Input impedance of cosine coil

$$\frac{V_x}{I_x} = \frac{s^3(L_{rso}L_x - M_x^2) + s^2C_{rso}(R_xL_{rso} + R_{rso}L_x) + s(L_x + R_{rso}R_xC_{rso}) + R_x}{s^2(L_{rso}C_{rso}) + sC_{rso}R_{rso} + 1} \quad (2.21)$$

Transfer function of cosine coil

$$\frac{E_{cos}}{V_x} = \frac{s^3(M_{Xcos}L_{rso}C_{rso} - M_{rso}M_xC_{rso}) + s^2M_{Xcos}R_{rso}C_{rso} + sM_{X\cos}}{s^3(L_{rso}L_x - M_x^2) + s^2C_{rso}(R_xL_{rso} + R_{rso}L_x) + s(L_x + R_{rso}R_xC_{rso}) + R_x} \quad (2.22)$$

2.2.4 Push Pull type Sensor

The push-pull sensors are the combination of P-N-P and the N-P-N transistors. The combination has the significance in terms of amplification. It acts as a dual-stage amplifier. The N-P-N transistor here acts as a push amplifier where the positive cycle is amplified. P-N-P transistor acts as the pull amplifier where it enacts on the negative cycle of the applied input signal**.** The Push Pull sensor configuration is shown in Fig 2.10.

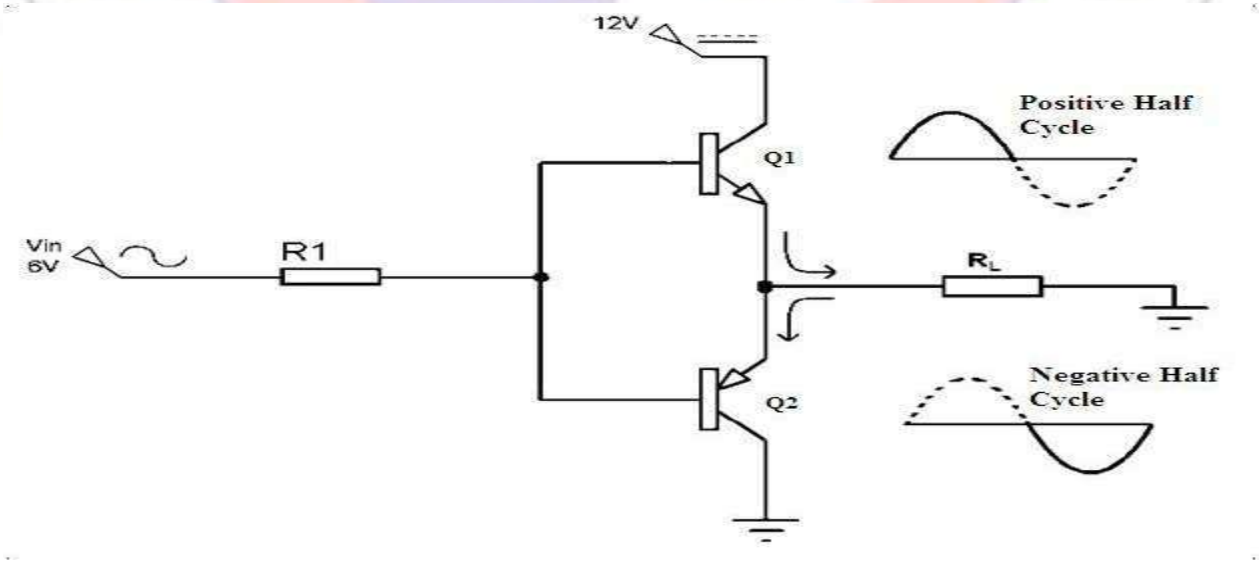

Fig 2.10 Push Pull Sensor Circuit diagram [8]

At the input side one single resistor is connected in between both the Q1 and the Q2 transistors. The other resistor that is connected at the output acts as a load. These two transistors

can be of type BJT or MOSFET. The one transistor that is connected provides the current to the load as the source. The other transistor that is connected acts in such a way that it sinks the current from the load.

The operation of the push-pull amplifiers is in such a way that it makes the signal to split into the form of out of phase that is 180 degree. At the input one transformer is connected such that it acts as an input coupler. The coupler splits the signal in such a way that one half of the signal is given to one transistor and the other is given to the other transistor. In this way, the push-pull amplifier works.

Advantages of Push Pull sensor are:

1. The sensor can eliminate distortions that occur in the circuit.
2. The sensor is capable of generating high gains

2.3 Monte Carlo Analysis

Monte Carlo analysis is defined as a simulation process that generates probabilities of risk using a mathematical model. The method provides a range of possible results based on the varying parameters that are measured in the analysis. The method was developed by a scientist developing the atomic bomb during World War II.

Monte Carlo analysis is about generating predictive situational results based on distributing factors that may influence the outcome of the process. It takes into account the maximum and minimum threshold of each parameter and randomly iterates the simulation with different values.

Various types of probability distributions are used in Monte Carlo analysis. They represent how the possible outcome values are distributed and give a good picture of the risk when presented in a histogram chart. Commonly used probability distributions are the Gaussian and uniform models. Depending on the parameters involved, completing a Monte Carlo analysis simulation may take hundreds or thousands of iterations. In contrast to single-point analysis, Monte Carlo gives a better picture of what may go wrong in terms of probability. Fig 2.11 shows the role of Monte Carlo to predict the risk of defects in PCB manufacturing [15].

A typical PCB design consists of hundreds of components, and it is foolish to assume that the values are strictly unchanging in every single PCB that is produced. When manufacturing hundreds or thousands of PCB counterous mistakes are spotted in every PCB. It is unimaginable to have a large number of the PCBs to be defective. The fact is, electronics components like

capacitors, resistors, inductors, and transistors are produced with a tolerance rate on their values. This means a 100 Ohm resistor may turn out to be 95 Ohm when measured. In some designs, accuracy is crucial, and the varying values can affect the functionality of the circuit. To have a good idea on the probability of failure, PCB designers depend on the Monte Carlo analysis.

The yield in PCB production must also take the tolerance of components into account. Sometimes, the fluctuation in parameters can result in a fraction of the production PCB to be rejected. Running the Monte Carlo analysis gives you a clearer picture of what to expect when the PCBs are produced. Basically, Monte Carlo analysis is about running a series of analysis like transient, noise, and AC/DC sweep over a specific circuit by substituting the parameters with possible values from the specified tolerance.

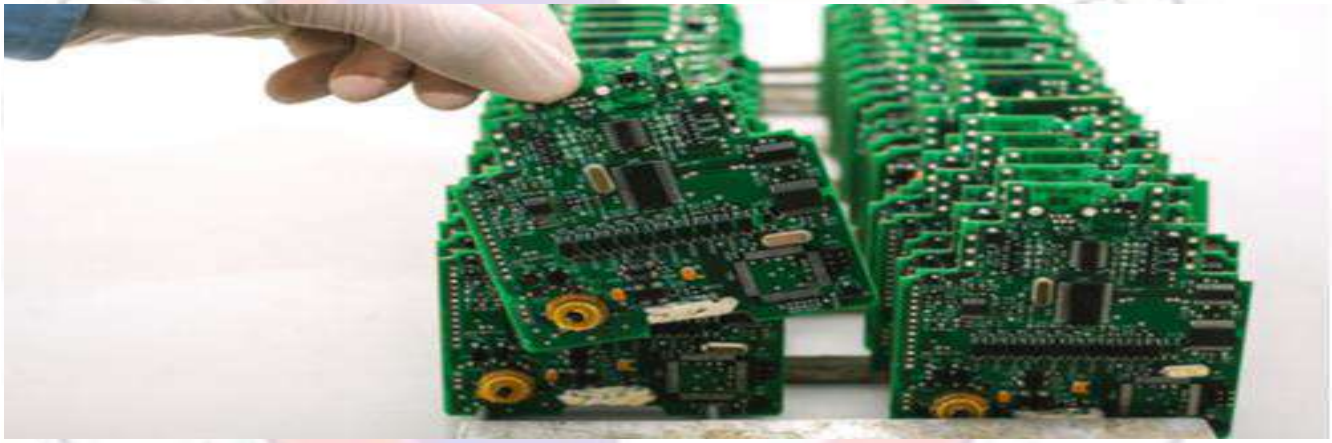

Fig 2.11 Monte Carlo analysis helps to predict the risk of defects in PCB manufacturing [15].

Generic Monte Carlo analysis gives total yield analysis. It is through multiple goal analysis, enables to analyze the variety of necessities the design requires or dynamic yield calculators that allows to change minimum and maximum ranges dynamically. An advanced Monte Carlo analysis tool makes the yield optimization process both more effective and efficient, especially when it comes to split products, product differentiation, or meeting the needs of multiple groups of users.

2.3.1 Simulation steps for Monte Carlo Analysis

Step 1: The simulation profile could be a DC Sweep analysis is shown in Fig 2.12.

Step 2: In Monte Carlo/Worst Case option, set I(Meter) as the Output variable, use Gaussian as distribution and is shown in Fig 2.13.

Step 3: Click on MC Load/Save, the Load/Save Monte Carlo Parameter File dialog box comes up. In the text box that is enabled, specify the name and the location of the file in which the parameter data is to be saved. After running the Monte Carlo analysis, the model parameter values used for various simulation runs will be stored in the .mcp file [15]. The step3 for Monte Carlo simulation is shown in Fig 2.14 .

Step 4: Click More Settings to choose a collating function e.g. YMAX. With the collating function is defined on which criteria the results are sorted in the output File and is shown in Fig 2.15.

Step 5: After the simulation the curves of I(Meter) is obtained. With many runs (1000 runs), the waveform display can look more like a band than a set of individual waveforms. This can be useful for seeing the typical spread for a particular output variable. As the number of runs increases, the spread more closely approximates the actual worst-case limits for the circuit. The schematic for step 5 is shown in Fig 2.16.

Step 6: Click the Performance Analysis button, add trace Max(I(Meter)) to display histograms and is shown in Fig 2.17.

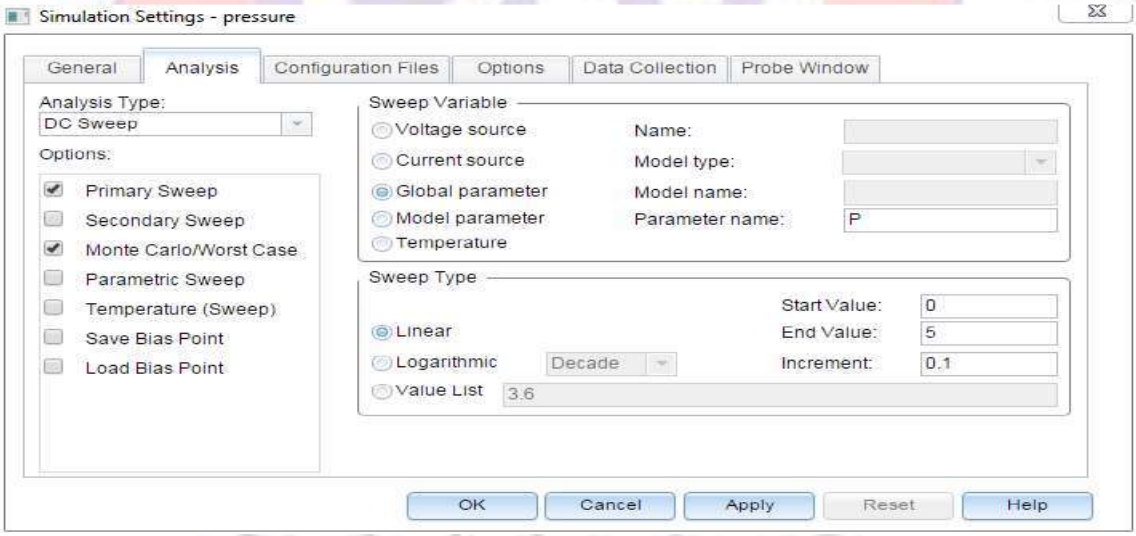

Fig 2.12 Step 1 for Monte Carlo Simulation [15]

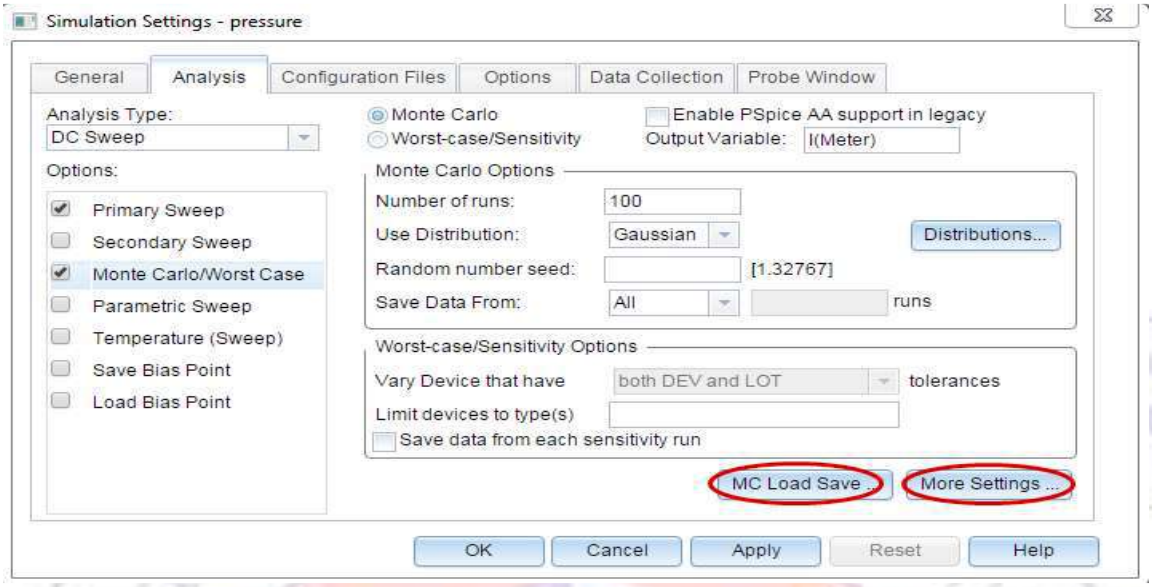

Fig 2.13 Step 2 for Monte Carlo Simulation [15]

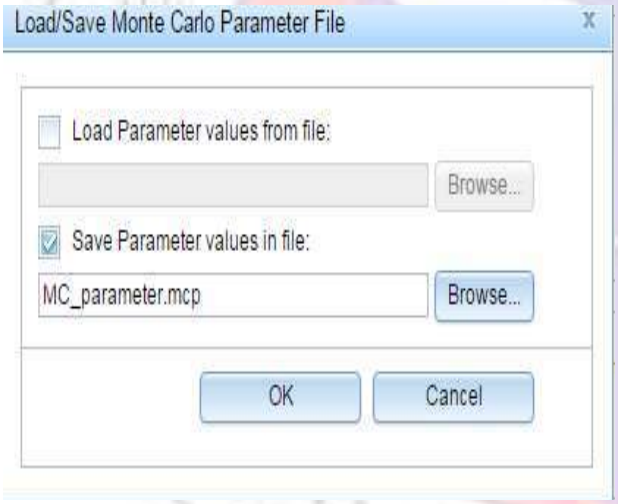

Fig 2.14 Step 3 for Monte Carlo Simulation [15]

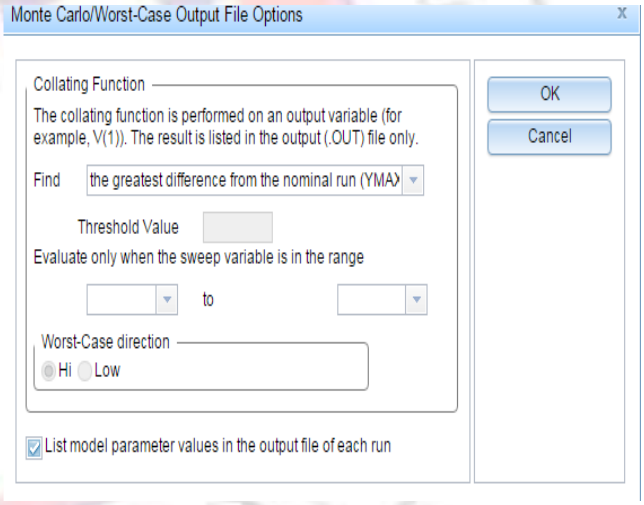

Fig 2.15 Step 4 for Monte Carlo Simulation [15]

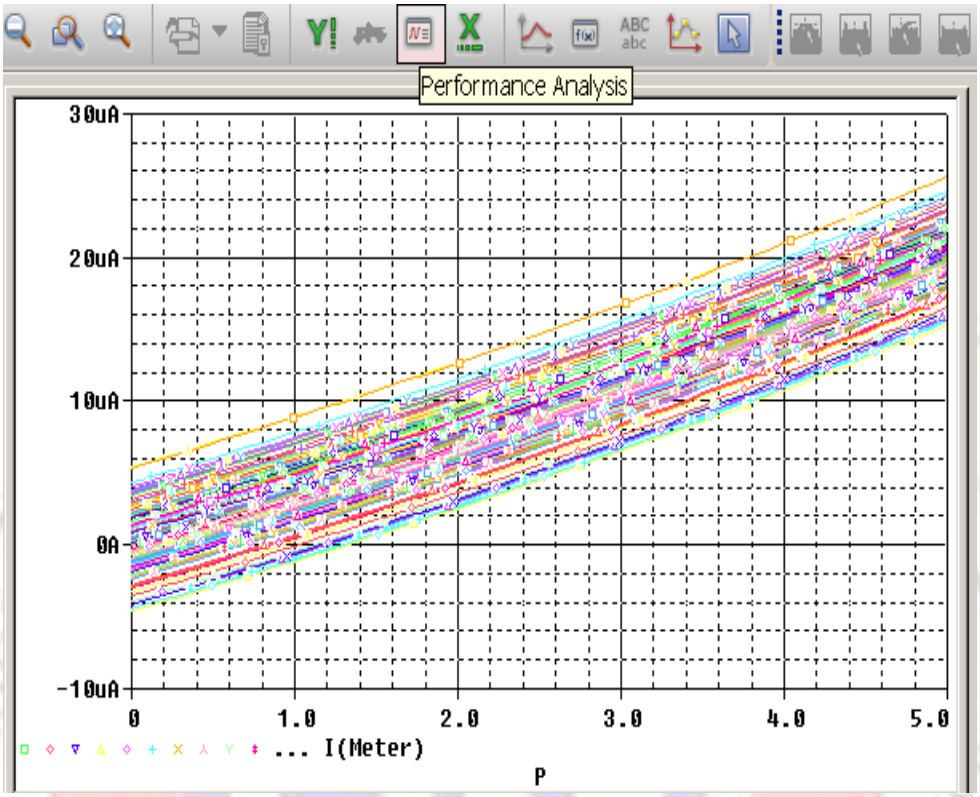

Fig 2.16 Step 5 for Monte Carlo Simulation [16]

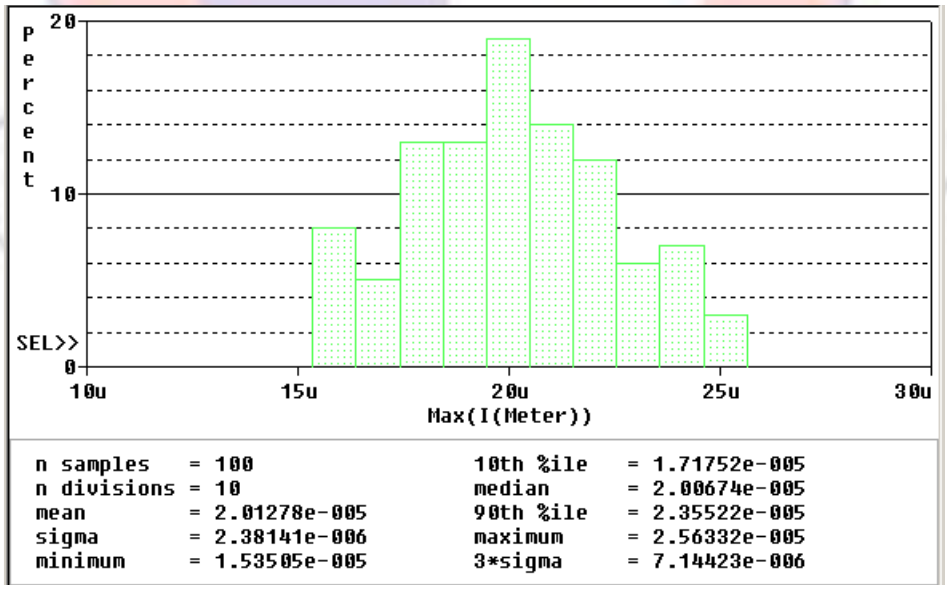

Fig 2.17 Step 6 for Monte Carlo Simulation [16]

2.4 Sensitivity Analysis

A simple definition of sensitivity is how much specific system behavior/characteristic changes as a individual component value changes. The general equation for sensitivity analysis is given as

$$S_x^y = \lim_{\Delta x \to 0} \frac{\frac{\Delta y}{y}}{\frac{\Delta x}{x}} = \frac{x}{y}\frac{\partial y}{\partial x} \tag{2.23}$$

Equation (2.23) is the general mathematical definition of circuit sensitivity.

Where S represents sensitivity,

X represents changing element/component and

Y is the characteristic of circuit which one want to evaluate as component value is varied.

The middle part of the equation shows that the percentage that the dependent variable Δy/y changes, relative to the percentage that the independent variable Δx/x changes. The sensitivity analysis is incorporated by using the formulae. Let us take a transfer function H(s).

$$\mathbf{H}(s) = \frac{N(s)}{D(s)} \tag{2.24}$$

Here N(s) represents the numerator part of transfer function and D(s) represents the denominator part of transfer function. From equation (2.23) and equation (2.24), new equation is written as same as equation (2.23)

In general, the AC-sensitivity is given by the following equation:

$$\text{Sens}\,(H(s), W) = \frac{W}{H(s)}\frac{\partial H(s)}{\partial W} \tag{2.25}$$

Substituting equation (2.23) into (2.24) and applying the chain rule,

$$\text{Sens}\,(\text{H(s)}, \text{W}) = \text{W}\left(\frac{1}{\text{N(s)}}\frac{\partial \text{N(s)}}{\partial \text{W}}\right) - \left(\frac{1}{\text{D(s)}}\frac{\partial \text{D(s)}}{\partial \text{W}}\right) \tag{2.26}$$

Here W is the component which one want to vary w.r.t. circuit transfer function. By using above equation (2.26) the sensitivity of circuit any circuit can be found.

Sensitivity analysis of analog circuit provides the information about various component present in the circuit. The design engineer needs to choose as many inexpensive components as

possible, by keeping the circuit performance stable, engineer needs to decide which elements are sensitive and how much value they required for the tolerance. With the help of sensitivity analysis knowledge about the component characteristics variation in circuit and their effect on performance of system output is known [17].

All circuits, analog or digital, have characteristics dependent on the values of their component parts. Invariably, such parts are non-ideal in many ways. Even the most fundamental characteristics, for example a resistor's resistance is slightly different from the specified value. The characteristics also vary over time and environmental conditions.

The wise circuit designer learns how to analyze the sensitivities of circuits critical characteristics to the variations in the components. With this knowledge, the designer better decides how to balance any tradeoffs between performance and cost. Deeper use of sensitivity analysis leads designers to modify circuit topologies or make completely different choices in order to optimize these tradeoffs. Sensitivity analysis helps to increase reliability and robustness of the system, reduce costs and improve performance of the system.

2.4.1 Simulation steps for Sensitivity Analysis

To perform sensitivity analysis, select model parameters for evaluation, and generate a representative set of parameter values to explore the design space. Create the parameter set by specifying parameter distributions such as normal or uniform. After generating the parameter values, plot them to check if generated parameter values match the desired specifications. This is particularly important to generate a small number of random samples for each parameter set [18].

To plot the generated parameters in the Sensitivity Analyzer using Matlab, following steps are followed.

1. Select the generated parameter set in the Parameter Sets area of the app and Fig 2.18 shows the schematic

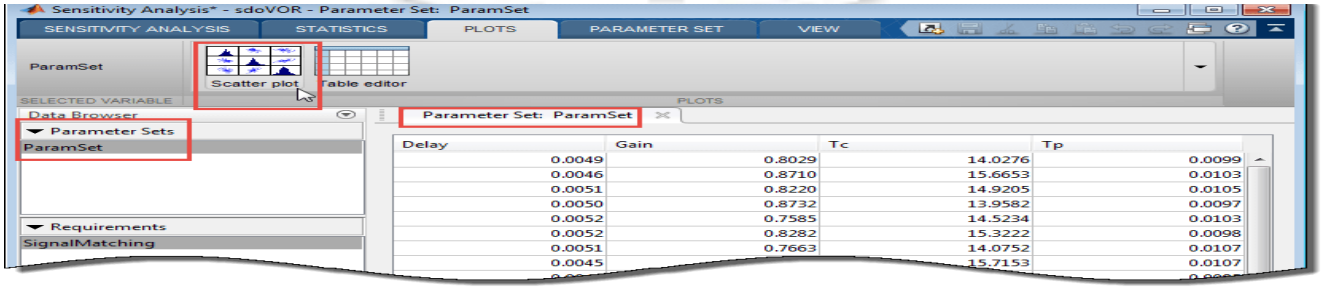

Fig 2.18 Generating parameter set for generating values [17]

2. In the Plots tab, select Scatter Plot.

The generated plot displays histograms of generated values for each parameter on the diagonal, and the pairwise scatter plot of the parameters on the off-diagonals. Fig 2.19 shows the scatter plot view used to evaluate the model.

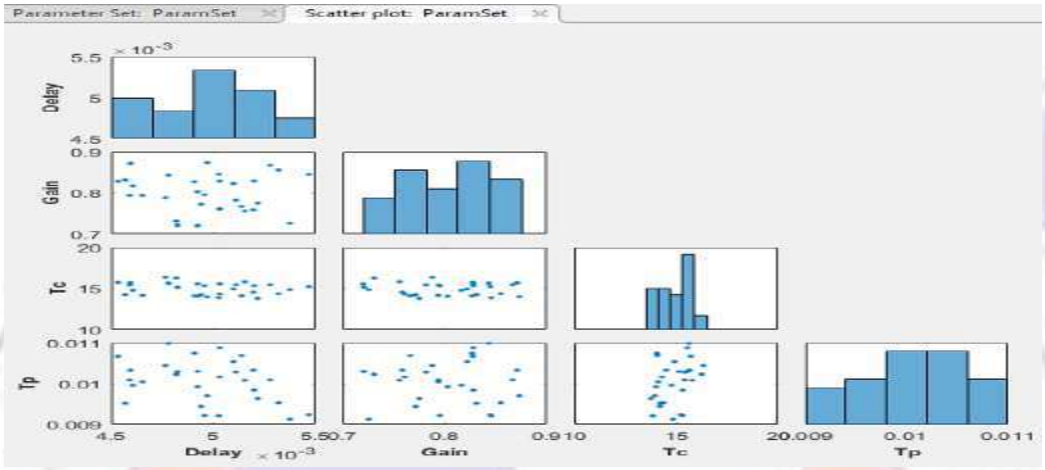

Fig 2.19 Scatter plot view for model evaluation [17]

3. Inspect the histograms to ensure that the generated parameter values match the intended parameter distributions. Inspect the off-diagonal scatter plots to ensure that any specified correlations between parameters are present.

4. After generating a parameter set, you define a cost function by creating a design requirement on the model signals and then evaluate the cost function at each set of parameter values. To validate the evaluation results, inspect the evaluated cost function values. If the cost function evaluations contain NaN values, that could indicate an issue. The result for model evaluation is shown in Fig 2.20.

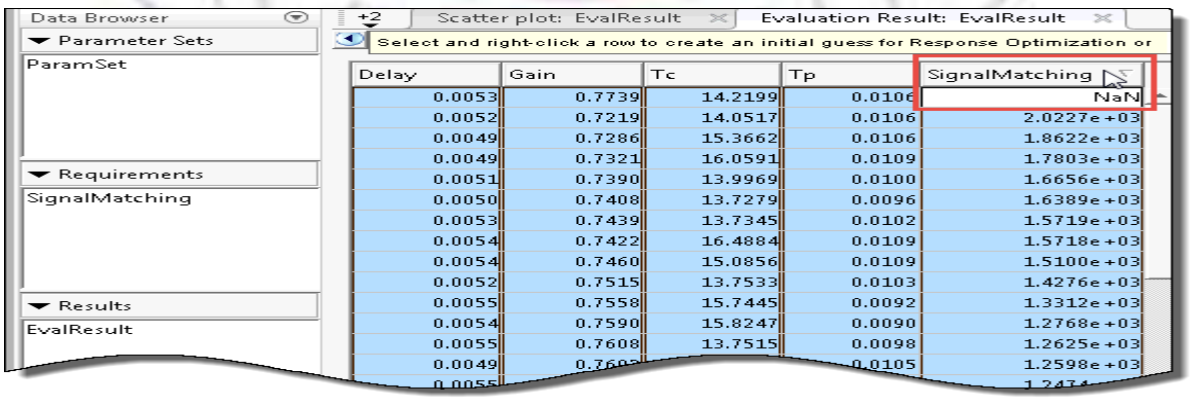

Fig 2.20 Evaluated Results for the model [17]

5. Inspect the parameter values that resulted in the NaN values for evaluated requirements. If NaN result does not occur for that row of parameter values, investigate the model furthe

2.5 Summary

This chapter incorporates description about automotive sensors, variable reluctance sensor, hall effect sensor, inductive sensor, push pull sensor, monte carlo analysis, steps for monte carlo analysis, sensitivity analysis, steps for sensitivity analysis. Monte carlo analysis technique is most commonly used in automotive industries and it gives a good picture risk analysis and it was presented on histogram chart. Sensitivity analysis was used to optimize the circuit design. A brief methodology is discussed on the next chapter.

CHAPTER 3

METHODOLOGY AND BLOCK DIAGRAM

This chapter involves the detailed explanation of methodology and block diagram of sensor interfacing to a sensor interface block for Engine control unit.

3.1 Methodology

Fig.3.1 shows the flow chart for the proposed methodology

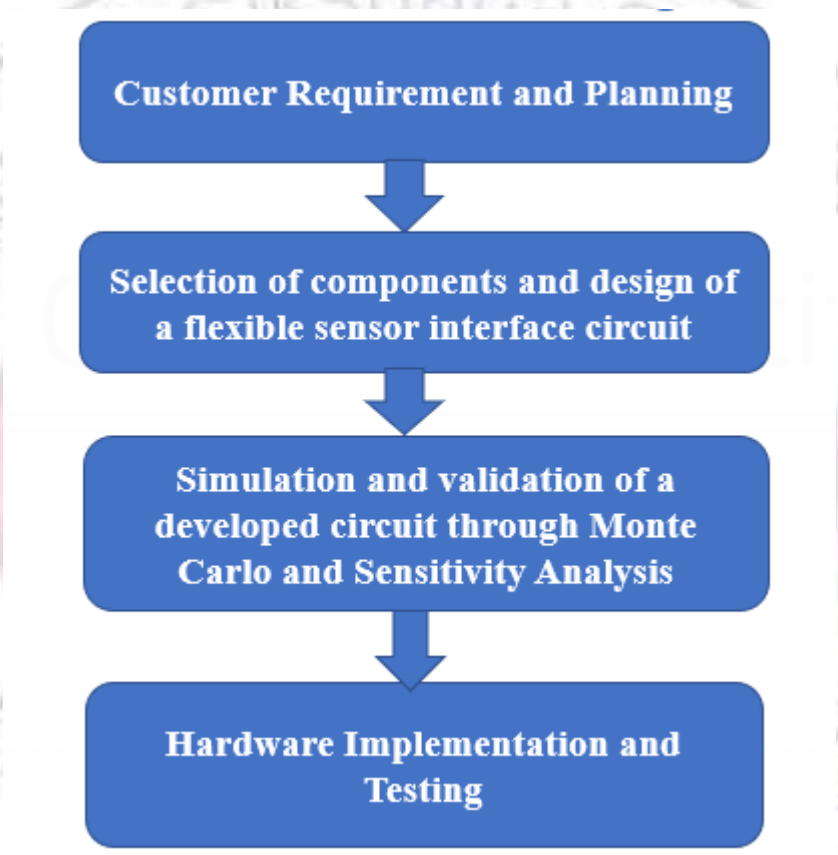

Fig 3.1 Methodology of the proposed system

The various tasks are as follows:

3.1.1 Customer requirements and planning

A detailed literature survey is carried out for selecting required topology and comparing it with various other topologies. The selected topology in this project is “Flexible Sensing Circuit”.

3.1.2 Design and selection of components

A sensor interface block is designed and flexinput L9966IC is modelled using simulation. Sensor interface platform is designed by considering the requirement of protection of the circuit

against electrostatic discharge and electromagnetic interference issues. The capacitors for electrostatic discharge protection are selected and designed using human body model. A suitable attenuator circuit is designed provide the output as desirable the circuit requires. Common mode capacitors and differential mode capacitors are designed and selected considering EMI/EMC isssues. From the frequency response analysis a low pass RC filter is designed. The details of these are presented in chapter 4.

3.1.3 Simulation and analysis

Matlab/Pspice tool is used for the simulation of flexible sensor interfacing circuit. The output voltage waveforms at VRSP, VRSN, VOUT pins of L9966 IC are obtained using simulation. The simulated results are verified and validated using Monte Carlo and Sensitivity Analysis.

3.1.4 Hardware Implementation and Testing

In this stage, the components such as BJT and resistors are assembled on the PCB board and soldered. A power supply of 5V is provided to the sensor interface block. The flex input L9966 IC is interfaced to the control block. A power supply of 5V and 12V is fed into VDD5 and UBSW pins of L9966 IC. Here, Here, Hall effect sensor, Inductive sensor, Push pull type sensors are tested for the functionality. The output waveforms are observed using digital storage oscilloscope (DSO).

3.2 Block diagram

Fig 3.2 shows the application of a flexible sensor interfacing circuit to interface different sensors and Fig 3.3 shows the basic block diagram of the sensor-actuator mechanism.

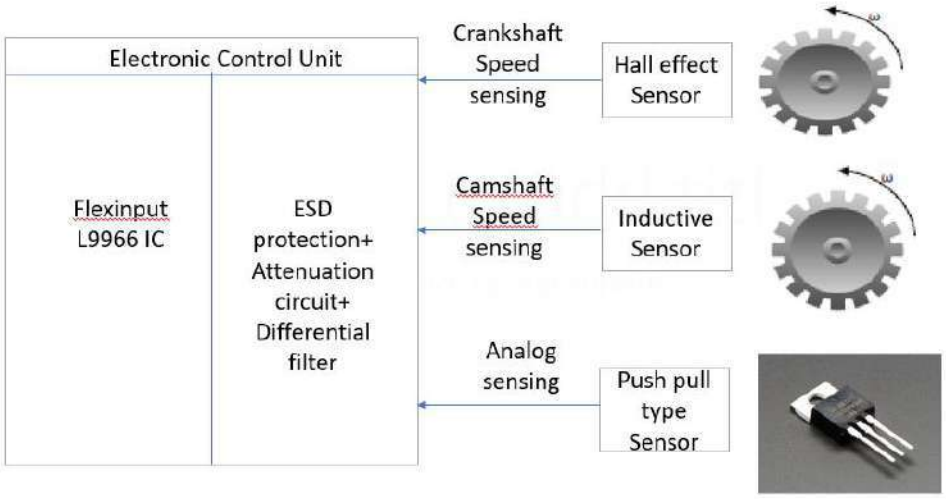

Fig 3.2 Application of flexible sensor interfacing circuit to interface different sensors

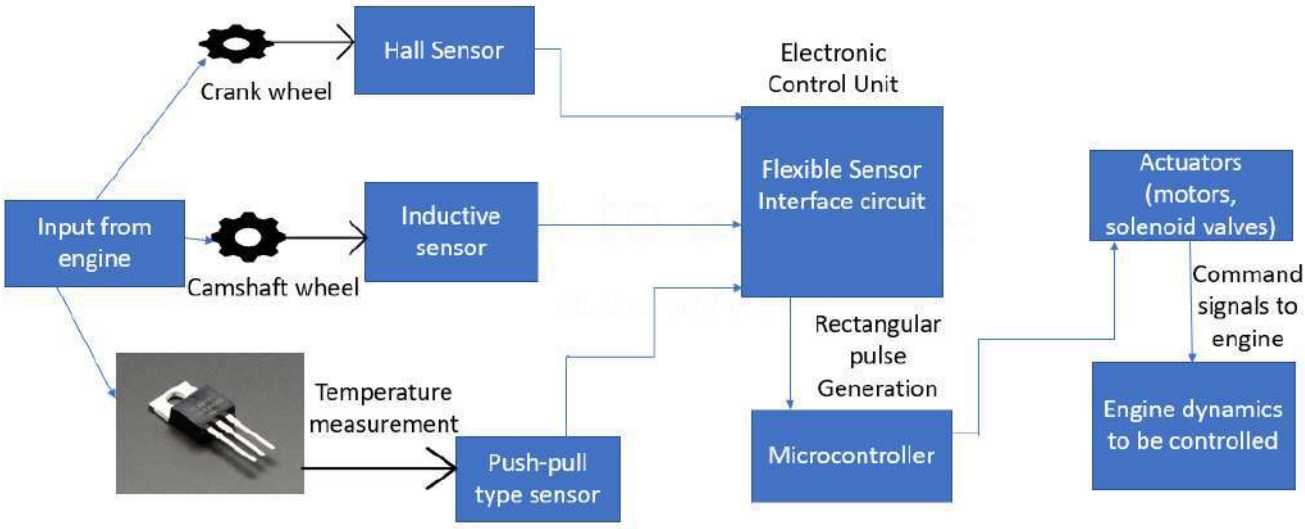

Fig 3.3 Block diagram of sensor Actuator mechanism

The input system forms the interface to which various field devices taken from engine are connected to the sensor interface. The purpose of the interfacing is to condition the various signals received from or sent from engine. Input devices from different parts of the engine such as crankshaft wheel, camshaft position are hardwired to the input terminals. Output devices such as small motors, solenoid valves, motor starters and indicator lights and buzzers are hardwired to the output terminals. The ECU acts as a transfer block for sensor and actuator. An ECU is basically an electronic control unit consists of a flexinput IC and a sensor interface block and the processor . The signals received from sensors are hardwired to the ECU input terminals. The common mode capacitors located at the input side of an ECU provide protection against electrostatic discharge. The differential capacitor located between pull up and pull down resistor shunts high frequency components into the ground and hence protects the circuit from EMC/EMI issues. A passive attenuator is a special type of electrical circuit made up of entirely resistive network designed to weaken or attenuate the power supplied by a source to a level that is suitable for the connected load. The lowpass RC filter helps in shunting high frequency components into the ground. The signal from the RC filter is fed to a L9966 IC. L9966 IC acts as a comparator and hence generates the output in the form of rectangular pulses. The rectangular pulses are fed into microcontroller. The microcontroller stores the digital pulses and the signal is processed and fed to a driver circuit such as H-bridge circuit, three phase inverter. The driver circuits drive the actuators such as

motors, solenoid valves. The alarm signal is generated and is used to control the engine mechanism.

3.2.1 Electrostatic discharge protection

Electronic devices are becoming increasingly versatile, faster, and smaller. To meet the requirements, semiconductor manufacturers steadily improve the performance and reduce the size of semiconductor devices for electronic applications by shrinking process geometries and increasing the dopant concentration. Because of the downscaling of the process and the ever-higher dopant concentration, semiconductor devices are becoming less immune to electrostatic discharge (ESD) damage. Unless countermeasures are taken, electronic devices are susceptible to degradation and damage due to ESD. In addition, electronic devices are subject to increasing exposure to ESD events as USB, LAN, and other cables are frequently plugged and unplugged for data communication with IoT and other devices and battery recharging. To protect against ESD, it is therefore becoming essential to add ESD protection diodes to USB, HDMI, and other external ports as well as to the parts that might come into contact with or close to the human body or any manufacturing system during production [19]-[21].

Static electricity is the charge generated on the surface of dielectric materials. Static electricity is discharged when positively and negatively charged objects are brought into contact with or close to each other. This phenomenon is called an electrostatic discharge (ESD). When a charged human body touches an electronic device, the resulting ESD can be several thousand volts.

When two different objects are rubbed together, brought into contact with each other, or separated from each other (e.g., when plastic wrap is unrolled), electrons may move from one object to the other. Some materials tend to lose electrons and become positively charged while others tend to receive electrons and become negatively charged. A list of materials arranged according to the tendency to gain or lose electrons easily is called the triboelectric series. The farther away two materials are from each other on the triboelectric series, the greater the charge transferred when they are brought into contact with each other. All materials consist of atoms, which normally have an equal number of positively charged protons and negatively charged electrons, making them electrically neutral. For example, friction causes electrons to move from one object to the other, creating an imbalance of positive and negative charges. Fig 3.4 shows the process of static electricity generation.

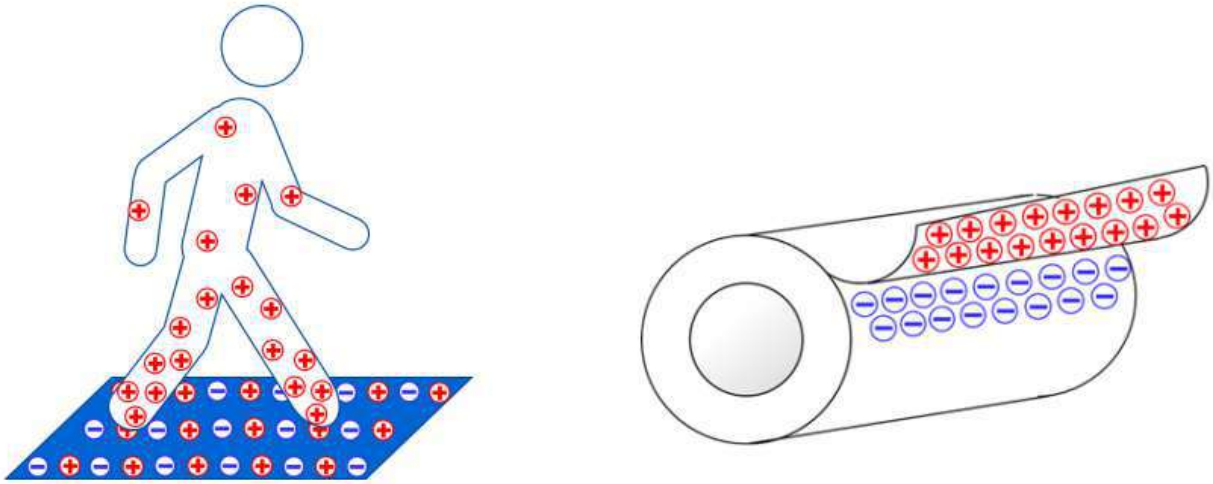

Fig 3.4 How static electricity occurs [19]

Semiconductor manufacturers have continually developed new processes with ever-smaller geometries to improve the performance and reduce the size of semiconductor devices for electronic applications. There is a law regarding transistor scaling, which states that scaling the size of transistors to 1/k reduces their area to 1/k^2 , power consumption to 1/k, and circuit delays to 1/k. According to this scaling law, geometry scaling helps reduce the size and power consumption and improve the performance of semiconductor devices. However, when the width and the length are scaled to 1/k, the thickness is also generally scaled proportionally. This means that the thickness of the insulation film used for semiconductor device fabrication is also reduced to 1/k. Silicon oxide (SiO2) is commonly used as an insulator for silicon semiconductor devices. SiO2 exhibits a dielectric strength of 8 to 10 MV/cm, which is constant per centimeter. Therefore, when the thickness of an insulation film is reduced to 1/k, its dielectric strength is reduced to 1/k. The shrinking of semiconductor processes described above is just one of the factors that make semiconductor devices more susceptible to static electricity. Reducing the size and improving the performance of semiconductors and other electronic components exacerbate the effect of ESD. Various factors also complicate ESD protection, including the size reduction of electronic devices themselves. Furthermore, the way in which people use electronic devices has considerably changed. Since most electronic devices were stationary devices used only at home twenty years

ago, their cables were rarely reconnected. At present, however, USB and LAN cables are plugged into and unplugged from smartphones, notebook PCs, and other mobile devices many times a week for battery recharging and data communication. As described in the previous subsection, ESD can be introduced into an electronic device when it is brought into contact with or close to another object. In other words, nowadays, electronic devices are exposed to ESD more frequently. Because of a decrease in ESD immunity and an increase in the number of ESD strikes, electronic devices have an increased risk of being degraded by ESD events. It is therefore becoming more important to use ESD protection devices than ever before.

3.2.2 Electrostatic discharge protection devices

Transient voltage suppressors or TVS are protection devices that are used to save the circuits from this sudden spike in voltage or current like electrostatic discharge protection(ESD). The primary way to protect a circuit from overvoltage is to place these TVS devices in parallel with the circuit**.**

3.2.3 Transient Voltage Suppressors (TVS Diodes)

Transient voltage suppressors or TVS are protection devices that are used to save the circuits from sudden spike in voltage or current. The primary way to protect a circuit from overvoltage is to place these TVS devices in parallel with the circuit.

There are many types of TVS device that can be used for Transient Voltage Suppression namely Metal Oxide Varistor, TVS Diode, Zener Diode or a Bypass Capacitor.

Transient Voltage Suppressor Diode is a solid-state PN- Junction diode that is specially designed to nullify the sudden or momentary overvoltage effects on sensitive semiconductors and circuits. Transient Voltage Suppressor Diode is a clamping device, so whenever the induced voltage exceeds the avalanche breakdown voltage, it absorbs the excess energy of the overvoltage event, and then it automatically resets after overvoltage condition. While it is true that, standard diodes and Zener diodes can also be used for overvoltage/transient protection, but they are not as robust as transient voltage suppressor diodes because standard and Zener diodes are designed for rectification and voltage regulation [23].

Types of TVS Diode:

1. Unidirectional TVS Diode
2. Bidirectional TVS Diode

A unidirectional Transient Voltage Suppressor Diode works as a rectifier in a circuit in the forward direction like any other avalanche diode, and this unidirectional diode is made to withstand very large peak currents. Symbol of a unidirectional TVS diode is shown in Fig 3.5 and it is much like a Zener diode.

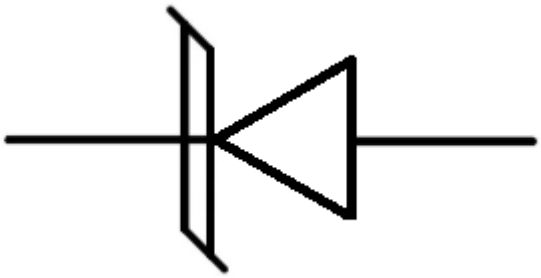

Fig 3.5 Unidirectional TVS Diode [20]

A bidirectional transient-voltage-suppression diode can be represented by two mutually opposing avalanche diodes connected in series with each other. These diodes are connected in parallel with the device or circuit to be protected. Unlike the symbol, these diodes are manufactured as a single component. Symbol of a Bidirectional TVS diode is shown in Fig 3.6.

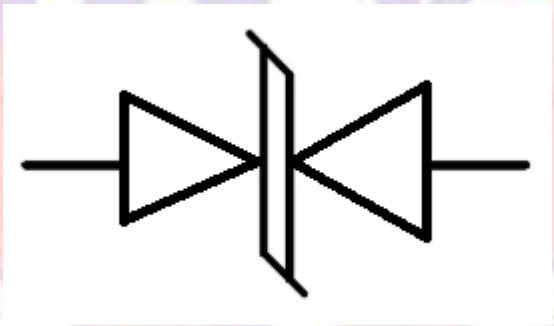

Fig 3.6 Bidirectional TVS Diode [20]

TVS Diodes are connected in parallel with the device or circuit to be protected. The TVS device is specifically designed to breakdown at a specific voltage level and conducts large amounts of current without sustaining damage.

While no ESD pulse is being introduced into a system (i.e., while a system is in normal operation), ESD protection diodes are disconnected from a device under protection (DUP) so as not to affect its operation. The cathode and anode of each ESD protection diode are connected to a signal line and GND respectively as shown below. When ESD protection diodes are connected in this manner, they do not act as transient voltage suppressors while a system is in normal

operation. Fig 3.7 shows the working of ESD diodes during normal operation.

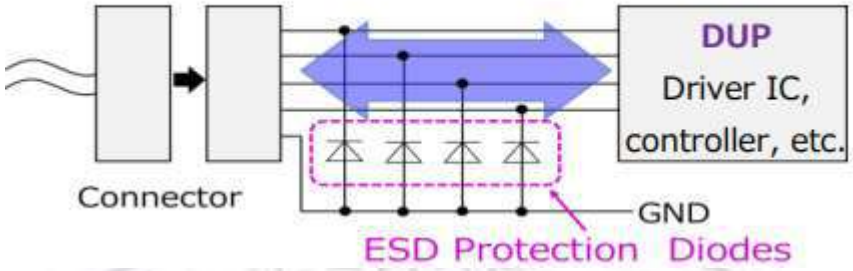

Fig 3.7 Normal system operation [20]

When an ESD pulse is introduced into the system, it is necessary to ensure that ESD protection diodes conduct to prevent the ESD pulse from reaching the DUP. From the connector, the ESD protection diodes and the DUP can be seen as being connected in parallel. It is therefore important to ensure that ESD protection diodes have low impedance so that most of the ESD energy is shunted through the ESD protection diodes. Fig 3.8 shows the role of ESD protection diodes in the event of ESD strike and Fig 3.9 shows the operation of ESD diodes during forward biased and reverse biased operation.

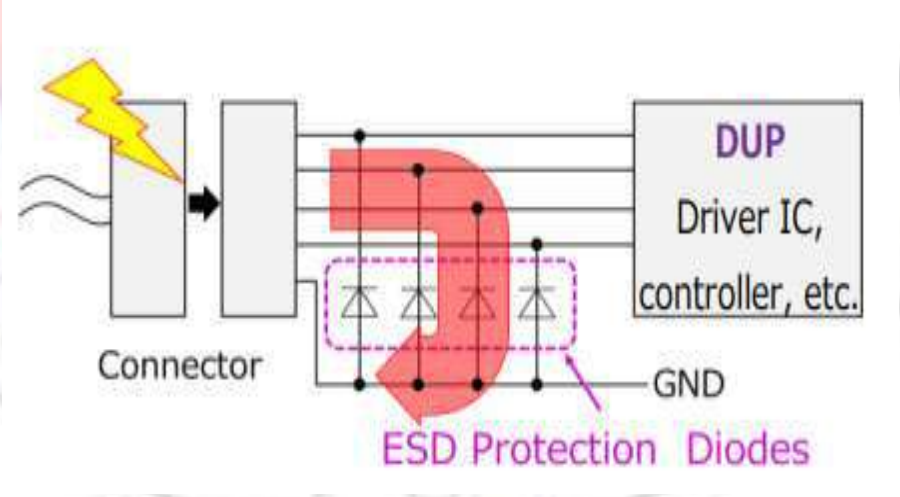

Fig 3.8 System operation in the event of an ESD strike [21]

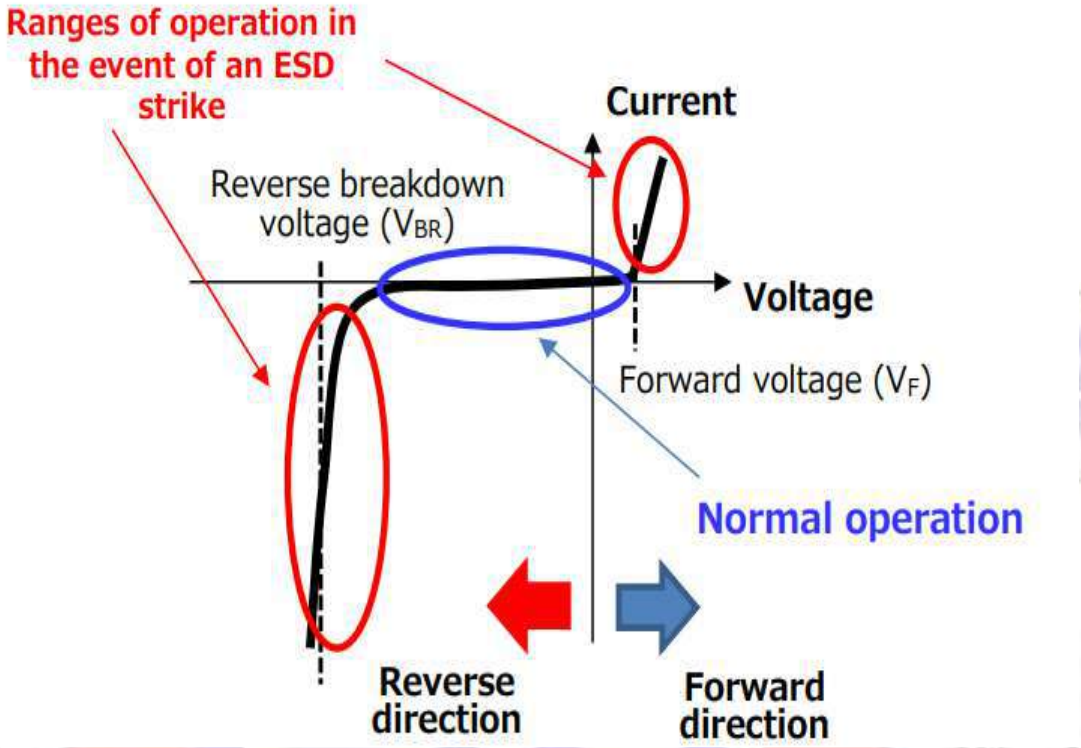

Fig 3.9 Voltage ranges in which ESD protection diodes act as transient voltage suppressors [21]

The V-I characteristics for both unidirectional and bidirectional TVS diode is shown in Fig 3.10. The characteristic graph displays voltage and current relationships. A bi-directional diode has the same characteristic curve in the positive and the negative direction, so it does not matter which way they are connected into the circuit. A unidirectional diode has a higher turn-on voltage in the positive direction compared to the negative direction.

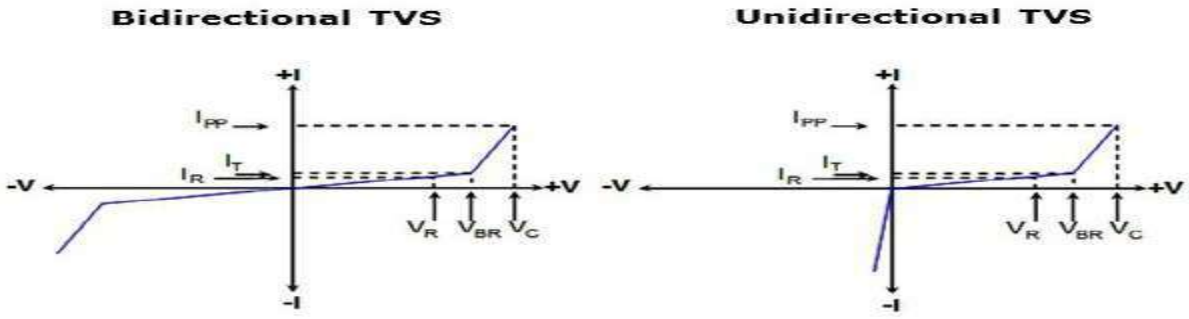

Fig 3.10 V-I characteristics of Bidirectional TVS and Unidirectional TVS [21]

3.2.4 TVS Diode Parameters

There are many types of TVS diode in the market, designed for a specific application. While selecting a TVS Diode one can look for the following terminologies in the datasheet to suit the design.

1. **Reverse Stand-Off Voltage (V_R):** Reverse stand-off voltage is the maximum voltage that can be applied to the protector without actually activating the device. The device V_R should be equal to or higher than the peak operating voltage of the circuit being protected. This is to ensure that the protection device does not clip the normal circuit operating or signal voltage.
2. **Breakdown Voltage (V_{BR}):** Breakdown voltage is the voltage at which the diode will begin to protect and conduct current. Generally, the V_{BR} is specified at 1mA.
3. **Clamping Voltage (V_C):** Clamping Voltage is the highest voltage that the protected circuit will be exposed to during the test waveform event. On most datasheets, the clamping voltage is given for a 1A or 2A waveform that has an 8µS rise time.
4. **Peak Pulse Current (I_{PP}):** The peak pulse current is the maximum current the protection device can withstand.

3.3 Attenuator Circuit

An attenuator is a two port resistive network designed to weaken or "attenuate" the power being supplied by a source to a level that is suitable for the connected load. A passive attenuator reduces the amount of power being delivered to the connected load by either a single fixed amount, a variable amount or in a series of known switchable steps. Attenuators are generally used in radio, communication and transmission line applications to weaken a stronger signal. The attenuator circuit configurations are shown in Fig 3.11.

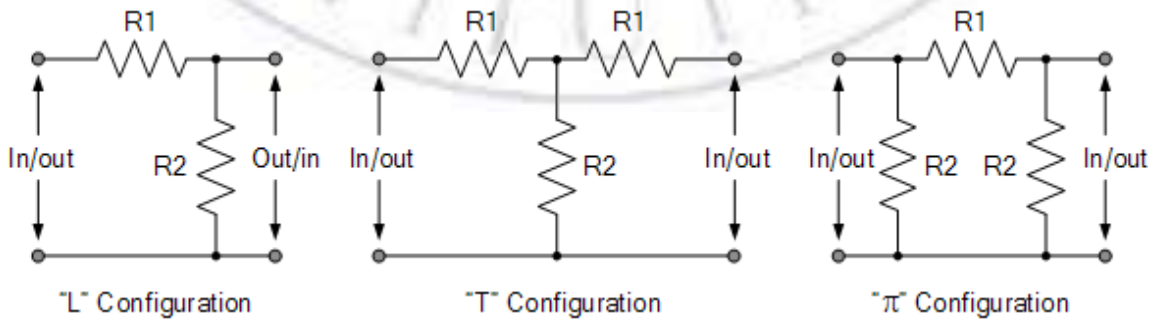

Fig 3.11 Attenuator Circuit types [23]

The Passive Attenuator is a purely passive resistive network (no supply) that is used in a wide variety of electronic equipment for extending the dynamic range of measuring equipment by adjusting signal levels, to provide impedance matching of oscillators or amplifiers to reduce the effects of improper input/output terminations or to simply provide isolation between different circuit stages depending upon the application [23].

Simple attenuator networks (also known as "pads") are designed to produce a fixed degree of "attenuation" or to give a variable amount of attenuation in pre-determined steps. Standard fixed attenuator networks generally known as an "attenuator pad" are available in specific values from 0 dB to more than 100 dB. Variable and switched attenuators are basically adjustable resistor networks that show a calibrated increase in attenuation for each switched step, for example steps of -2dB or -6dB per switch position. The schematic of Pi-pad attenuator circuit is shown in Fig 3.12.

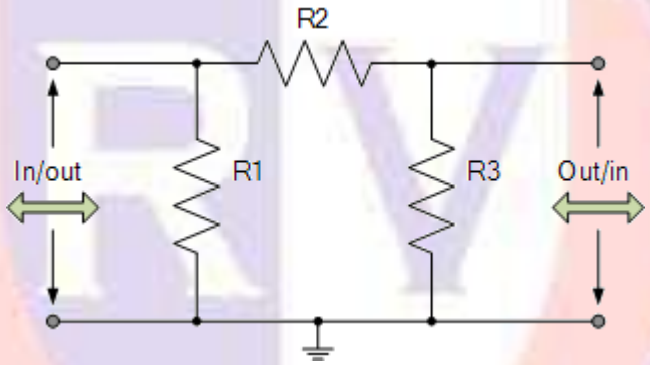

Fig 3.12 Pi-pad attenuator [23]

Pi-pad Attenuators or π-pad attenuators are commonly used in radio frequency and microwave transmission lines and can be of balanced or unbalanced designs. The Pi-pad attenuator is so called because its basic layout and design resembles that of the Greek letter pi (π), meaning that it has one series resistor and two parallel shunt resistors to ground at the input and the output. The Pi-pad attenuator is another fully symmetrical purely resistive network that can be used as a fixed attenuator between equal impedances or for impedance matching between unequal impedances. The three resistive elements are chosen to ensure that the input impedance and output impedance match the load impedance which forms part of the attenuator network. As the Pi-pad's input and output impedances are designed to perfectly match the load, this value is called the "characteristic impedance" of the symmetrical Pi-pad network

The equations to calculate the resistor values of a Pi-pad attenuator circuit used for

impedance matching at any desired attenuation are given as:

$$Z_S = Z_L = Z \tag{3.1}$$

$$R1 = R3 = Z\left(\frac{K+1}{K-1}\right) \tag{3.2}$$

$$R2 = Z\left(\frac{K^2-1}{2K}\right) \tag{3.3}$$

3.4 RC low pass Filter Circuit

A simple passive RC Low Pass Filter or LPF is easily made by connecting together in series a single resistor with a single capacitor as shown in Fig 3.13. In this type of filter arrangement the input signal (Vin) is applied to the series combination (both the resistor and capacitor together) but the output signal (Vout) is taken across the capacitor only. This type of filter is known generally as a "first-order filter" or "one-pole filter" because it has only one reactive component, the capacitor, in the circuit.

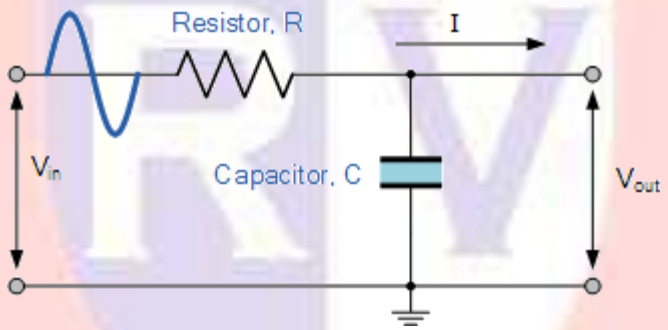

Fig 3.13 RC low pass Filter circuit [23]

The reactance of a capacitor varies inversely with frequency, while the value of the resistor remains constant as the frequency changes. At low frequencies the capacitive reactance, (Xc) of the capacitor will be very large compared to the resistive value of the resistor, R.

The voltage potential, Vc across the capacitor will be much larger than the voltage drop, Vr developed across the resistor. At high frequencies the reverse is true with Vc being small and Vr being large due to the change in the capacitive reactance value.

The capacitive reactance of a circuit is given by

$$X_C = \frac{1}{2\pi fC} \text{ in Ohms} \tag{3.4}$$

The circuit impedance is written as

$$Z = \sqrt{R^2 + X_C^2} \tag{3.5}$$

By using the potential divider equation of two resistors in series and substituting for impedance we can calculate the output voltage of an RC Filter for any given frequency.

$$V_{\text{out}} = V_{\text{in}} \times \frac{X_C}{\sqrt{R^2+X_C^2}} = V_{\text{in}} \frac{X_C}{Z} \tag{3.6}$$

3.4.1 Frequency Response of a first order RC low pass filter

The frequency response curve of a RC lowpass filter is shown in Fig 3.14

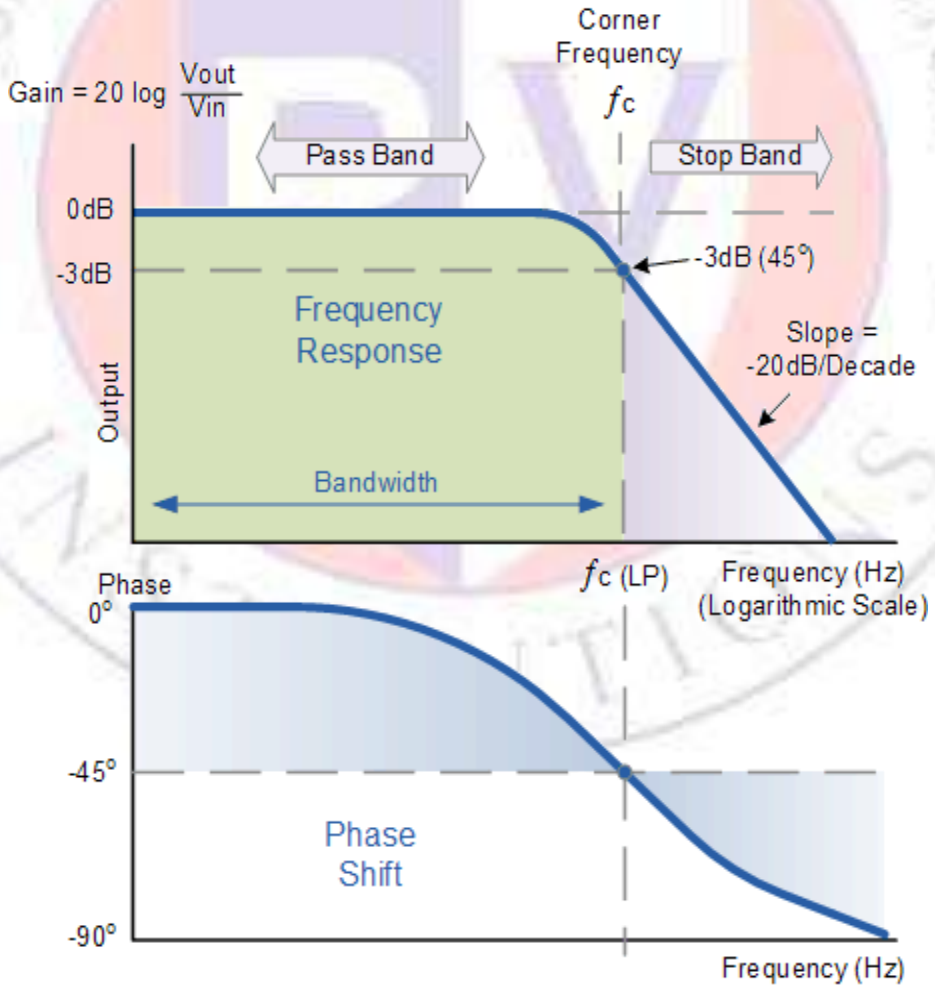

Fig 3.14 Frequency Response Curve of RC low pass Filter circuit [23]

The Fig 3.14 shows the frequency response of the filter to be nearly flat for low frequencies and all of the input signal is passed directly to the output, resulting in a gain of nearly 1, called unity, until it reaches its cut-off frequency point (fc). This is because the reactance of the capacitor is high at low frequencies and blocks any current flow through the capacitor. After this cut-off frequency point the response of the circuit decreases to zero at a slope of -20dB/ Decade or (-6dB/Octave) "roll-off". Note that the angle of the slope, this -20dB/ Decade roll-off will always be the same for any RC combination.

Any high frequency signals applied to the low pass filter circuit above this cut-off frequency point will become greatly attenuated, that is they rapidly decrease. This happens because at very high frequencies the reactance of the capacitor becomes so low that it gives the effect of a short circuit condition on the output terminals resulting in zero output. Then by carefully selecting the correct resistor-capacitor combination, we can create a RC circuit that allows a range of frequencies below a certain value to pass through the circuit unaffected while any frequencies applied to the circuit above this cut-off point to be attenuated, that is commonly called as Low Pass Filter.

For this type of "Low Pass Filter" circuit, all the frequencies below this cut-off, fc point that are unaltered with little or no attenuation and are said to be in the filters Pass band zone. This pass band zone also represents the Bandwidth of the filter. Any signal frequencies above this point cut-off point are generally said to be in the filters Stop band zone and they will be greatly attenuated.

The cut-off frequency point and phase shift angle can be found by using the following equation:

$$fc = \frac{1}{2\pi RC} \tag{3.7}$$

$$\text{Phase Shift } \varphi = -\arctan(2\pi f\ \text{RC}) \tag{3.8}$$

3.5 Pull up and Pull down resistors

The application of a pull up resistor and pull down resistor employed in digital circuits is shown in Fig 3.15

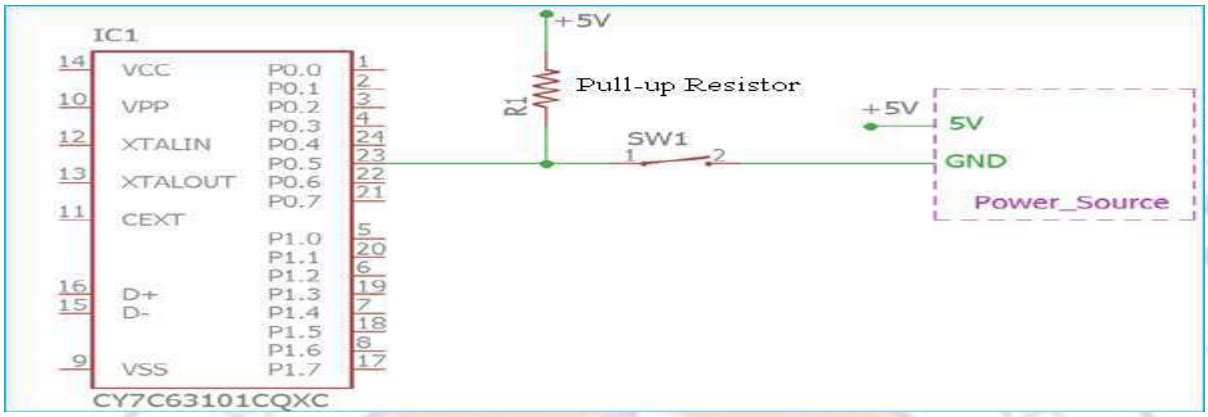

Fig 3.15 Application of a Pull up resistor [24]

If the high state as default is needed and want to change the state to Low by some external interaction, the Pull-up resistor is used. The digital logic input pin P0.5 can be toggled from logic 1 or High to the logic 0 or Low using the switch SW1. The R1 resistor acts as a pull-up resistor. It is connected with the logic voltage from the supply source of 5V. So, when the switch is not being pressed, the logical input pin has always a default voltage of 5V or the pin is always high until the switch is pressed and the pin is shorted to ground making it logic low. Fig 3.15 and Fig 3.16 represent the application of a Pull up and Pull down resistor.

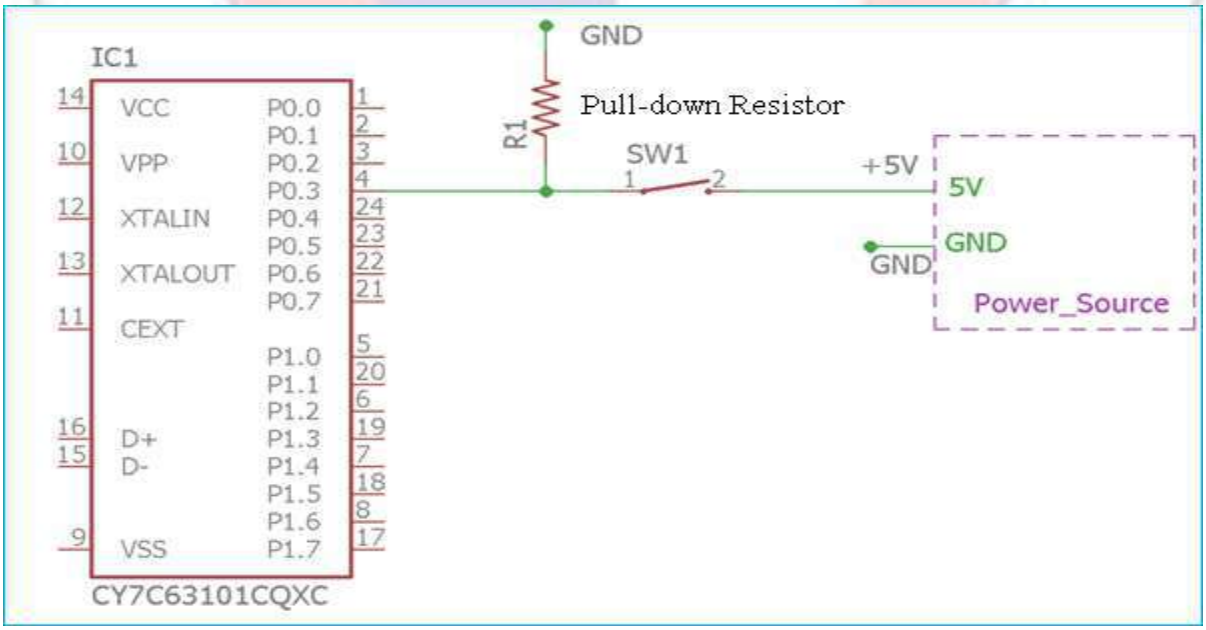

Fig 3.16 Application of a Pull down resistor [24]

The pull-down resistor R1 is connected with the ground or 0V and making the digital logic level pin P0.3 as default 0 until the switch is pressed and the logic level pin become high. In such case, the small amount of current flows from the 5V source to the ground using the closed switch and Pull-down resistor, hence preventing the logic level pin to getting shorted with the 5V source.

3.6 Flexible Input Circuit

The L9966 is an automotive graded Flexible Input IC designed to be used as sensor interface. Up to 15 channels are available for analog sensing, resistance measurement and digital sensing (e.g. temperature, lambda, pressure, position sensors). The L9966 allows replacing a number of discrete components and it gives the possibility to change the sensors across different applications without modifying the PCB hardware. Target applications are Engine Control Units and Body/Chassis Modules. Fig 3.17 shows the Flex input L9966 IC schematic diagram.

Fig 3.17 Flex Input L9966 Integrated Circuit

Features of L9966 IC are

- AEC-Q100 qualified.
- 12 V and 24 V systems compatible (operating battery supply voltage 5.5 V-36 V).
- Programmable interface with 15 total inputs: – 12 for connection to external analog loads (with connection to VVAR, VDD5 and clamped battery VPRE, with resistance measurement)

  1. 4 with also λ sensor functionality.

  2. 4 with also SENT functionality.

  3. for connection to external digital switches (with connection to VPRE) •

- Programmable pull-up/down current sources.

- Integrated precise resistance measurements.
- 12 bit ADC for voltage measurements.
- 15 bit ADC for resistance measurements.
- Variable reluctance sensor / Hall sensor Interface.
- 1 analog output channel + 4 digital output channels • SPI interface for device configuration and data communication.
- Overtemperature protection.
- Thermal resistance Rth(j-c) = 3 K/W.

3.7 Summary

This chapter incorporates the procedure of methodology and block diagram for the proposed work. The methodology for the implementation is discussed. The block diagram demonstrating the flow of each block is explained.A brief specification and design details are explained in the next chapter.

CHAPTER 4

SPECIFICATIONS AND DESIGN DETAILS

Several components are involved in the design and development of the proposed. This chapter presents the design and selection of various components as per the required specifications.

4.1 Design of ESD capacitors

Device-level tests model a factory or similar environment to ensure that unmounted semiconductor devices are not degraded or destroyed by ESD pulses in places where ESD is controlled.

There are three major ESD models:

1. Human body model (HBM): Models a discharge that might occur when a charged human touches a device.
2. Machine model (MM): Models a discharge that might be released from charged machines such as manufacturing systems .
3. Charged-device model (CDM): Models a discharge that might occur when a charged electrically isolated device touches an earthed circuit board during assembly.

4.1.1 Human body model

When a person is walking on a carpeted or rough surface, the charge in human's body is can be considered as the initial charge [11]. From charge equation Q=CV, the formulation of equation from the Fig 4.1. Fig 4.2 shows the ESD protection provided to IC.

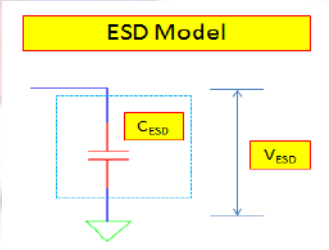

Fig 4.1 Generalized ESD Model [11]

$$Qinitial = CESD * VESD \quad (4.1)$$

Where CESD→ Body capacitance

VESD→ Peak voltage associated with body capacitance

When human touches the exposed pin, the charge from human body will transfer to the pin and the capacitor installed on it and the final charge will be

$$Qfinal = Cfinal * Vfinal \quad 4.2$$

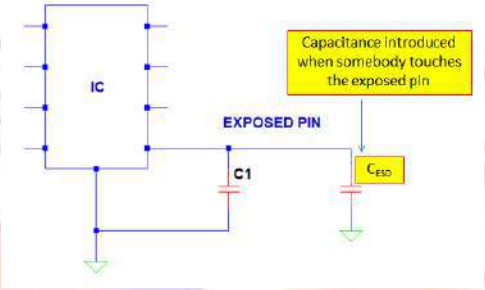

Fig 4.2 ESD protection provided to IC [11]

- By the virtue of conservation of charges,

$$Qinitial = Qfinal \quad 4.3$$

- Expressing C1,

$$C1 = \left(CESD * \frac{VESD}{Vfinal}\right) - CESD \quad 4.4$$

- From customer specifications, CESD=330pF and VESD=8kV and working voltage, Vfinal=875V.

- As a rule of thumb,use only 60% of the 875V which is 525V

$$C1 = \left(CESD * \frac{VESD}{Vfinal}\right) - CESD = \left(330pF * \frac{8kV}{525V}\right) - (330pF)$$

$$C1 = 4.7nF$$

Hence CSTvrsp = 4.7nF and CSTvrsn = 4.7nF

4.2 Design of differential Noise Capacitor Filter

The parasitic resistance of a capacitor is mainly determined from the capacitor data sheet [13]. Most capacitor datasheets provide a graph of capacitor impedance versus frequency as shown in Fig 4.3.

	NP0	X7R
Capacitance Tolerance	+50%, -20%	+50%, -20%
Voltage Rating	100V	50V
Current Rating	300mA	300mA
Insulation Resistance	1000MΩ	1000MΩ
DC Resistance	<0.6Ω	<0.6Ω
Operating Temperature Range	-55 to +125°C	

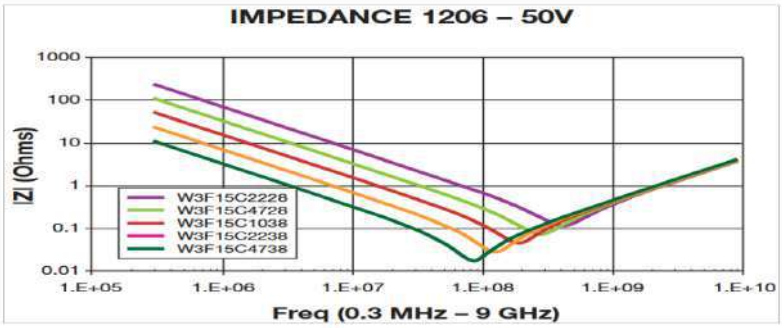

Fig 4.3 Frequency vs Impedance graph of a capacitor [13]

- From the graph, Rparasitic=6*10^-3 ohm, fc=2.65*10^10 Hz

$$fc = \frac{1}{2*3.142*Rparasitic*Cvrspn} \quad 4.5$$

$$Cvrspn = \frac{1}{2*3.142*2.65*10^{10}*6*10^{-3}} = 1nF$$

4.3 Design of common mode capacitor of RC low pass filter

Fig 4.4 shows the frequency response curve for VRSP and VRSN signals.

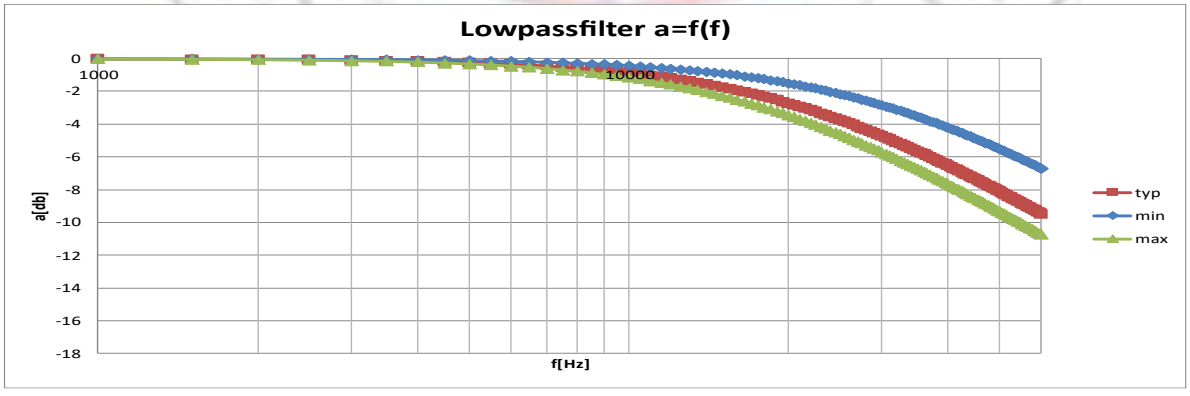

Fig 4.4 Frequency response curve of signals at VRSP and VRSN pins of L9966 IC

RC low pass filter is a first order filter that passes low frequency signals and rejects high frequency signals. From frequency response curve of RC low pass filter, the cut off frequency of signals passing at VRSP pin of flex input IC is fcutvrsp =12.271kHz and the cut off frequency of signals passing at VRSN pin of flex input IC is fcutvrsn = 12.271kHz. Let Rsrup1=46.4kohm, Rsrup2=68.1kohm

- Req1=Rsrup1 || Rsrup2 = 27596.8559 ohm
- $Cvrsp = 1/(2 * 3.142 * Req1 * fcutvrsp)$ 4.6
- $Cvrsp = 1/(2 * 3.142 * 27.596 * 10\text{^}3 * 12.271 * 10\text{^}3)$ = 470pF
- Let Rsrlo1=46.4kohm, Rsrup2=68.1kohm
- Req2=Rsrlo1 || Rsrlo2 = 27596.8559 ohm
- $Cvrsn = 1/(2 * 3.142 * Req2 * fcutvrsn)$ 4.7
- $Cvrsn = 1/(2 * 3.142 * 27.596 * 10^3 * 12.271 * 10\text{^}3)$= 470pF

4.4 Hysteresis level selection

The various specifications for Variable Reluctance Sensors are shown in Table 4.1

Table 4.1 Specifications of Variable Reluctance Sensor

Input parameters	Typical Values
Vdiagnosis	1 V
Idiagnosis	$5.7 * 10^{-5}$A
Rsensor	600 ohm
Short circuit to ground voltage (VSCG)	0 V
Short circuit to battery voltage (VSCB)	12 V
Vithl (Differential Voltage)	0 V
Ibias	0 A
Hysteresis current level 1	$6 * 10^{-6}$A

Hysteresis current level 2	$1.15 * 10^{-5}$ A
Hysteresis current level 3	$2 * 10^{-5}$ A
Hysteresis current level 4	$5.25 * 10^{-5}$ A
Hysteresis current level 5	$8 * 10^{-5}$ A
Peak Voltage 1	$9 * 10^{-1}$ V
Peak Voltage 2	1.5 V
Peak Voltage 3	2.1 V
` Peak Voltage 4	2.8 V

The quantized output is sent to a logic block (Hysteresis Selection Table) that chooses the proper hysteresis value (HIi) depending on the input peak voltage (PVi). Peak voltage range correspondence with hysteresis selection is shown in Table 4.2.

Table 4.2 Hysteresis selection corresponding to Peak Voltage Range

0-PV1	Hysteresis level 1
PV1-PV2	Hysteresis level 2
PV2-PV3	Hysteresis level 3
PV3-PV4	Hysteresis level 4
>PV4	Hysteresis level 5

Peak detector and Hysteresis Selection Table circuits are enabled by VRS_OUT signal according to VRS_HYST_FB bit value in the VRS SPI register that establishes if the feedback signal is before or after the filter time. VRS input differential voltage is continuously acquired to its max value, reached while VRS_OUT signal is high(hysteresis current off), is latched through the peak detector. Peak detector, in turn, defines the hysteresis current value. Hysteresis current is turned on as soon as the VRS_OUT falls to zero and it is switched OFF at next VRS_OUT rising edge. Based on the hysteresis current, the signal is processed by a square circuit which processes the output signal of the comparator to the microcontroller. Table 4.3 shows the sensor interface circuit parameters

4.5 Specifications of Sensor Interface Circuit

Table 4.3 Sensor Interface Circuit Parameters

Components	Description	Values
CSTvrsp	Positive variable reluctance sensor input capacitor for ESD protection	4.7nF
CSTvrsn	Negative variable reluctance sensor input capacitor for ESD protection	4.7nF
Rpu	Pull up resistor	10kohm
Cvrspn	Differential noise capacitor filter for EMC/EMI protection	1nF
Rpd	Pull down resistor	10kohm
RIN1,RIN2,RIN3,RIN4	Parallel resistances for signal attenuation	31.6kohm
Rsrup1,Rsrup2	Series up resistances for signal attenuation	46.4kohm,68.1kohm

Rsrlo1,Rsrlo2	Series low resistances for signal attenuation	46.4kohm,68.1kohm
Radj	Resistance used for signal attenuation	26.1kohm
Cvrsp	Variable reluctance positive common mode capacitor for EMC/EMI protection	470pF
Cvrsn	Variable reluctance negative common mode capacitor for EMC/EMI protection	470pF
VDD5	Supply Voltage	5 V
Vgndshift	Ground shift voltage	1 V
Vposmax	Input signal high clamping voltage	3.3 V
Vnegmax	Input signal low clamping voltage	-0.6 V

V3V3	Internal 3V3	3.3 V
Vcm	Common mode Voltage	1.6 V
Vhyst	Hysteresis Voltage	6 uV

4.6 Summary

This chapter incorporates the design procedure of ESD protection circuit, design details of differential noise capacitor filter, design method of common mode capacitor of RC low pass filter, details about hysteresis level selection, specifications of sensor interface block. The detailed explanation of simulation and hardware implementation is discussed in the next chapter.

CHAPTER 5

SIMULATION AND HARDWARE IMPLEMENTATION

This chapter explains the simulation of hall effect sensor interfacing, inductive sensor interfacing and push pull type sensor interfacing to a sensor interface block and flex input L9966 IC in Pspice. The hardware implementation is also presented. The waveforms obtained during simulation and hardware testing are discussed in next chapter. The results of Monte Carlo Analysis and Sensitivity Analysis for each sensor interfacing are discussed in next chapter.

5.1 Hall Effect Sensor Interfacing:

Fig 5.1 shows Hall effect sensor interfacing to sensor interface block and L9966 IC.

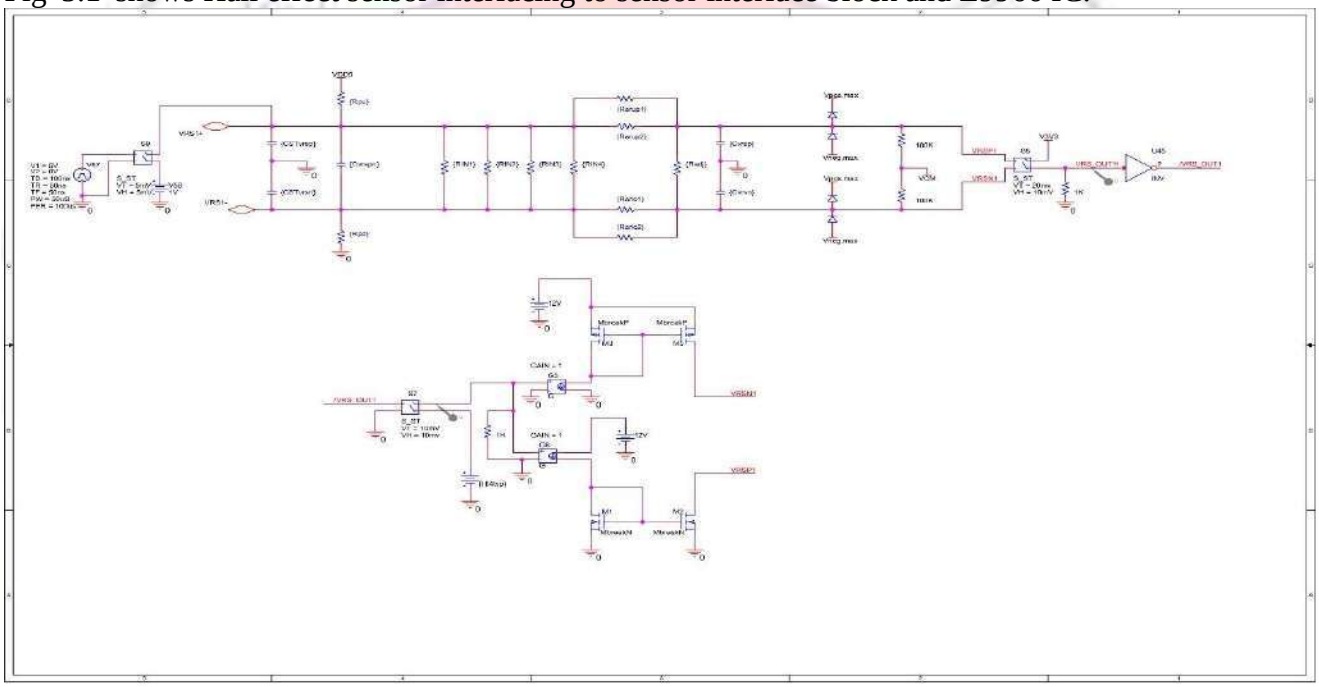

Fig 5.1 Circuit diagram for Hall Effect Sensor Interfacing

5.1.1 Simulation Circuit: Here the voltage controlled switch is modelled as "Hall Effect Sensor". The sensor senses the signal and is converted into electrical quantity. The signal is fed into input interface of a sensor interface block. The ESD capacitors at the input side prevents the circuit from electrostatic discharge phenomenon by shunting high frequency components into the ground. The pull up resistor pulls the voltage level equivalent to supply voltage level. The pull down resistor pulls down the voltage level equivalent to ground. The differential capacitor filter protects the circuit from electromagnetic interference. The resistive network acts as a pi attenuator

helps in signal attenuation such that desirable amount of power is delivered to load. The signal passes to the next stage. Here the RC low pass filter passes the low frequency signals at VRSP pin and VRSN pin of L9966 IC and rejects high frequency signals. The details of flex input modelling is discussed and the process of signal processing is explained in next section. The modelling of L9966 IC and schematic of L9966 IC are shown in Fig 5.2 and Fig 5.3.

5.1.2 Modelling of L9966 IC

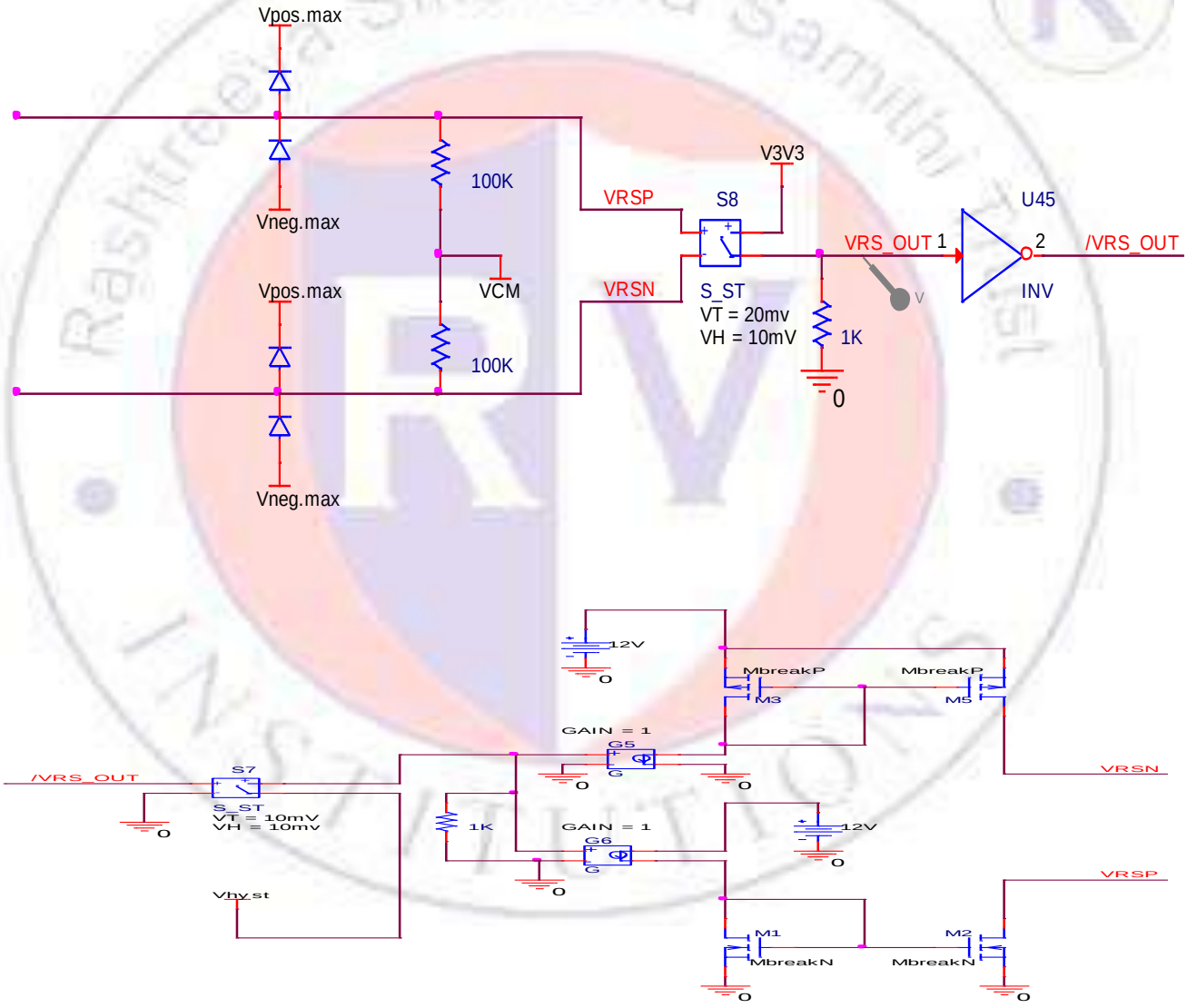

Fig 5.2 Modelling of Flex Input L9966 IC

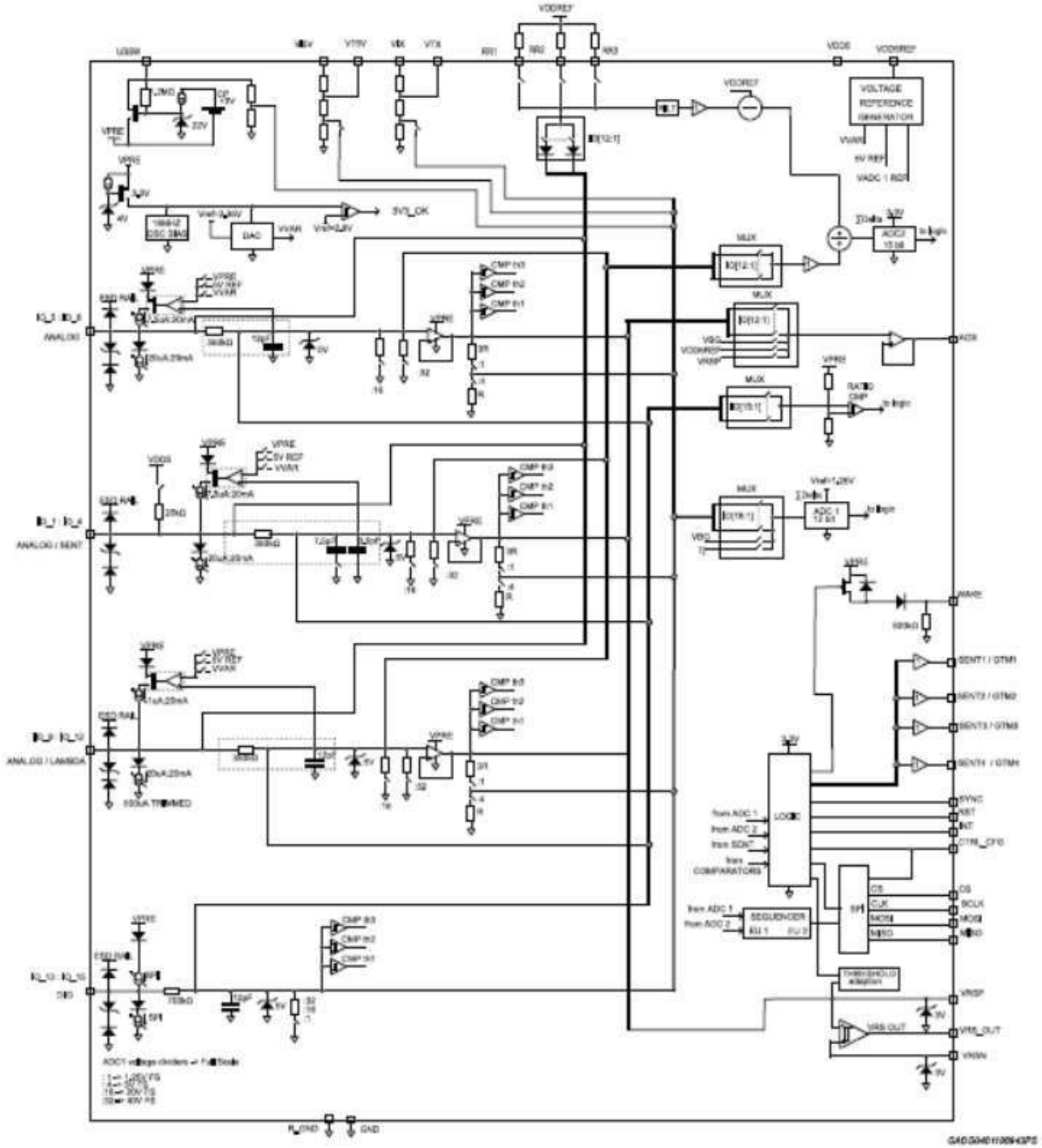

Fig 5.3 Schematic of Flex Input L9966 IC

5.1.3 Voltage Controlled Switch

Fig 5.4 shows the schematic of voltage controlled switch with hysteresis

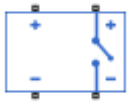

Fig 5.4 Voltage controlled switch with hysteresis

The Voltage-Controlled Switch block as shown in Fig 5.4 represents the electrical characteristics of a switch and the state is controlled by the voltage across the input ports (the controlling voltage). The block models either a variable-resistance or a short-transition switch. For a variable-resistance switch, set the Switch model parameter to Smooth transition between Von and Voff. For a short-transition switch, set Switch model to Abrupt transition after delay.

5.1.4 Short transition Switch

In a short-transition switch, the transition between the off and on states is instantaneous.

- When the controlling voltage is greater than or equal to the sum of the Threshold voltage, VT and Hysteresis voltage, VH parameter values, the switch is closed and has a resistance equal to the On resistance, RON parameter value.
- When the controlling voltage is less than the Threshold voltage, VT parameter value minus the Hysteresis voltage, VH parameter value, the switch is open and has a resistance equal to the Off resistance, ROFF parameter value.
- When the controlling voltage is greater than or less than the Threshold voltage, VT parameter value by an amount less than or equal to the Hysteresis voltage, VH parameter value, the voltage is in the crossover region and the state of the switch remains unchanged.

5.1.5 Voltage Controlled Current Source

Fig 5.5 shows the schematic of voltage controlled current source block.

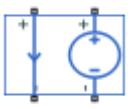

Fig 5.5 Voltage controlled current source

The Voltage Controlled Current Source block as shown in Fig 5.5 models a linear current-controlled voltage source, described with the following equation:

$$V=K\cdot I1 \qquad 5.1$$

Where V→ Voltage

K→ Transresistance

I1→ Current flowing from the + to the – control port

The block has four electrical conserving ports. Connections + and – on the left side of the block are the control ports. The arrow indicates the positive direction of the current flow. The other two ports are the electrical terminals that provide the output voltage. Polarity is indicated by the + and – signs.

5.1.6 Current Mirror Circuit

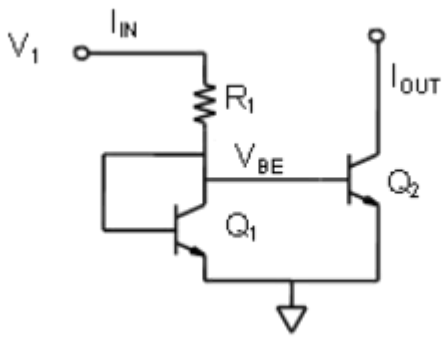

Fig 5.6 Current mirror circuit

A current mirror is a circuit block that functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. An important feature of the current mirror is that it has a relatively high output resistance that helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is that it has a relatively low input resistance that helps to keep the input current constant regardless of drive conditions. The current being 'copied' can be and often is a varying signal current. The current mirror is often used to provide bias currents and active loads in amplifier stages.

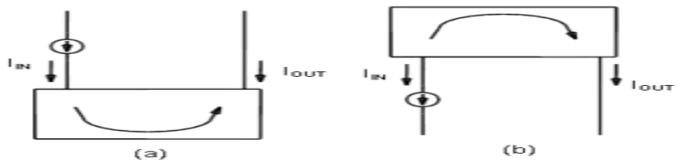

Fig 5.7 Current mirror circuit (a) Sink (b) Source

The ideal block level concept of the current mirror is shown in Fig 5.6. Given a current source as the input, the input section of the current mirror looks like a virtual short circuit and reflects (swaps the direction of flow) this current to produce a current sink (the current exiting the mirror). As a result, a current sink is obtained (Fig 5.7 (a)). Conversely, given a current sink as the input, the current mirror reflects this current to control current source. As a result, a current source is obtained (Fig 5.7 (b)). A current mirror consists of a low impedance input stage connected to a high impedance output current stage. Fig 5.8 and Fig 5.9 represent current to voltage conversion stage and voltage to current conversion stage.

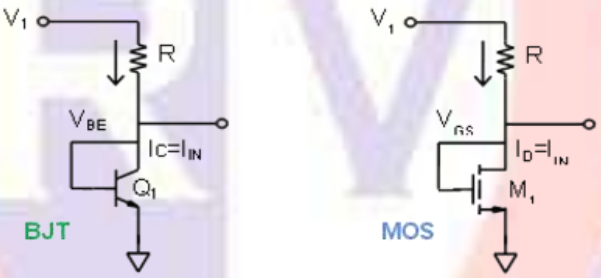

Fig 5.8 Current to Voltage Converter

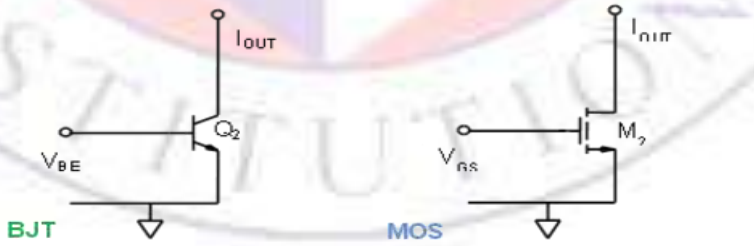

Fig 5.9 Voltage to Current Converter

The BJT current mirror circuit and MOSFET current mirror circuit are shown in Fig 5.10 and Fig 5.11.

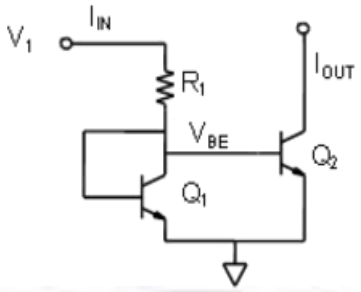

Fig 5.10 BJT Current Mirror Circuit

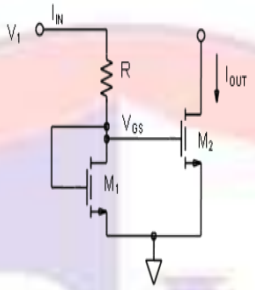

Fig 5.11 MOSFET Current Mirror Circuit

5.1.7 An input stage to convert current to voltage

The active element, a single transistor, serves as the desired current-to-voltage converter. For BJT the base emitter voltage controls the collector current or for the FET the gate source voltage controls the drain current. Producing the opposite where the collector current controls the V_{BE} is not possible in the conventional use of the device as a common emitter amplifier. In this case the transistor adjusts its base emitter or gate source voltage, V_{BE} or V_{GS}, so that the collector or drain current is $I_{IN} = (V_1\text{-}V_{BE})/R$. For this purpose, simply connect the collector to the base or gate to drain or "diode connect" the transistor. This classic "diode" connection results in 100% parallel negative feedback (Fig 5.8). As a result, with this diode connected transistor, the collector current serves as the input quantity while the base-emitter voltage V_{BE} serves as the output quantity with the logarithmic transfer function of the base emitter junction. Similarly, a diode connected enhancement mode MOSFET (gate tied to drain) will serve as a similar current to voltage converter with V_{GS} as the output quantity rather than V_{BE}.

5.1.8 An output stage to convert voltage to current

A bipolar transistor can be driven by a voltage or by a current. If the base emitter voltage V_{BE} is considered as the input and the collector current I_C as the output (Fig 5.9), a transistor as a non-

linear voltage-to-current converter having an exponential characteristic is considered. The base can be directly driven by the voltage output of the I-to-V converter. The collector provides the output terminal of a simple current mirror. The output V to I converter stage of the simple current mirror is just a transistor acting as a non-linear (exponential for BJT) voltage-to-current converter. If a MOS transistor is used for the input stage, the output stage would be a MOS transistor with the gate serving as the voltage input and the drain as the current output.

5.1.9 Signal processing in L9966 IC

The two signals incoming from the sensor interface block are fed and processed into VRSP and VRSN pins of an IC. The integrated circuit consists of 2 comparators. The difference between the two signals VRSP and VRSN is considered as the control voltage. A comparator1 compares the control voltage with the reference voltage. If the control voltage is greater than the sum of hysteresis voltage and threshold voltage, the output will be 3.3V of logic high state. If the control voltage is less than difference between threshold voltage and hysteresis voltage, the output will be logic low state. The overall voltage VRS_OUT is inverted with the help of a NOT gate and is sent to comparator 2. A comparator2 compares the control voltage. Here the control voltage will be the difference between complement of VRS_OUT and 0V. The control voltage is compared. If the control voltage is greater than the sum of hysteresis voltage and threshold voltage, the output will be logic low state. If the control voltage is less than difference between threshold voltage and hysteresis voltage, the output will be logic high state of 6uV. The overall output voltage signal is sent to 2 voltage controlled current source blocks. Voltage controlled current source 1 generates the hysteresis current 1 of 6uA and is sent to the current mirror circuit 1. Similarly voltage controlled current source 2 generates the hysteresis current 2 of 6uA and is sent to the current mirror circuit 2. In current mirror circuit 1, MOSFET MbreakP1 acts as current to voltage converter and MOSFET MbreakP2 acts as voltage to current converter and there by generating the copy of the reference circuit and same current is sinked (-6uA) at VRSN pin of L9966 IC. In current mirror circuit 2, MOSFET MbreakN1 acts as current to voltage converter and MOSFET MbreakN2 acts as voltage to current converter and there by generating the copy of the reference circuit and same current is sourced (6uA) at VRSP pin of L9966 IC. The resultant rectangular digital output from VRS_OUT pin of L9966 IC is fed to a microcontroller. The signal from the microcontroller produces an alarm signal and actuates the actuator. This is the process of signal conditioning of flex input L9966 IC.

5.2 Inductive Sensor Interfacing:

The circuit diagram for inductive sensor interfacing is shown in Fig 5.12.

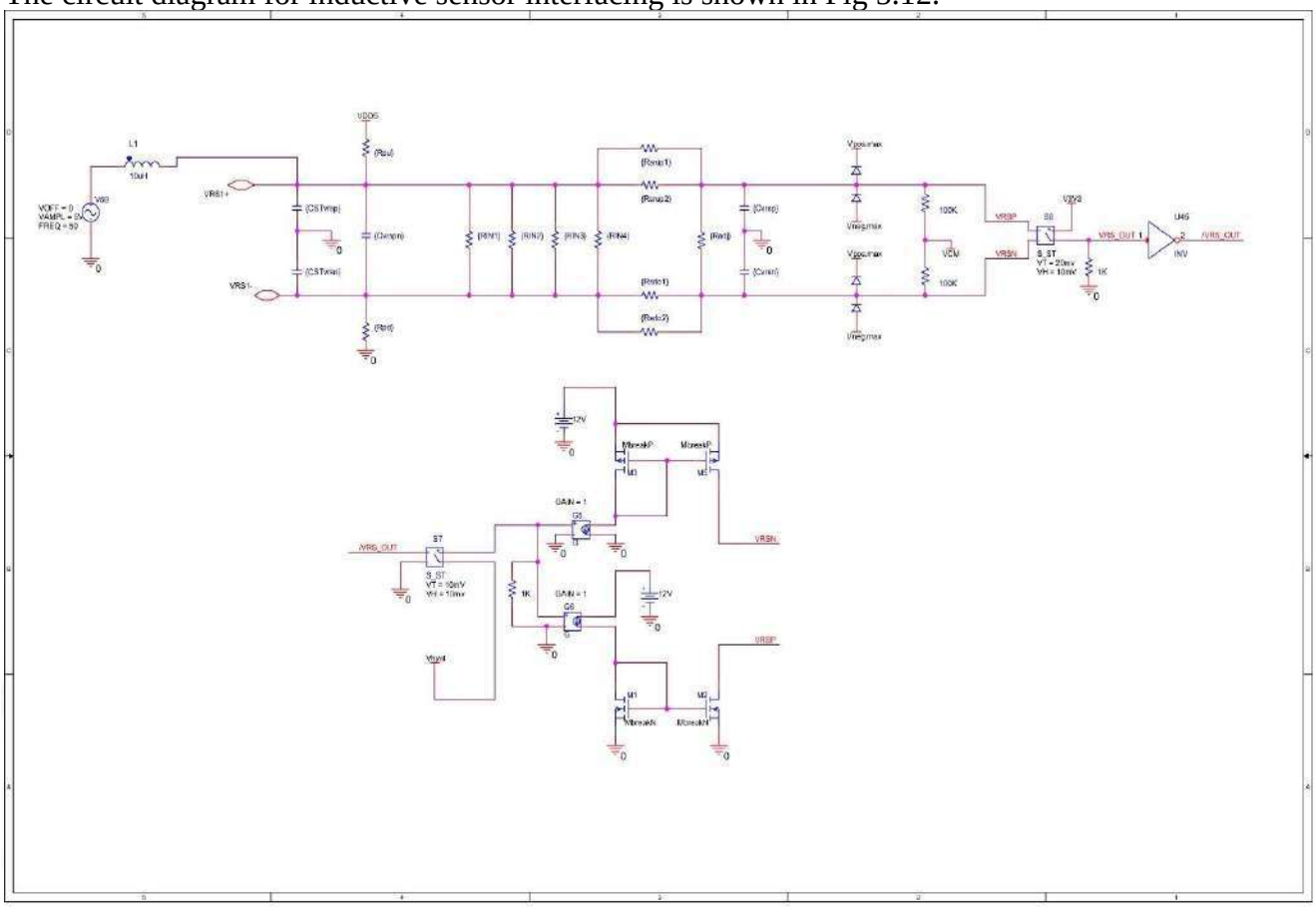

Fig 5.12 Circuit diagram for Inductive Sensor Interfacing

The circuit consists of an AC voltage source and an inductor of 10 uH. The inductive sensor senses the speed of the crankwheel and the signal is fed to a sensor interface block and the signal output from the sensor interface block is fed to a flexible input L9966 IC. Similarly like Hall Effect Sensor, by the comparator action located inside L9966 IC, rectangular pulses are obtained and are sent to a microcontroller. The microcontroller activates the actuator and there by completing the mechanism.

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5.3 Push Pull type Sensor Interfacing:

The simulated circuit diagram for Push Pull type Sensor Interfacing is shown in Fig 5.13.

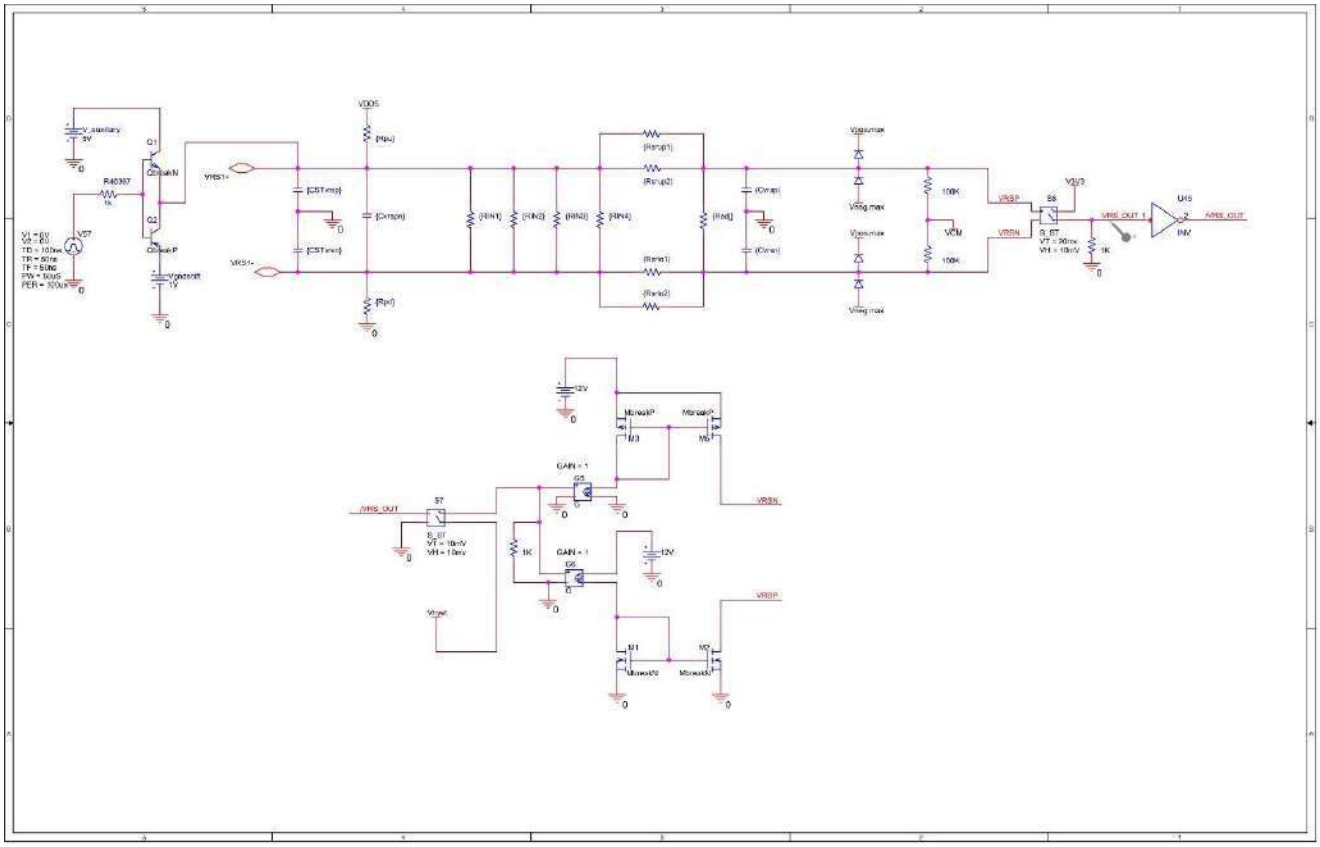

Fig 5.13 Circuit diagram for Push Pull type Sensor Interfacing

The push-pull sensors are the combination of P-N-P and the N-P-N transistors. It acts as a dual-stage sensor. The N-P-N transistor here acts as a push sensor during turn on time. P-N-P transistor acts as a pull sensor during turn off time. The push pull type sensor is capable of sensing any analog parameter from engine control section, The sensed signal is processed to a sensor interface block. The sensed signal is converted to a undistorted signal by sensor interface block. During next stage, the signal is processed to a flexible input L9966 IC. The comparator located inside L9966 IC generates the digital rectangular pulses and are fed to a microcontroller. Microcontroller generates an actuating signal and there by drives an actuator and there by completing the mechanism.

5.4 Hardware Implementation for Flexible Sensor Interface Module

The Hardware module of flexible sensor interfacing is shown in Fig 5.14.

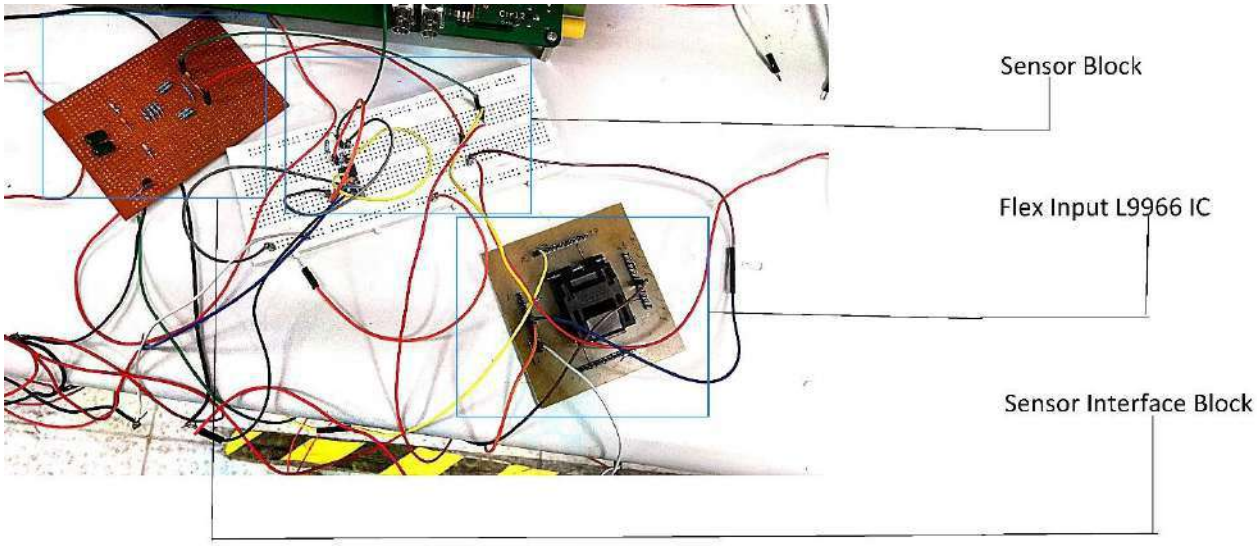

Fig 5.14 Hardware Module of Flexible Sensor Interfacing

The hardware module consists of following parts.

1. Sensor Block
2. Sensor Interface Block
3. Flex Input L9966 IC

5.5 Sensor Block

The sensor block consists of three types of sensors:

- Hall Effect Sensor: Here BJT is modelled as Hall Effect sensor.
- Inductive Sensor**:** Here two sinusoidal voltage sources one with phase angle of 0 degree and other source with phase angle of 180 degree are connected in parallel. This combination is modelled as inductive sensor.
- Push Pull type Sensor: Here 555 timer in astable mode is modelled as a push pull sensor.

The three sensors are tested for functionality by interfacing to sensor interface block and flex input L9966 IC.

5.6 Sensor Interface Block

Fig 5.15 shows the hardware module of sensor interface block.

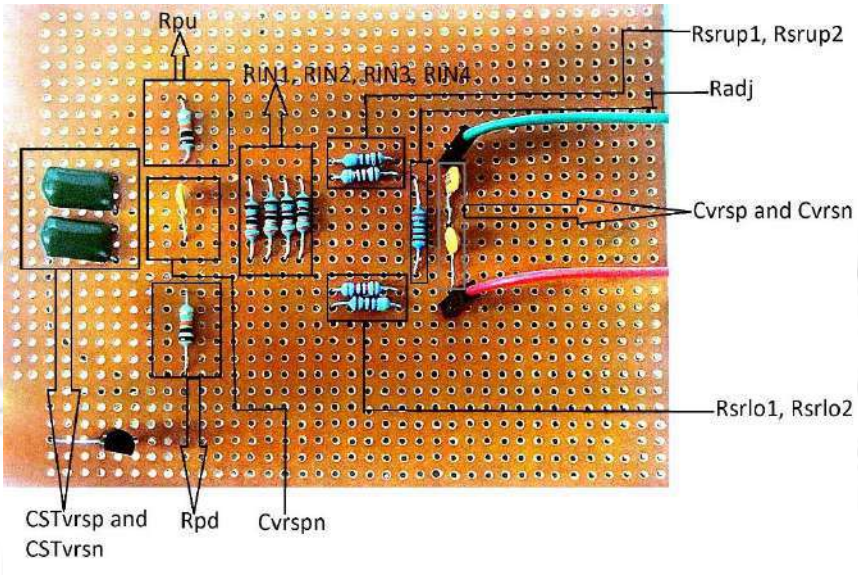

Fig 5.15 Hardware Module of Sensor Interface Block

Table 5.1 Ratings of components used in Sensor Interface Block

Component	Rating
CSTvrsp, CSTvrsn	4.7 nF
Rpu, Rpd	10kohm
Cvrspn	1nF
RIN1, RIN2, RIN3, RIN4	31.6kohm
Rsrup1, Rsrup2	46.4kohm, 68.1kohm
Rsrlo1, Rsrlo2	46.4kohm, 68.1kohm
Radj	26.1kohm
Cvrsp, Cvrsn	470pF

The sensor interface block comprises of capacitors for electrostatic discharge protection, differential capacitor for EMC/EMI protection, pull up and pull down resistors, pi attenuator circuit, RC low pass filter to filter high frequency components.

5.7 Flex Input L9966 IC

The pin connection diagram and details about pin numbers are shown in Fig 5.16 and Table 5.2.

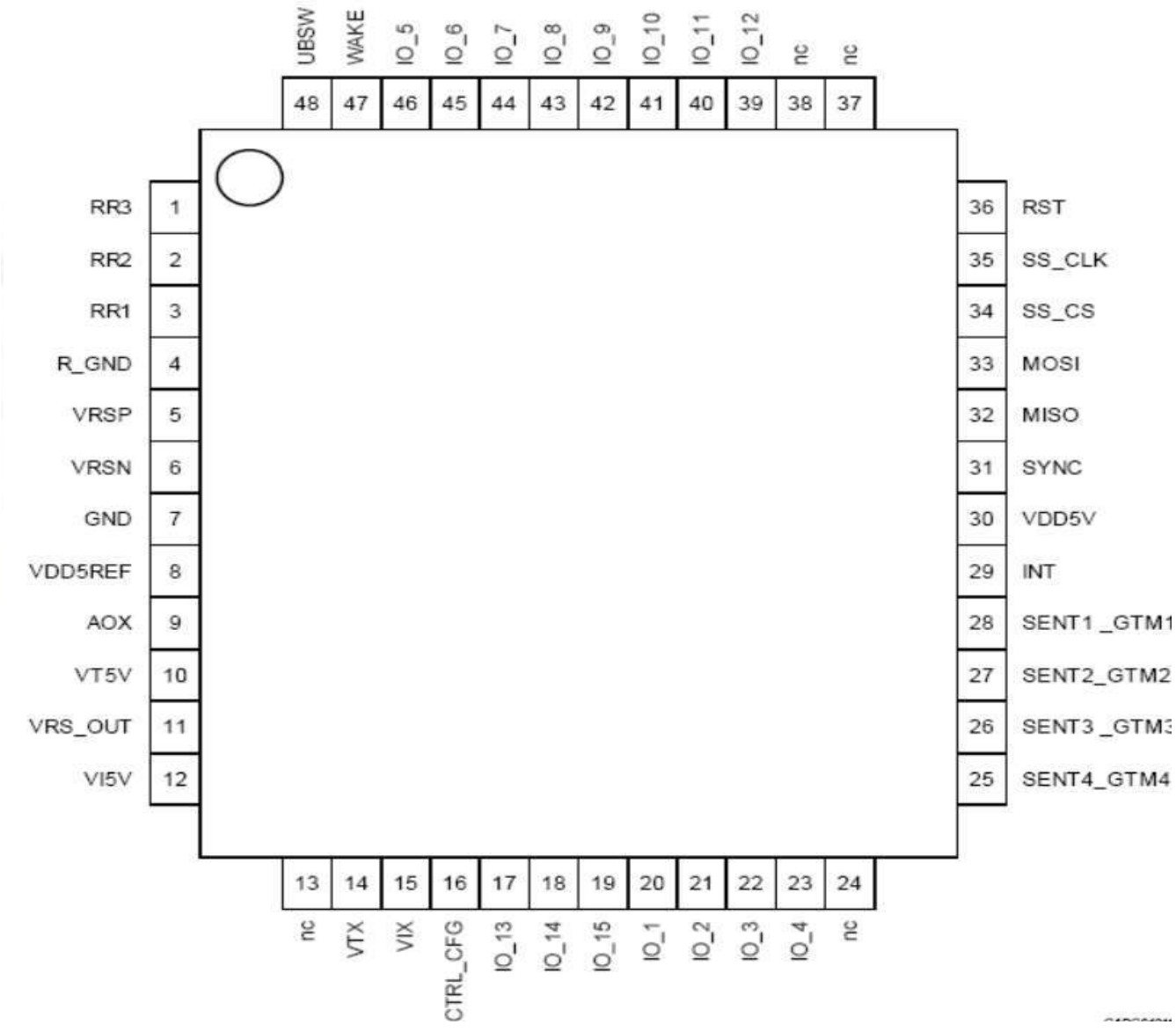

Fig 5.16 Pin connection diagram of flex input L9966 IC

L9966 is an automotive graded IC that can used as a major component of sensor interface block. L9966 IC comprises of 48 pins. The hardware module of flex input is shown in Fig 5.17 and it consists of 48 pins.

Table 5.2 Details of Pin Description

Pin Number	Pin Name	Pin Description
1	RR3	Reference Pullup Resistor 3 for R-Measurement
2	RR2	Reference Pullup Resistor 2 for R-Measurement
3	RR1	Reference Pullup Resistor 1 for R-Measurement
4	R_GND	Reference Ground for high accuracy signals
5	VRSP	Positive variable reluctance sensor input
6	VRSN	Negative variable reluctance sensor input
7	GND	Ground for supply voltage
8	VDD5REF	Positive reference to both ADC
9	AOX	Analog output for input channel x
10	VT5V	Ratiometric Voltage output VI5V
11	VRS_OUT	Digital Output of Variable reluctance sensor
12	VI5V	Input Voltage
13	NC	Not connected
14	VTX	Ratiometric Voltage output VIX
15	VIX	Input Voltage

16	CTRL_CFG	Input to control current source / Configuration input to select SPI Address-Mux during Reset
17	IO_13	Flexible Input and current output 13
18	IO_14	Flexible Input and current output 14
19	IO_15	Flexible Input and current output 15
20	IO_1	Flexible Input and current output 1 / SENT1
21	IO_2	Flexible Input and current output 2 / SENT2
22	IO_3	Flexible Input and current output 3 / SENT3
23	IO_4	Flexible Input and current output 4 / SENT4
24	NC	Not connected
25	SENT4_GTM4	Digital Output for SENT 4 channel / GTM_TO_SENT_4
26	SENT3_GTM3	Digital Output for SENT 3 channel / GTM_TO_SENT_3
27	SENT2_GTM2	Digital Output for SENT 2 channel / GTM_TO_SENT_2
28	SENT1_GTM1	Digital Output for SENT 1 channel / GTM_TO_SENT_1
29	INT	Interrupt (result status for controller)
30	VDD5V	5 V Power supply
31	SYNC	Digital input to synchronize sequencer start
32	MISO	Communication interface clock for Master-

		IN/ Slave-OUT
33	MOSI	Communication interface for Master-OUT/ Slave-IN
34	SS_CS	Communication interface chip select
35	SS_CLK	Communication interface clock
36	RST	Reset
37	NC	Not connected
38	NC	Not connected
39	IO_12	Flexible Input and current output 12 / LAMBDA
40	IO_11	Flexible Input and current output 11 / LAMBDA
41	IO_10	Flexible Input and current output 10 / LAMBDA
42	IO_9	Flexible Input and current output 9 / LAMBDA
43	IO_8	Flexible Input and current output 8
44	IO_7	Flexible Input and current output 7
45	IO_6	Flexible Input and current output 6
46	IO_5	Flexible Input and current output 5
47	WAKE	Output for wake-up
48	UBSW	Battery supply

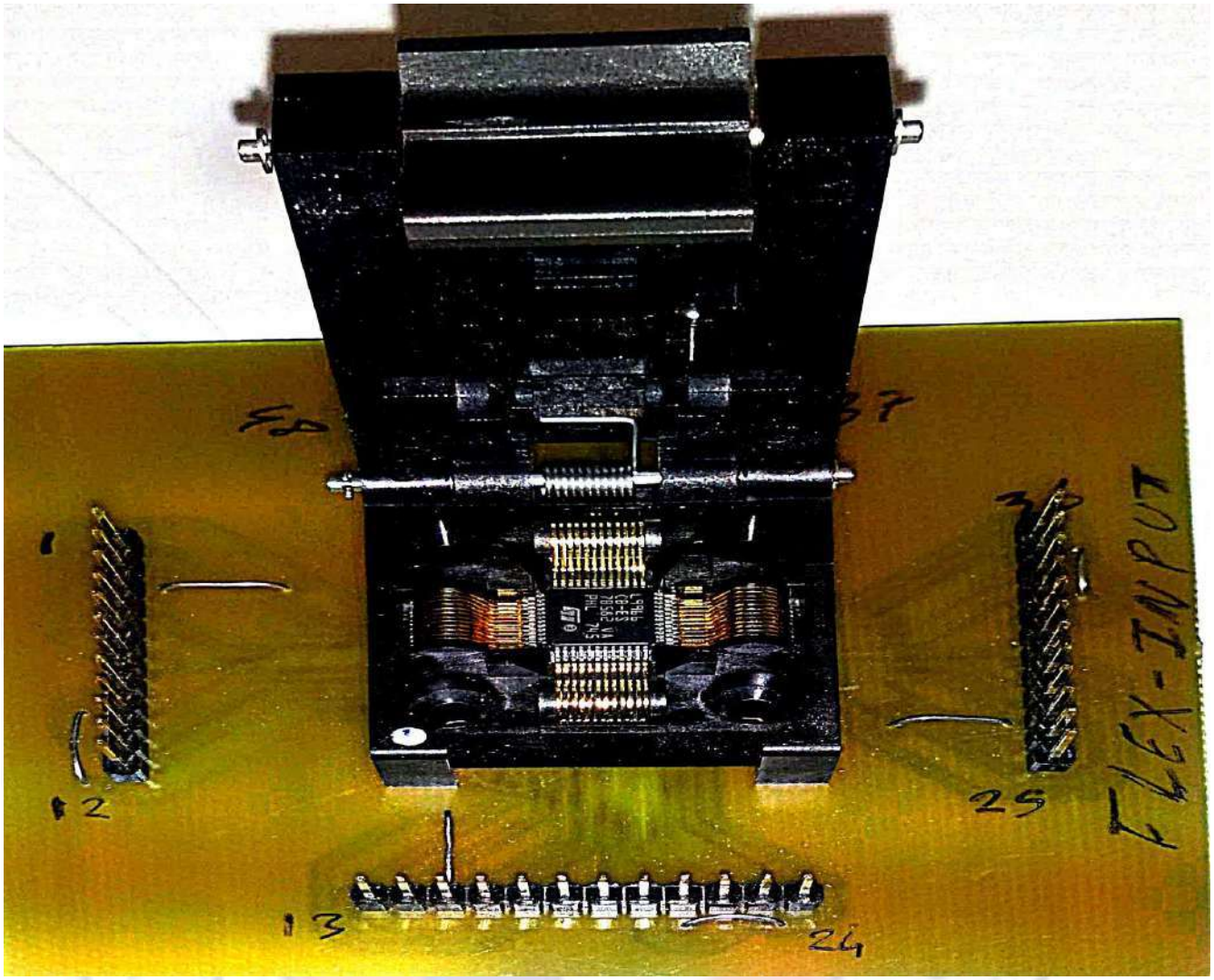

Fig 5.17 Hardware Module of flex input L9966 IC

Using Flexible sensor hardware interface module, Hall effect sensor, inductive sensor and push pull type sensor are interfaced to sensor interface model and L9966 IC. A power supply of 5 V is used to power the sensor interface block and VDD5 pin of L9966 IC. A power supply of 12 V is used to power the UBSW pin of L9966 IC. The output generated at VRS_OUT pin is in the form of digital rectangular pulses. The digital pulses are fed into microcontroller and microcontroller generates an alarm signal for actuator and there by terminating the process.

5.8 Summary

This chapter presents the simulation of Hall sensor interfacing, Inductive Sensor interfacing and Push Pull type Sensor interfacing to a sensor interface block and flex input L9966 IC using Pspice simulation tool and hardware circuit for the proposed simulation circuit was constructed.

CHAPTER 6

RESULTS AND DISCUSSIONS

A simulation result helps to analyze the performance of flexible sensor interfacing circuit. The result is verified and validated using Monte Carlo and Sensitivity Analysis. The simulation analysis is used to implement the hardware. This chapter consists of detailed results of the simulation and Monte Carlo simulated result and result obtained from Sensitivity Analysis and hardware results of the project.

6.1 Simulation

Hall Effect Sensor Interfacing circuit, Inductive Sensor Interfacing circuit and Push Pull type Sensor Interfacing circuit are simulated. Simulation is done in Pspice. Monte Carlo and Sensitivity Analysis are used for validation of the designed circuit. Thewaveforms of VRSP, VRSN and VRS_OUT are computed and analysed.

6.2 Simulation results of Hall Effect Sensor Interfacing

Simulation results of Positive variable reluctance sensor input (VRSP), Negative variable reluctance sensor input (VRSN) and Output voltage (VRS_OUT), Monte Carlo on Pulse width measurement of output voltage and application of Sensitivity Analysis on output voltage is presented.

6.3 Hall Sensor Interfacing

The waveforms of VRSP, VRSN and VRS_OUT are shown in Fig 6.1. In VRSP and VRSN waveforms, the signal charges to 6uA pull up and discharges to 6uA pull down and both the waveforms are triangular in nature. The signals VRSP and VRSN are compared with the reference signal, there by rectangular digital pulses are generated at VRS_OUT pin. The average output voltage obtained was 3.3 V.

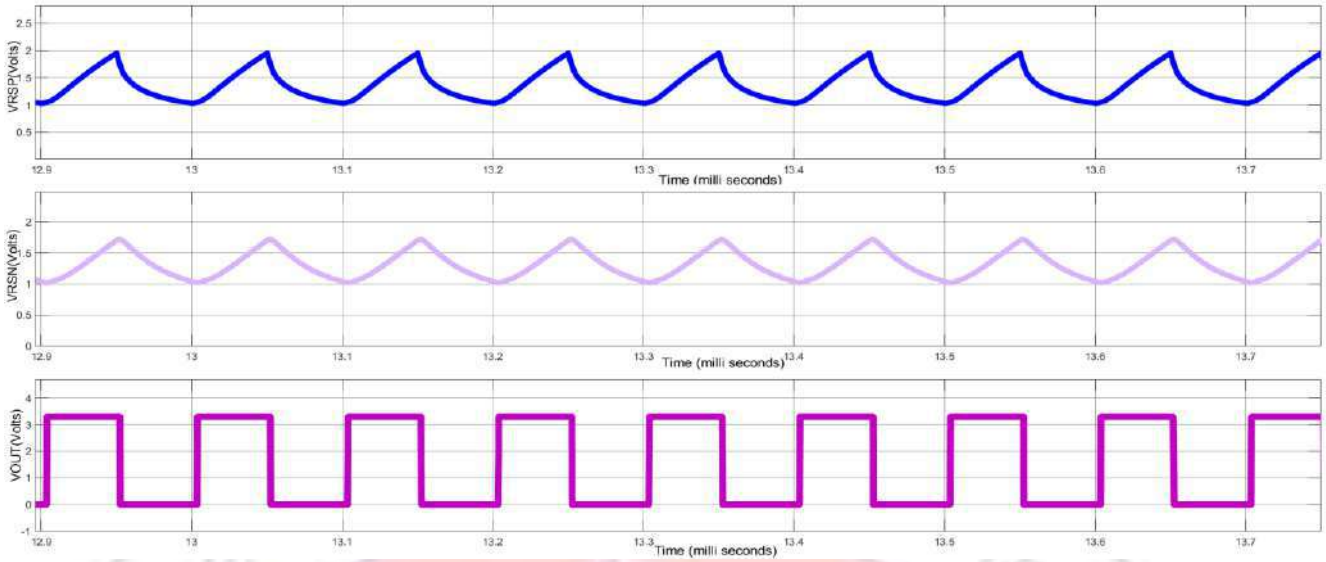

Fig 6.1 Waveforms of Hall Sensor Interfacing Circuit

6.3.1 Monte Carlo Result

Various factors such as resistance positive or negative temperature coefficient, thermal conditions such as soldering or extended high or low-temperature, operating conditions such as humidity, pressure, and exposure to vibration or shock will affect the tolerance value of resistors and hence the tolerance value of resistors is set as +3.5% and -3.5% . Various factors such as capacitor ageing rate, ESD/EMI protection tolerance, conductive tolerance will affect the tolerance value of capacitors and hence the tolerance value of capacitors is set as +20% and -20%. The Histogram view of Monte Carlo Run for 1000 test cases is shown in Fig 6.2.

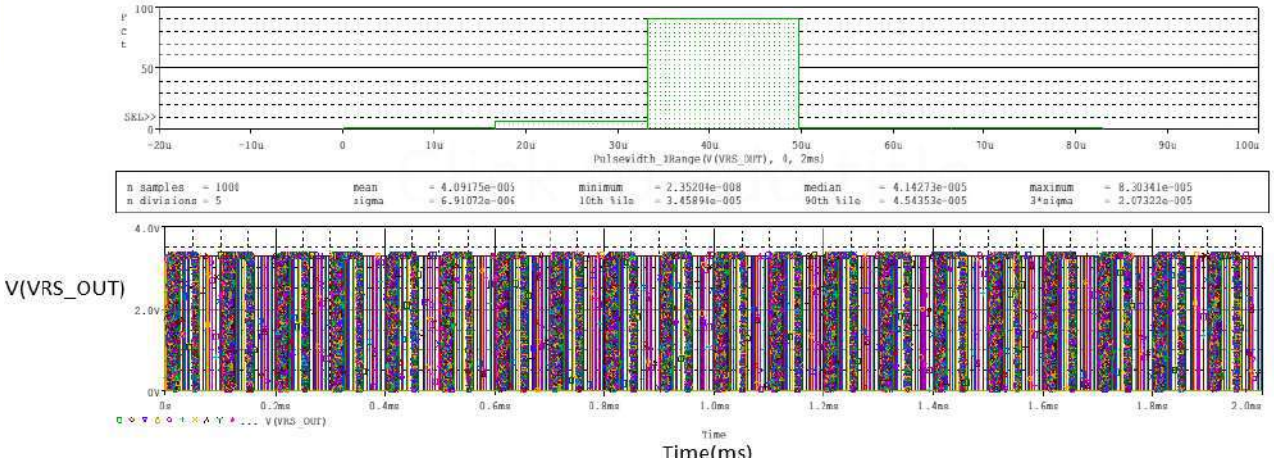

Fig 6.2 Monte Carlo Histogram distribution for pulse width measurement

The Hall sensor measures the speed of the crank wheel. The measured pulse width from Monte Carlo histogram is a measure of engine rpm (crank speed). The histogram indicates the boundary values. The measured engine speed lies between minimum and maximum value. From histogram distribution, it can be understood that the average pulse width is 40.91 usec which implies that average rpm of the engine would be equivalent to 40.91 usec. The pulse width is also a measure of life cycle of engine rpm. The measured 3 sigma value indicates that 99.7% of the values will lie within three standard deviations from the average pulse width value which means that for all 1000 runs, the resulted output is 99.7% accurate under this region.

6.3.2 Sensitivity Analysis Result

Sensitivity Analysis tool examines how much each component affects circuit behaviour by itself and in comparison to the other components. Fig 6.3 and Fig 6.4 show the process of generating the values for Sensitivity Analysis of Hall Sensor interfacing. Fig 6.5, Fig 6.7, Fig 6.10 show that the components CSTvrsn, Cvrsn and RIN1 have perfectly negative correlationship with respect to variation in output voltage. Fig 6.8 and Fig 6.13 show that the components Cvrsp and Rpu have low negative correlation with respect to variation in output voltage. Fig 6.6, Fig 6.9, Fig 6.15, Fig 6.16 show that the components CSTvrsp, Cvrspn, Rsrlo2, Rsrup1 have perfectly positive correlationship with respect to variation in output voltage. Fig 6.14 and Fig 6.17 shows that Rsrlo1 and Rsrup2 have high positive correlationship with respect to variation in output voltage. Fig 6.11 shows that Radj has low positive correlationship with respect to variation in output voltage. Fig 6.12 indcates that the component Rpd has no correlation with respect to output voltage. Fig 6.18 gives an instance of tornado plot representing the percentage contribution of each component to output voltage measured in terms of regression, standardized regression and partial correlation. Fig 6.19 represents the numerical data generated showing the sensitivity of each component to the output voltage measured interms of linear correlation, linear standardized regression, linear partial correlation.

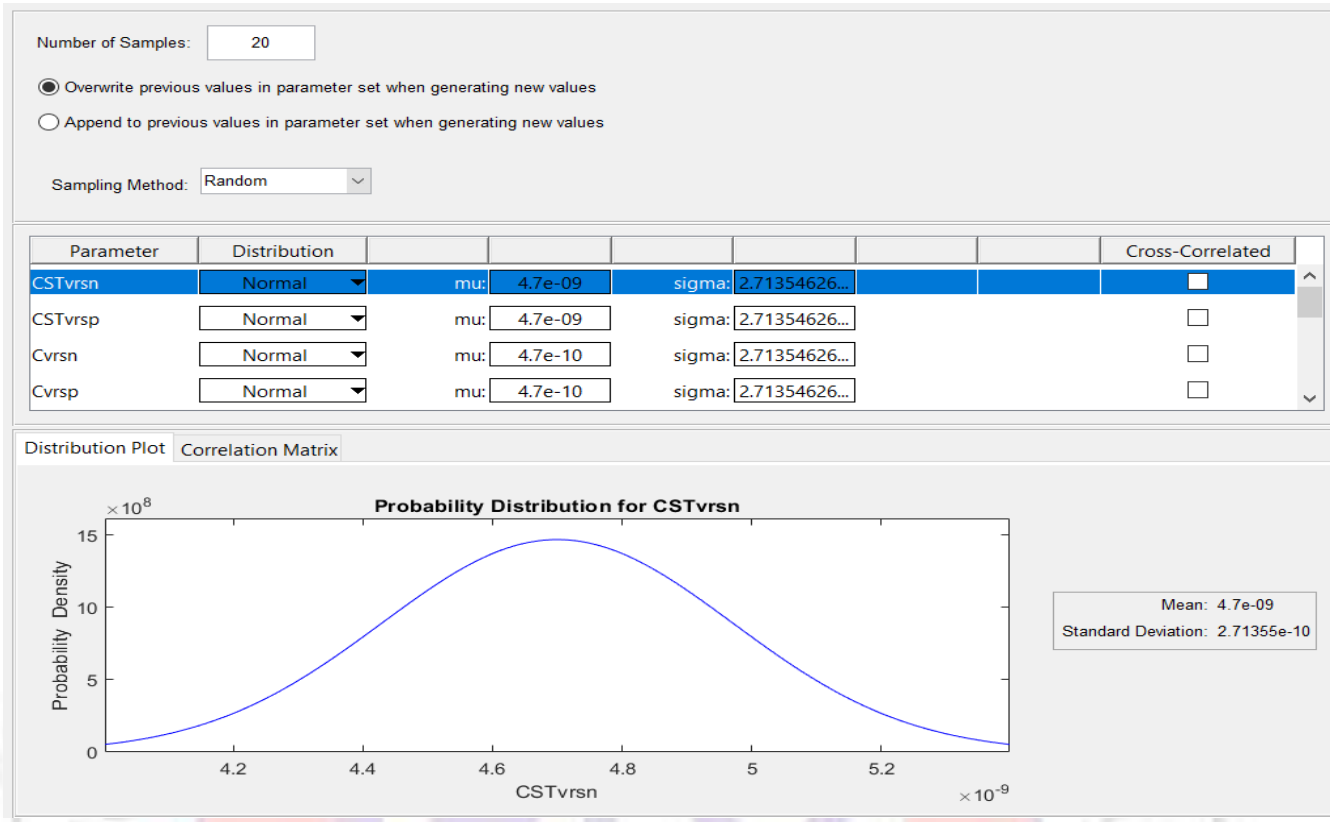

Fig 6.3 Sensitivity Analysis for Hall Sensor Interfacing

CSTvrsn	CSTvrsp	Cvrsn	Cvrsp	Cvrspn	RIN1	Radj	Rpd	Rpu	Rsrlo1	Rsrlo2	Rsrup1	Rsrup2	VRS_OUT
4.5655e-09	4.9983e-09	4.2043e-10	4.4461e-10	9.6047e-10	3.2690e+04	2.7619e+04	9.3978e+03	1.0712e+04	4.8317e+04	8.7272e+04	4.5138e+04	8.1762e+04	3.2967
4.4711e-09	4.6116e-09	5.0958e-10	4.4872e-10	1.0935e-09	3.0165e+04	2.6509e+04	9.2419e+03	9.9432e+03	4.1752e+04	8.5866e+04	4.7525e+04	8.1304e+04	3.2967
5.2737e-09	4.7230e-09	4.8893e-10	5.0332e-10	9.2216e-10	2.8276e+04	2.6386e+04	1.0748e+04	8.9497e+03	4.8560e+04	8.3823e+04	4.6600e+04	8.0989e+04	3.2967
5.0298e-09	4.5581e-09	4.6084e-10	4.5843e-10	9.6113e-10	3.4453e+04	2.5365e+04	1.0155e+04	1.0127e+04	4.6381e+04	8.5808e+04	4.4192e+04	7.8196e+04	3.2967
5.3502e-09	4.8891e-09	4.4662e-10	4.3460e-10	9.8921e-10	3.1010e+04	2.7455e+04	1.0006e+04	9.9737e+03	4.9543e+04	8.9896e+04	4.6107e+04	8.4114e+04	3.2967
5.0271e-09	4.7795e-09	5.1466e-10	4.5315e-10	9.8607e-10	3.2977e+04	2.6552e+04	9.0188e+03	1.0357e+04	5.0093e+04	8.6211e+04	4.6555e+04	7.7647e+04	3.2967
4.6793e-09	5.0462e-09	4.4473e-10	4.5609e-10	1.0677e-09	3.4564e+04	2.4674e+04	1.0379e+04	9.2701e+03	4.9099e+04	7.6377e+04	4.5748e+04	7.8645e+04	3.2967
5.0483e-09	4.9552e-09	4.8731e-10	4.3147e-10	1.0030e-09	2.9471e+04	2.4685e+04	9.9924e+03	8.3580e+03	4.2518e+04	8.4624e+04	4.6690e+04	8.3352e+04	3.2967
4.9909e-09	3.8761e-09	5.1489e-10	4.6288e-10	1.0878e-09	2.9973e+04	2.2938e+04	9.2180e+03	9.6786e+03	4.1889e+04	7.9124e+04	5.0442e+04	8.0718e+04	3.2967
4.6045e-09	4.4561e-09	4.8994e-10	3.9625e-10	1.0736e-09	3.0684e+04	2.3369e+04	9.9911e+03	1.0380e+04	4.8747e+04	8.0379e+04	4.8070e+04	8.8383e+04	3.2967
4.9791e-09	4.7978e-09	4.5196e-10	4.5690e-10	9.7249e-10	3.2248e+04	2.3539e+04	8.6488e+03	9.3350e+03	4.6258e+04	8.6390e+04	4.8975e+04	8.1355e+04	3.2967
4.3946e-09	4.5469e-09	4.9105e-10	4.7953e-10	1.0106e-09	3.2332e+04	2.6974e+04	9.7725e+03	1.0829e+04	4.4345e+04	8.0011e+04	4.4702e+04	7.2473e+04	3.2967
4.7788e-09	4.6458e-09	4.3539e-10	4.4964e-10	1.0077e-09	2.8763e+04	2.6750e+04	9.0189e+03	1.0698e+04	4.5962e+04	8.4328e+04	4.5154e+04	8.1581e+04	3.2967
4.3845e-09	4.7888e-09	4.6436e-10	4.7742e-10	1.1159e-09	3.2780e+04	2.5639e+04	1.0088e+04	8.2061e+03	4.6986e+04	8.3522e+04	4.7810e+04	8.6591e+04	3.2967
4.6665e-09	4.3919e-09	5.1893e-10	4.5770e-10	1.0162e-09	3.2346e+04	2.4212e+04	1.0001e+04	9.8302e+03	4.9375e+04	8.5363e+04	4.5379e+04	7.5351e+04	3.2967
4.8705e-09	4.9859e-09	4.6945e-10	5.2516e-10	1.0231e-09	3.1680e+04	2.5034e+04	1.1216e+04	9.4176e+03	4.9479e+04	8.4487e+04	5.3524e+04	8.3523e+04	3.2967
4.5380e-09	4.6104e-09	5.1557e-10	4.8374e-10	1.0591e-09	3.4352e+04	2.5074e+04	9.4252e+03	1.0089e+04	4.8627e+04	7.8941e+04	4.5089e+04	7.9576e+04	3.2967
4.6173e-09	5.3467e-09	4.6025e-10	4.4709e-10	1.1812e-09	3.2267e+04	2.5632e+04	9.3704e+03	1.0047e+04	4.7815e+04	7.9238e+04	4.4242e+04	8.6620e+04	3.2967
4.4896e-09	4.7522e-09	4.6530e-10	4.9565e-10	9.7048e-10	3.1904e+04	2.4809e+04	1.1091e+04	1.0027e+04	4.4777e+04	7.4342e+04	4.7523e+04	7.9709e+04	3.2967
4.8303e-09	4.3998e-09	5.4174e-10	4.8051e-10	9.7466e-10	3.2048e+04	2.5640e+04	9.5605e+03	9.8803e+03	4.4710e+04	6.8110e+04	4.2580e+04	7.9609e+04	3.2967

Fig 6.4 Generation of Values for Sensitivity Analysis

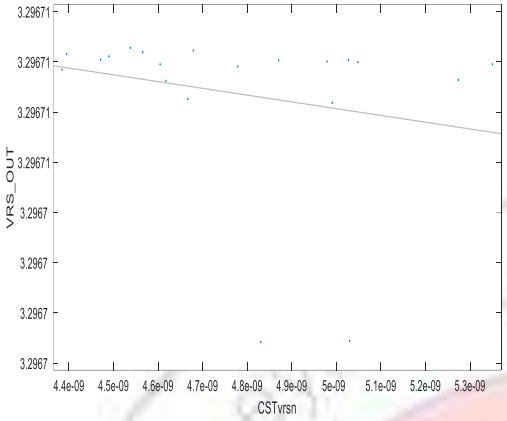

Fig 6.5 CSTvrsn vs VRS_OUT

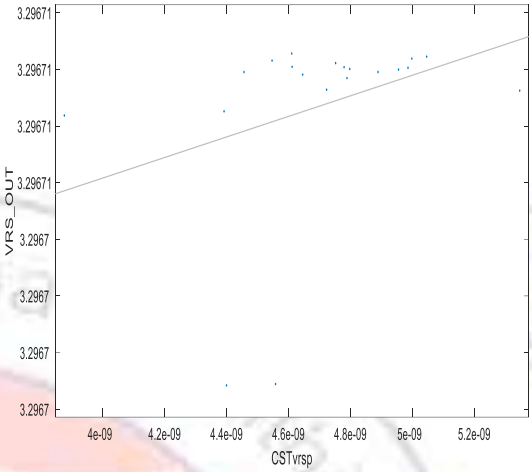

Fig 6.6 CSTvrsp vs VRS_OUT

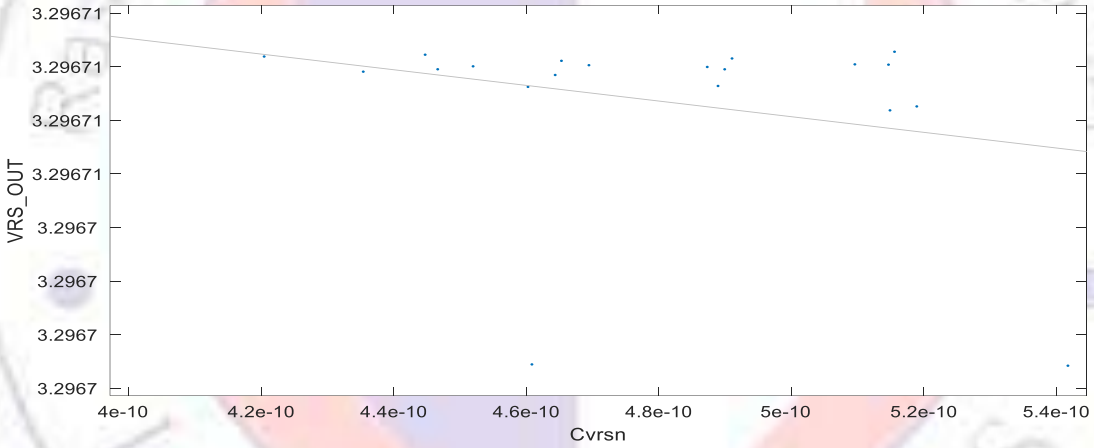

Fig 6.7 Cvrsn vs VRS_OUT

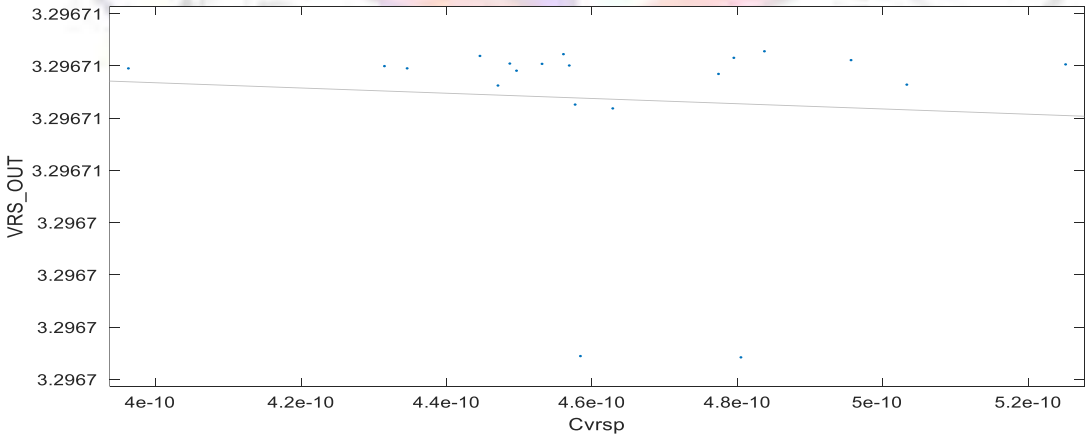

Fig 6.8 Cvrsp vs VRS_OUT

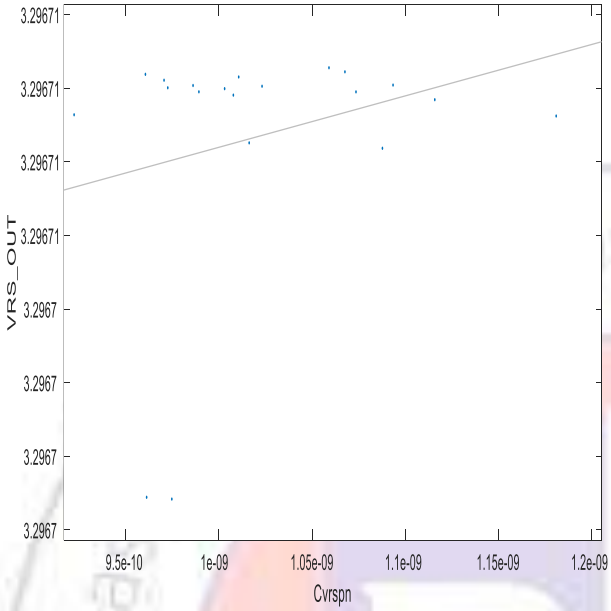

Fig 6.9 Cvrspn vs VRS_OUT

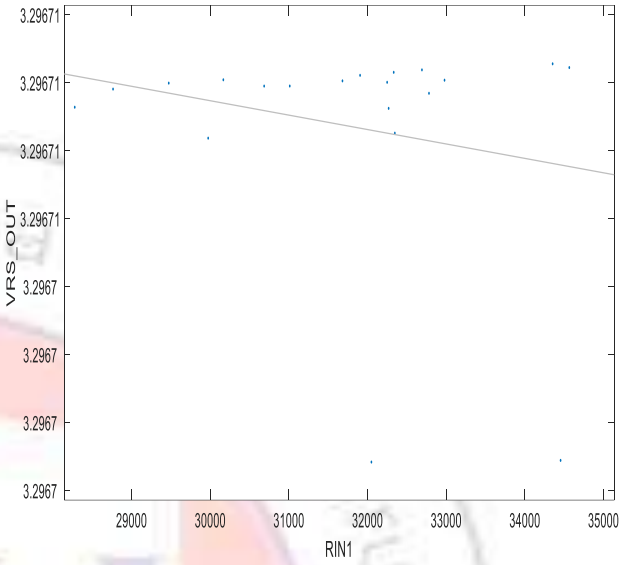

Fig 6.10 RIN1 vs VRS_OUT

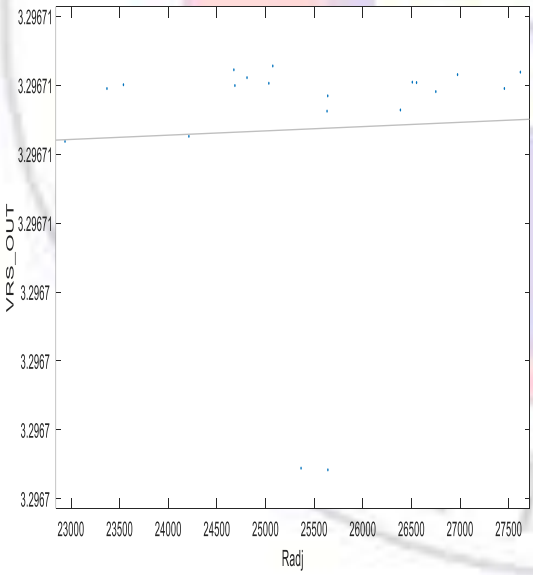

Fig 6.11 Radj vs VRS_OUT

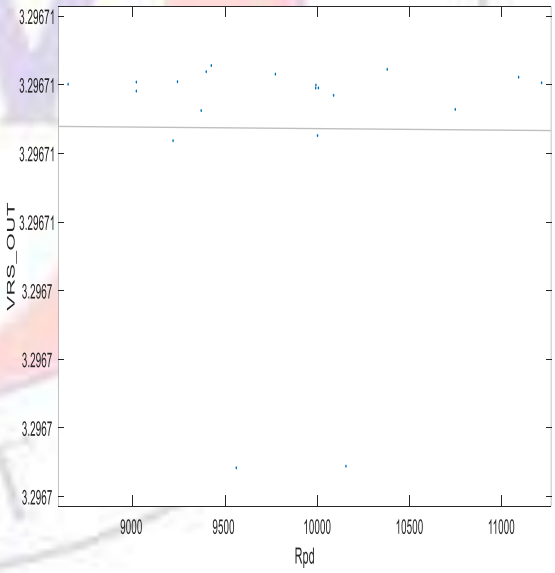

Fig 6.12 Rpd vs VRS_OUT

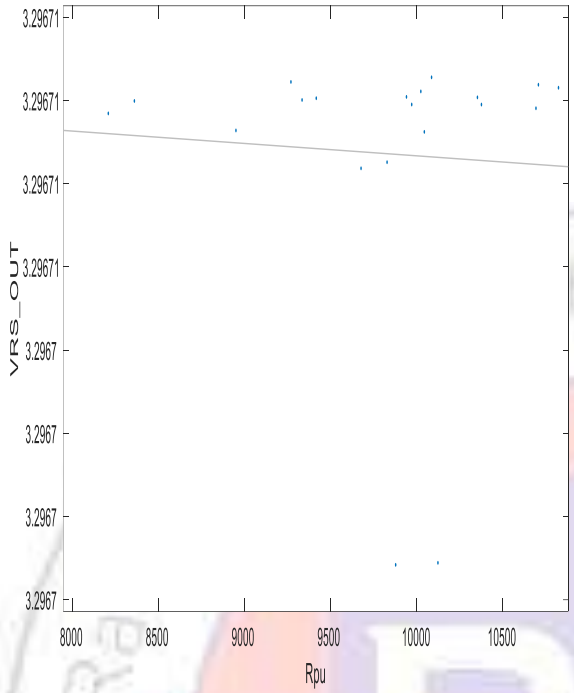

Fig 6.13 Rpu vs VRS_OUT

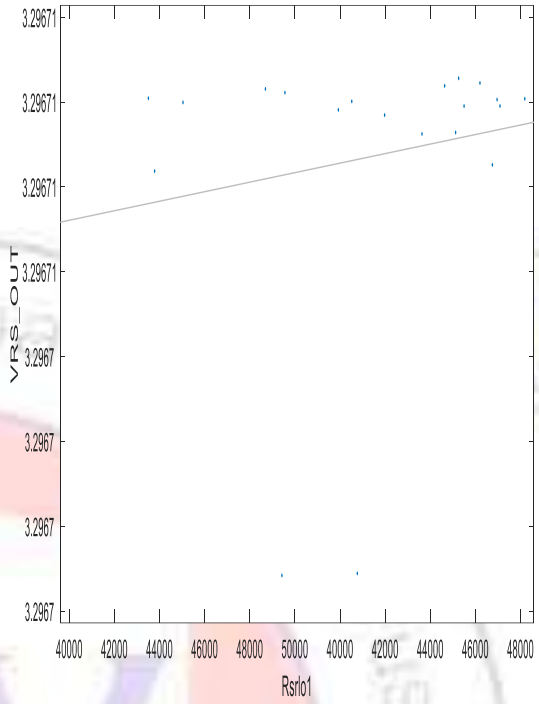

Fig 6.14 Rsrlo1 vs VRS_OUT

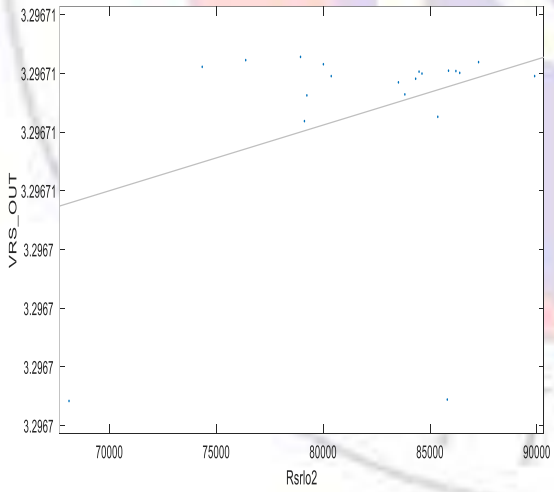

Fig 6.15 Rsrlo2 vs VRS_OUT

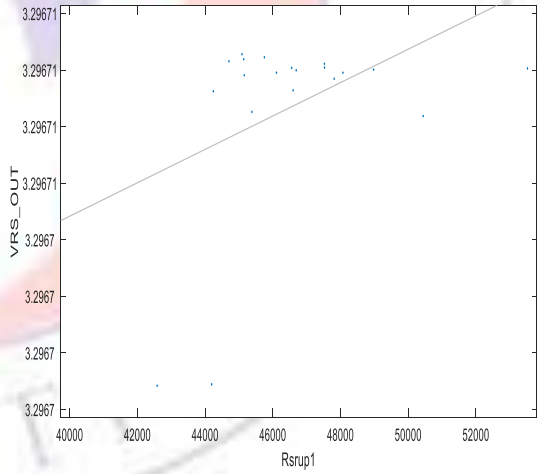

Fig 6.16 Rsrup1 vs VRS_OUT

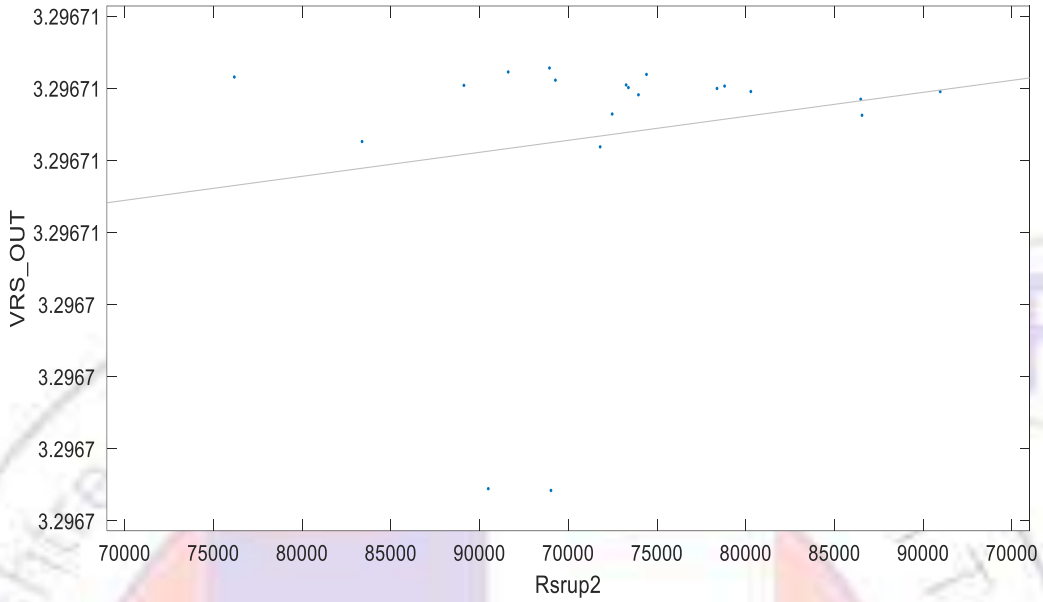

Fig 6.17 Rsrup2 vs VRS_OUT

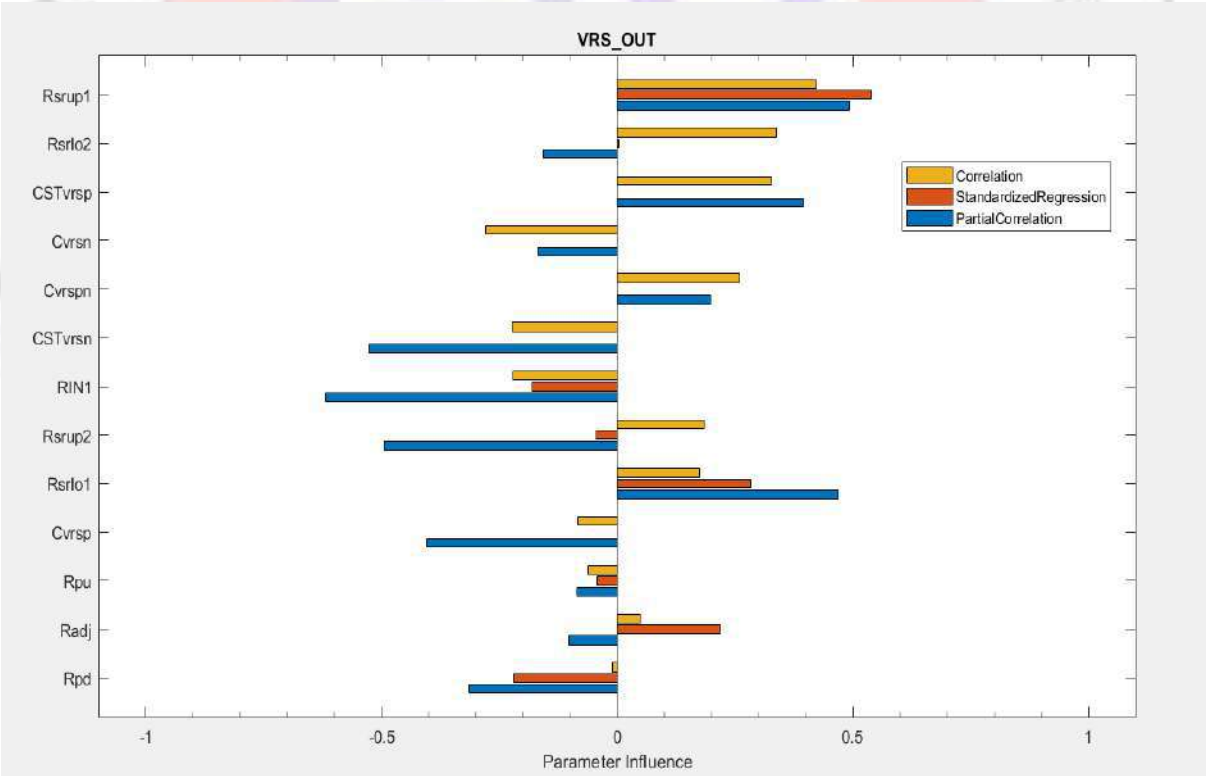

Fig 6.18 Components influence on Output Voltage

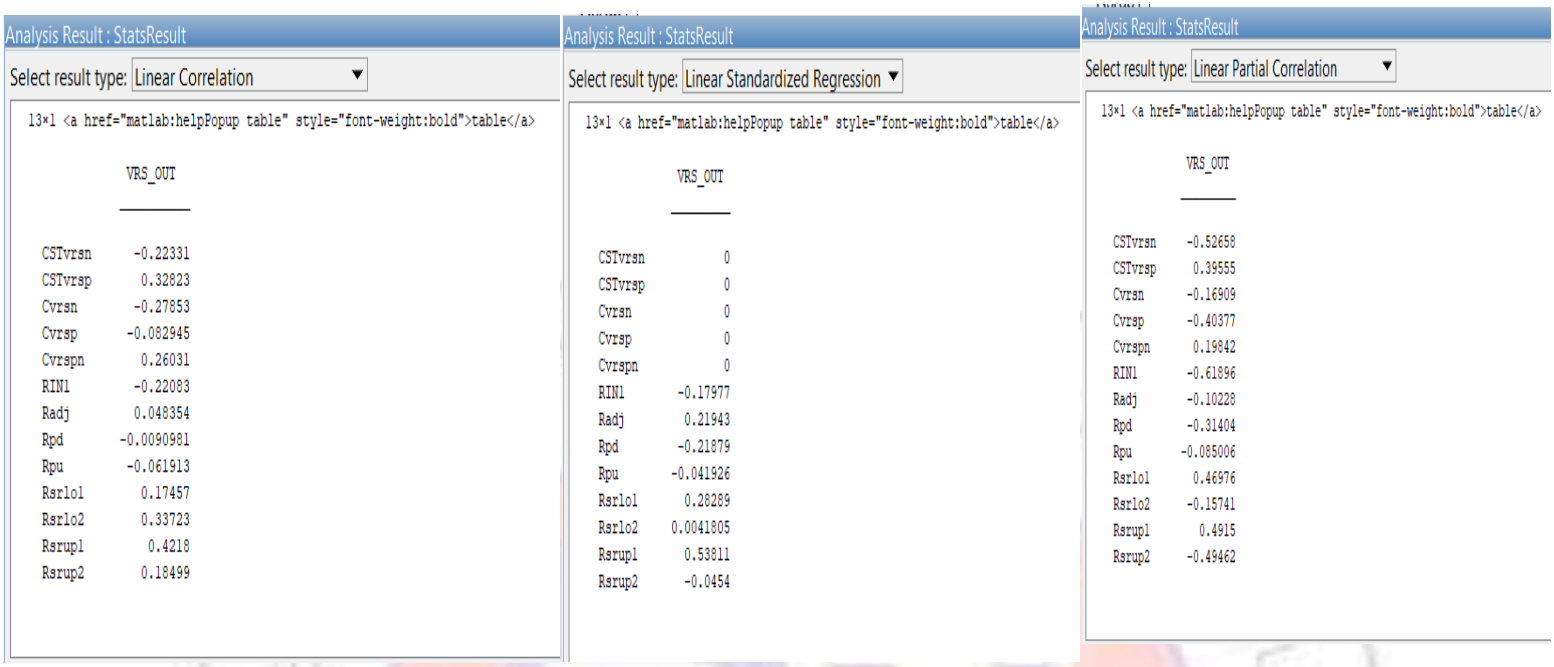

Fig 6.19 Statistical Data for Sensitivity Analysis

6.4 Inductive Sensor Interfacing

The waveforms of VRSP, VRSN and VRS_OUT are shown in Fig 6.20. In VRSP and VRSN waveforms, the current source is charged to 6uA pull up and discharges to 6uA pull down and both the waveforms are sinusoidal in nature. The signals VRSP and VRSN are compared with the reference signal, there by rectangular digital pulses are generated at VRS_OUT pin. The average output voltage obtained is 3.3 V.

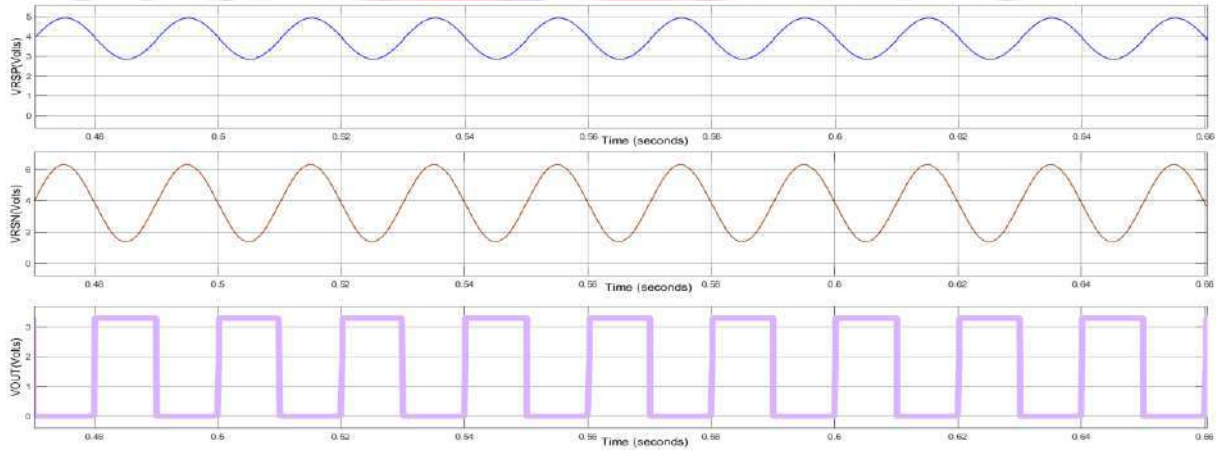

Fig 6.20 Waveforms of Inductive Sensor Interfacing

6.4.1 Monte Carlo Result

The Inductive sensor measures the speed of the camshaft. The measured pulse width from Monte Carlo histogram is a measure of camshaft speed. The histogram indicates the boundary values. The measured engine speed lies between minimum and maximum value. From histogram distribution, it can be understood that the average pulse width is 84.26*10^(-8) sec which implies that average rpm of the camshaft would be equivalent to 84.26*10^(-8) sec. The pulse width is also a measure of life cycle of camshaft rpm. The measured 3 sigma value indicates that 99.7% of the values will lie within three standard deviations from the average pulse width value which means that for all 1000 runs, the resulted output is 99.7% accurate. The Histogram view for Monte Carlo run of 1000 runs is shown in Fig 6.21.

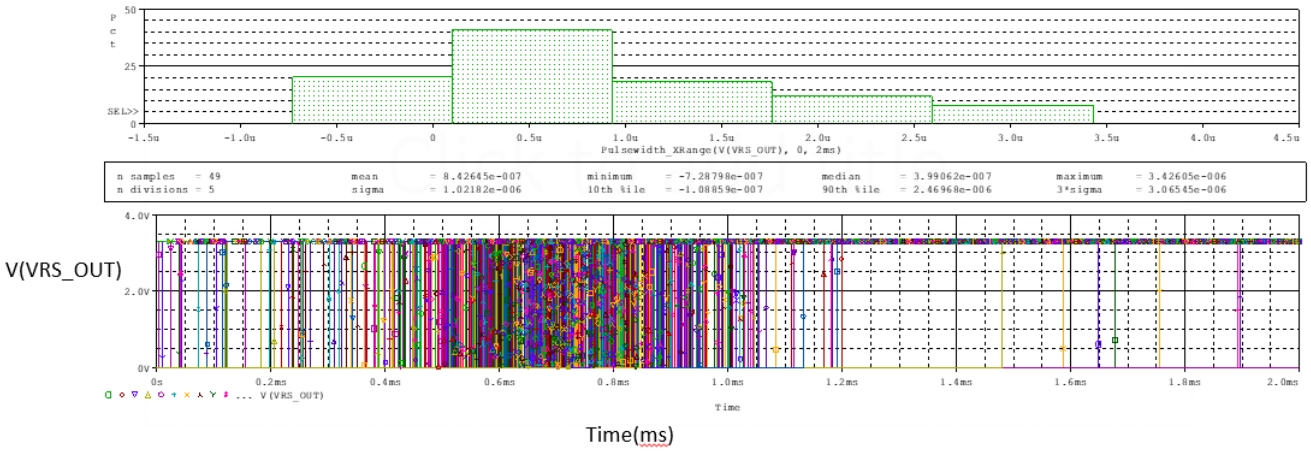

Fig 6.21 Monte Carlo Histogram distribution for pulse width measurement

6.4.2 Sensitivity Analysis Result

Fig 6.22 and Fig 6.23 show the process of generating the values for Sensitivity Analysis of Inductive Sensor interfacing. Fig 6.30, Fig 6.31, Fig 6.34 and Fig 6.35 show that the components Radj, Rpd, Rsrlo2 and Rsrup2 have perfectly negative correlationship with respect to variation in output voltage. Fig 6.24 and Fig 6.29 show that the components CSTvrsn and RIN1 have high negative correlation with respect to variation in output voltage. Fig 6.35 shows that the component Rsrup1 has perfectly positive correlationship with respect to variation in output voltage. Fig 6.25, Fig 6.26 show that CSTvrsp and Cvrsn have high positive correlation with respect to variation in output voltage. Fig 6.27, Fig 6.28, Fig 6.33 show that the components Cvrsp, Cvrspn, Rsrlo1 have low positive correlationship with respect to variation in output voltage. Fig 6.32 indcates that the component Rpu has no correlation with respect to output voltage. Fig 6.37

gives an instance of tornado plot representing the percentage contribution of each component to output voltage measured in terms of regression, standardized regression and partial correlation. Fig 6.38 represents the numerical data generated showing the sensitivity of each component to the output voltage measured interms of linear correlation, linear standardized regression, linear partial correlation.

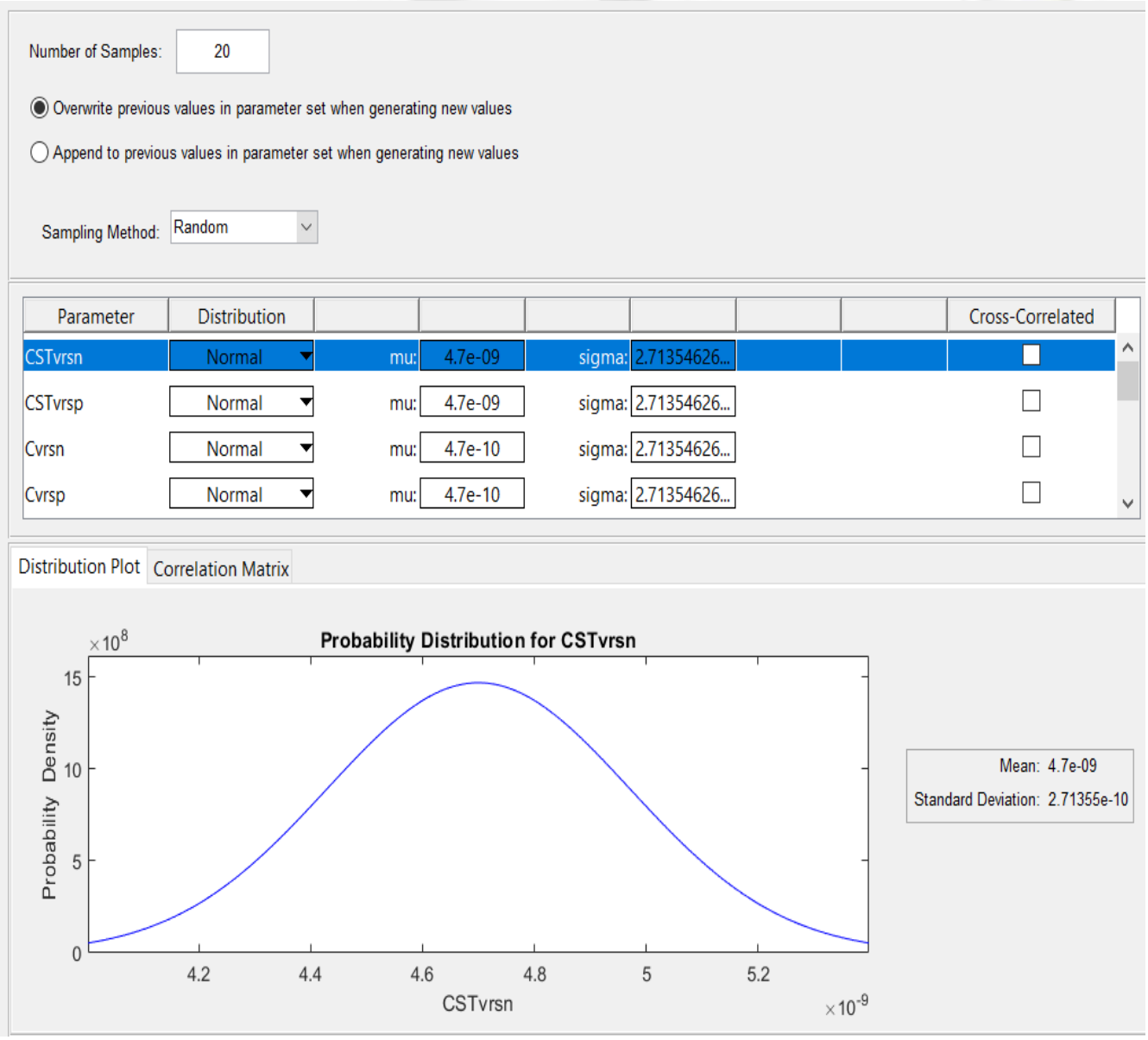

Fig 6.22 Sensitivity Analysis for Inductive Sensor Interfacing

CSTvrsn	CSTvrsp	Cvrsn	Cvrsp	Cvrspn	RIN1	Radj	Rpd	Rpu	Rsrlo1	Rsrlo2	Rsrup1	Rsrup2	VRS_OUT_1
4.9927e-09	4.6158e-09	4.5412e-10	4.7238e-10	9.6085e-10	2.9689e+04	2.8615e+04	1.0818e+04	1.0717e+04	4.3232e+04	8.0544e+04	4.6423e+04	7.7405e+04	3.2967
5.0216e-09	4.7311e-09	4.7424e-10	4.7437e-10	1.0543e-09	3.1755e+04	2.6874e+04	9.4188e+03	1.0676e+04	5.1661e+04	7.5489e+04	4.5845e+04	7.5638e+04	3.2967
4.7981e-09	5.1241e-09	4.2941e-10	4.4889e-10	1.0187e-09	2.7589e+04	2.7251e+04	9.9404e+03	9.4402e+03	4.4386e+04	8.3722e+04	4.1553e+04	8.0286e+04	3.2967
4.4340e-09	4.7977e-09	4.3500e-10	4.4200e-10	1.0124e-09	3.3524e+04	2.7325e+04	1.0575e+04	9.4169e+03	4.6365e+04	8.6596e+04	4.7089e+04	8.5637e+04	3.2967
5.2415e-09	5.0339e-09	4.5358e-10	4.6151e-10	9.7148e-10	2.8942e+04	2.4165e+04	1.0030e+04	1.1224e+04	4.2913e+04	8.5498e+04	4.9877e+04	8.5706e+04	3.2967
5.2799e-09	4.5500e-09	4.6069e-10	4.8343e-10	1.0072e-09	3.1612e+04	2.8779e+04	9.7759e+03	1.0628e+04	4.6533e+04	8.0023e+04	4.6472e+04	8.1953e+04	3.2967
4.5731e-09	4.5516e-09	4.6596e-10	4.8702e-10	1.0235e-09	3.4938e+04	2.7328e+04	9.5423e+03	9.5907e+03	4.4459e+04	8.3435e+04	4.3967e+04	7.7478e+04	3.2967
4.2237e-09	4.1609e-09	4.9154e-10	4.5589e-10	9.0896e-10	3.0066e+04	2.6606e+04	9.8091e+03	9.7800e+03	4.3606e+04	7.5560e+04	4.6505e+04	8.1318e+04	3.2967
4.7498e-09	4.5892e-09	4.6483e-10	4.4667e-10	1.0123e-09	3.2381e+04	2.7154e+04	1.1310e+04	9.0804e+03	4.4484e+04	7.6033e+04	4.7156e+04	8.1421e+04	3.2967
4.9357e-09	4.9223e-09	5.1503e-10	4.6723e-10	1.0147e-09	3.3105e+04	2.4418e+04	9.8778e+03	1.0792e+04	4.5458e+04	7.7756e+04	4.9969e+04	8.4256e+04	3.2967
4.3464e-09	4.3515e-09	4.5324e-10	4.4773e-10	9.7335e-10	2.9264e+04	2.6972e+04	9.6813e+03	9.6129e+03	4.2050e+04	8.1496e+04	4.4708e+04	7.2577e+04	3.2967
4.7237e-09	4.1833e-09	4.6898e-10	4.1892e-10	9.7542e-10	3.0579e+04	2.7424e+04	9.7502e+03	9.5568e+03	4.9013e+04	7.6794e+04	5.0355e+04	7.6024e+04	3.2967
4.8340e-09	4.6347e-09	4.3155e-10	4.2104e-10	9.0578e-10	3.1620e+04	2.7097e+04	1.0066e+04	1.0602e+04	4.5843e+04	8.7667e+04	5.0177e+04	8.7108e+04	3.2967
5.0143e-09	4.3280e-09	4.8082e-10	4.2945e-10	1.0133e-09	3.0885e+04	2.3877e+04	1.0285e+04	1.0570e+04	4.2723e+04	8.4747e+04	4.4180e+04	8.3183e+04	3.2967
4.6642e-09	4.6751e-09	4.2068e-10	4.6984e-10	9.4995e-10	3.1394e+04	2.7619e+04	9.8992e+03	9.7653e+03	4.6539e+04	7.0246e+04	4.7163e+04	8.0991e+04	3.2967
5.0770e-09	5.1582e-09	4.8812e-10	4.4264e-10	1.0491e-09	3.1544e+04	2.2695e+04	9.8856e+03	9.2782e+03	4.7848e+04	8.4432e+04	4.5743e+04	8.6455e+04	3.2967
4.3437e-09	4.9082e-09	4.5526e-10	4.7976e-10	9.5703e-10	3.0948e+04	2.7030e+04	9.7943e+03	9.5111e+03	4.2381e+04	8.7540e+04	4.9126e+04	8.0939e+04	3.2967
4.8979e-09	4.6180e-09	4.6480e-10	4.8987e-10	1.0948e-09	3.2317e+04	2.6532e+04	9.8478e+03	1.0221e+04	4.3171e+04	9.0247e+04	4.7152e+04	8.2691e+04	3.2967
4.8072e-09	4.5928e-09	4.5128e-10	4.7816e-10	9.8207e-10	3.1066e+04	2.5124e+04	9.7415e+03	1.0281e+04	5.1083e+04	9.0352e+04	4.4874e+04	7.9090e+04	3.2967
4.8073e-09	4.9878e-09	4.3131e-10	4.8053e-10	9.8890e-10	3.0305e+04	2.6466e+04	1.0847e+04	1.0544e+04	4.0675e+04	8.7360e+04	4.7706e+04	8.8392e+04	3.2967

Fig 6.23 Generation of Values for Sensitivity Analysis

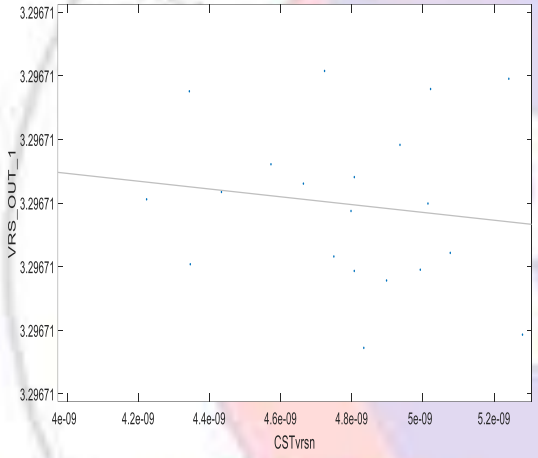

Fig 6.24 CSTvrsn vs VRS_OUT_1

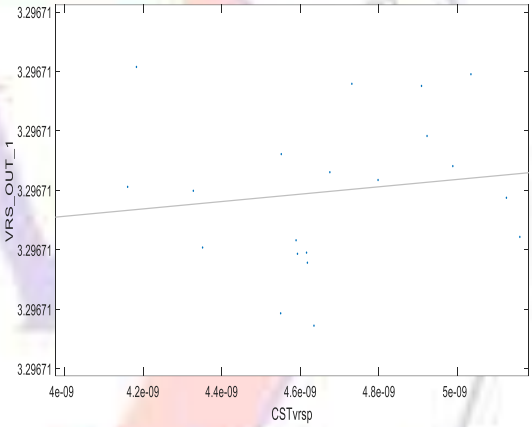

Fig 6.25 CSTvrsp vs VRS_OUT_1

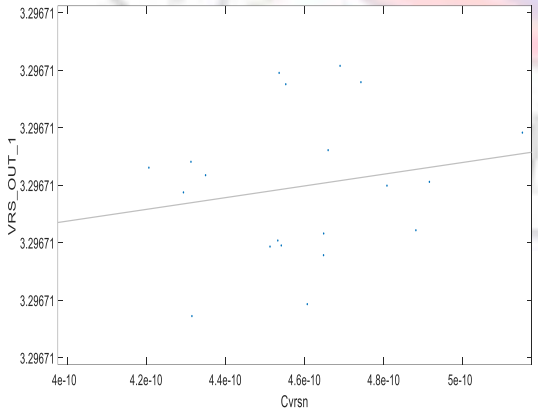

Fig 6.26 Cvrsn vs VRS_OUT_1

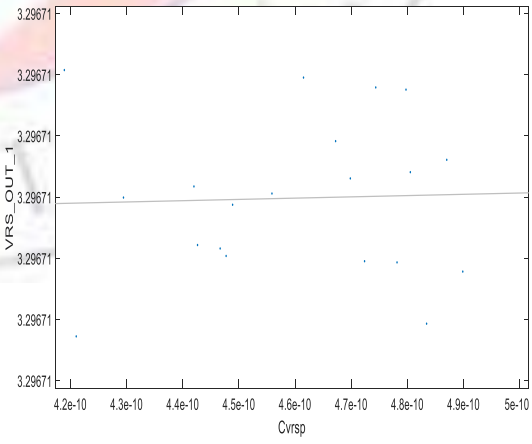

Fig 6.27 Cvrsp vs VRS_OUT_1

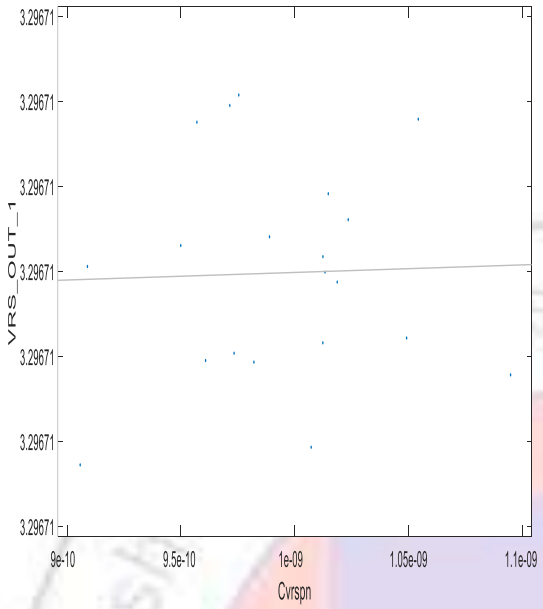

Fig 6.28 Cvrspn vs VRS_OUT_1

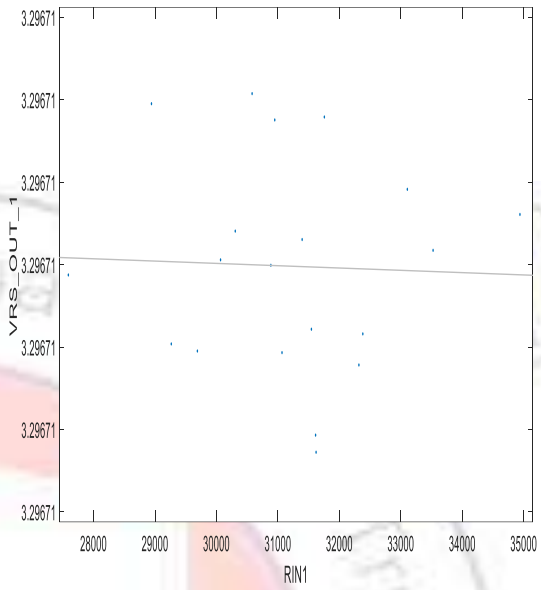

Fig 6.29 RIN1 vs VRSP_OUT_1

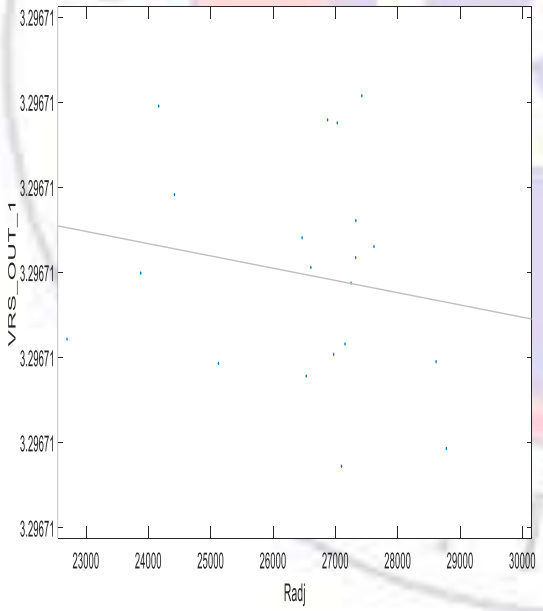

Fig 6.30 Radj vs VRS_OUT_1

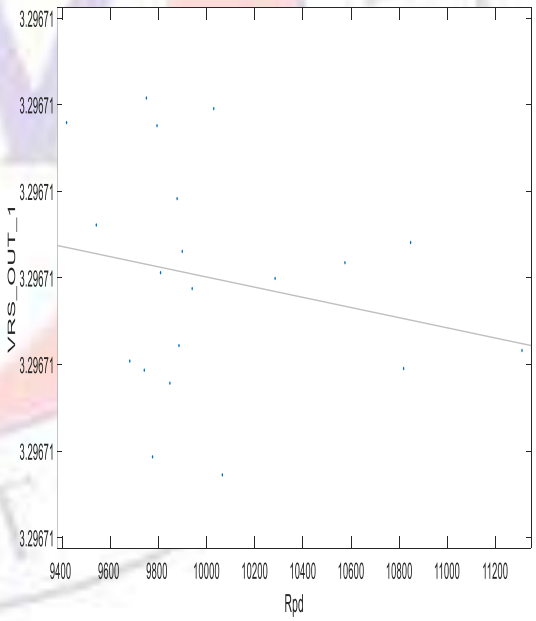

Fig 6.31 Rpd vs VRS_OUT_1

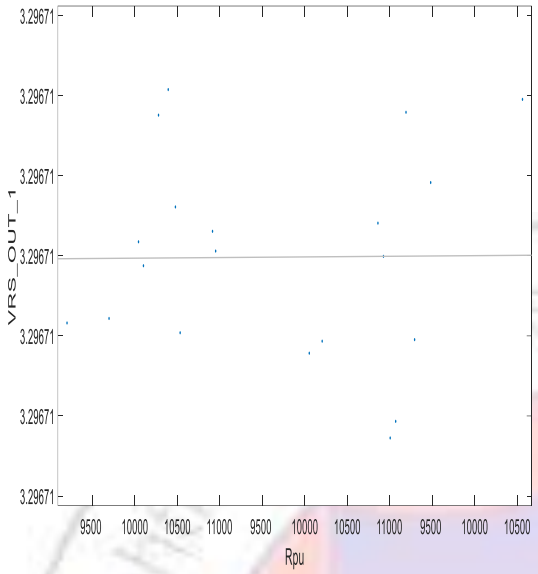

Fig 6.32 Rpu vs VRS_OUT_1

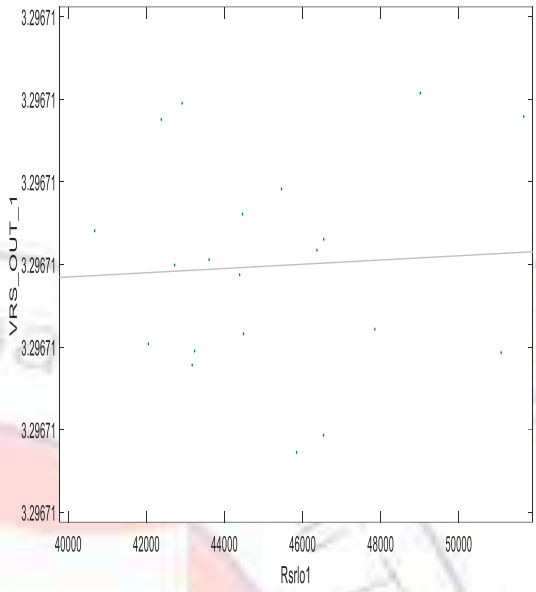

Fig 6.33 Rsrlo1 vs VRS_OUT_1

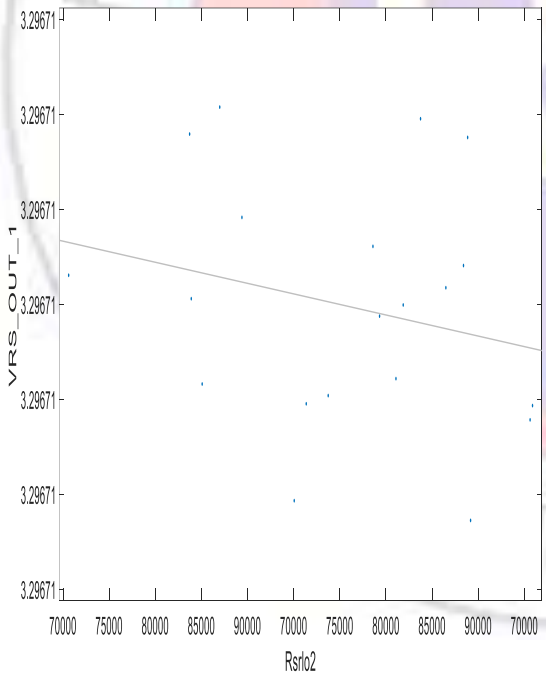

Fig 6.34 Rsrlo2 vs VRS_OUT_1

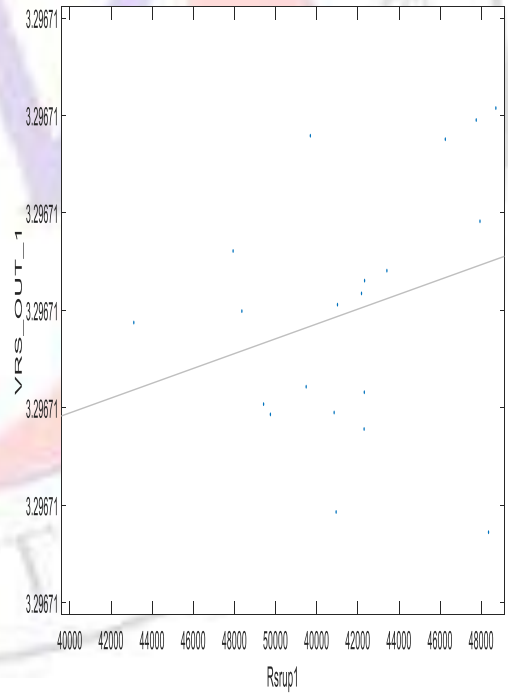

Fig 6.35 Rsrup1 vs VRS_OUT_1

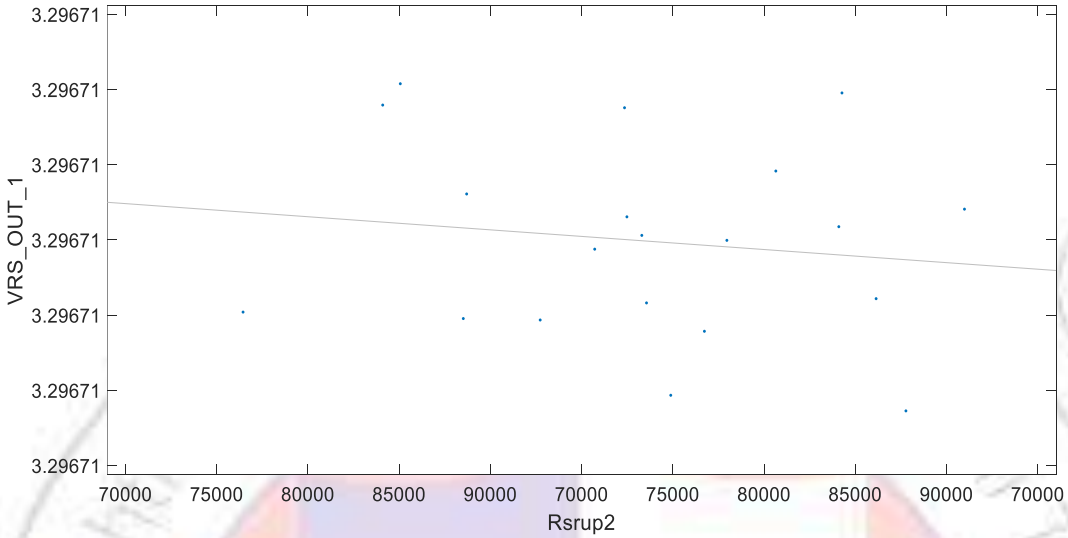

Fig 6.36 Rsrup2 vs VRS_OUT_1

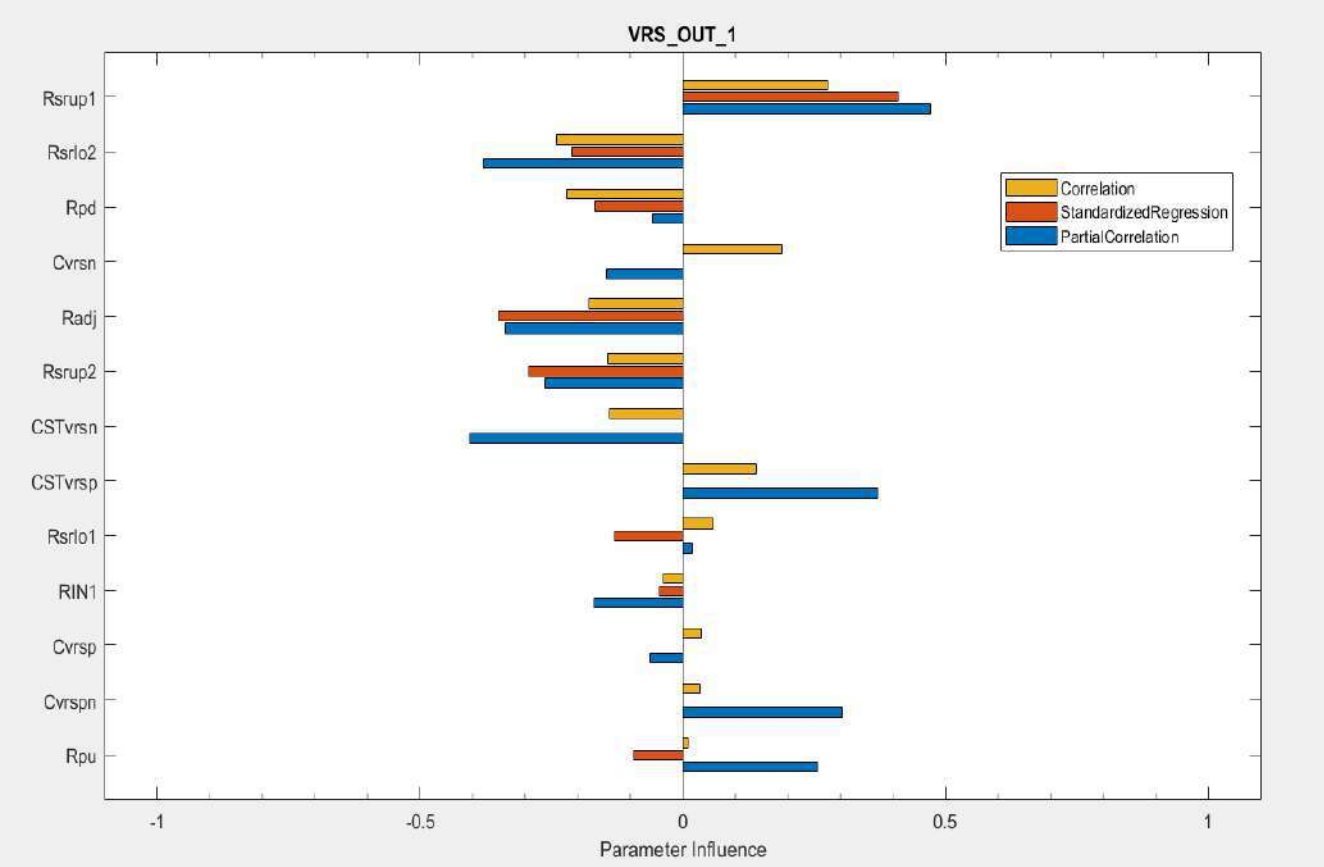

Fig 6.37 Components influence on Output Voltage

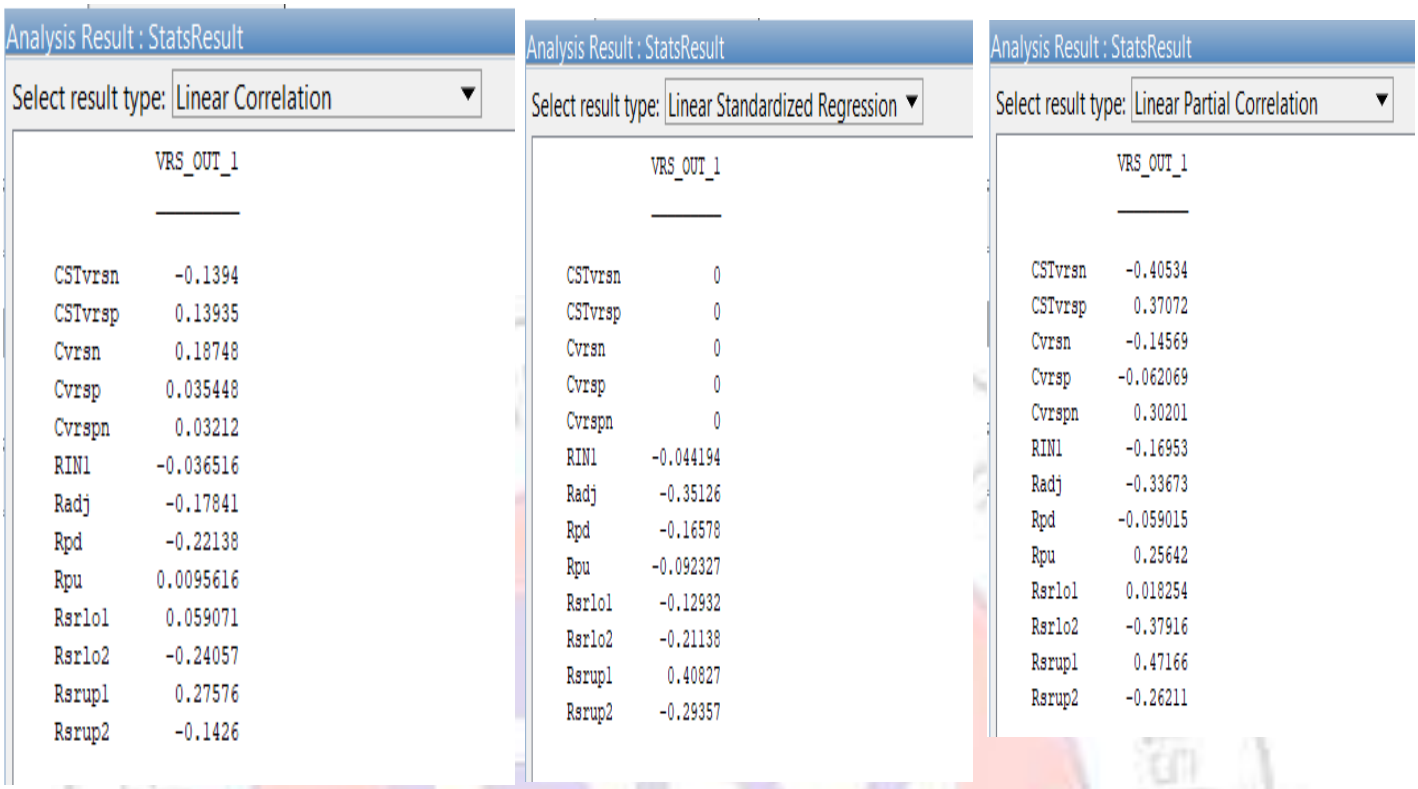

Fig 6.38 Statistical Data for Sensitivity Analysis

6.5 Push Pull type Sensor Interfacing

The waveforms of VRSP, VRSN and VRS_OUT are shown in Fig 6.39. In VRSP and VRSN waveforms, the current source is charged to 6uA pull up and discharges to 6uA pull down and both the waveforms are pulsating in nature. The signals VRSP and VRSN are compared with the reference signal, there by rectangular digital pulses are generated at VRS_OUT pin. The average output voltage obtained is 3.3 V.

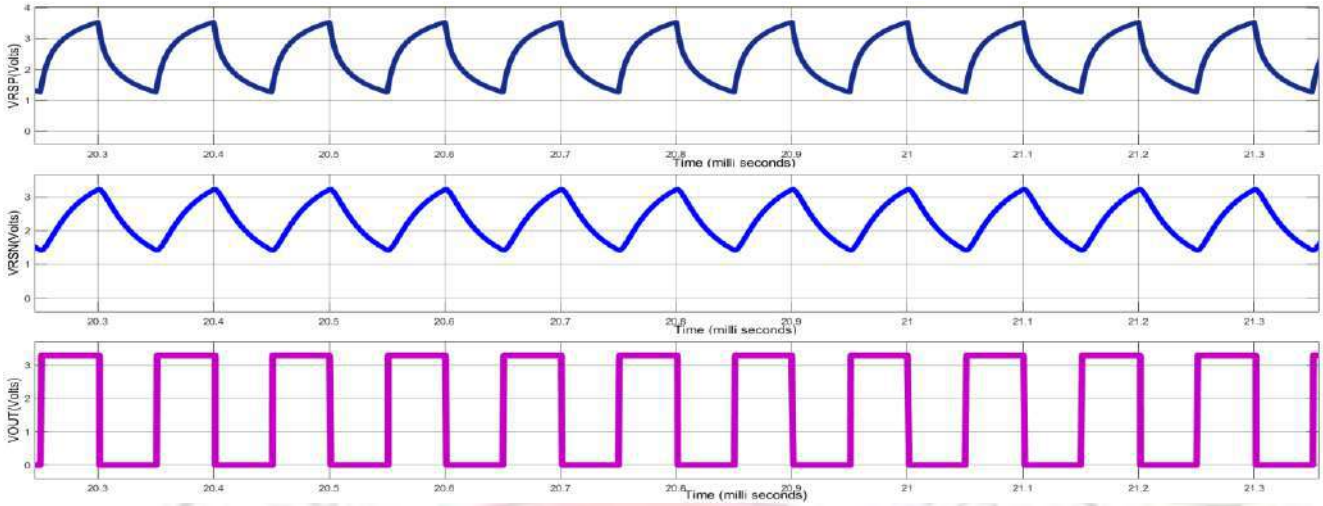

Fig 6.39 Waveforms of Push Pull type Sensor Interfacing

6.5.1 Monte Carlo Result

The Push pull type sensor measures the analog parameter such as temperature. The histogram plot of Monte Carlo Run is shown in Fig 6.40. The measured pulse width from Monte Carlo histogram is an implication of healthiness of the sensor. The histogram indicates the boundary values. The measured temperature lies between initial and final value. From histogram distribution, it can be understood that the average pulse width is 58.07 usec which implies that average feasible temperature at which the engine would operate would be equivalent to 58.07 usec. The pulse width is also a measure of life cycle of engine. The measured 3 sigma value indicates that 99.7% of the values will lie within three standard deviations from the average pulse width value which means that for all 1000 runs, the resulted output is 99.7% accurate.

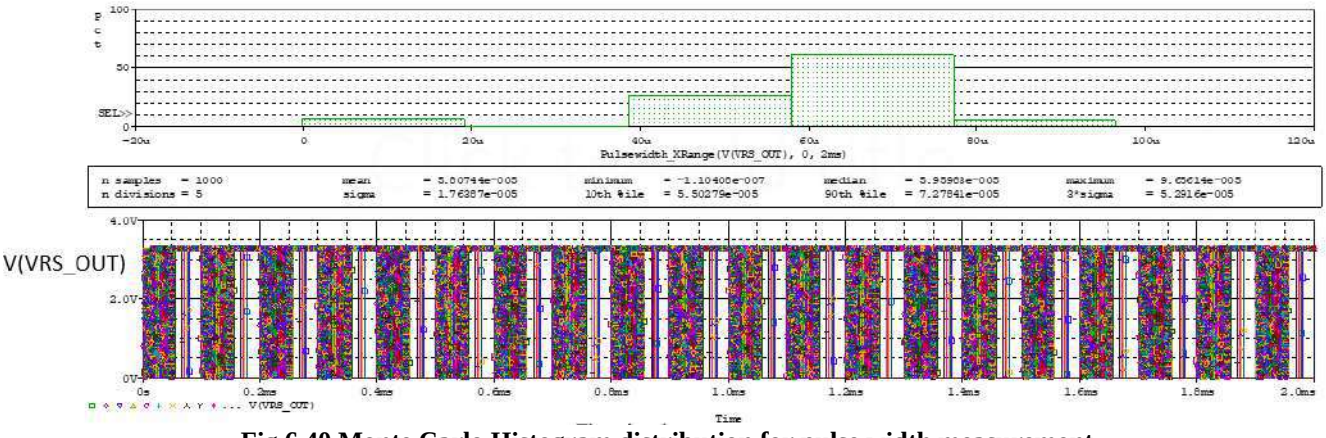

Fig 6.40 Monte Carlo Histogram distribution for pulse width measurement

6.5.2 Sensitivity Analysis Result

Fig 6.41 and Fig 6.42 show the process of generating the values for Sensitivity Analysis of Push Pull type Sensor interfacing. Fig 6.49, Fig 6.51 show that the components Cvrspn, Rsrlo2 have perfectly negative correlationship with respect to variation in output voltage. Fig 6.49 and Fig 6.51 show that the components Radj and Rpu have high negative correlation with respect to variation in output voltage. Fig 6.46 show that Cvrsp has low negative correlation with respect to variation in output voltage. Fig 6.43, Fig 6.44, Fig 6.45, Fig 6.48, Fig 6.54 show that the components CSTvrsn, CSTvrsn, Cvrsn, RIN1 Rsrup1 have perfectly positive correlation with respect to variation in output voltage. Fig 6.50, Fig 6.52 indcate that the components Rpd and Rsrlo1 have low positive correlation with respect to output voltage. Fig 6.56 gives an instance of tornado plot representing the percentage contribution of each component to output voltage measured in terms of regression, standardized regression and partial correlation. Fig 6.57 represents the numerical data generated showing the sensitivity of each component to the output voltage measured interms of linear correlation, linear standardized regression, linear partial correlation.

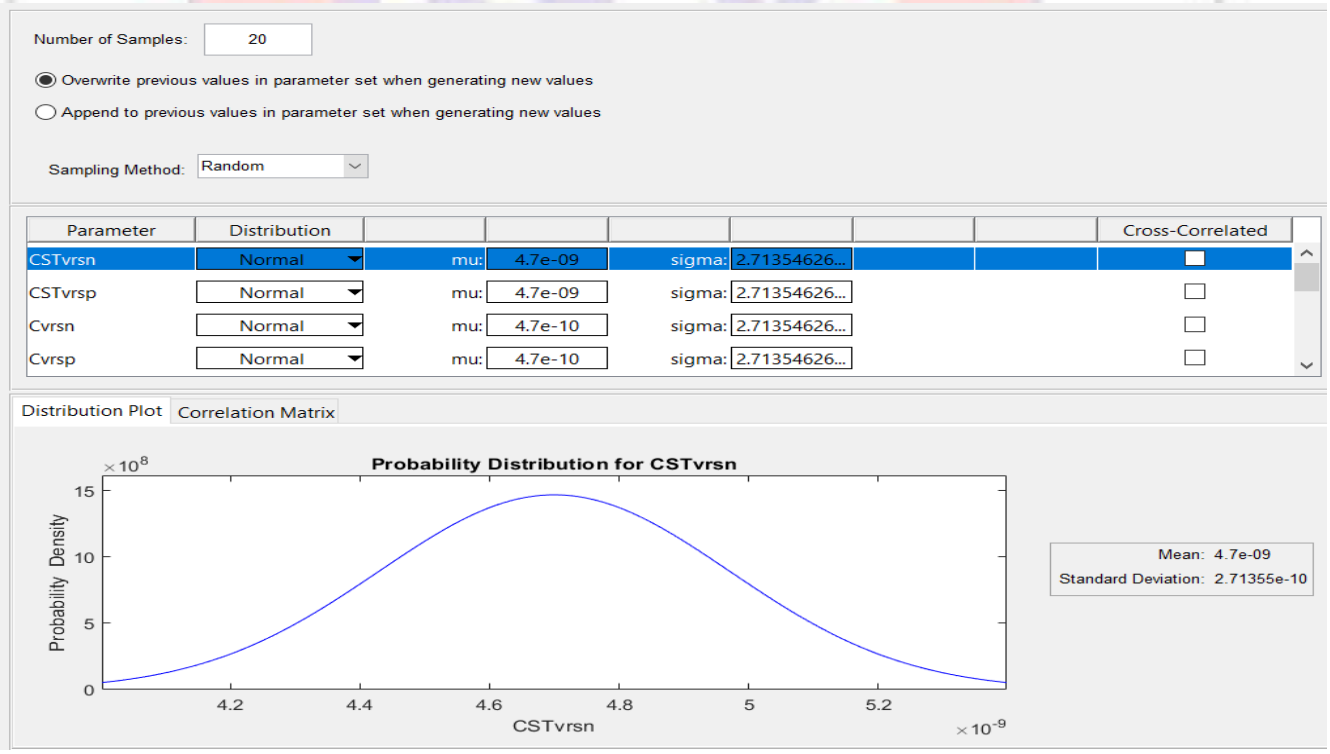

Fig 6.41 Sensitivity Analysis for Push Pull type Sensor Interfacing

CSTvrsn	CSTvrsp	Cvrsn	Cvrsp	Cvrspn	RIN1	Radj	Rpd	Rpu	Rsrlo1	Rsrlo2	Rsrup1	Rsrup2
4.5690e-09	4.5020e-09	4.3997e-10	4.5824e-10	1.0256e-09	3.3359e+04	2.5049e+04	9.5495e+03	1.0403e+04	5.0564e+04	8.2292e+04	4.9923e+04	8.5788e+04
4.4176e-09	4.5638e-09	4.4693e-10	4.9249e-10	1.0284e-09	3.4042e+04	2.8434e+04	1.0556e+04	1.0873e+04	4.3120e+04	8.6888e+04	4.7082e+04	8.0677e+04
4.6357e-09	4.7288e-09	4.2649e-10	5.2325e-10	1.0257e-09	3.3315e+04	2.4853e+04	9.7452e+03	1.0436e+04	4.4511e+04	8.4924e+04	4.5878e+04	9.1161e+04
4.5816e-09	4.5794e-09	4.8450e-10	4.8257e-10	1.0093e-09	3.3986e+04	2.6805e+04	9.0436e+03	8.5407e+03	4.4095e+04	8.6221e+04	4.7625e+04	8.9972e+04
5.2169e-09	4.8455e-09	5.1090e-10	4.5223e-10	9.8759e-10	3.2754e+04	2.4923e+04	1.0106e+04	1.0007e+04	5.5858e+04	7.1820e+04	4.0651e+04	8.3152e+04
4.8865e-09	4.6458e-09	5.2035e-10	4.3891e-10	9.8319e-10	3.0880e+04	2.5805e+04	1.0403e+04	1.0359e+04	4.4174e+04	7.4976e+04	5.1402e+04	7.9430e+04
5.0691e-09	5.1307e-09	4.7881e-10	5.0269e-10	1.0335e-09	3.2163e+04	2.5636e+04	9.6996e+03	1.0010e+04	4.2837e+04	8.0738e+04	4.7156e+04	7.8327e+04
4.5331e-09	4.7615e-09	4.3944e-10	4.3987e-10	1.0681e-09	2.9841e+04	2.5067e+04	9.8366e+03	1.0278e+04	4.3001e+04	8.4645e+04	4.5106e+04	9.0800e+04
4.2698e-09	4.4336e-09	4.8034e-10	4.2511e-10	9.9319e-10	3.1516e+04	2.6119e+04	1.1805e+04	1.0279e+04	4.7709e+04	7.1125e+04	4.7736e+04	8.0277e+04
4.4499e-09	4.9338e-09	4.6802e-10	4.5951e-10	1.0666e-09	3.0414e+04	2.5446e+04	9.6522e+03	9.6070e+03	4.3173e+04	7.3710e+04	4.4658e+04	7.6734e+04
4.7107e-09	4.5684e-09	4.7237e-10	5.1091e-10	1.0108e-09	3.1032e+04	2.6248e+04	1.0414e+04	9.7059e+03	4.5566e+04	8.2856e+04	4.4266e+04	8.3358e+04
4.4288e-09	4.4301e-09	4.4190e-10	4.7628e-10	1.0334e-09	2.9304e+04	2.6350e+04	9.6143e+03	1.0208e+04	4.6912e+04	8.4010e+04	4.6744e+04	8.4923e+04
5.0181e-09	4.6599e-09	4.3225e-10	4.5423e-10	9.4910e-10	3.0816e+04	2.4064e+04	1.0643e+04	1.0130e+04	4.8132e+04	7.9609e+04	4.8412e+04	7.8046e+04
4.8248e-09	4.2270e-09	4.5974e-10	4.7466e-10	1.0239e-09	2.7502e+04	2.4862e+04	1.0186e+04	1.0984e+04	4.9719e+04	8.2036e+04	4.7509e+04	8.0607e+04
5.2872e-09	4.8473e-09	4.7659e-10	4.6669e-10	8.4408e-10	3.1114e+04	2.3540e+04	1.0769e+04	1.0935e+04	4.4621e+04	8.5911e+04	4.7723e+04	8.6686e+04
4.9190e-09	4.8733e-09	4.2433e-10	4.6781e-10	1.0415e-09	3.0732e+04	2.6468e+04	9.5919e+03	1.0053e+04	4.7006e+04	8.8936e+04	5.4758e+04	8.2391e+04
4.8067e-09	4.8927e-09	4.9541e-10	4.1807e-10	8.8560e-10	3.4180e+04	2.6987e+04	9.6898e+03	1.0919e+04	4.7870e+04	8.6626e+04	4.7058e+04	8.8617e+04
4.7134e-09	4.8357e-09	4.6753e-10	4.8707e-10	1.0427e-09	2.9441e+04	2.7927e+04	1.0786e+04	1.0289e+04	4.6101e+04	8.6031e+04	4.7256e+04	8.5253e+04
4.6179e-09	4.8379e-09	4.2294e-10	4.6121e-10	1.1095e-09	3.1133e+04	2.7352e+04	1.0623e+04	1.0066e+04	4.5256e+04	9.3161e+04	4.3357e+04	9.1925e+04
5.1046e-09	4.6516e-09	4.4101e-10	4.8701e-10	1.0315e-09	2.8904e+04	2.6539e+04	1.0454e+04	9.9650e+03	4.0540e+04	8.7533e+04	4.5299e+04	8.7922e+04

Fig 6.42 Generation of values for Push Pull type Sensor Interfacing

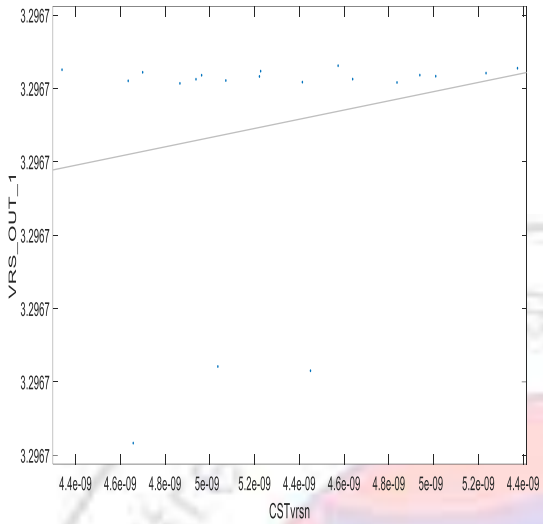

Fig 6.43 CSTvrsn vs VRS_OUT_2

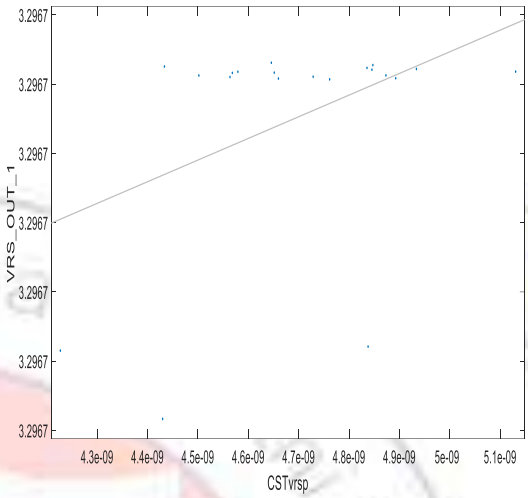

Fig 6.44 CSTvrsp vs VRS_OUT_2

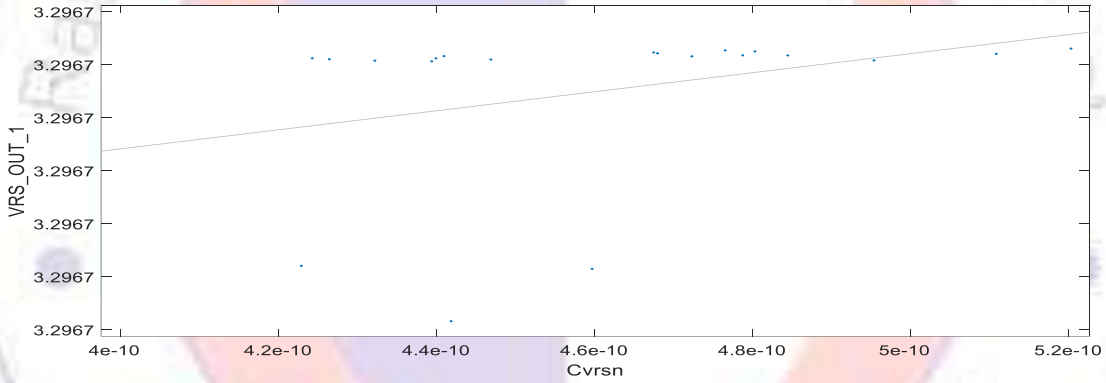

Fig 6.45 Cvrsn vs VRS_OUT_2

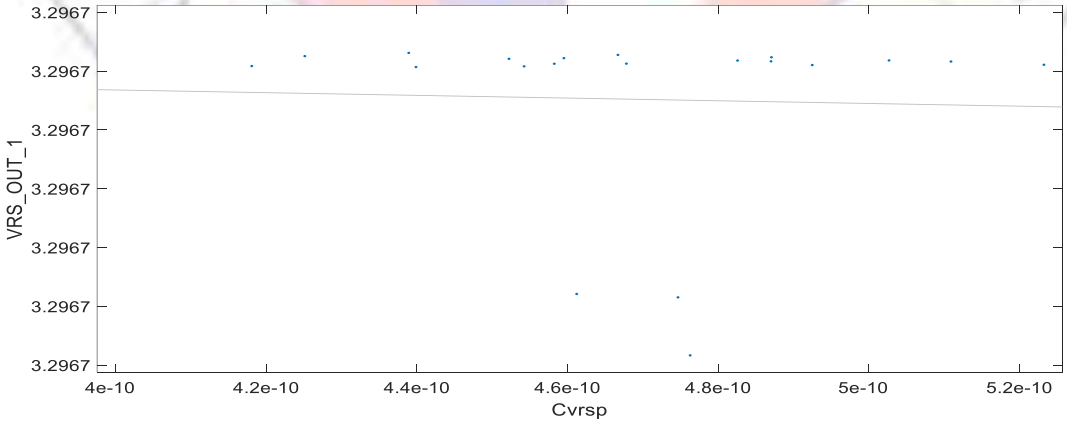

Fig 6.46 Cvrsp vs VRS_OUT_2

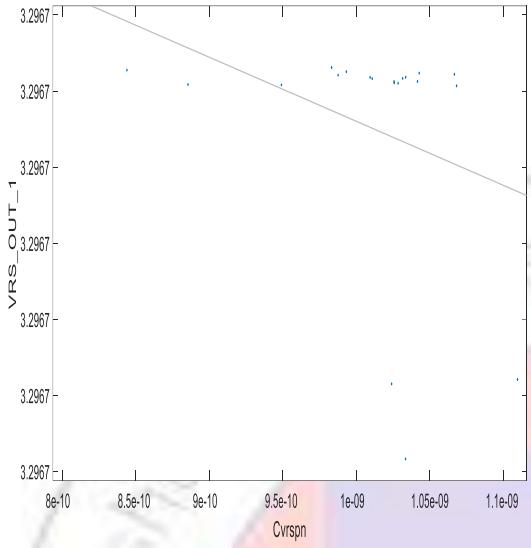

Fig 6.47 Cvrspn vs VRS_OUT_2

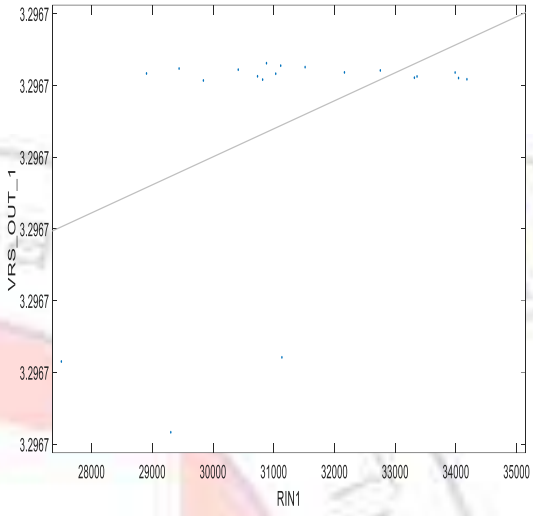

Fig 6.48 RIN1 vs VRS_OUT_2

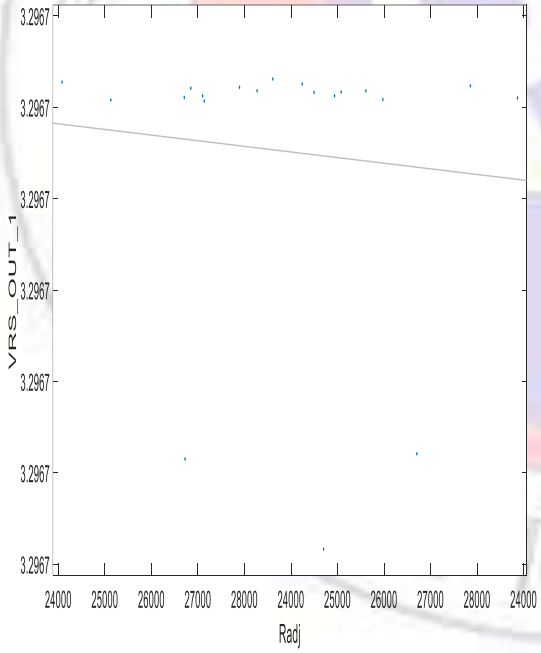

Fig 6.49 Radj vs VRS_OUT_2

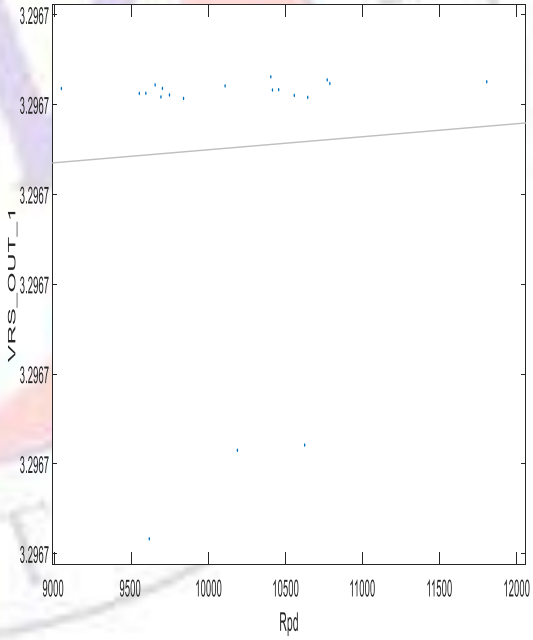

Fig 6.50 Rpd vs VRS_OUT_2

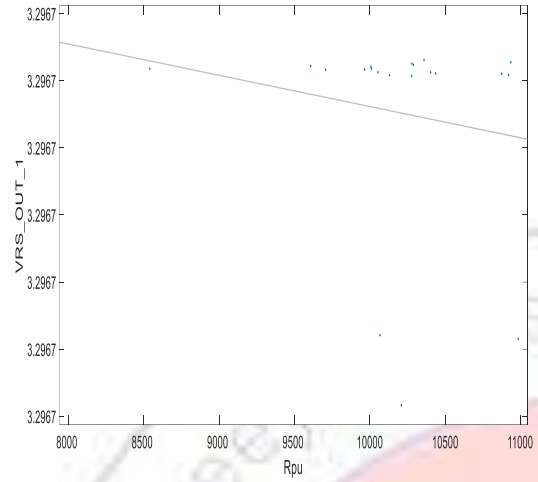

Fig 6.51 Rpu vs VRS_OUT_2

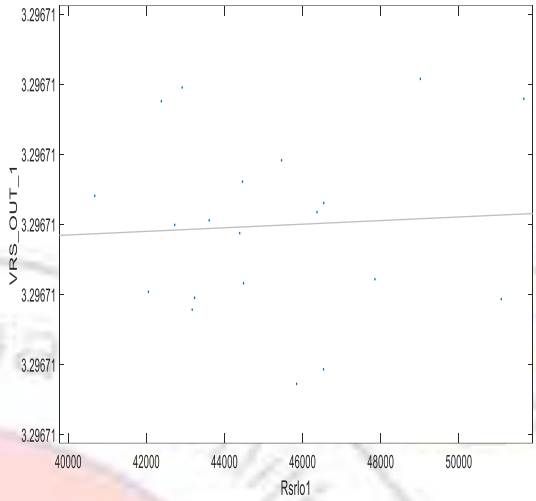

Fig 6.52 Rsrlo1 vs VRS_OUT_2

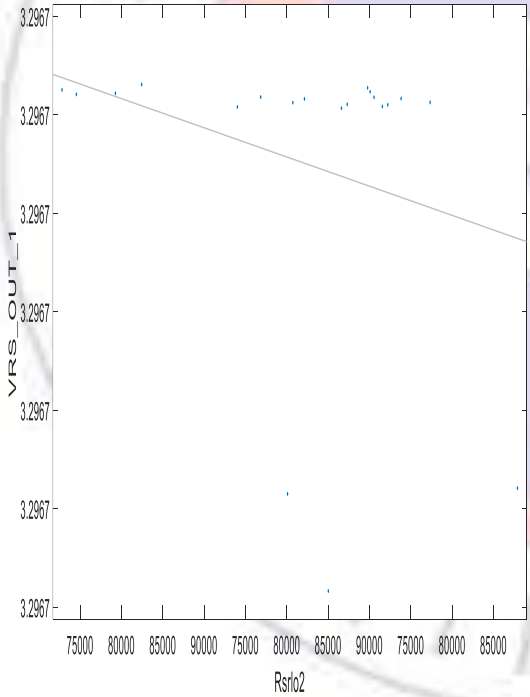

Fig 6.53 Rsrlo2 vs VRS_OUT_2

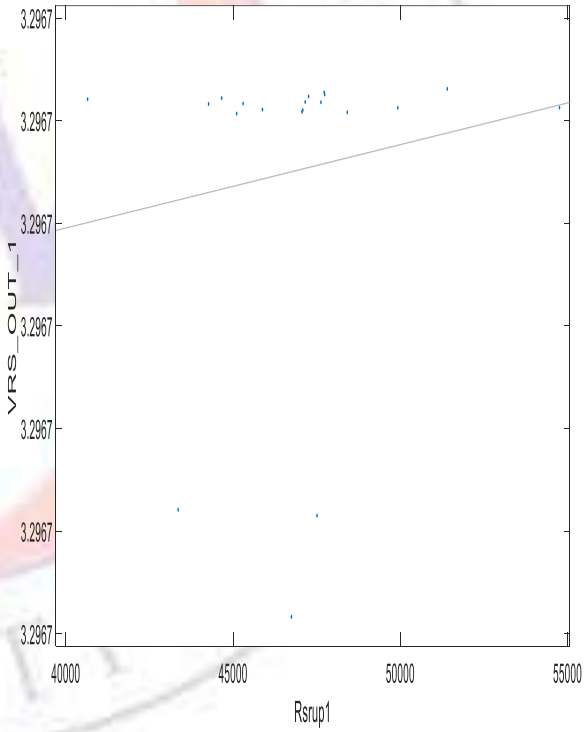

Fig 6.54 Rsrup1 vs VRS_OUT_2

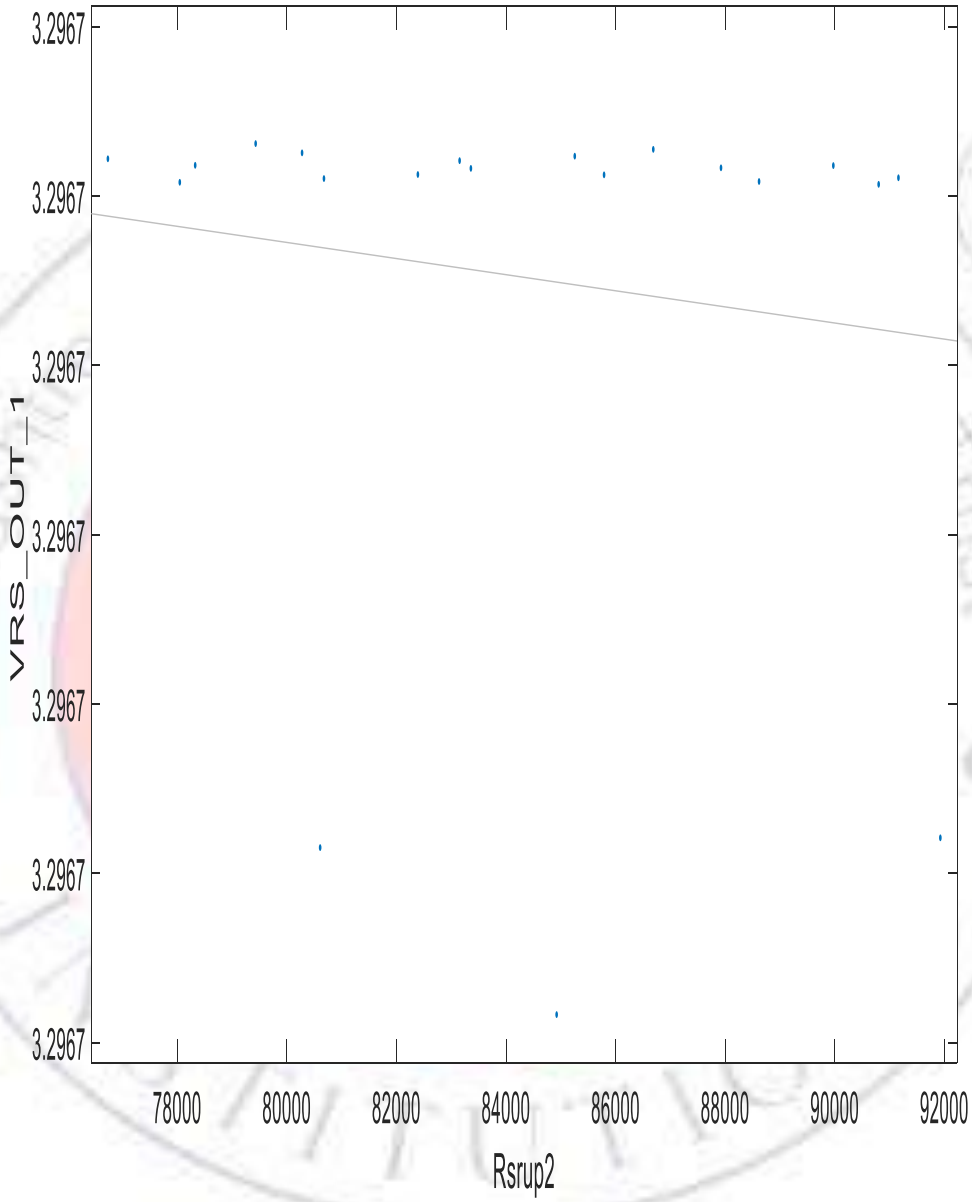

Fig 6.55 Rsrup2 vs VRS_OUT_2

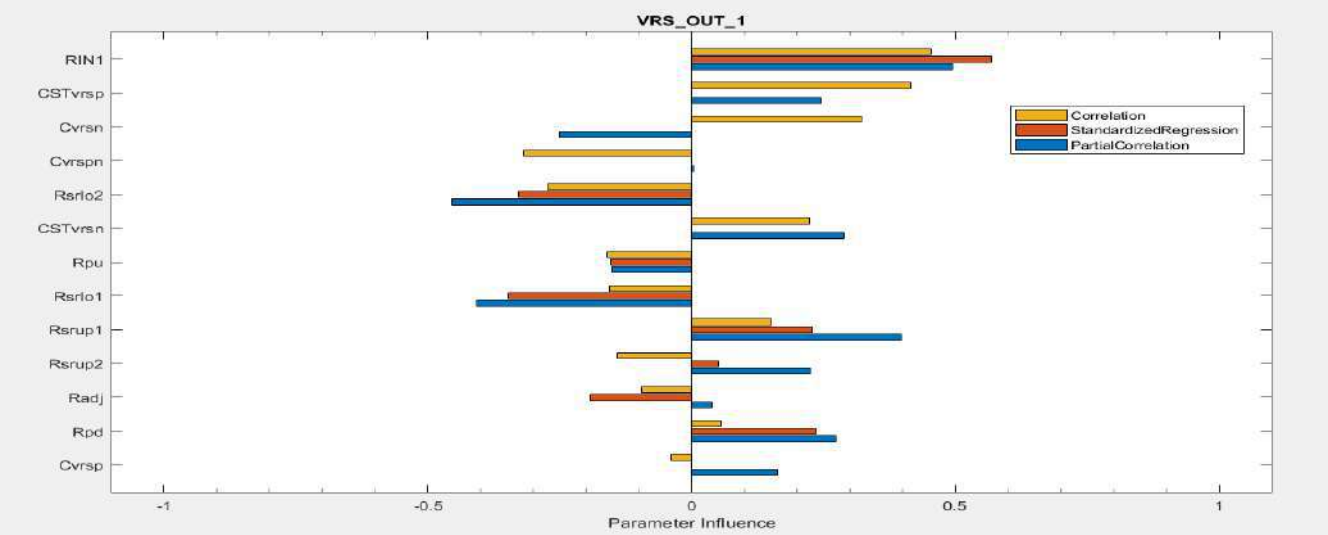

Fig 6.56 Components influence on Output Voltage

Select result type: Linear Correlation

13×1 table

	VRS_OUT_1
CSTvrsn	0.22335
CSTvrsp	0.41546
Cvrsn	0.32186
Cvrsp	-0.039453
Cvrspn	-0.31842
RIN1	0.45428
Radj	-0.095914
Rpd	0.056904
Rpu	-0.16085
Rsrlo1	-0.15535
Rsrlo2	-0.27235
Rsrup1	0.15032
Rsrup2	-0.14083

Select result type: Linear Standardized Regression

13×1 <a href="matlab:helpPopup table" style="font-weight:bold">tab

	VRS_OUT_1
CSTvrsn	0
CSTvrsp	0
Cvrsn	0
Cvrsp	0
Cvrspn	0
RIN1	0.56759
Radj	-0.19252
Rpd	0.23687
Rpu	-0.15338
Rsrlo1	-0.3461
Rsrlo2	-0.32776
Rsrup1	0.2286
Rsrup2	0.050328

Select result type: Linear Partial Correlation

13×1 table

	VRS_OUT_1
CSTvrsn	0.289
CSTvrsp	0.2456
Cvrsn	-0.24931
Cvrsp	0.16311
Cvrspn	0.0030182
RIN1	0.49345
Radj	0.038284
Rpd	0.27367
Rpu	-0.15173
Rsrlo1	-0.40742
Rsrlo2	-0.45289
Rsrup1	0.3976
Rsrup2	0.22458

Fig 6.57 Statistical Data for Sensitivity Analysis

6.5 Hardware Implementation Results

The setup for hardware implementation is shown in Fig 6.58.

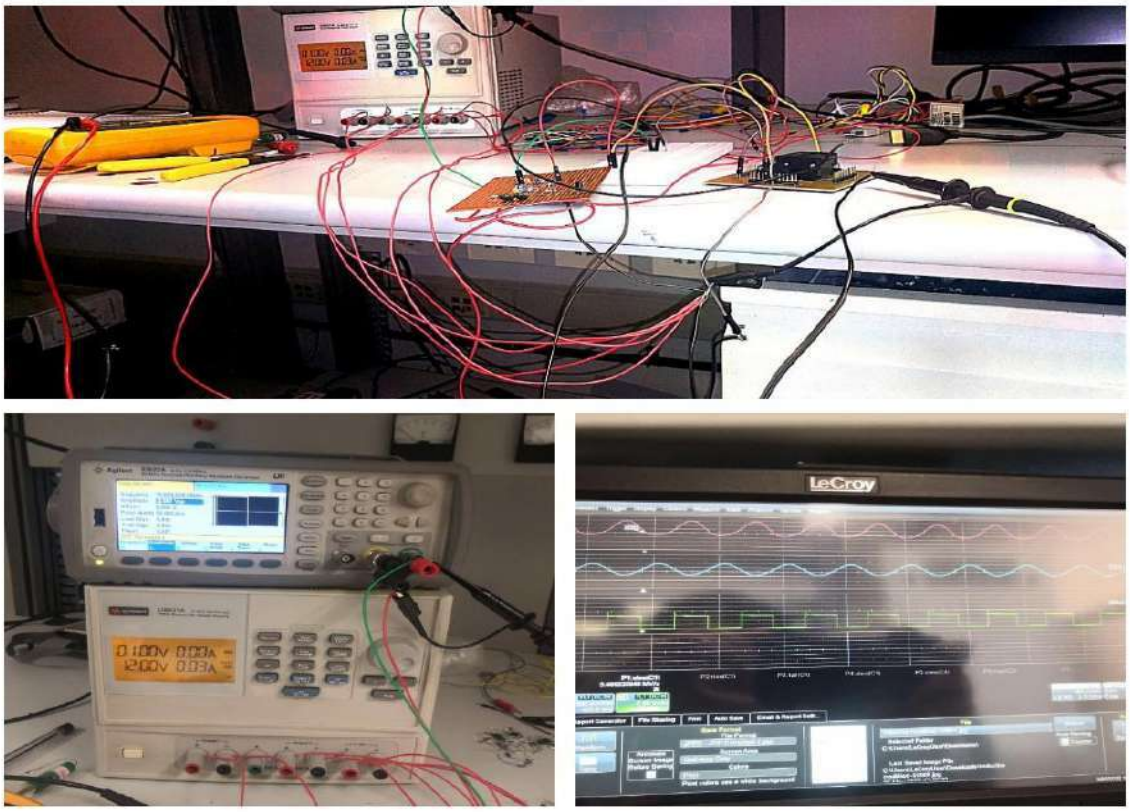

Fig 6.58 Hardware Implementation and Testing

6.7 Hall Effect Sensor Interfacing

The results for Hall Sensor Interfacing shown in Fig 6.59. The waveform in pink color indicates VRSP signal and the waveform in blue color indicates VRSN signal. The waveform in green color indicates VRS_OUT signal. The generated VRS_OUT signal is in the form of digital rectangular pulses. The average output voltage value obtained is 5 V. The waveforms are observed using digital storage oscilloscope.

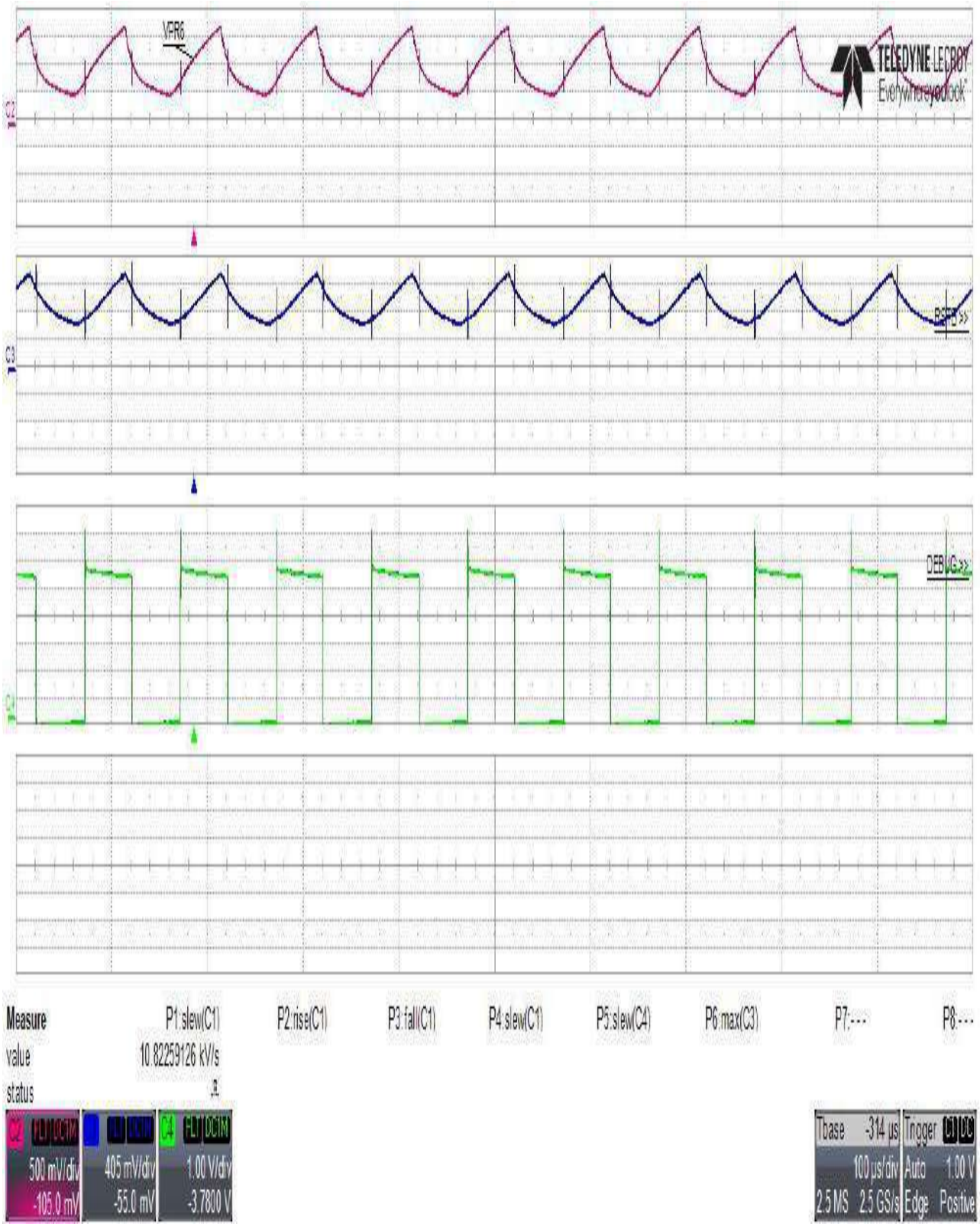

Fig 6.59 Results for Hall Sensor Interfacing

6.8 Inductive Sensor Interfacing

The results for Inductive Sensor Interfacing is shown in Fig 6.60. The inductive sensor is modelled as two sinusoidal AC voltage sources are connected in parallel and are 180 degree out of phase with each other and in synchronism with each other. The waveform in pink color indicates VRSP signal and the waveform in blue color indicates VRSN signal. The waveform in green color indicates VRS_OUT signal. The generated VRS_OUT signal is in the form of digital rectangular pulses. The average output voltage value obtained is 5 V. The waveforms are observed using digital storage oscilloscope.

Fig 6.60 Results for Inductive Sensor Interfacing

6.8 Push Pull type Sensor Interfacing

The results for Push Pull type Sensor Interfacing is shown in Fig 6.63. The Push Pull type sensor is modelled as 555 timer is shown in Fig 6.61 operated in astable mode to produce push pull oscillations. The capacitor charging and discharging process and push pull oscillations generated using 555 timer is shown in Fig 6.62. The waveform in pink color indicates VRSP signal and the waveform in blue color indicates VRSN signal. The waveform in green color indicates VRS_OUT signal. The generated VRS_OUT signal is in the form of digital rectangular pulses. The average output voltage value obtained is 5 V. The waveforms are observed using digital storage oscilloscope.

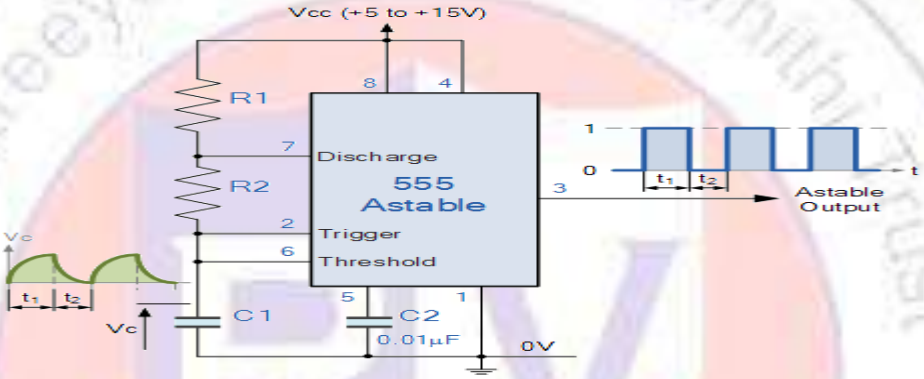

Fig 6.61 Astable multivibrator as Push Pull sensor

Table 6.1 Parameters of 555 timer modelled as Push Pull type sensor

Parameters	Values
R1-Charging Resistor	39kohm
R2-Discharging Resistor	39kohm
C1-Capacitor	0.01uF
TON(Turn on time)=0.693*(R1+R2)*C1	0.54msec
TOFF(Turn off time)=0.693*R2*C1	0.27msec
F(Frequency)=1/(TON+TOFFF)	1.2 kHz

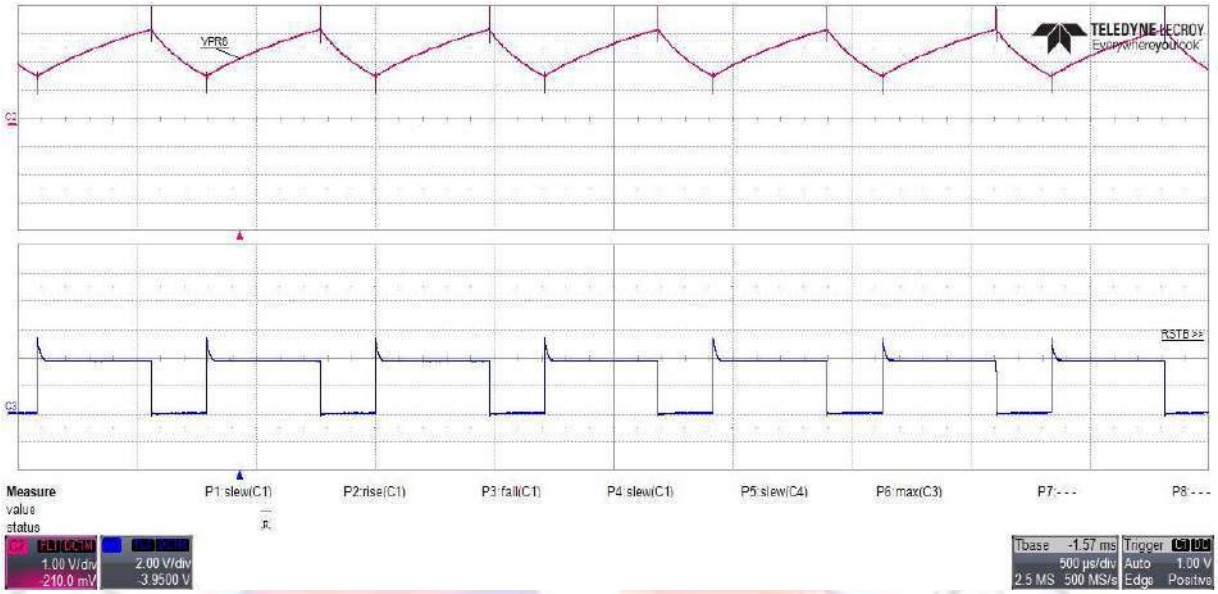

Fig 6.62 Voltage across the capacitor and output voltage generated by 555 timer

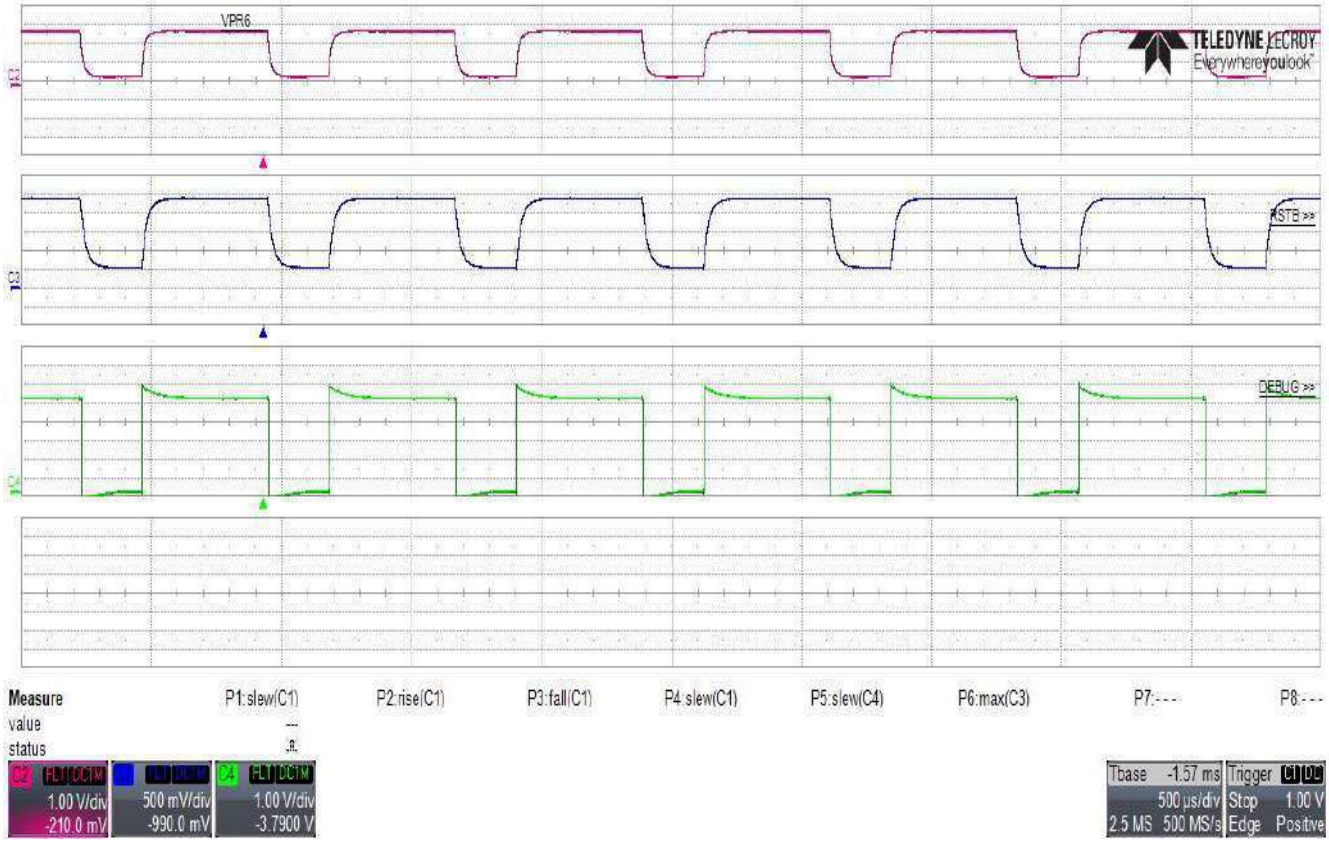

Fig 6.63 Results for Push Pull type Sensor Interfacing

6.9 Summary

This chapter includes the simulation results of Hall sensor interfacing, Inductive sensor interfacing and Push Pull type sensor interfacing, results of monte carlo and sensitivity analysis. The chapter also included Hardware implementation results of Hall sensor interfacing, Inductive sensor interfacing and Push Pull type sensor interfacing.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

Complexity of SoC (System on a Chip) design, especially in sensor conditioning applications is dramatically increased over the last years while time-to-market requirements showed a decrement trend. Cost reduction and performance enhancement of electronic and electromechanical sensors (MEMS) are pushing the demand for the introduction of new electronic applications to increase car safety (airbag, ABS, ESP, etc.) and comfort levels (Assisted Guidance, Cruise Control, etc). Simultaneously as sensors become more sophisticated, according to market requirements, they need more accurate, specific and complex sensing elements. In this work, a flexible sensor interface block inverter was designed for sensor interfacing and signal conditioning. The Hall Effect Sensor, Inductive Sensor, Push Pull type sensor are tested for the functionality. The sensor functionality testing was performed using Pspice tool. The experimentally obtained parameters such as VRSP, VRSN, VRS_OUT for each sensor interfacing were analysed. The Monte Carlo simulation and Sensitivity Analysis technique were implemented for validation and verification of the developed simulated circuit. using Pspice. After validation same circuit was implemented in hardware. The simulated results and hardware results were compatible.

7.1 Conclusion

The flexible sensor interfacing circuit was designed for functionality testing and signal conditioning and was simulated in Pspice and hardware implementation was carried out for the same. The major conclusions from the work are,

- The designed circuit comprised of sensor block, sensor interface block and flex input L9966 IC. The sensor block consisted of Hall Effect sensor, Inductive sensor and Push pull type sensor. Each sensor was interfaced to sensor interface block and L9966 IC.
- The L9966 was able to condition all the three sensors to its input terminals resulting in digital rectangular pulses.
- The average output voltage obtained for Hall sensor, Inductive sensor, Push Pull type sensor interfacing using Pspice Simulation was 3.3 V.
- Without modifying sensor interface, flex input L9966 IC was able to convert any signal into rectangular pulses, resulting in increased flexibility. The increased flexibility resulted in variant reduction and overall cost of the system.

- The developed circuit was validated using Monte Carlo Analysis and Sensitivity Analysis. The 3 sigma in Monte Carlo simulation implied that the circuit design was 99.7% accurate considering all boundary conditions and worst case conditions. The view of Sensitivity analysis gave an idea how to optimize the circuit as per the design requirements.
- The Hardware testing for designed sensor interfacing circuit was carried out.
- The average output voltage obtained during hardware testing for Hall sensor, Inductive sensor and Push Pull type sensor interfacing was 5 V.
- The single chip solution offered an advantage such that it was compatible with a wide set of sensors and helped in achieving optimal solution for a given sensor. Flex Sensor Interface occupied less area and it offered high performances dedicated to various type of sensors.

7.2 Future Scope

The scope for further improvements in the outcomes are:

- The increased flexibility nature of L9966 IC can be implemented in Electric Vehicles that can result in sustainable Green ecosystem.
- The flexibility of L9966 IC can be applied to improve the performance of self driving and autonomous driving vehicles.
- The Flex input can be a driving future of Automotive Electronics system that can result in increased safety of passengers and decreased exhaust emissions and increased fuel economy.

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APPENDIX A

Datasheet

L9966

Data brief

FlexInput IC for automotive applications

TQFP48 (7x7 mm)

Features

- AEC-Q100 qualified
- 12 V and 24 V systems compatible (operating battery supply voltage 5.5 V-36 V)
- Programmable interface with 15 total inputs:
  - 12 for connection to external analog loads (with connection to VVAR, VDD5 and clamped battery VPRE, with resistance measurement)
    - 4 with also λ sensor functionality
    - 4 with also SENT functionality
  - 3 for connection to external digital switches (with connection to VPRE)
- Programmable pull-up/down current sources
- Integrated precise resistance measurements
- 12 bit ADC for voltage measurements
- 15 bit ADC for resistance measurements
- Variable reluctance sensor / Hall sensor Interface
- 1 analog output channel + 4 digital output channels
- SPI interface for device configuration and data communication
- Overtemperature protection
- Thermal resistance $R_{th(j-c)}$ = 3 K/W

Product status link
L9966

Product summary	
Order code	L9966CB-TR
Package	TQFP48
Packing	Tape and reel

Description

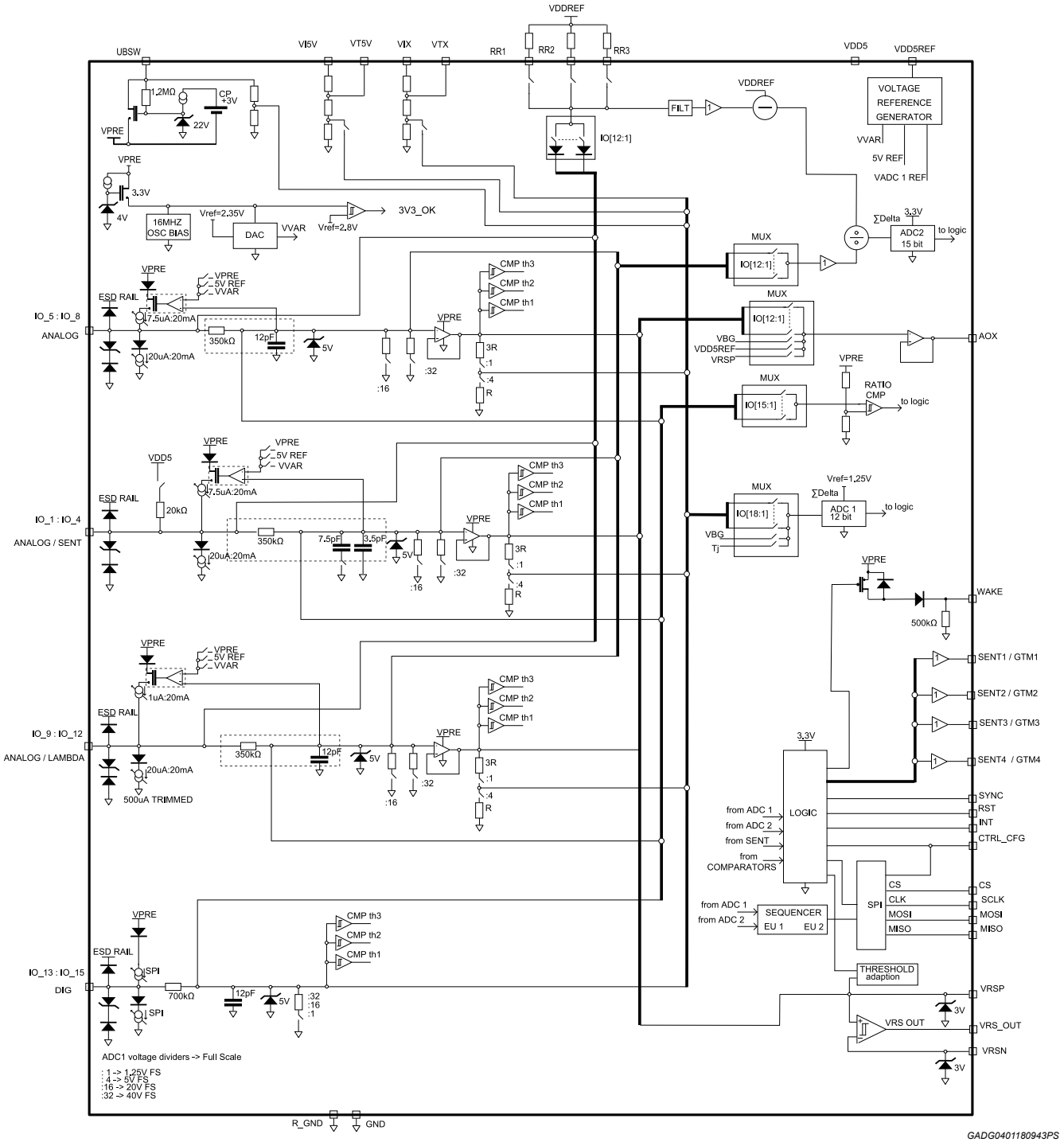
The L9966 is an automotive grade IC designed to be used as sensors interface. Up to 15 channels are available for analog sensing, resistance measurement and digital sensing (e.g. temperature, lambda, pressure, position sensors).

The L9966 allows replacing a number of discrete components and it gives the possibility to change the sensors across different applications without modifying the PCB hardware.

Target applications are Engine Control Units and Body/Chassis Modules.

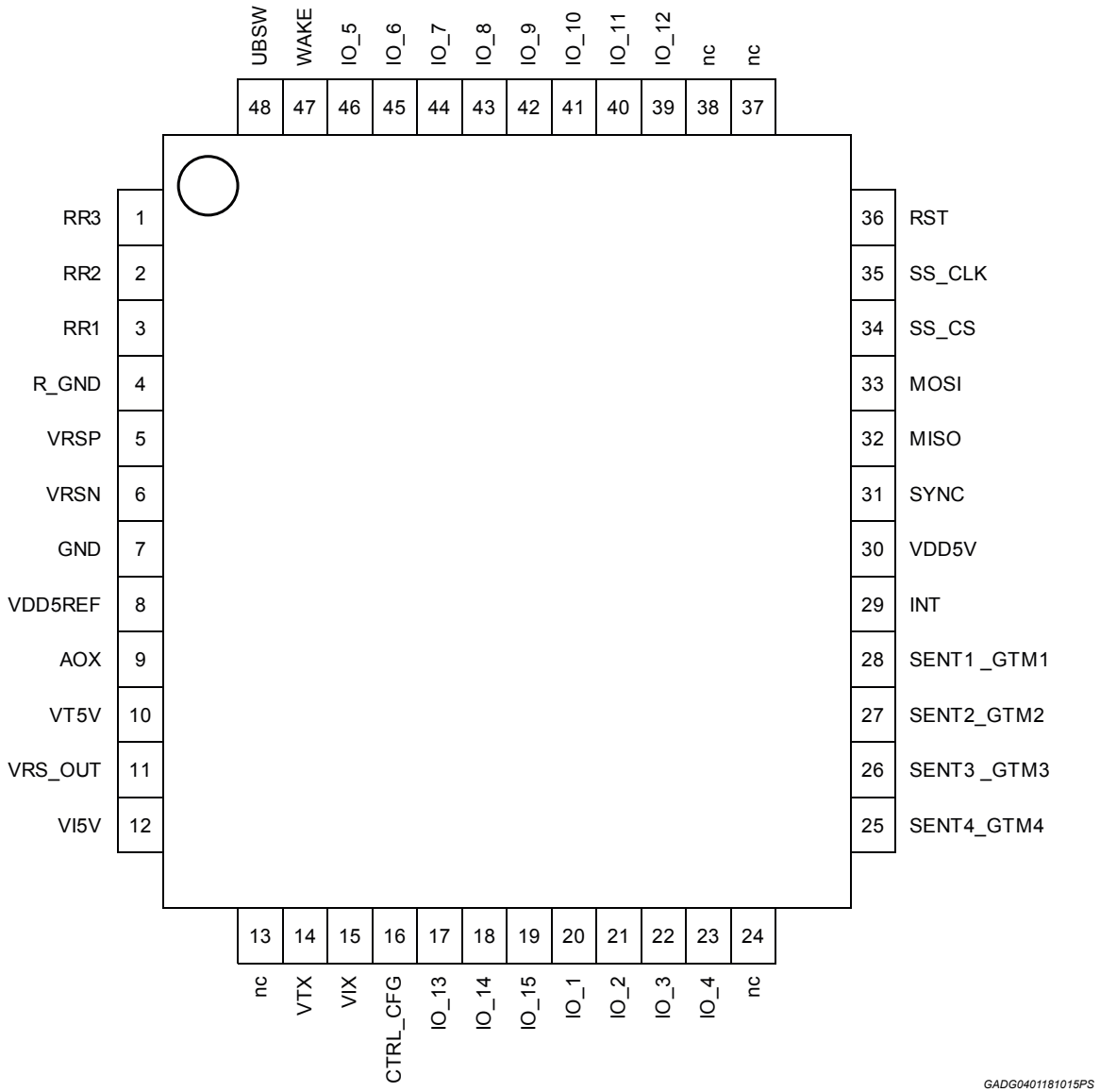
1 Block diagram

Figure 1. **Block diagram**



2 Pin description

Figure 2. **Pin connection diagram**



GADG0401181015PS

Table 1. **Pin description**

Pin-Nr.	Pin-name	Description	Pin-class (1)
1	RR3	Reference Pullup Resistor 3 for R-Measurement	I
2	RR2	Reference Pullup Resistor 2 for R-Measurement	I
3	RR1	Reference Pullup Resistor 1 for R-Measurement	I
4	R_GND (2)	Reference Ground for high accuracy signals	I
5	VRSP	Positive variable reluctance sensor input	A
6	VRSN	Negative variable reluctance sensor input	A

Pin-Nr.	Pin-name	Description	Pin-class (1)
7	GND	Ground for supply voltage	S
8	VDD5REF	Positive reference to both ADC	I
9	AOX	Analog output for input channel x	I
10	VT5V	Ratiometric Voltage output VI5V	I
11	VRS_Out	Digital Output of Variable reluctance sensor	I
12	VI5V	Input Voltage	I
13	nc	Not connected	-
14	VTX	Ratiometric Voltage output VIX	I
15	VIX	Input Voltage	I
16	CTRL_CFG	Input to control current source / Configuration input to select SPI Address-Mux during Reset	I
17	IO_13	Flexible Input and current output 13	D
18	IO_14	Flexible Input and current output 14	D
19	IO_15	Flexible Input and current output 15	D
20	IO_1	Flexible Input and current output 1 / SENT1	A
21	IO_2	Flexible Input and current output 2 / SENT2	A
22	IO_3	Flexible Input and current output 3 / SENT3	A
23	IO_4	Flexible Input and current output 4 / SENT4	A
24	nc	Not connected	-
25	SENT4_GTM4	Digital Output for SENT 4 channel / GTM_TO_SENT_4	I
26	SENT3_GTM3	Digital Output for SENT 3 channel r/ GTM_TO_SENT_3	I
27	SENT2_GTM2	Digital Output for SENT 2 channel / GTM_TO_SENT_2	I
28	SENT1_GTM1	Digital Output for SENT 1 channel / GTM_TO_SENT_1	I
29	INT	Interrupt (result status for controller)	I
30	VDD5V	5 V Power supply	I
31	SYNC	Digital input to synchronize sequencer start	I
32	MISO	Communication interface clock for Master-IN/ Slave-OUT	I
33	MOSI	Communication interface for Master-OUT/ Slave-IN	I
34	CS	Communication interface chip select	I
35	SCLK	Communication interface clock	I
36	RST	Reset	I
37	nc	Not connected	-
38	nc	Not connected	-
39	IO_12	Flexible Input and current output 12 / LAMBDA	A
40	IO_11	Flexible Input and current output 11 / LAMBDA	A
41	IO_10	Flexible Input and current output 10 / LAMBDA	A
42	IO_9	Flexible Input and current output 9 / LAMBDA	A
43	IO_8	Flexible Input and current output 8	A
44	IO_7	Flexible Input and current output 7	A
45	IO_6	Flexible Input and current output 6	A
46	IO_5	Flexible Input and current output 5	A

Pin-Nr.	Pin-name	Description	Pin-class (1)
47	WAKE	Output for wake-up	I
48	UBSW	Battery supply	S

1. *see **Pin-class legend:***
2. *R_GND is the ground reference for ADC1, ADC2, VDD5REF voltage divider, input channel voltage dividers. In case R_GND connection to ground on the PCB is lost, R_GND is referenced one diode voltage drop above GND.*

Pin-class legend:

I: ECU Internal Pins: connection to other electrical components on the ECU (Local pins).

S: Supply Pins: connection to supply sources with protected battery supply (Local pins except UBSW that is a global pin).

A: Analog Inputs: connection to external ECU pins (Global pin).

D: Digital Inputs: connection to external ECU pins (Global pin).

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

3.1 TQFP48 (7x7x1 mm exposed pad down) package information

Figure 3. TQFP48 (7x7x1 mm exposed pad down) package outline

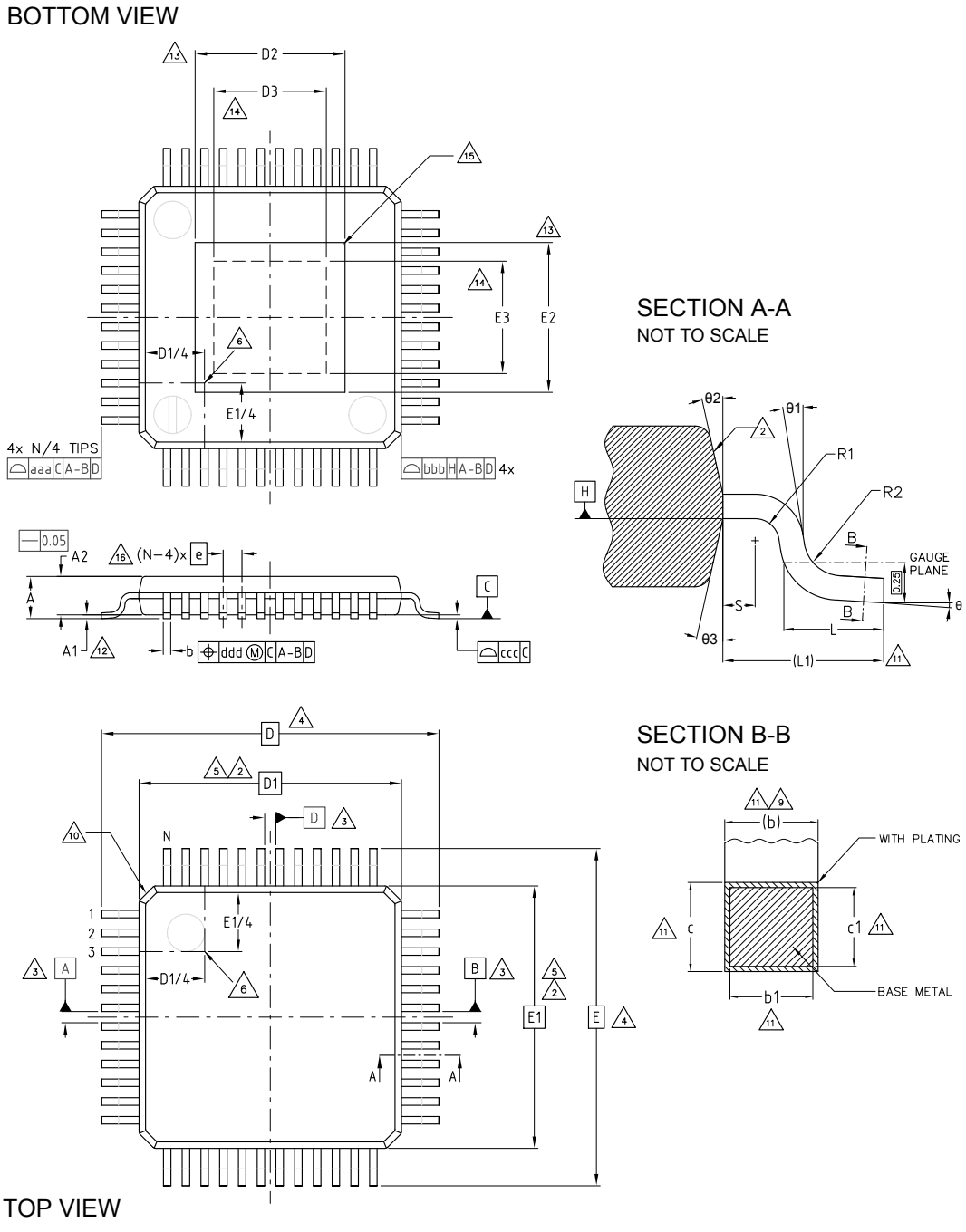


Table 2. TQFP48 (7x7x1 mm exp. pad down) package mechanical data

Symbol	Dimensions			Note
	Min.	Typ.	Max.	
Θ	0°	3.5°	7°	
Θ1	0°	-	-	
Θ2	11°	12°	13°	
Θ3	11°	12°	13°	
A	-	-	1.20	15
A1	0.05	-	0.15	12
A2	0.95	1.00	1.05	15
b	0.17	0.22	0.27	9, 11
b1	0.17	0.20	0.23	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D	9.00 BSC			4
D1	7.00 BSC			2, 5
D2	-	-	4.15	13
D3	3.89	-	-	14
e	0.50 BSC			
E	9.00 BSC			4
E1	7.00 BSC			2, 5
E2	-	-	4.15	13
E3	3.89	-	-	14
L	0.45	0.60	0.75	
L1	1.00 REF			
N	48			16
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	
Tolerance of form and position				
aaa	0.20			1, 7
bbb	0.20			
ccc	0.08			
ddd	0.08			

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
22-Nov-2018	1	Initial release.

Contents

Design, Development and Validation of a Flexible Sensor Interface Module for Engine Control

Gangadhar M Akki [1RV20EPE02]
M.Tech in Power Electronics, Department of Electrical and Electronics Engineering
R.V College of Engineering, Bangalore - 560059, INDIA

Objective

Design and performance analysis of flexible sensor interface module and validation of a developed module using Monte Carlo and Sensitivity Analysis techniques

Project Methodology

The flexible sensor interfacing circuit is designed as per the customer requirements. Here, Hall effect sensor, Inductive sensor, Push pull type sensors are interfaced to flexible sensor interface block and are tested for functionality. Here both simulation analysis and hardware implementation are carried out. The output waveforms are observed using Pspice software during simulation analysis and digital storage oscilloscope (DSO) during hardware testing.

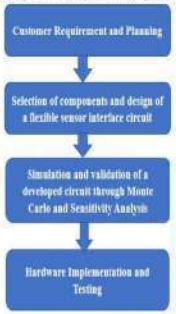


Fig 1 Methodology

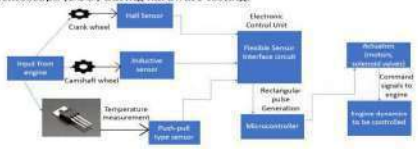


Fig 2 Block diagram of the proposed Methdology

Sensor Interface Components	Rating
CSTvrsp, CSTvrsn	4.7 nF
Rgu, Rpd	10kohm
Cvrspn	1nF
RIN1, RIN2, RIN3, RIN4	31.6kohm
Rsrup1, Rsrup2	46.4kohm, 68.1kohm
Rsrlo1, Rsrlo2	46.4kohm, 68.1kohm
Radj	26.1kohm
Cvrsp, Cvrsn	470pF

Fig 3 Sensor Interface block components

Fig 4 Flex Input L9966 IC

Simulation Analysis and Hardware Implementation

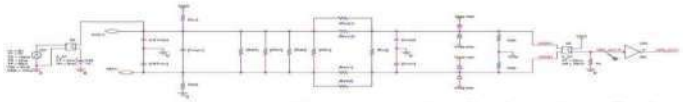


Fig 5 Simulation Circuit for Sensor Interfacing

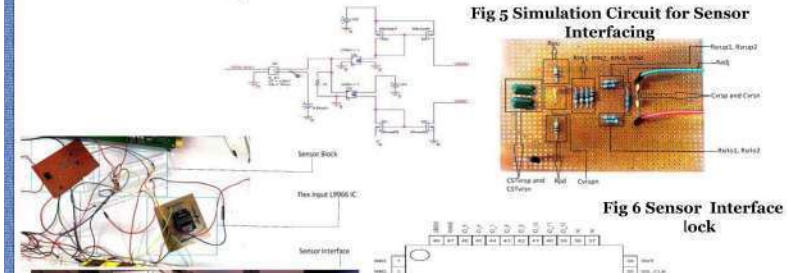


Fig 6 Sensor Interface lock

Fig 7 Hardware Implementation

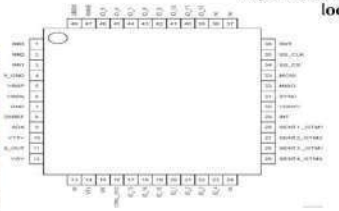


Fig 8 Pin Connection Diagram of L9966 IC

VRSP□Variable Reluctance Sensor Positive(Pin5), VRSN□Variable Reluctance Sensor Negative(Pin6)

The circuit diagram for sensor interfacing is shown in Fig 5 and Fig 6. The sensor takes input from the engine and the signal is fed to a sensor interface block and the signal output from the sensor interface block is fed to a flexible input L9966 IC. The VRSP and VRSN signals are generated and the difference between the two signals is known as the control signal and is compared with the reference voltage. By the comparator action, rectangular pulses are obtained and are sent to a microcontroller. The microcontroller activates the actuator and there by completing the mechanism. The Monte Carlo and Sensitivity Analysis are applied for the circuit validation and verification.

Results and Discussions

Simulation Results

Fig 9 Simulated View of VRSP, VRSN and Output Voltage for Hall Sensor, Inductive Sensor,Push Pull type sensor

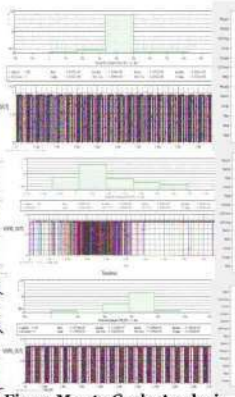


Fig 10 Monte Carlo Analysis on Output Voltage for Hall Sensor, Inductive Sensor and Push Pull type Sensor

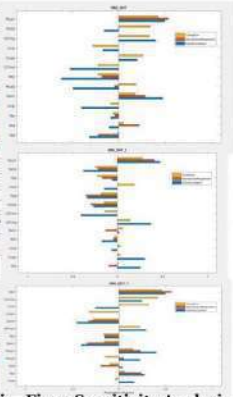


Fig 11 Sensitivity Analysis on output Voltage for Hall Sensor, Inductive Sensor and Push Pull type Sensor

Hardware Results

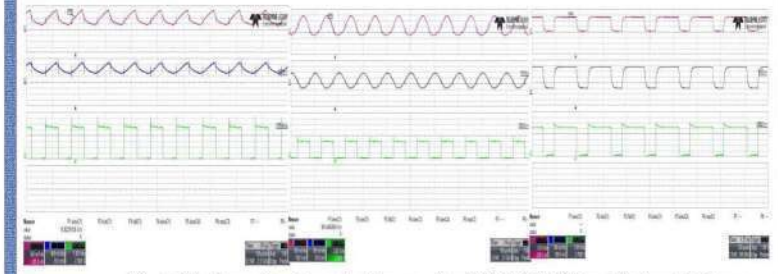


Fig 12 Hardware Implementation results of VRSP, VRSN and Output Voltage for Hall Sensor, Inductive Sensor, Push Pull type Sensor Interfacing

The results for Hardware testing are shown in above Figures. The waveform in pink color indicates VRSP signal and the waveform in blue color indicates VRSN signal. The waveform in green color indicates VRS_OUT signal. The generated VRS_OUT signal is in the form of digital rectangular pulses. The average output voltage value obtained duing simulation was 3.3 V and during hardware testing was 5 V.

Conclusions

- The L9966 was able to condition to all the three sensors to its input terminals resulting in digital rectangular pulses. Without modifying sensor interface, flex input L9966 IC was able to convert any signal into rectangular pulses, resulting in increased flexibility. The increased flexibility resulted in variant reduction and overall cost of the system.
- The developed circuit was validated using Monte Carlo Analysis and Sensitivity Analysis. The 3 sigma in Monte Carlo simulation implied that the circuit design was 99.7% accurate considering all boundary conditions and worst case conditions. The view of Sensitivity Analysis gave an idea how to optimize the circuit as per the design requirements.
- The single chip solution offers an advantage such that it was compatible with a wide set of sensors and helped in achieving optimal solution for a given sensor and it has resulted in overall cost reduction of the system.

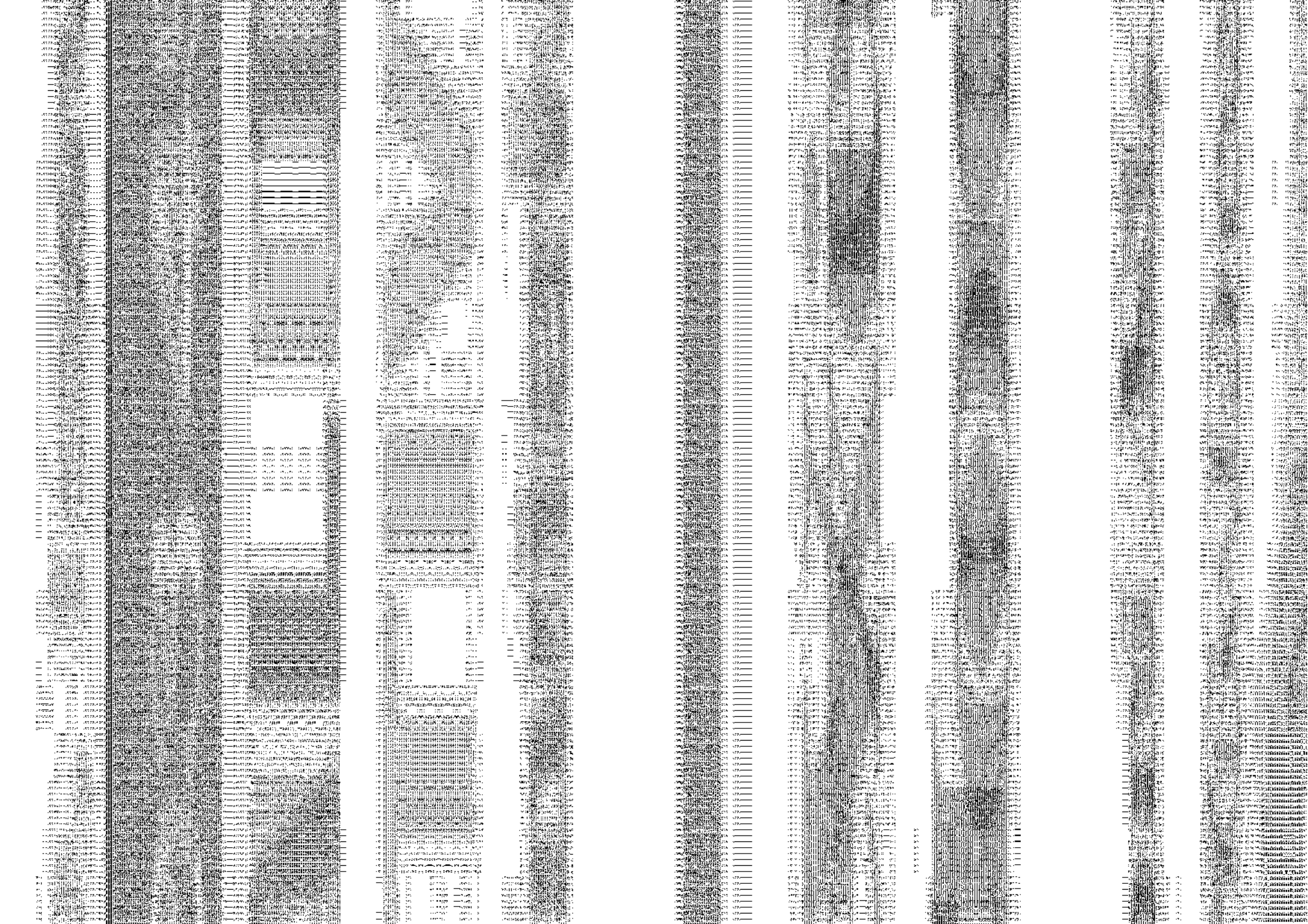
Future Scope

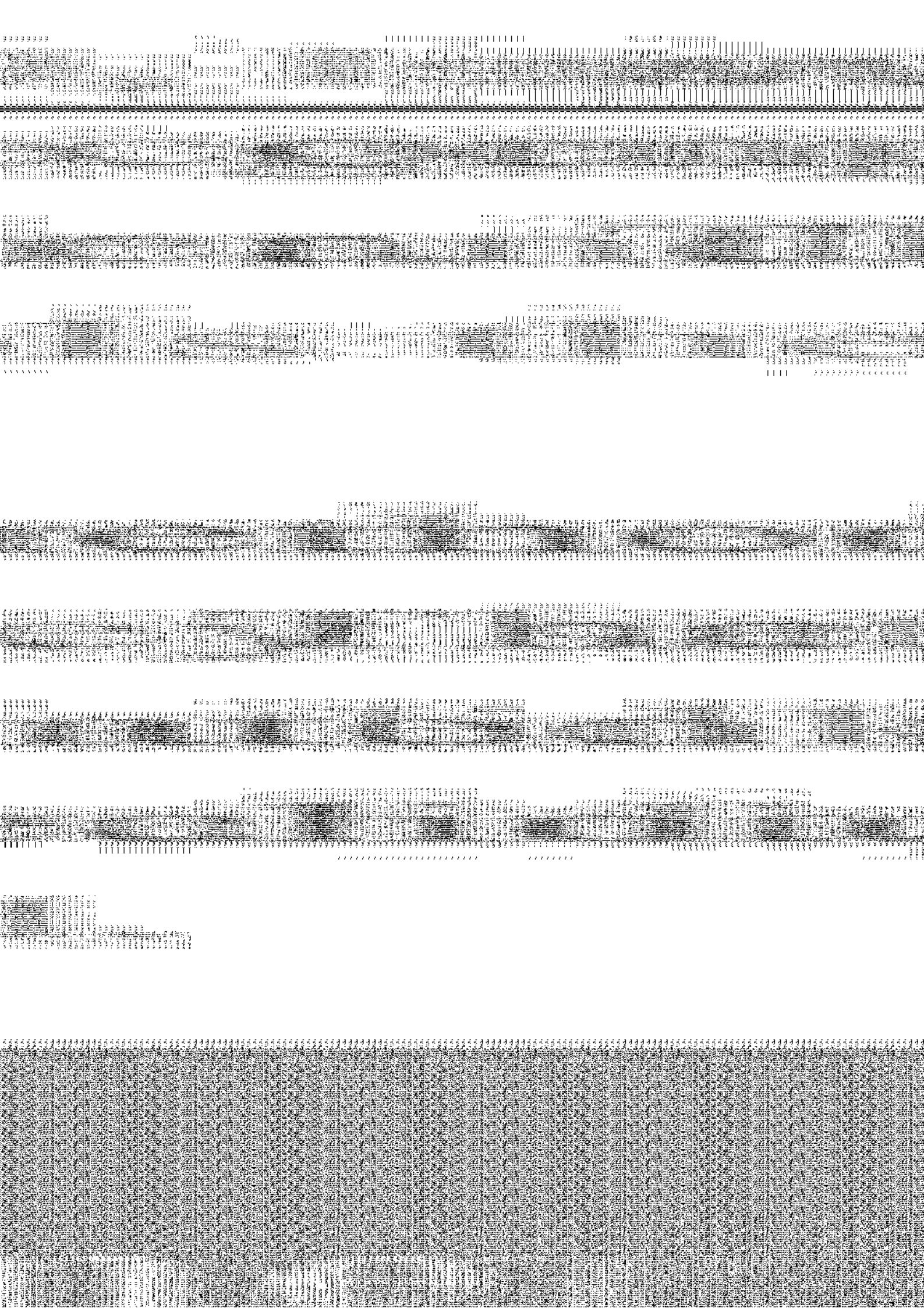
The increased flexibility nature of L9966 IC can be implemented in Electric Vehicles that can result in sustainable Green ecosystem. The flexibility of L9966 IC can be applied to improve the performance of self driving and autonomous driving vehicles, resulting in decreased exhaust emissions and improved fuel economy and increased safety of passengers.

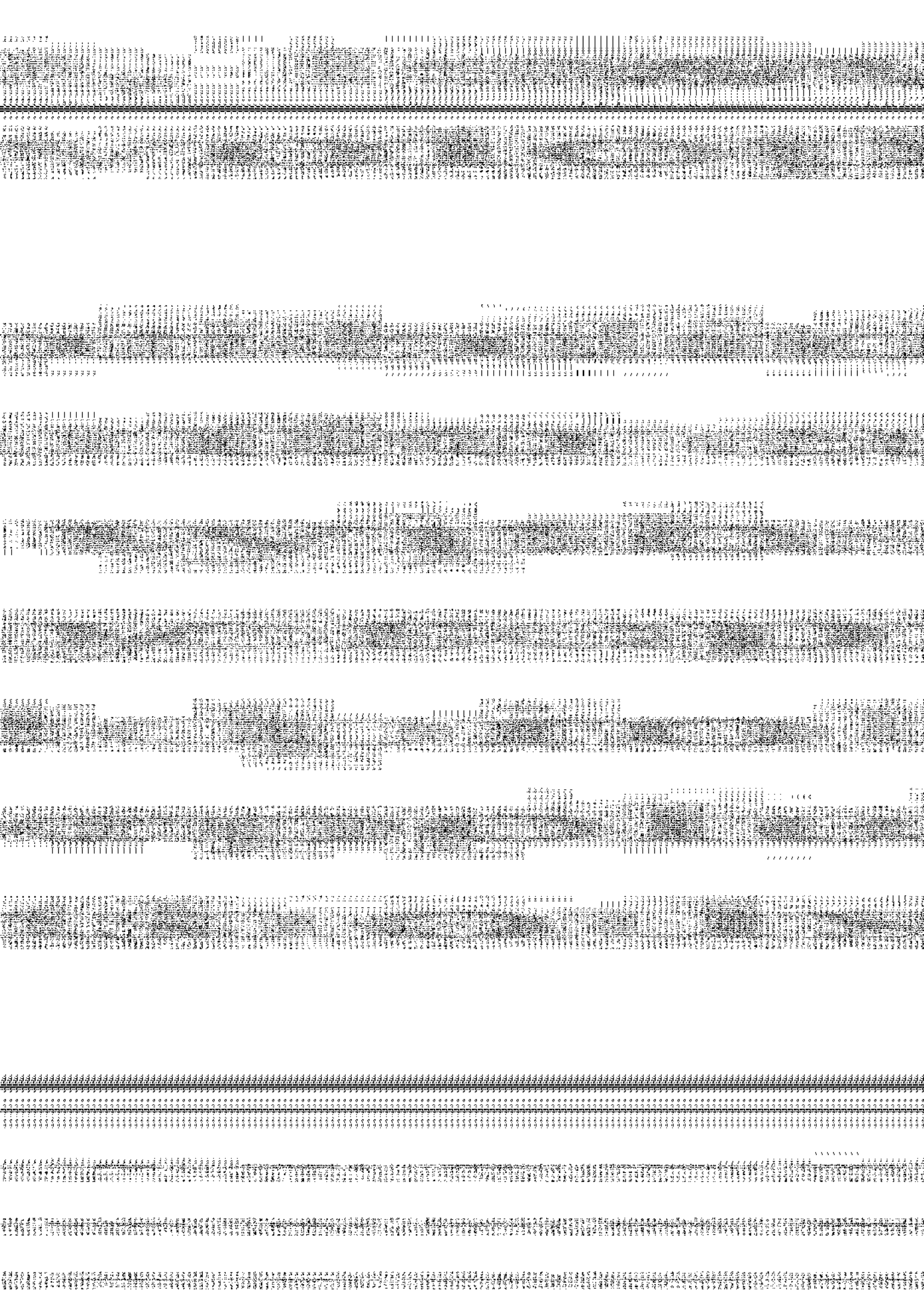
Acknowledgements

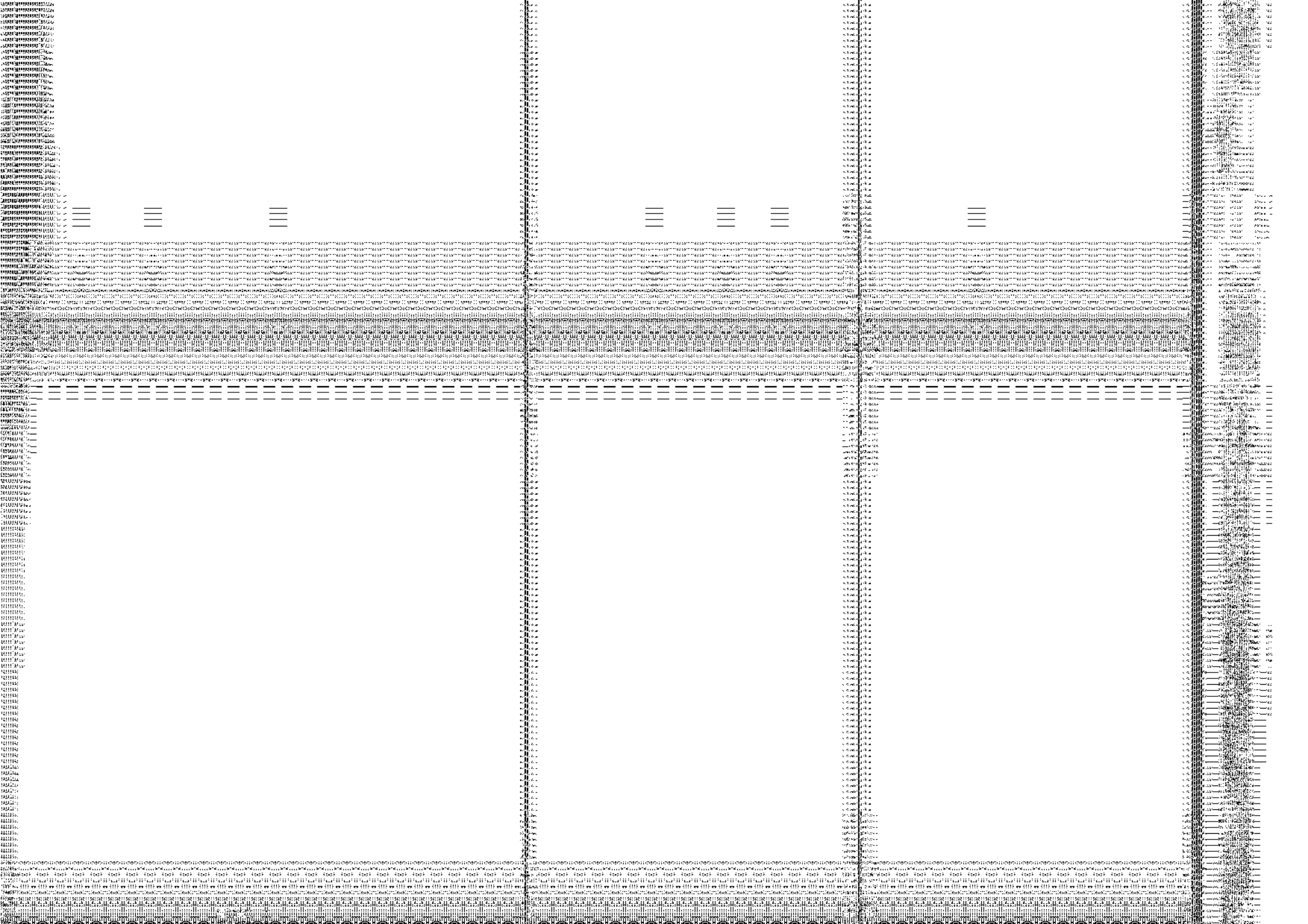
- I deeply express my sincere gratitude to my guide Dr S G Srivani, Professor and Associate PG Dean ,Dept of EEE, RVCE, Principal and HOD, Dept of EEE, RVCE and Panel members for their patience and valuable guidance throughout this project.
- I would like to express my deepest appreciation to Bosch Global Software Technologies, Bengaluru for providing me an opportunity to carry out the project in their organization.

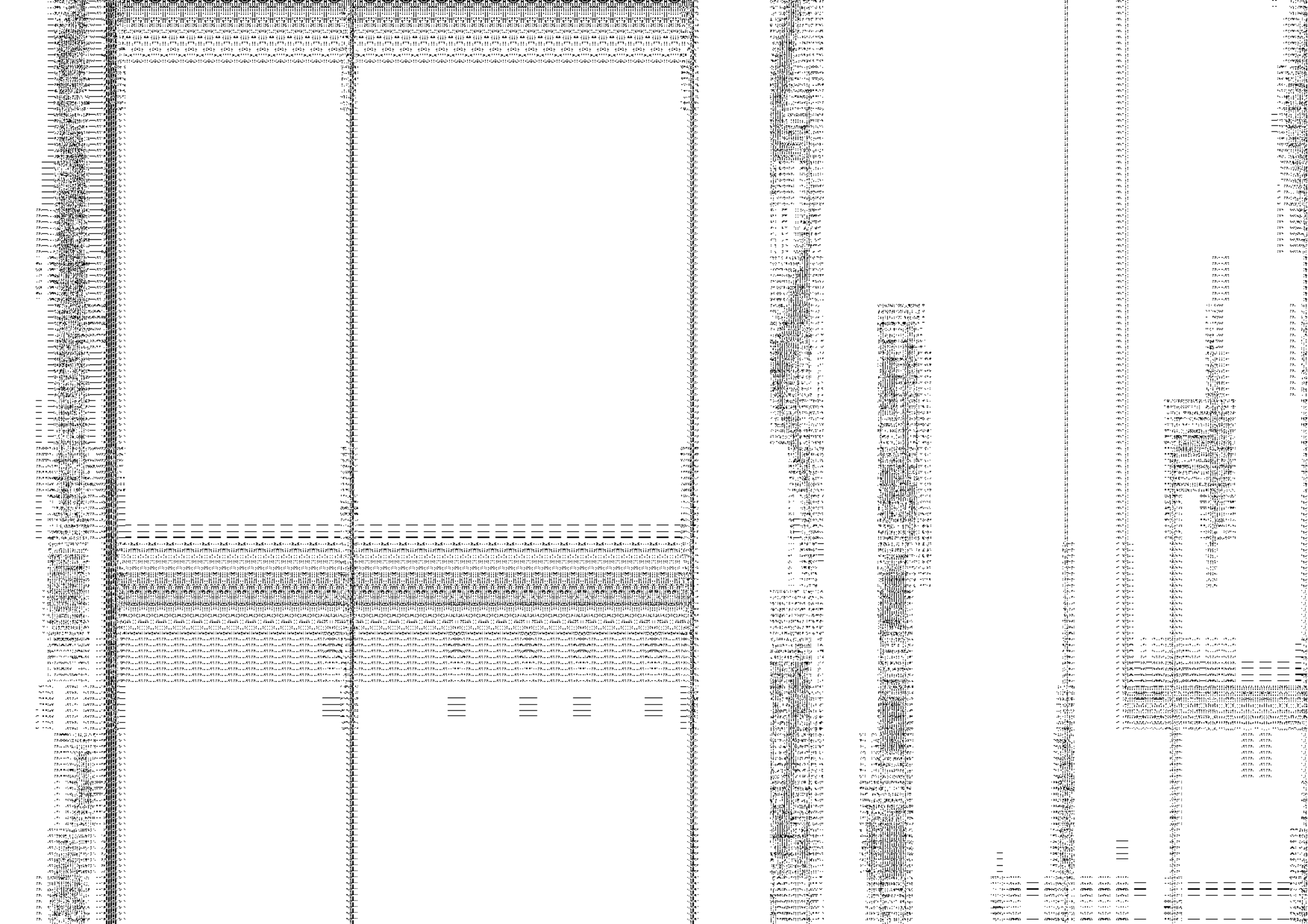
Guide Information: Dr.S.G.Srivani, Professor and Associate PG Dean, Dept of Electrical and Electronics Engg, RVCE, e-mail: srivanisg@rvce.edu.in

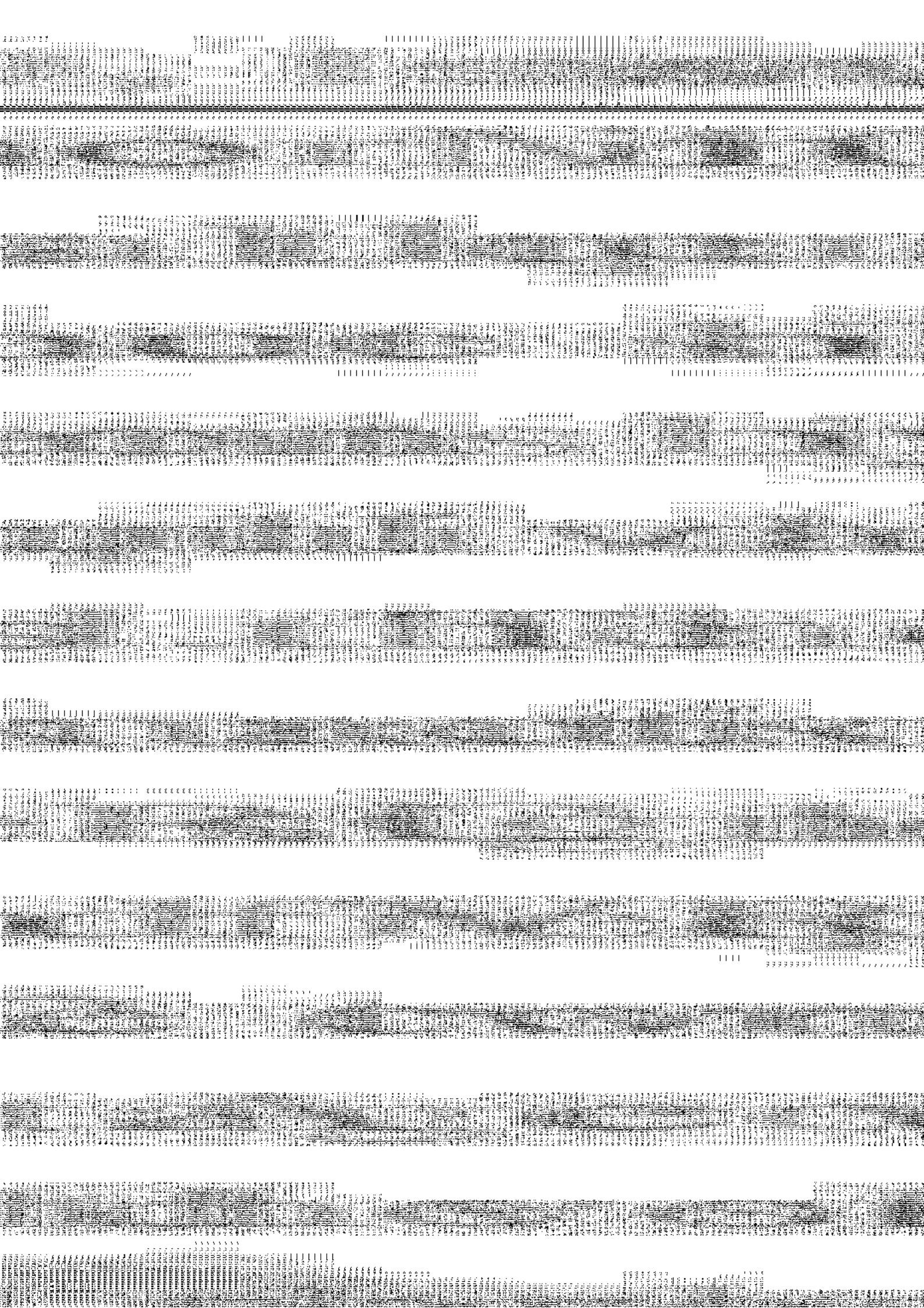


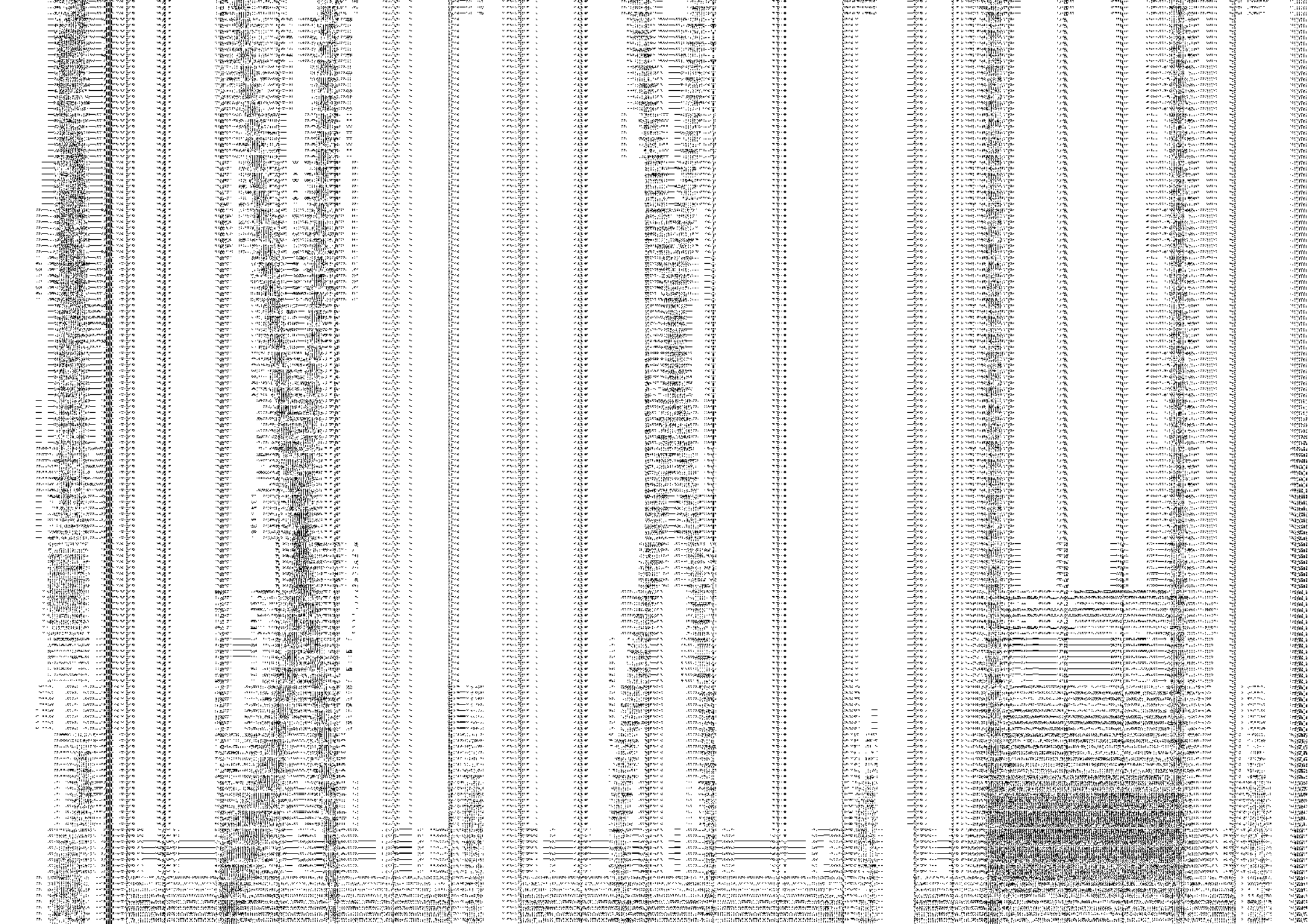


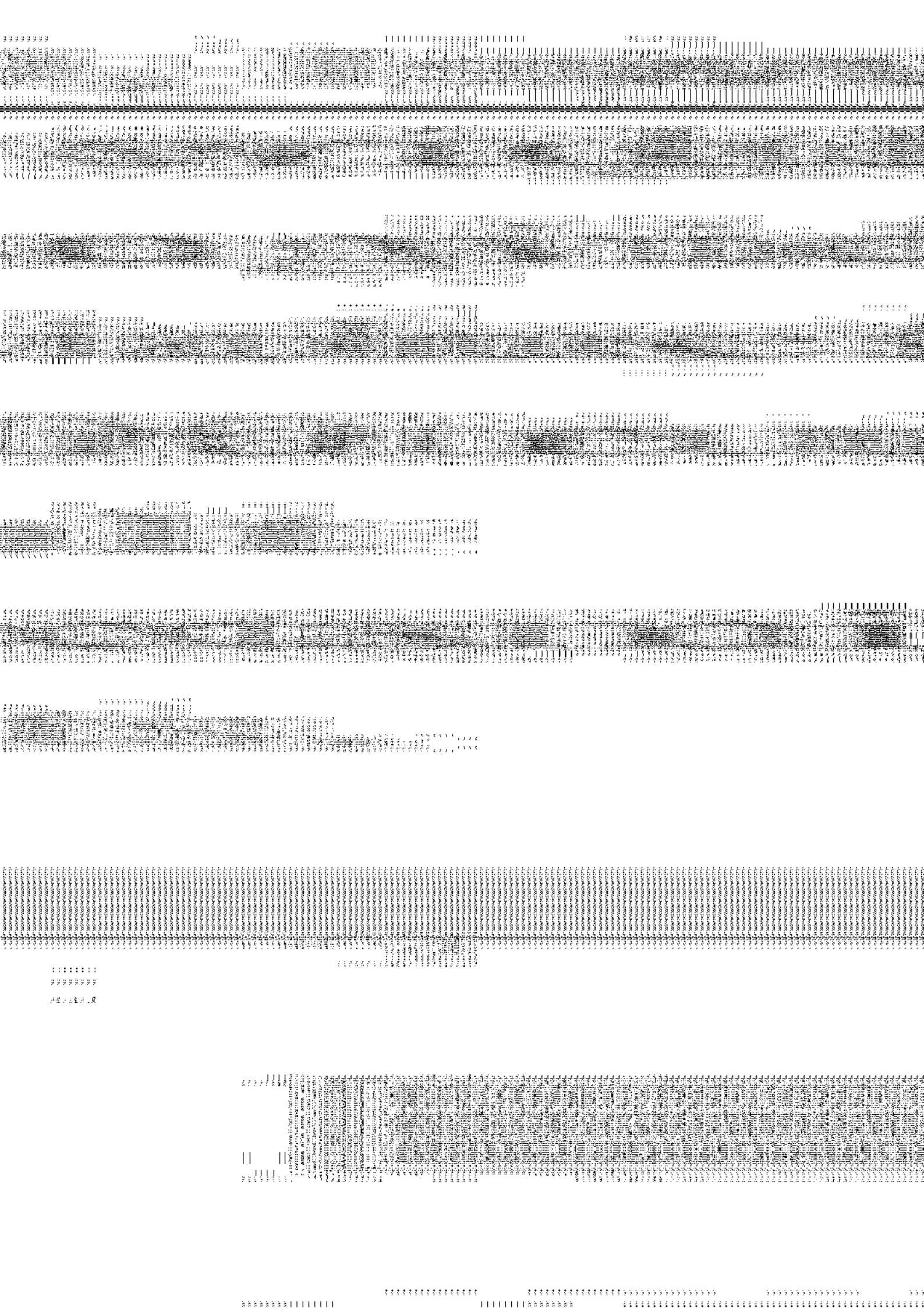


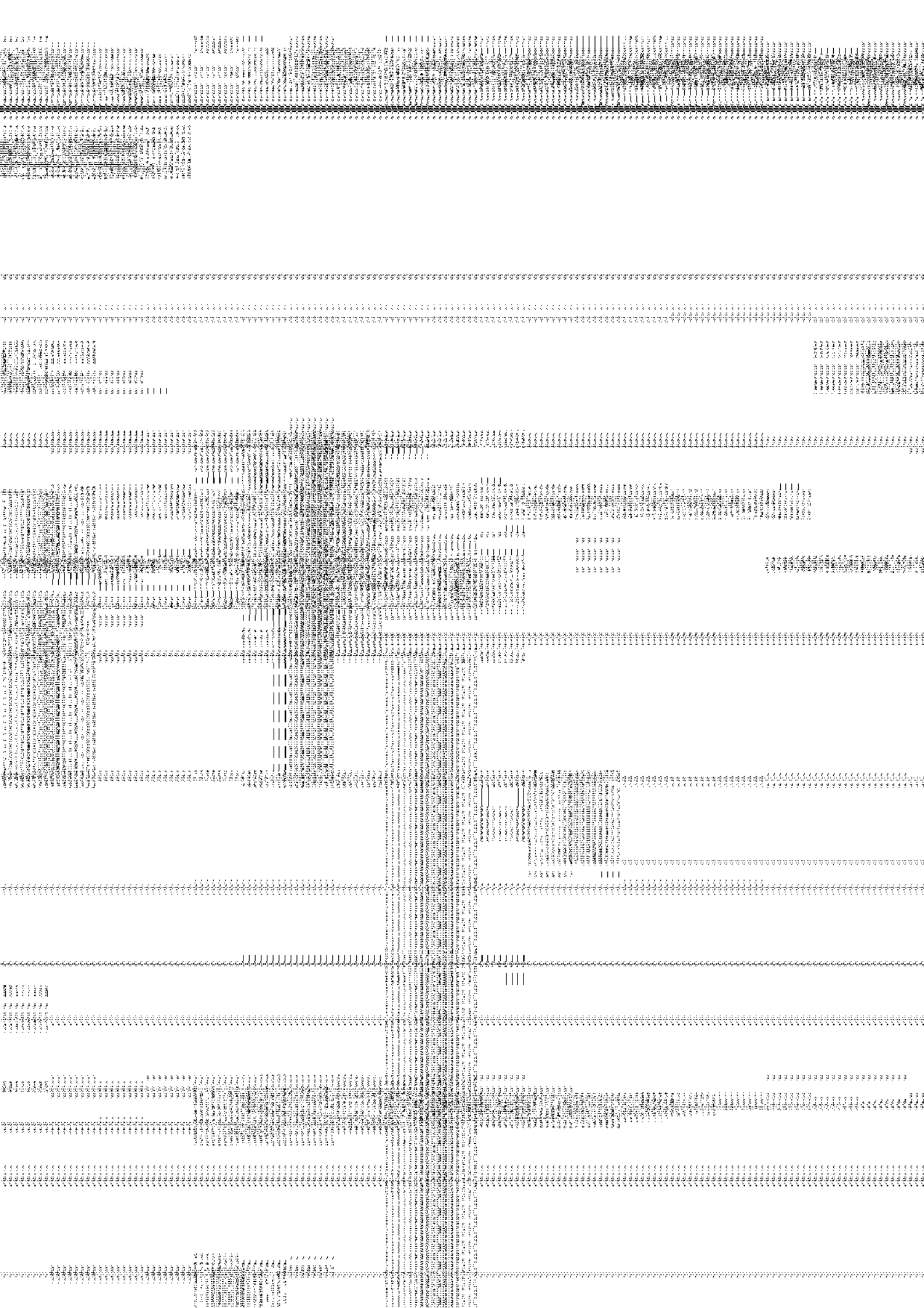


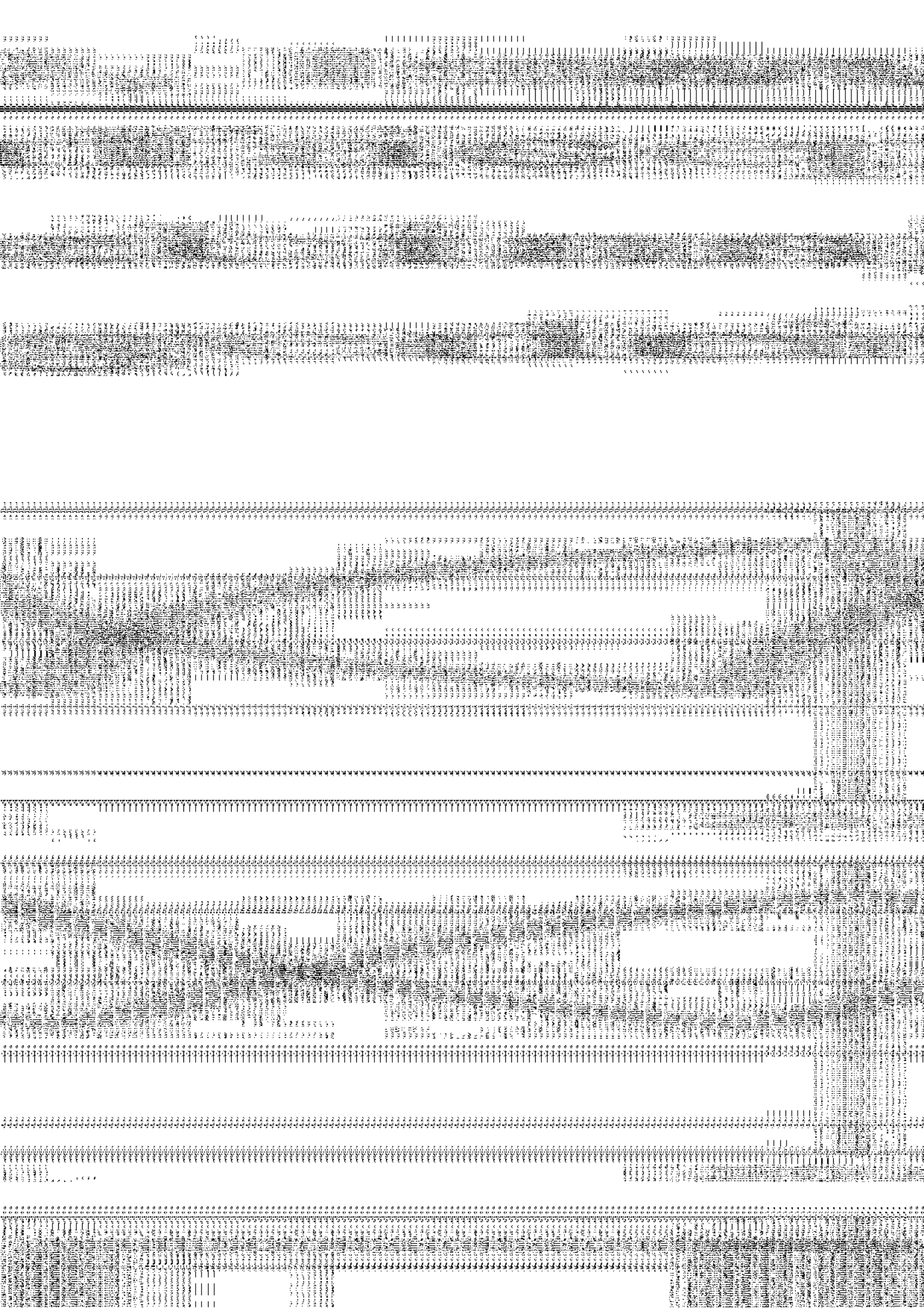


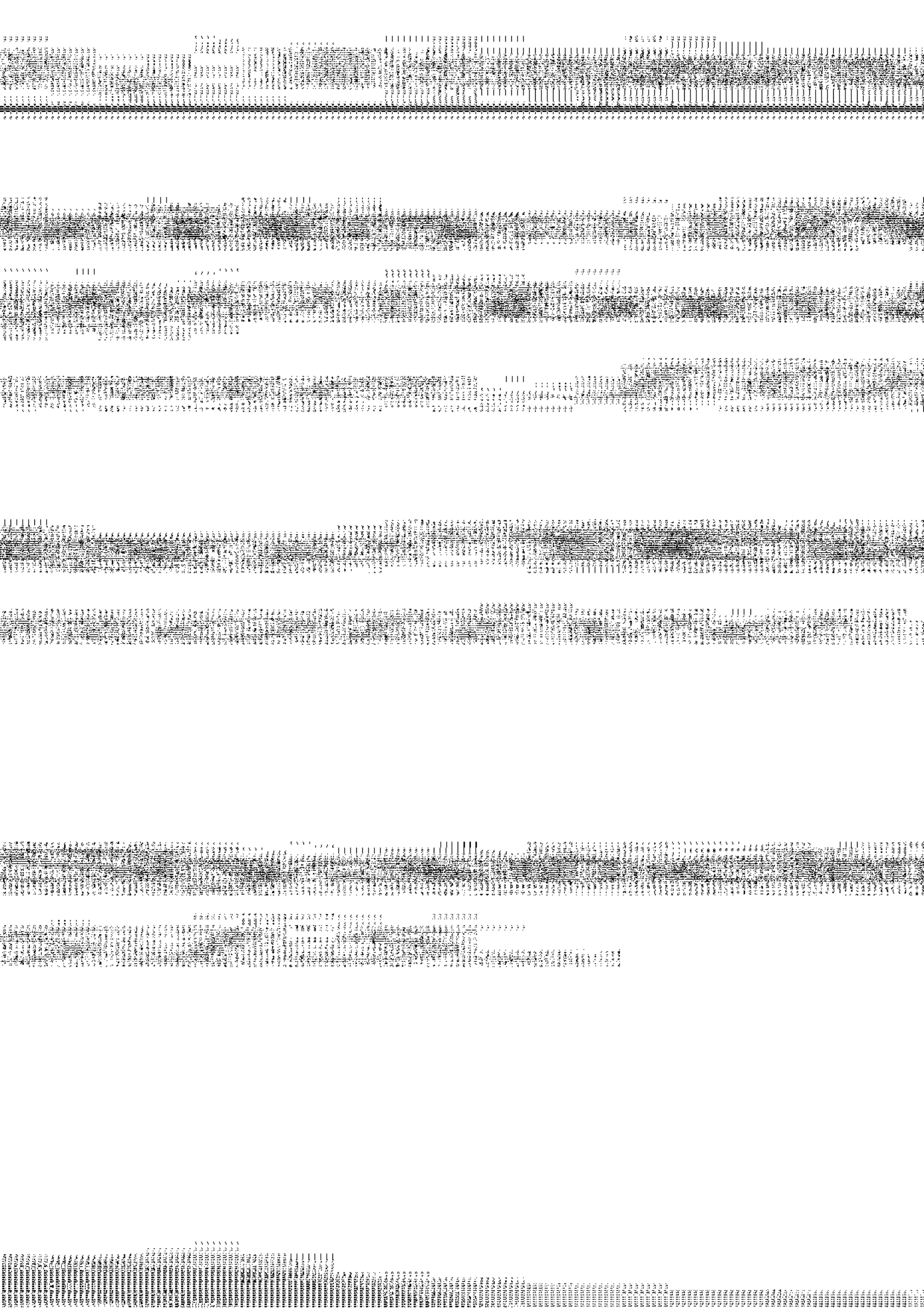


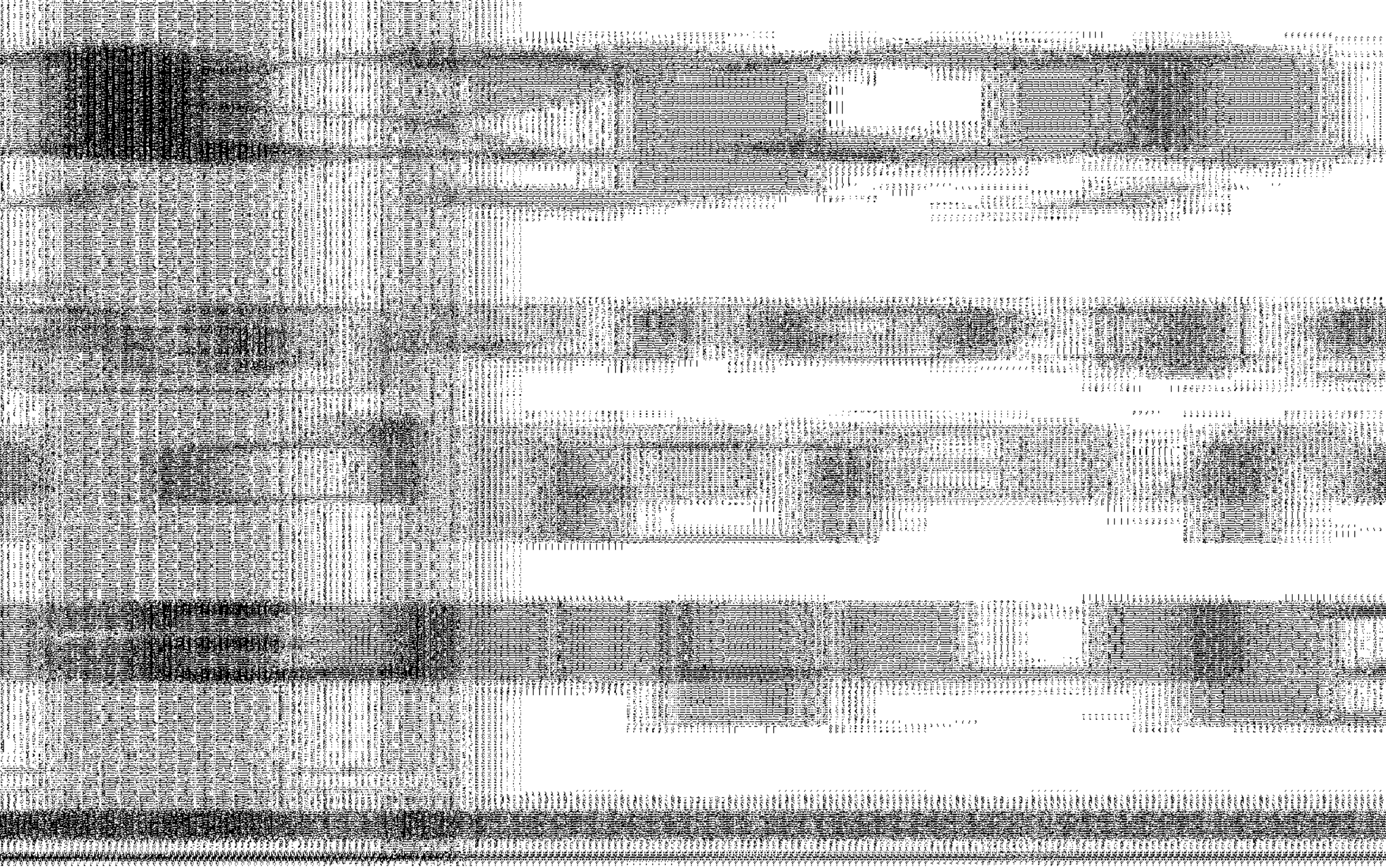


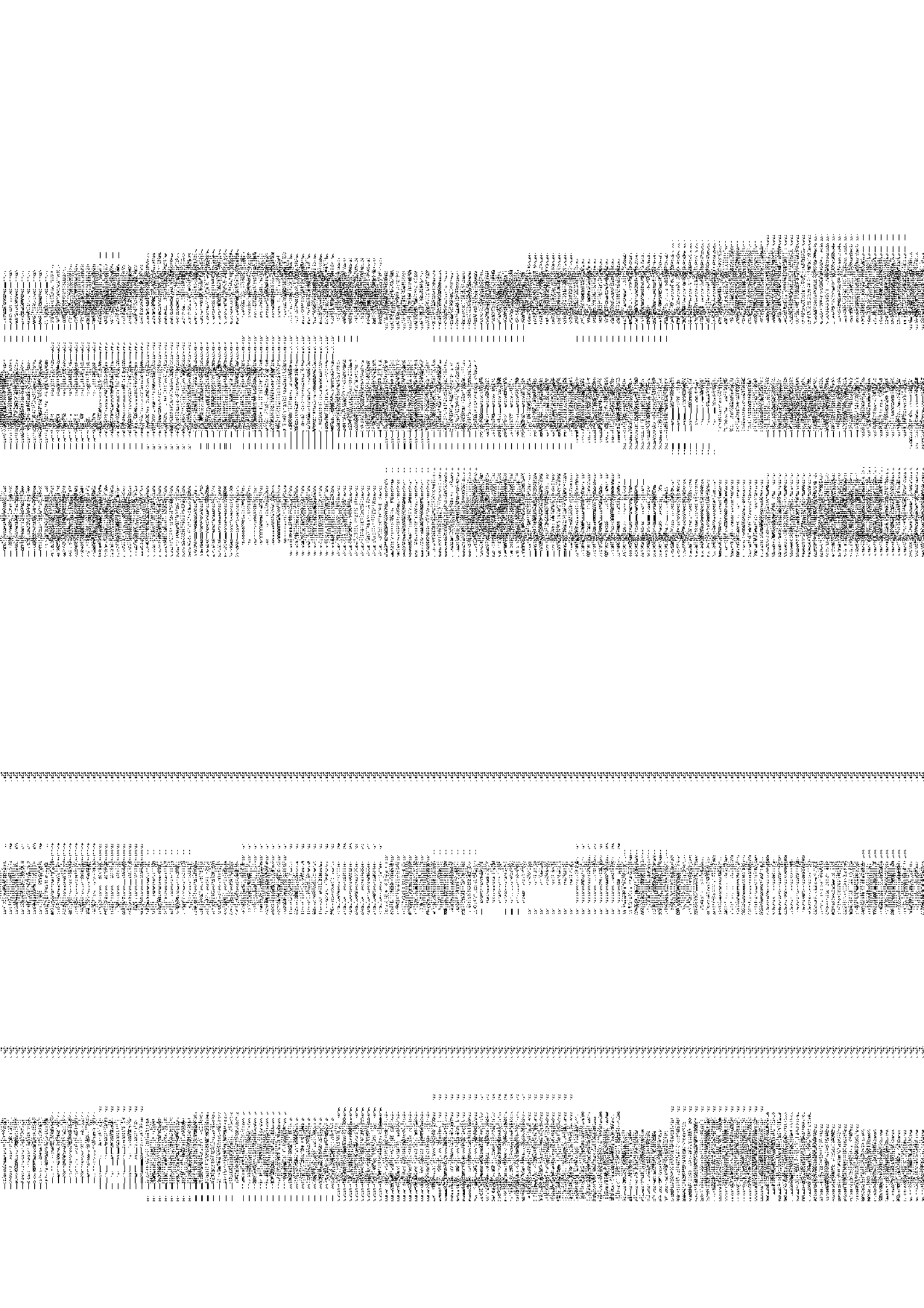












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Major Project: Phase-II Report

on

DESIGN AND IMPLEMENTATION OF MULTIPLE OUTPUT FORWARD CONVERTER WITH VOLTAGE FEED FORWARD CONTROL FOR SPACE APPLICATION

18MPE41

Submitted by

VARSHITHA R

USN: 1RV20EPE17

Under the Guidance

of

Dr. Hemalatha J N
Associate Professor
Electrical & Electronics Engg. Dept.
RV College of Engineering
Bengaluru – 560059

Boopendra Kumar Singh
Director
Centum Electronics Limited
Bengaluru – 560064

Submitted in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY

in

POWER ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

2021-22

RV COLLEGE OF ENGINEERING®

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Bengaluru– 560059

CERTIFICATE

Certified that the project work titled **"Design and Implementation of Multiple Output Forward Converter with Voltage Feed Forward Control for Space Application"** carried out by **Varshitha R, USN: 1RV20EPE17**, a bonafide student, submitted in partial fulfillment for the award of **Master of Technology** in **Power Electronics** of **RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi,** during the year **2021-22**. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

Dr. Hemalatha J N	**Dr. S G Srivani**	**Dr. K. N. Subramanya**
Associate Professor,	Head of Department,	Principal,
Department of EEE,	Department of EEE,	RVCE, Bengaluru–59
RVCE, Bengaluru –59	RVCE, Bengaluru–59	

Prof. & Head
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Name of the Examiners	**Signature with Date**
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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Bengaluru– 560059

DECLARATION

I, Varshitha R, student of fourth semester M.Tech in **Power Electronics, Department of EEE,** RV College of Engineering®, Bengaluru, declare that the project titled **"Design and Implementation of Multiple Output Forward Converter with Voltage Feed Forward Control for Space Application"**, has been carried out by me. It has been submitted in partial fulfilment for the award of degree in **Master of Technology** in **Power Electronics** of RV College of Engineering®, Bengaluru, affiliated to Visvesvaraya Technological University, Belagavi, during the academic year **2021-22**. The matter embodied in this report has not been submitted to any other university or institution for the award of any other degree or diploma.

Date of Submission: 18/07/2022

Signature of the Student

Student Name: Varshitha R

USN: 1RV20EPE17

Department of Electrical and Electronics Engineering

RV College of Engineering®,

Bengaluru-560059

CENTUM

30th May 2022

TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Ms. Varshitha R (USN: 1RV20EPE17),** student of R V College of Engineering has completed the project work entitled **"Design and Implementation of Multiple output forward converter with voltage feed forward control for space application"** in partial fulfilment for the award of **Master of Technology in Power Electronics** during the time period 2021 - 2022 under the guidance of **Mr. Bhoopendra Kumar Singh (Director – Power Electronics Design).**

During the period her conduct was good.

We wish her good luck and success in her future endeavors.

Thanking you,

Yours faithfully,

For Centum Electronics Limited

Soumya A

Authorized Signatory

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CIN - L85110KA1993PLC013869

ACKNOWLEDGEMENT

Any achievement, be it scholastic or otherwise does not depend solely on the individual efforts but on the guidance, encouragement and cooperation of intellectuals, elders and friends. A number of personalities, in their own capacities have helped me in carrying out this project titled, "**Design and Implementation of Multiple Output Forward Converter with Voltage Feed Forward Control for Space Applications**". I would like to take this opportunity to thank them all.

Firstly, I deeply express sincere gratitude to my guide **Dr. Hemalatha J N**, Associate Professor, Department of Electrical and Electronics Engineering, for her patience, valuable guidance, suggestions, advice and assistance throughoutthis project. she has been a constant and regular source of encouragement to me during this period.

I would like to express my thanks to **Dr. S.G Srivani**, Professor, Head of the department and Associate Dean, P.G. studies, Department of Electrical and Electronics Engineering, RVCE, Bengaluru, for her motivation and constant support throughout thisproject.

I owe my deepest gratitude to **Dr. K N Subramanya**, Principal, RVCE, Bengaluru, for his support towards completion of this project.

It is a genuine pleasure to express my deep sense of thanks and gratitude to **Boopendra Kumar Singh,** Director, **T.K Nagaraju**, Assistant Manager and **Nishanth B Kulkarni**, Senior Engineer, Design Team at Centum Electronica Limited, Bengaluru. Their dedication and keen interest above all overwhelming attitude to help me has been the main reason for me to be able to complete my work.

I would like to thank all the faculty members and non-teaching staff of the Department of Electrical and Electronics Engineering, RVCE for their constant support.

I am indebted to my parents for their constant support and encouragement throughout my life. I thank all my friends provided me with valuable suggestions to improve the project.

Varshitha R

Power Electronics

Department of Electrical and Electronics Engineering

RV College of Engineering

Bengaluru-59

ABSTRACT

DC-DC converters are power converters, used to provide regulated output power. Various applications like telecom, industrial, automotive, military and aerospace sectors use DC-DC converters to power up the devices. Linear Power Supplies are less efficient, complex construction, heavy size. Switched Mode power supplies has become conventional in space grade application than linear power supplies, because of higher efficiency as switching elements avoids operation in active region but operates either in saturation or cut-off region, reduces power losses. The other critical aspects are compact size, lightweight and high reliability to operate under intense temperature conditions. Forward Converter is used for safety purpose, the converter is operated with isolation. The Converter is designed to meet some basic requirements like regulated output, electricalisolation and multiple outputs.

The work was aimed at design and implementation of Multiple Output Forward Converter with Feed-Forward Control for Space Applications. Voltage feed forward mode control technique was implemented to regulate the output voltage, also used to modulate pulse width for MOSFET switch. The main specifications were, an input voltage in the range of 26 V to 45V, considered duty of cycle 0.6. The Forward Converter was designed with 250 kHz switching frequency using PWM controller IC. Converter had inherent features such as overvoltage protection, Input undervoltage protection, and external disable inherent features circuit. Under ambient temperature, the electrical test was carried out to validate the design results.

Simulation of the proposed Forward Converter was performed using LTSPICE software, the obtained simulation results were, regulated output voltages of 24V,12.7V,5.6V and 3.8V and output currents of 4.A, 0.25A, 0.1A and 1A respectively. Hardware implementation was carried out for proposed converter and tested for various input and load conditions to validate the design. Experimental results proved that the efficiency more than 80% and line and load regulations less than 1%, cross regulation less than 2%, the output voltage ripple less than 100 mVp-p for 24V and 12.7V, less than 50 mVp-p for 5.6V and 3.8V.

LIST OF PUBLICATIONS

Publication Type	Publication Details
Journal	Varshitha R, Dr.Rudranna Nandihalli, T.K Nagaraju Nishanth B Kulkarni, B.K Singh, "Implementation of Multiple Output Forward Converter with Voltage Feed Forward Control for Space Application", *Journal of Emerging Technologies and Innovative Research (JETIR)*, pp 533-540 Vol No 9 Issue 6 June 2020

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GLOSSARY

CS	:	Conducted Susceptibility
DFD	:	Data Flow Diagram
DSO	:	Digital Storage Oscilloscope
EMC	:	Electromagnetic Compatibility
EMI	:	Electromagnetic Interference
IC	:	Integrated Circuit
LDO	:	Low Drop Out
LED	:	Light Emitting Diode
MOSFET	:	Metal Oxide Semiconductor Filed Effect Transistor
OCP	:	Over Current Protection
OPAMP	:	Operational Amplifier
OVP	:	Over Voltage Protection Circuit
PCB	:	Printed Circuit Board
POL	:	Point of Load
PSM	:	Power System Module
PWM	:	Pulse Width Modulation
RMS	:	Root Mean Square
SAC	:	Space Application Centre
SMPS	:	Switched Mode Power Supplies
SOA	:	Safe Operating Area
UVL	:	Under Voltage Lockout
UVP	:	Under Voltage Protection Circuit

CHAPTER 1

INTRODUCTION

Power supply unit forms an interface between power source and the electric load. The main function of the power supply unit is to modulate or convert the available electrical energy from the power supply into the form required by the load. It is quite rare that the power source directly matches the requirements of a particular load [1]. So, the power supply units find extensive applications in various industries. Input power source is either AC or DC, while the load is either a motor, an electronic equipment, or a computer [2]-[4]. The electronic devices require DC power for functioning. The electronic devices are different in nature, the requirements do not meet with a single, fixed DC power source. DC power supply unit has to be installed between the power source and the end electronic circuits, are considered as loads [5]-[8].

Switched Mode power supplies has become more conventional in space grade application than linear power supplies, because of higher efficiency as switching elements avoids operation in active region but operates either in saturation or cut-off region, reduces power losses [9]-[12]. The other critical aspects are compact size, lightweight and high reliability to operate under intense temperature conditions [13]-[15]. The main applications of SMPS are battery charging, Military, biomedical equipment and electronic devices [16]. DC-DC isolated converters are significant to obtain regulated outputs, provides electrical isolation with multiple outputs and are widely used in computer power supplies, uninterrupted power supplies and telecommunication [17]-[19].

Forward converter is most widely used for space application among DC-DC converter becauseof its high transformer utilization, more efficient and is often chosen for output power under 200W and voltage range of 60V- 200V [20]. Power electronic circuits for deep spacemissions are to be designed such that they operate reliably and efficiently under extreme temperature [21]-[23]. Research and development of electronics capable low temperature operation and their utilization in space missions along with fulfilling the advanced technology requirements, also contributes towards improving circuit performance and efficiency improvement thus reducing the cost.

1.1 Overview

Power Electronic Devices are performed as connection between the sources and loads. In many of the applications DC-DC Converters are employed and stability is the main consideration. In order to maintain the system stability, Feedback of Feed Forward Voltage Mode Control is employed. Type 2 compensation network is used for the system circuit analysis. PWM Controller IC is designed with 250 kHz switching frequency. The IC is selected for better soft start, maximum control on duty. The MOSFET switch is employed with snubber circuit, in order to reduce the voltage stress on the switch.

The protection circuits are employed to protect the Forward Converter. Over Voltage Protection Circuit is designed, it includes Voltage shunt regulator TL431 IC. The IC is designed to maintain the reference voltage of 2.5 V. The signal is provided to the operational amplifier. The inverting terminal is provided with 2.5 V reference and non- inverting terminal is provided with error voltage feedback. The error voltage feedback obtained is more compared to the reference voltage, the output of the operational amplifier is high. The signal is providedto the pulse width modulation Controller IC. The controllers stop the signal to the MOSFET switch. The operation of the converter is now turned OFF.

1.2 Specific Details

Multiple Output Forward Converter with Feed Forward Control is to be design for Space Applications. The input voltage ranges from 26 V to 45 V with nominal voltage of 37V.The Duty cycle is 0.6 with switching frequency of 250 kHz reduces the size of the transformer, Filter Inductor and Filter Capacitor. The output voltages to be obtained are 24V, 12.7V, 5.6V and 3.8 V, and the respective output currents are 4.3A, 0.25A,1.0A and 0.1 A. The specification for output voltages ripple is to be less than 100mVpp for 24V and 12.7V and less than 50 mVp-p for 5.6V and 3.8V. The voltage for the Over Voltage Protection Circuit is 125% of the output voltage and for current is 150%.

1.3 Literature Review

A review is presented on various DC-DC converters such as isolated and non-isolated. In the isolated converter, forward topologies are capable of providing the improved efficiency, lower switching losses, low voltage and current stresses of the switches. Many non-isolated converters provide high voltage gain such topology provides competitive solution for different converters [1]-[3].

The miniaturization of the converter is achieved by selecting high switching frequency reduce size and mass of magnetics and output low pass filtering components. Multiple-output converters have been widely used to obtain individual outputs. Compared with conventional separate converters, the advantage of multiple outputs is to have a lower

number of active and passive components [4]-[6].

The overall efficiency of flyback converter is lower than forward converter. because of core and copper losses on magnetic components [7].

Power Amplifiers need switching power to process received radio frequency signals. Depending on rise and time of the signal processing technique of power supply, high current has to be discharged in very short time interval. In this paper, challenging aspects of designing 33Wmultiple outputs forward converter with tight load regulation and quick transient response [8]-[10].

Feed - forward method responds to control signal of the predefined and it is not depending on the load variation. It is used to reduce the sudden variations in the output voltage due to input line voltage changes and provides the better regulation and line transients [11]-[13].

Multiple-output converters have been widely used where individual outputs are required. Compared with conventional separate converters, the advantage of multiple outputs is to have a lower number of active and passive components [14]-[15].

Low drop out regulators are used as post regulators, provides constant DC output Voltage irrespective of input voltage change [16].

Forward converter has been utilized in low and medium force applications because of the cost viability, effortlessness, wide information and yield variety. Many reset methods are created to reset the transformer charging current [17]-[19].

Considering the Electromagnetic Compatibility during the initial phase of the design ensures a smooth and optimal product design. Component selection, proper design techniques for Electromagnetic interference reduction and Component placement are essential for better EMI performance of the product [20]-[21].

Snubber is non-dissipative. It is capable of resetting the transformer core along with reducing the spike across the power switch due to leakage inductance of the transformer [22].

Lossless snubber is associated across essential MOSFET for resetting of transition in off period (Toff), there by accomplishing wide scope of obligation cycle tasks. Likewise,it lessens the voltage stress forced on the MOSFET [23]-[25].

The signal processing technique of power supply, high current has to be discharged in very short time interval. In this paper, challenging aspects of designing 33W multiple outputs forward converter with tight load regulation and quick transient response [26].

1.4 Motivation

For space applications, the power density of Switched Mode power supplies is very critical as it determines the size and weight of the system. Reliability, robustness and low cost are other important factors. The switched mode DC-DC converters are most widely used power electronic circuit because of its high conversion efficiency. At high frequencies, size of transformer, filter inductor and filter capacitor are reduced considerably.

High frequency DC-DC converter is necessary in miniaturizing the power supply unit. Telecommunication modules are very sensitive to any voltage variations thus it is necessary to use switch-mode power supplies followed by post regulators in such applications.

1.5 Problem Statement

Design, Simulation and Implementation of Multiple Output Forward converter using Voltage feed forward control technique for Space application.

1.6 Objectives

The main objective of the project is to design and implement Multiple Output Forward Converter

- To design and implement 110 W Forward converter with Multiple Outputs.
- To design Voltage feed forward control technique to improve line transient performance and line regulation.
- To implement Low drop out regulators as post regulator to meet load and cross regulation.
- To implement overvoltage and undervoltage protection circuit.

1.7 Organization of Report

The project work is organized in seven chapters.

Chapter-1 consists of literature survey carried out to understand the issues in multiple output forward converters and solutions. It includes the problem definition, objectives of the project motivation behind carrying out this project and the methodology.

Chapter-2 includes basics of Forward Converter, the operation of forward converter with Feed-Forward Control and various modes of operation are discussed. Concepts of voltage mode feed forward control are discussed.

Chapter-3 consists of the proposed converter Block diagram with explanation of working and Methodology.

Chapter-4 presents the design details of forward converter and protection circuits

Chapter-5 describes simulation of Forward Converter using LTSPICE software and Hardware Implementation of the circuit.

Chapter-6 discusses the simulation and hardware of the proposed Forward Converter.

Chapter-7 includes the overall conclusion drawn from the project and the future worksthat can be carried out.

References includes the list of references referred in the successful completion of the project

CHAPTER 2

FORWARD CONVERTER TOPOLOGY

The chapter explains the Forward Converter topology principle with two modes of operation.

2.1 Forward Converter

Forward converter is an isolated version of buck converter. One of the most widely used topology for obtaining regulated dc voltage from an unregulated input. Forward converter is highly efficient and is often chosen for output power under 200W [2]. Forward converter is magnetically coupled, provides isolation between source and load.Forward transformer does not store energy hence, ferrite core is most widely used as core material, transforms energy instantly from primary to secondary winding for high power application with high voltage conversion ratio [5]. Reset winding has to be provided on the primary side to restore flux to zero value in every cycle to avoid saturation. The forward converter circuit is as shown in Figure 2.1.

Input voltage is applied to primary winding at the time switch Q is turned ON. Secondary voltage is reflected based on turns ratio. Diode D1 rectifies voltage and energy is stored in inductance L, is delivered to load during switch Q is in OFF condition. freewheeling diode D2 provides path for load current and constant voltage is maintained by output capacitance C

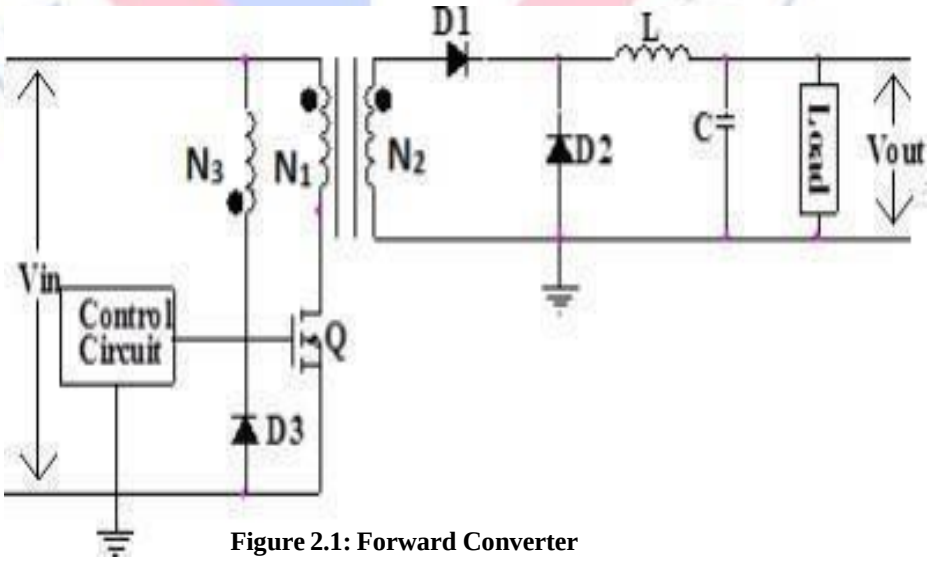


Figure 2.1: Forward Converter

The Brief operation of the forward converter is as follows

Mode 1: The switch is closed and the input voltage is applied across the primary winding of the transformer. Primary current starts to flow. The equivalent circuit is as shown in Figure 2.2. Due to the dot polarity of the transformer a voltage appears across the secondary winding and energy is transferred from primary to secondary. The voltage and current at the primary and secondary are related through the turn's ratio (Ns/Np) of the transformer [3].

As the switch is closed, the diode D1 becomes forward biased and the transformer secondary voltage appears across a low pass filter constituted by L and C. The high frequency ripple is filtered by the low pass filter and the output is delivered to the load. The freewheeling diode D2 remains OFF as it is reverse biased by the positive voltage appearing across its cathode. This mode is the powering mode as the input power is transferred to the load. Because of the opposite dot polarity, diode D3 is reverse biased and remains OFF.

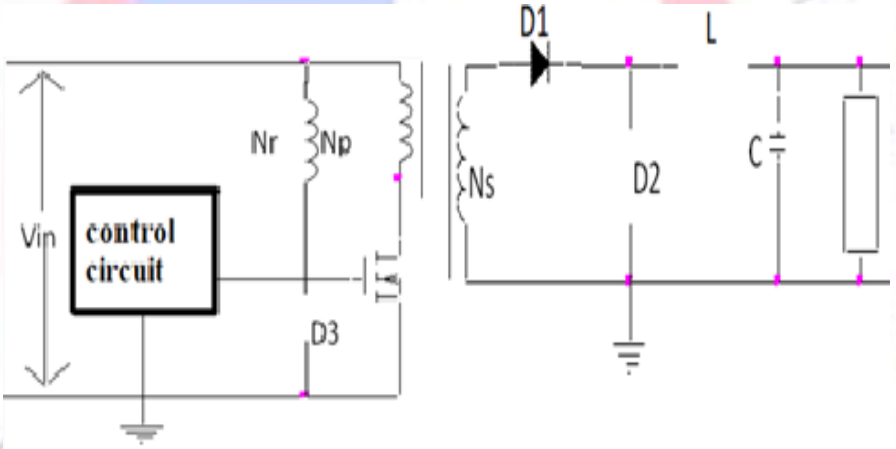


Figure 2.2: Forward Converter Equivalent Circuit During Mode 1

The equations governing this mode are as follows

Voltage across the primary winding Np is

$$V_p = V_{in} - V_Q \tag{2.1}$$

Voltage across the reset winding Nr is

$$V_r = \frac{N_r}{N_p}\left(V_{\text{in}} - V_Q\right) \tag{2.2}$$

Voltage across the secondary winding Ns is

$$V_S = \frac{N_S}{N_p}\left(V_{in} - V_Q\right) \tag{2.3}$$

Voltage at the cathode of Diode D1 is

$$V_b = \frac{N_s}{N_p}(V_{in} - V_Q) - V_{D1} \quad (2.4)$$

Voltage across the Output Inductor is

$$V_L = \frac{N_S}{N_p}(V_{\text{in}} - V_Q) - V_{D1} - V_{\text{out}} \quad (2.5)$$

Current flowing through the output inductor

$$I_L = \frac{\frac{N_S}{N_p}(V_{in} - V_Q) - V_{D1} - V_{\text{out}}}{L} * DT \quad (2.6)$$

Mode 2: This is the freewheeling mode. This mode begins at the switch opens. The transformer current falls to zero. But, the filter inductor at the secondary side maintains a continuous current to the load through the freewheeling diode D2. The forward diode D1 remains OFFduring this state. Due to the opposite dot polarity of reset and primary winding, diode D3 conducts and the magnetizing current flows in the opposite direction, thus resetting the core. The equivalent circuit is as shown in Figure 2.3.

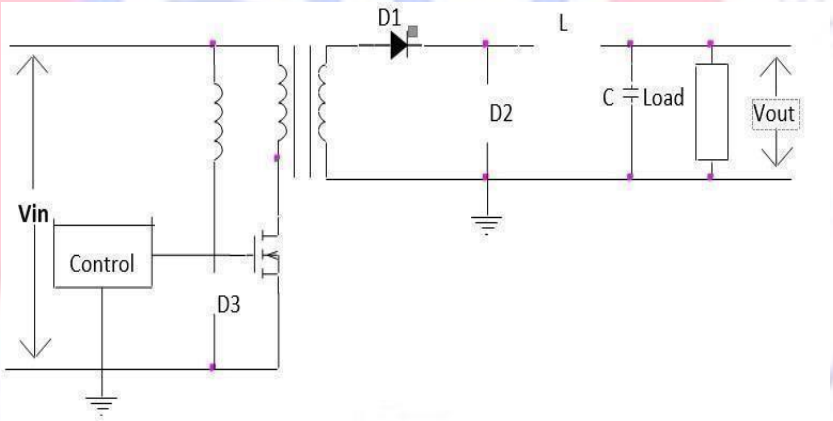


Figure 2.3: Forward converter Equivalent circuit during Mode 2

The equations governing this mode are as follows:

Voltage across the reset winding Nr is

$$V_r = -(V_{in} + V_{D3}) \quad (2.7)$$

Voltage across the primary winding N_p is

$$V_p = \frac{N_r}{N_p}(V_{in} + V_{D3}) \quad (2.8)$$

Maximum voltage that appears across the switch Q is

$$V_Q = \left(1 + \frac{N_p}{N_r}\right) V_{in\,max} \tag{2.9}$$

Voltage across the secondary winding N_s is

$$V_s = -\frac{N_r}{N_s}(V_{in} + V_{D3}) \tag{2.10}$$

Voltage across the output inductor

$$V_L = -V_{Out} - V_{D2} \tag{2.11}$$

Current flowing through the output inductor decreases

$$I_L = (V_{D3} - V_{Out})(1 - D) \tag{2.12}$$

From volt second balance, the output equation becomes

$$V_{out} = \frac{N_s}{N_P}(V_{in} - V_Q)D - V_D \tag{2.13}$$

Where description of the terms are:

Vin: Input Voltage

Np: Number of turns in the primary winding

Nr: Number of turns in the reset winding

Ns: Number of turns the secondary winding

VD3: Voltage drop across diode D3

D: Duty ratio

T: Time period

VD1: Voltage drop across diode D1

VQ: Voltage across the Switch Q

Vout: Output Voltage

Figure 2.4 shows the waveforms of forward converter operating in continuous conduction mode

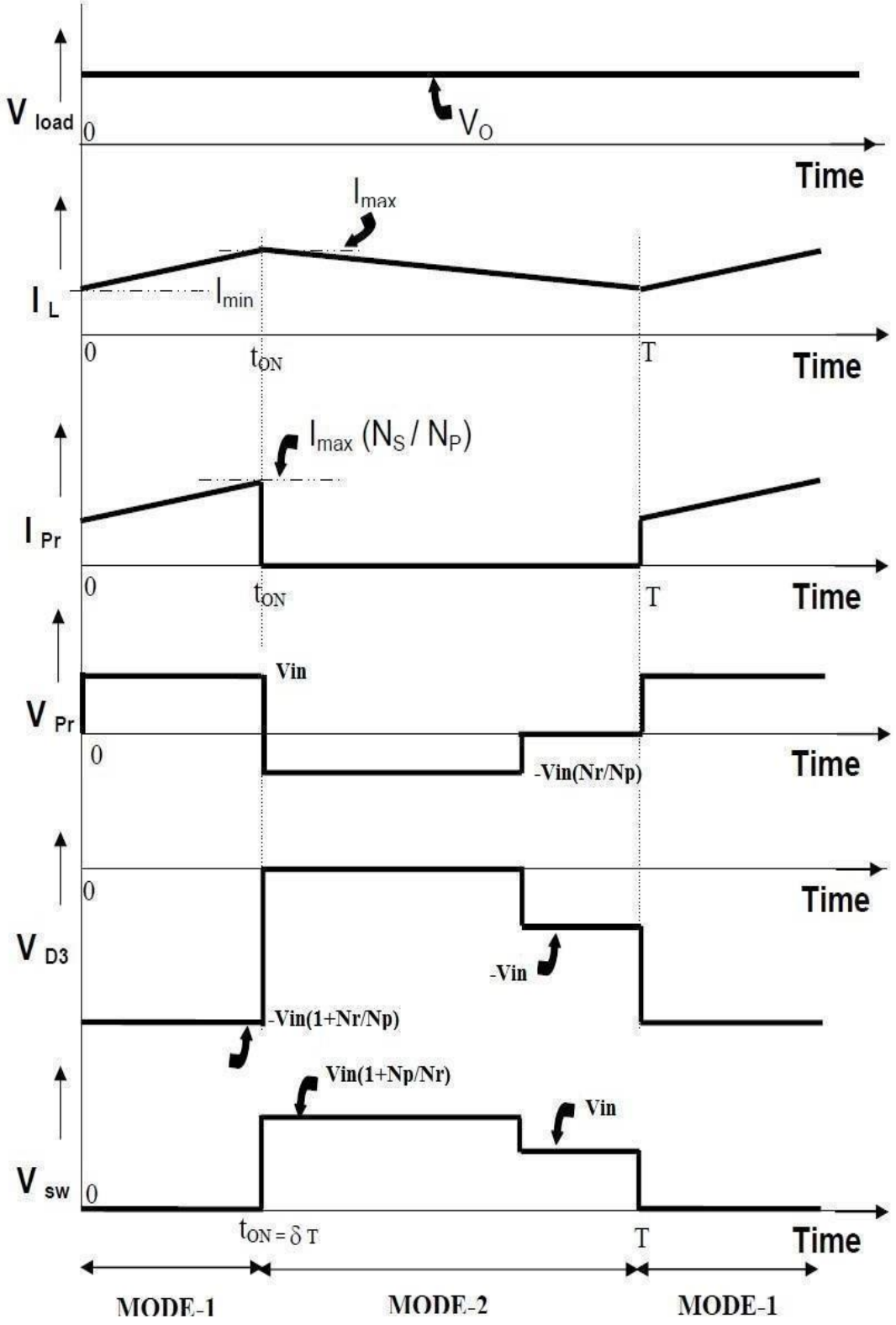


Figure 2.4 :waveforms of forward converter operating in continuous conduction mode.

2.3 Control Techniques

There are various control techniques available for DC-DC converters like

Voltage mode control

Voltage feed forward control

2.3.1 Voltage Mode control

Figure 2.5 shows a conventional voltage mode control circuit. The circuit has a voltage divider network, an error amplifier, a PWM modulator, a constant frequency sawtooth ramp and a reference voltage. Voltage divider network is used to scale down the output voltage so that an error signal be generated using an error amplifier. This error is proportional to the error between the scaled output voltage and the reference voltage. This error signal is compared with a fixed frequency fixed slope saw tooth ramp voltage to generate the desired PWM pulses and to drive the switch. Due to the negative feedback in the loop, error amplifier output changes such that duty cycle is modulated to maintain the constant output voltage. Impedances Z1 and Z2 are used to provide a proper gain, bandwidth and frequency compensation for the loop tobe stable under all operating condition [6].

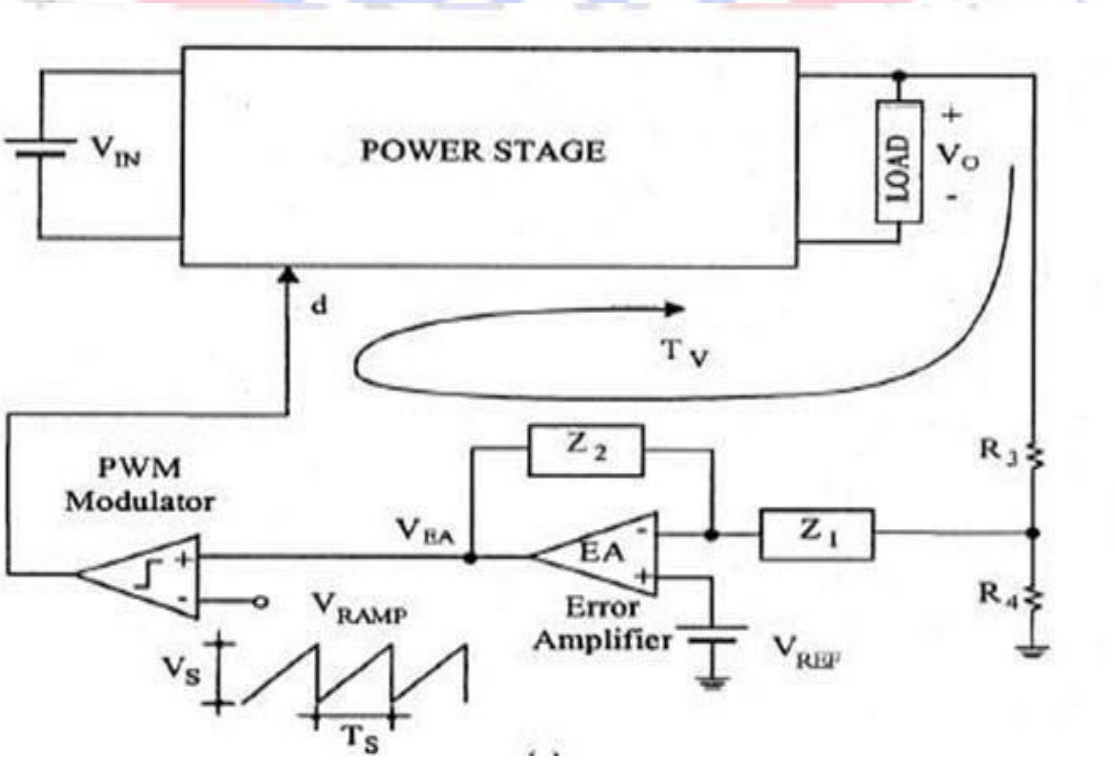


Figure 2.5: Block Diagram of Voltage Mode Control Method.

Figure 2.6 shows the transient response waveforms for the voltage mode control for a positive line voltage transient. At t=To, voltage Vin experiences a positive step change. Because of the slow response of the voltage feedback loop, the control voltage voltage error amplifier starts responding slowly after some time. The duty cycle remains unchanged in the event of sudden change in input voltage, the output voltage experiences a high voltage overshoot transient [7].

Thus, the voltage mode control technique suffers from a major drawback of slow response to input voltage transients. To fasten the response and to reduce the transient output voltage overshoot caused by the input voltage change, the duty cycle of the controller has to respond instantaneously to input voltage changes. This is accomplished by voltage feed forward control technique.

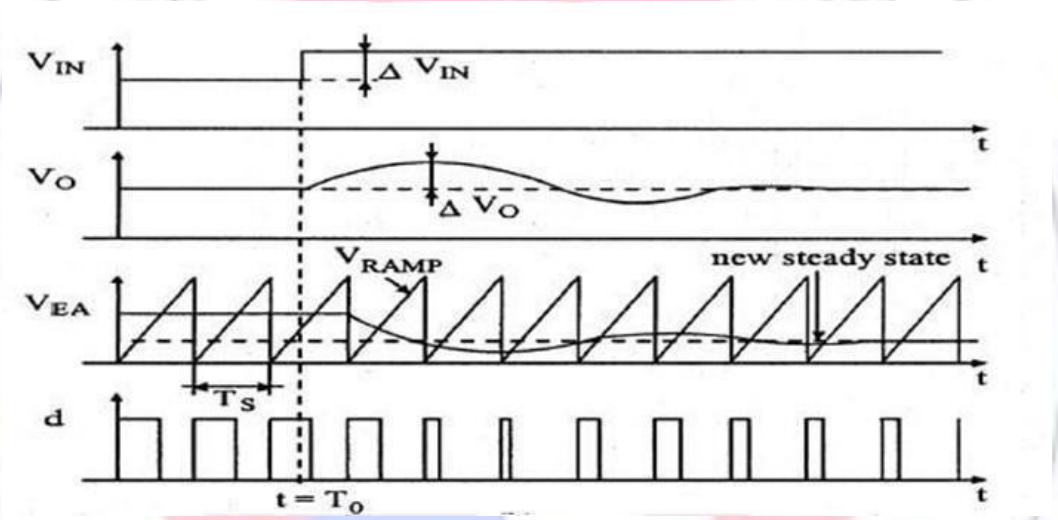
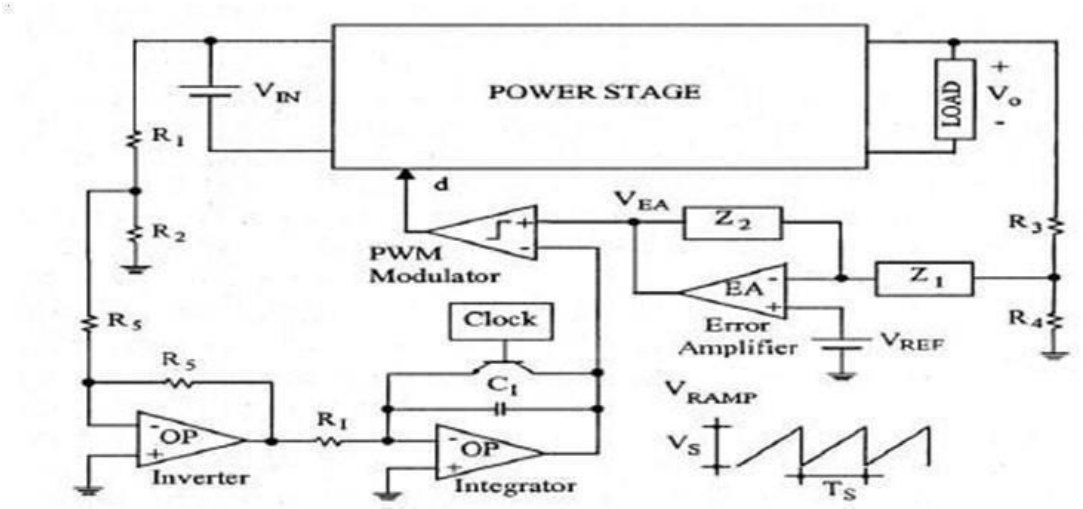


Figure 2.6: Key Waveforms During Step Change in Vin for Voltage Mode Control.

2.3.1 Voltage Feed Forward Control

The Block diagram of voltage feed forward control is demonstrated in figure 2.7. In this technique rather than fixed slant saw tooth incline, a slope to slope differs in relation to the voltage variety is utilized at the PWM Modulator input. The voltage is first detected and constricted utilizing the voltage divider comprised of Resistor R1 and R2. Itis then Inverted before being brought to the input to the integrator.

Integrator is reset at the beginning of each cycle by an outside fixed recurrence clock signal [9]. Since in this control method the slant of the slope is corresponding to the ramp is proportional to the input voltage, and the output voltage of the error amplifier is compared with this ramp to generate duty cycle. Any change in the input voltage causes immediate change in the duty cycle even if the bandwidth of voltage loop is very low [10].



.Figure 2.7: Block Diagram of Voltage Feed Forward Control

After the input voltage is increased, at t=To, the slope of the ramp increases causing the duty cycle to reduce immediately so as to maintain the output voltage constant as shown in Figure 2.8. Because of this instantaneous change in duty cycle, output voltage overshoot caused because of the input step change is decreased [8]. Any increase in input causes the decrease in duty cycle such that constant volt-second product is provided to the primary of the transformer. Thus, good line regulation is achieved.

The operation of the feed forward scheme is described by following equations.

$$V_s = \frac{V_{in}}{K} \quad (2.14)$$

$$D = \frac{T_{on}}{T} \quad (2.15)$$

The description is as follows:

D: Duty cycle

K: Constant

Vin: Input voltage

Vs: Peak to Peak sawtooth voltage

Vc: Control voltage

Input Voltage feed forward technique provides the following advantages:

- Improved line transient performance.
- Variation of Vo from Vin dependence minimizes the error Amplifier gain requirements maintaining the adequate regulation.

- The audio susceptibility of the feed-forward method is good because of the cycle-by cycle compensation for input voltage variations.
- The constant volts-second product of the main transformer primary allows the designer to optimize the size and cost.

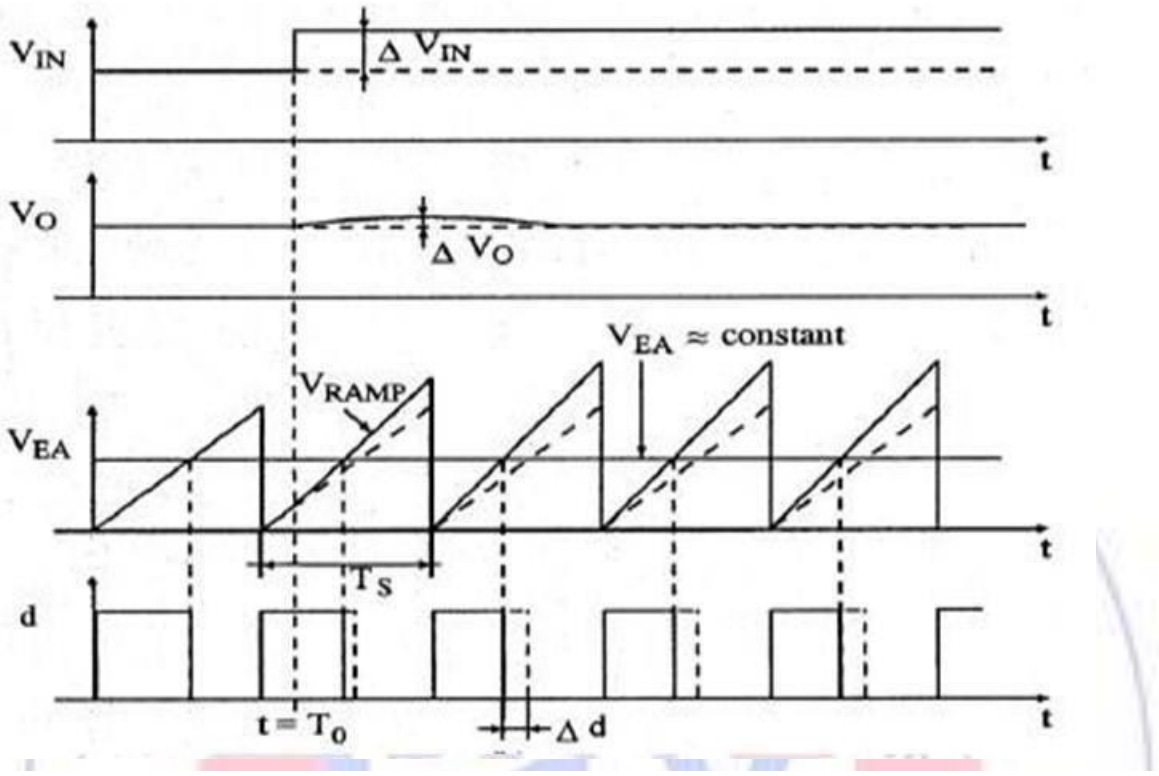


Figure 2.8: Key Waveforms During Step Change in Vin For Voltage Mode Feed ForwardControl.

2.3 Summary

A detailed working and analysis of Forward converter has been discussed with two modes of operation. This was followed by a brief discussion on the principle of Feed- Forward Control and voltage control.

CHAPTER 3

METHODOLGY AND BLOCK DIAGRAM

The chapter includes the brief explanation of methodology of the Forward Converter to be employed in the project. The chapter also briefly explains the working of the converter circuit and process flow for the simulation and hardware implementation and contains the description of block diagram of the project.

3.1 Methodology

The methodology involved in developing the work is as shown in Figure 3.1

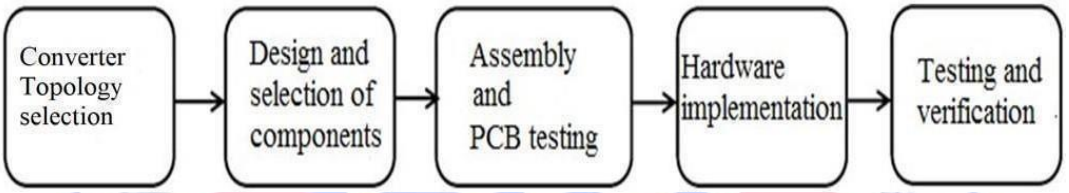


Figure 3.1: Methodology Involved in Developing Work

- **Converter topology Selection:**

Efficient converter topology is selected by comparing with various topologies. Theselected topology in this project is "single-switch forward converter" [3].

- **Design and selection of components**

A forward converter with Multiple output for a wide-range of input has to be designed. The designing of forward converter involves design of transformer, selection of the switching devices, selection of secondary MOSFETS, design of filter components and design of inductor. The tools used for design is "MATHCAD", and for schematics and simulations are "ORCAD" and "LTSPICE"

- **Simulation Analysis**

For the Proposed Forward Converter simulation has to be carried out using LTSPICE software. The feedback is required to be provided with Type 2 Compensation circuit.

- **Hardware Implementation.**

The assembled PCB needs to be checked and the test setup is made for the analysis and testing purposes.

- **Testing and verification**.

The converter needs to be analyzed and the performance of converter is tested after its implementation various input and output load conditions.

3.2 Block diagram

The 110W Multiple output DC-DC Converter is realized based on the specifications obtained by the Space Application Centre (SAC). Figure 3.2 shows the Detailed block diagram of the power supply. The power supply is provided with four Numbers of isolated outputs (24/4.3A ,12.7V/0.25A,3.8V/1.0A & 5.6V/3A) that are realized using forward followed by buck converter and low drop out regulators

Input Bus voltage (26V-45V): Range is set based on the requirements of Input under voltage protection) is connected directly to power supply through EMI filter that is designed to meet the differential mode CE and CS tests requirement. Filtered input is provided to primary side of the forward transformer; start-up circuit generates initial voltage for PWM Controller circuit of forward converter. PWM Controller turns ON and initiates gate Pulses atswitching frequency. With this switching action of MOSFET's, Input Bus voltage is appliedto Forward transformer and energizes it. Feed-forward voltage topology is being used forfast response of closed loop control with change in line voltage or load.

The primary side of Forward Converter is energized, the MOSFET switch is turned ON. The primary winding is applied with supply voltage. According to the number of turns the is varied, it is regulated using the feedback circuit. On primary side of forward transformer secondary winding voltage is induced. Bias winding is used to the bias voltage to power the controller circuits. The bias winding voltage is kept higher than the start-up circuit voltage so that a PWM controller circuit starts drawing the current from the bias winding instead of the start-up circuit [15]. The bias voltage is considered for feedback for the PWM controller. Hence bias winding act as the House Keeping Bus and continue to power the PWM IC and associated ICs.

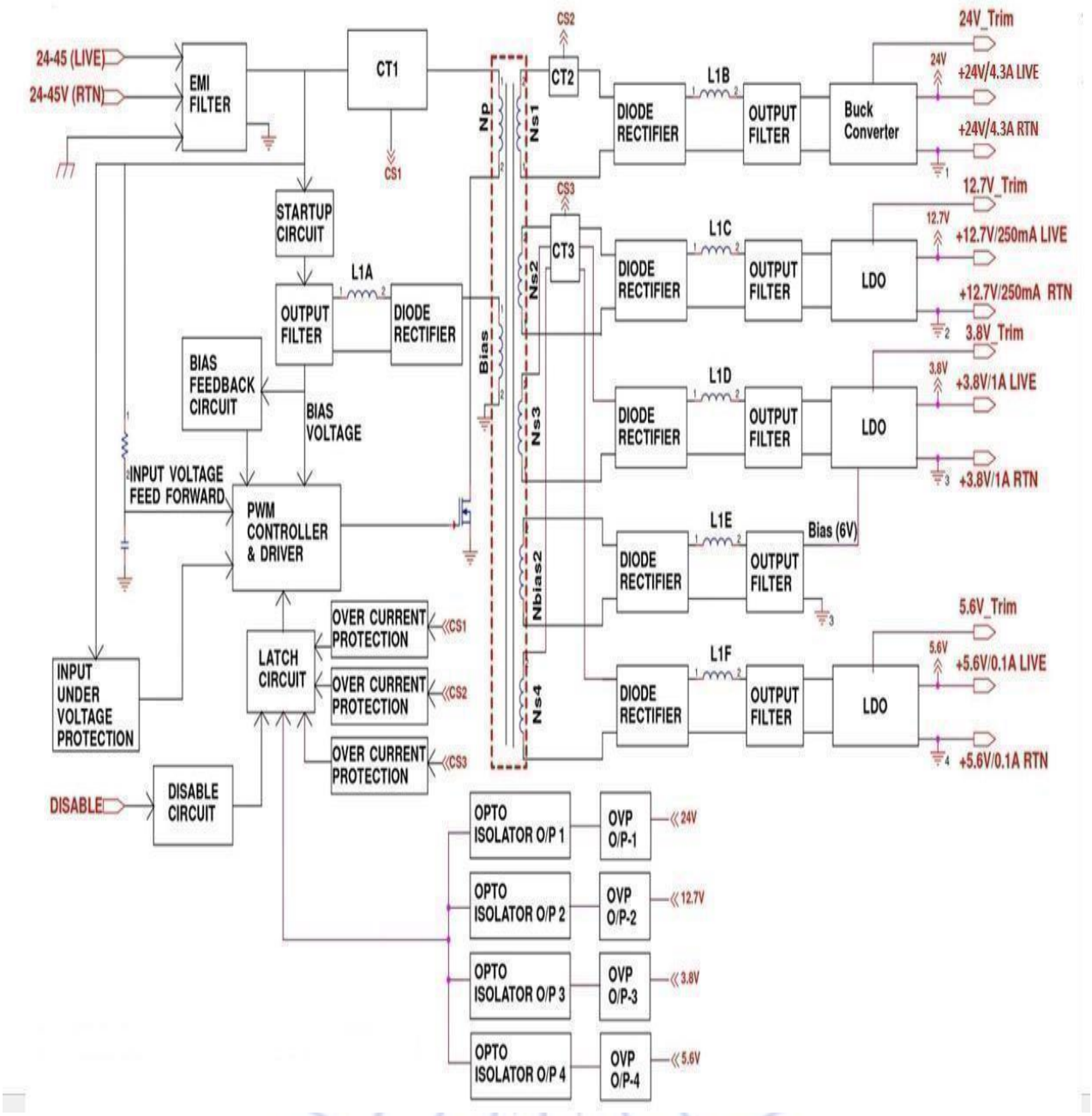


Fig 3.2 Block diagram of Multiple output forward converter

The Secondary side voltage is rectified and filtered and connected to buck converters and Low drop out regulators for generating regulated outputs.

The Functions of various blocks in block Diagram are shown in Table 3.1. Converter consists of various blocks that explain the working functions. The points are shown in table.

Table 3.1: Functions of Various blocks in Block diagram

Sl. No	Block	Function
1	Input Filter	LC filter to filter out line transients
2	Current Transformer	To sense the primary current
3	Current Sense	Convert the sensed current to voltage to be used for short circuit protection
4	Turn On Circuit	ON command to turn on the converter
5	Turn Off Circuit	OFF command to turn off the converter
6	Bias Network	To power all active components in the converter
7	Feed Forward Network	To generate varying slope sawtooth waveform
8	Protection Circuits	To protect the converter from OVP, SCP and UVP
9	PWM Controller	To set the operating frequency and generate duty cycle
10	MOSFET Driver	To amplify the gate pulses to be able to drive the MOSFET
11	MOSFET	Main switching device
12	Transformer	To have isolation and multiple outputs
13	Low drop out Regulators	Used as Post regulators
14	Diode Rectifier	To rectify the output voltage
15	Output Filter	To filter the ripple on the output side

3.5 Summary

The chapter discussed the block diagram of the Forward Converter with Feed-Forward Control for space applications and methodology for the project.

CHAPTER 4

SPECIFICATION AND DESIGN

This chapter presents specification and design details of the Forward Converter, Area product calculation of transformer, Turns calculation, Inductance calculation.

Design is considered to achieve higher efficiency against the specification considering the other losses such as copper traces, controller circuitry losses. so that converter meets the efficiency specifications. Switching frequency is selected 250 kHz considering the switching losses, mass, size of filters and transformer design. The Specifications of the Forward Converter Topology is shown in Table 4.1.

Table 4.1: Specifications of Forward Converter Topology

Input voltage	26V-45V
Topology	Forward converter
Multiple outputs	1. +24V/4.3A 2. +12.7V/0.25A 3. +5.6V/0.1A 4. +3.8V/1A
Duty cycle	0.6
Line regulation	1%
Load regulation	1%
Cross regulation	2%
Efficiency	80%

4.1 Specification

The specifications of the Converter are as follows, Input Voltage range is 26V to 45V and converter should switch off below 22V. There will be voltage drop in EMI/EMC filter, MOSFET, input Connector and printed circuit board traces and hence, Input voltage range for designing the converter is considered 20V to 46V.

$$V_{in(min)} = 20\text{V}$$

$$V_{in(max)} = 45\text{V}$$

$$Dmax = 0.6$$

$$T_S = 4\ \text{us}$$

$$Dmin = Dmax * \frac{V_{in(min)}}{V_{in(max)}} = 0.6 * (\frac{20}{45}) = 0.2609 \qquad (4.1)$$

$$\text{Efficiency} = 0.8$$

- **Output voltages and current**

Bias winding powers the PWM controller circuit and other circuits of primary side that is also considered for feedback. Feedback does not require isolation since, itis in primary side. It also avoids the use of Optocoupler for feedback. Secondary Output voltage is regulated by using individual buck regulators or LDO

Output1

$$V_{out1} = 36\text{V}$$

$$I_{out1} = 4.3\text{A}$$

$$V_{D1} = 0.6\text{V}$$

$$V_{TD1} = V_{D1} + V_{lD1} = 0.6 \quad (4.2)$$

Output2

$$V_{out2} = 14\text{V}$$

$$I_{out2} = 0.25\text{A}$$

$$V_{D2} = 0.6\text{V}$$

$$V_{LD2} = 0.6\text{V}$$

$$V_{TD2} = V_{D2} + V_{lD2} = 1.2\text{V} \quad (4.3)$$

Output3

$$V_{out3} = 6\text{V}$$

$$I_{out3} = 0.1\text{A}$$

$$V_{D3} = 0.6\text{V}$$

$$V_{LD3} = 0.6\text{V}$$

$$V_{TD3} = V_{D3} + V_{lD3} = 1.2\text{V} \quad (4.4)$$

Output4

$$V_{out4} = 4\text{V}$$

$$I_{out4} = 1\text{A}$$

$$V_{D4} = 0.6\text{V}$$

$$V_{LD4} = 0.6\text{V}$$

$$V_{TD4} = V_{D4} + V_{lD4} = 1.2\text{V} \quad (4.5)$$

12V Primary Bias

$$Vbias1 = 12\text{V}$$

$$I_{bias1} = 0.1\text{A}$$

$$V_{Db1} = 0.6\text{V}$$

12V Buck Bias

$$Vbias2 = 12\text{V}$$

$$I_{bias2} = 0.1\text{A}$$

$$V_{Db2} = 0.6\text{V}$$

V_D *is* the forward voltage drop of diodes in the secondary windings. V_{LD} is the required extra voltage for the regulator except for the bias winding. Δv is the required ripple voltages.

- **Output Power and flat-topped pulse current**

Total output power calculation

$Pout1 = Vout1 * Iout1 = 154$ watts

$Pout1 = Vout1 * Iout1 = 3.5$watts

$Pout1 = Vout1 * Iout1 = 4.18$watts

$Pout1 = Vout1 * Iout1 = 0.616$ watts

$P_{bias1} = V_{bias1} * I_{bias1} = 1.2$ watts

$P_{bias2} = V_{bias2} * I_{bias2} = 1.2$ watts

$Pout1$ $Pout2$ $Pout3$ $Pout4$ is required output power. P_{bias1} is required power for primary side PWM-ICs, OPAMP circuits etc. P_{bias2} is supply for 24V buck controller. Pout is total output power for the transformer needs to be designed.

- **Calculation for Flat-Topped Pulse Input Current**

Input Power drawn from transformer is shown by following formula

$$P_{in} = \frac{P_{out}}{Efficiency} = V_{in(\min)} * I_{pft} * D_{max} \quad (4.6)$$

$$I_{pft} = \frac{P_{out}+P_{bias}}{Efficiency * V_{in(\min)} * D_{max}} = \frac{163+2.4}{0.8 * 22 * 0.6} = 16\text{A}$$

I_{pft} is input pulsating current used to design transformer. The OCP (Over current protection) is provided by sensing this peak current. Usually 125% of this peak current is sensed by CT2 (current transformer) for OCP.

4.2 Area Product Calculation

$K_w = 0.3$, $J = 6A/mm\text{^}2$, $B_m = 0.1\ Tesla$, $P_{out} = 163\ W$, $P_{bias} = 2.4$ W

$$A_p = \frac{\sqrt{D_{max} * (P + P_{bias}) * (1+\frac{1}{Efficiency})}}{K_w * J * Bm * 10^{-6} * f_{sw}} = \frac{\sqrt{0.6 * (163+2.4) * (1+\frac{1}{0.8})}}{0.3 * 6 * 0.1 * 10^{-6} * 250 * 10^3} = 4272.89\ mm^4$$

Description of the terms is as follows

Kw: Window Factor

Bm: Flux Density (Tesla)

J: Current Density (Amp/mm^2)

Kw, Bm & J are used for optimum design of transformer. The optimum design is finally decided by the small size & lower power dissipation of Transformer. Designer optimizes Kw, Bm & J for these purposes. Normally, Window Factor (Kw) vary from 0.3 to 0.5. Flux Density (Bm) depends on core material and it vary from

0.1 to 0.2 for ferrite core material. Current Density (J) vary from 3Amp/mm^2 to 6Amp/mm^2

Requirement of Core selection. An appropriate core is selected to have area product greater than the calculated Ap. Area product (Ap) is provided as the product of the core cross section (Ac) and the window area (Aw). These data is available in ferrite magnetic core design catalog.

Selected Toroid Core: ZP-42207TC, Material, Ur:2500, AL: 1875nH/1000T

$$Ve = 1740\ mm^3$$

$$Lc = 54.1\ m$$

$$Ac = 32.1\ mm^2$$

$$Aw = 148\ mm^2$$

$$Ap = Ac \times Aw = 4810 mm^4$$

- **Turns Ratio Calculation**

Turns ratio is calculated as

$$T_{ratio_{bias}} = \frac{(V_{bias} + V_{LDB}) + V_{Db} * D_{max}}{D_{max} * V_{in(\min)}} = 0.981$$

$$N_p = \frac{V_{in(\min)} * D_{max}}{B_m * A_c * 10^{-6} * f_{sw}} = \frac{20 * 0.6}{0.1 * 32.1 * 10^{-6} * 250 * 10^3} = 10 \text{turns}$$

$$N_{bias} = T_{ratio_{bias}} * N_p = 0.981 * 10 = 10 \text{ turns}$$

$$N_{s1} = \frac{(V_{out1} + V_{LD1}) * N_{bias}}{V_{bias}} = \frac{(36+0.6)*10}{12} = 30 \text{ turns}$$

$$N_{s2} = \frac{(V_{out2} + V_{LD2}) * N_{bias}}{V_{bias}} = \frac{(14+0.6)*10}{12} = 12 \text{ turns}$$

$$N_{s3} = \frac{(V_{out3} + V_{LD3}) * N_{bias}}{V_{bias}} = \frac{(6+0.6)*10}{12} = 5 \text{ turns}$$

$$N_{s4} = \frac{(V_{out4} + V_{LD4}) * N_{bias}}{V_{bias}} = \frac{(4+0.6)*10}{12} = 6 \text{ turns}$$

$$N_{bias1} = \frac{(V_{bias1} + V_{LD1}) * N_{bias}}{V_{bias}} = \frac{(12+0.6)*10}{12} = 10 \text{turns}$$

$$N_{mag} = \frac{N_P*(1-D_{max})}{D_{max}} = \frac{10*(1-0.6)}{0.6} = 6 \text{ turns}$$

- **Calculation of Winding Inductance (for nominal AL value)**

$$Lp = Np^2 * AL = 10^2 * 1875 * 10^{-9} = 188 \text{ uH}$$

$$Ls1 = Ns1^2 * AL = 30^2 * 1875 * 10^{-9} = 169 \text{ mH}$$

$$Ls2 = Ns2^2 * AL = 12^2 * 1875 * 10^{-9} = 270 \text{ uH}$$

$$Ls3 = Ns3^2 * AL = 5^2 * 1875 * 10^{-9} = 46.9 \text{ uH}$$

$$Ls4 = NS4^2 * AL = 6^2 * 1875 * 10^{-9} = 67.5 \text{ uH}$$

$$Lbias = Nbias^2 * AL = 10^2 * 1875 * 10^{-9} = 188 \text{ uH}$$

4.3 MOSFET Selection and Snubber Design

MOSFET is selected based on Drain to Source Voltage, Drain Current, Drain to Source ONstate resistance. The drain to source ON state resistance is to be small for low losses. Snubber circuit is designed to reduce the voltage stress on the switch

4.3.1 MOSFET Selection and Loss Calculation

MOSFET selection is depending on the Drain to Source voltage (Vds), Drain current (Id), Drain to Source ON state resistance (Rds), Gate charge (Qg), and Output Capacitance (Coss).

The package and size of the MOSFET depending on the losses takes place in MOSFET. Following two types of losses are calculated while selecting the MOSFET

- Conduction losses
- Switching losses

Conduction losses is calculated as per equation. Multiplication of 1.4 is considered for the normalized resistance corresponding to 110 Degree Celsius of Junction temperature.

The selected MOSFET is BUY25CS45B, 250V, 45A, 0.05 Ohm

$$R\_DS = 0.05\ \Omega$$

$$R\_GATE = 4.75\ \Omega$$

$$Q_{GATE} = 100\times 10^{-9}\ C$$

$$Coss = 400 \times 10^{-9}\ F$$

$$V_{TH} = 5\,V$$

$$V_{GATE} = 11\,V$$

Conduction loss, $P_{conduction} = 1.6 * R_{DS} * (I_{prms})^2 = 1.6 * 0.05 * (12)^2 = 4.5$ watt

Gate charge loss, $P_{gate} = Q_{gate} * V_{gate} * f_s = 100^{*}10^{-9} * 11 * 250 * 10^3 = 0.275$ watt

Output capacitor loss, P_{coss} = 0.5*Coss*$(V_{off})^2$*f_s = 0.5*400 *10^{-9} * 90^2 *250 *10^3

= 0.405 watt

Rise time, $T_r = \frac{Q_{gate} * R_G}{(V_{gate} - V_{TH})} = \frac{100*10^{-9}*4.75}{(11-5)} = 79$ns

Fall time, $T_f = \frac{Q_{gate} * R_G}{V_{TH}} = \frac{100*10^{-9}*4.75}{5} = 95$ns

$P_{switch_on} = \frac{V_{in(min)}*I_{pft}*T_r*f_s}{3} = \frac{22*16*79**250*10^3}{3} = 2.26$watt

$P_{Switch\_off} = \frac{V_{off}^{*}\,I_{pft}*T*f*f_s}{3} = \frac{90*16*95*10^{-9}*250*10^3}{3} = 12.2$ watt

Total Losses in MOSFET

$$P_{MOSFET\_loss} = P_{conduction} + P_{gate} + P_{coss} + P_{switch\_on} + P_{switch\_off}$$

$$PMOSFET\_loss = 4.5 + 0.1 + 0.275 + 0.405 + 2.26 + 12.2 = 18.9 \text{ watt}$$

4.3.2 Snubber Design

Snubber is designed to operate MOSFET in SOA (Safe operating area) also to limit switching transients like dv/dt and help to lower EMI by reducing ringing noise occur due to leakage inductance of transformer.

$$Csnubber = 2.2 \text{ nF}$$

$$Lsnubber = 0.8 \text{ uH}$$

4.4 Synchronous Buck converter

$V_{in} = 36V,\ V_{out} = 24V,\ I_{out} = 4.3A,\ f_s = 250kHz,\ \Delta v = 30mV$, k =20mA

Duty ratio, $D = \frac{V_{out}}{V_{in}} = 0.66$

Output Inductance, $L = \frac{V_{out}*(1-D)}{I_{out}*f_s*k} = \frac{24*(1-0.66)}{4.3*250*10^3*0.2} = 37.9uH$

Output Capacitance, $C = \frac{k*I_{out}}{L*f_s*\Delta v} = \frac{0.2*4.3}{38*10^{-6}*250*10^3*30*10^{-3}} = 14.33uF$

Load Resistance, $R = \frac{V_{out}}{I_{out}} = 5.5$ ohm

4.5 Summary

The chapter discussed the selection of MOSFET and the Transformer core. The design of transformer winding, Filter Inductor, Filter Capacitor, Coupled Inductor, Snubber Circuit,Output Diodes and selection of PWM controller IC, Diode Rectifiers.

CHAPTER 5

SIMULATION AND HARDWARE IMPLEMENTATION

The simulation of the Multiple Output Forward Converter with Feed-Forward Control for Space Applications is carried out in LTSPICE software. The hardware implementation is performed to get the regulated output voltage.

5.1 Simulation Analysis

The selected topology is simulated in LTSPICE Simulink environment. The effectiveness of the converter is designed and performance of the converter is checked. The Table 5.1 shows the parameter values considered for the LTSPICE simulation of the circuit.

Table 5.1: Parameters of the Forward Converter Considered for LTSPICE Simulations

PARAMETERS	SYMBOLS	VALUES
Inductor Filter	L	40 uH
Capacitor Filter	C	21.5 uF
Primary Inductance	Lp	188 uH
Secondary Inductance	Ls	1.69mH
Magnetizing Inductance	Lm	43 uH
Snubber Capacitor	Cs	2.2nF
Snubber Inductance	Rs	0.8 uH
Load resistance	R	8.3 Ohm

The simulation circuit for Multiple Output of the Forward Converter with Feed-Forward Control for Space Applications is shown in the Figure 5.1. The circuit consists of Snubber circuit, coupled inductor, Filter Inductor and Capacitor, Type 2 Compensation Circuit and a Comparator circuit. The input to the circuit is 26 V DC supply. The input to the circuit is varied from 26 to 45 V. The circuit shown here with input of nominal voltageof 37 V. Th e feedback circuit is connected to the type 2 compensation for providing the regulated output voltage. The snubber circuit is connected to the MOSFET for reducing the voltage stress on the MOSFET. The four output circuits are coupled magnetically through magnetically coupled inductor. If one output is varied then other output also gets affected for providing the regulated output voltage.

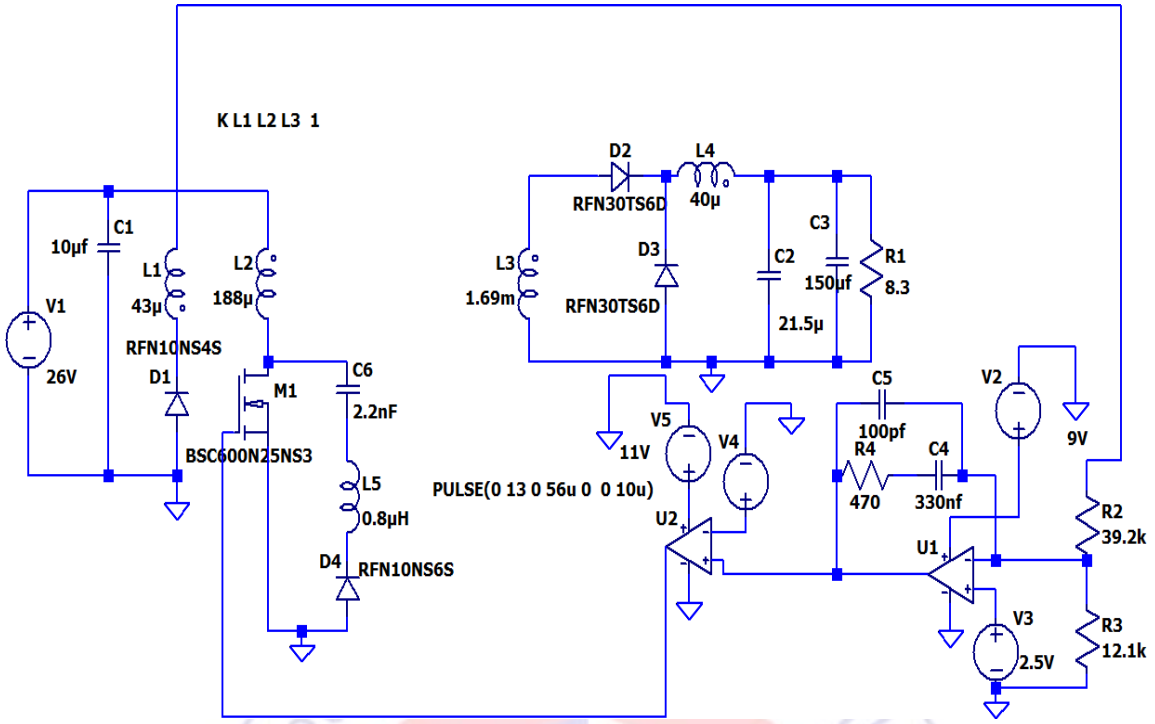


Figure 5.1: Simulation Circuit of Forward Converter

The inverting input to operation amplifier U2 is of ramp voltage is compared with the output voltage of Error amplifier U1 to generate gate pulse for MOSFET switch. The simulation waveform of the ramp signal generated from PWM controller is shown in Figure 5.2

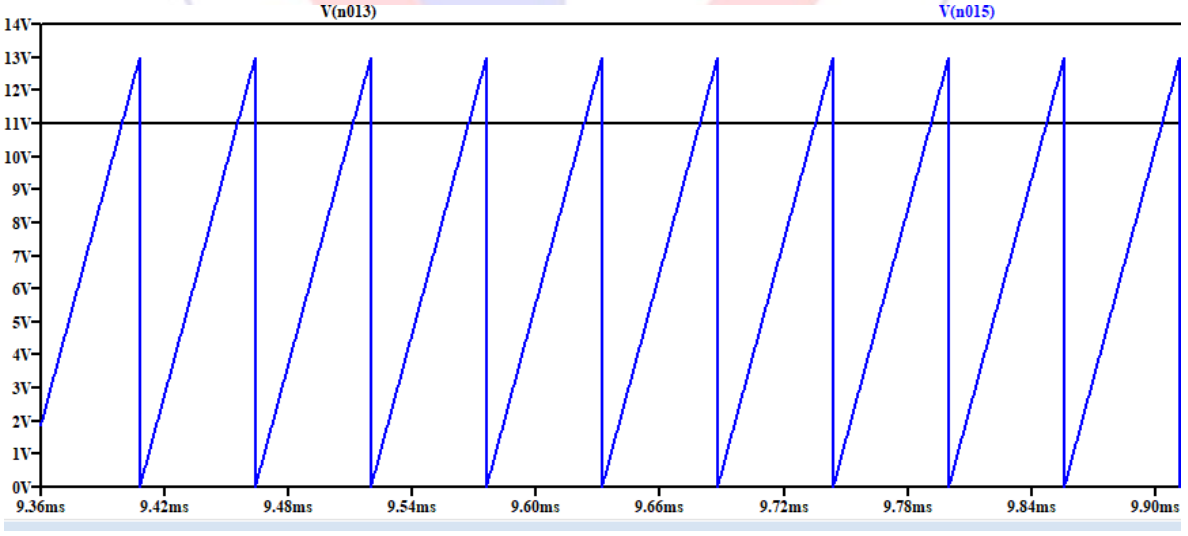


Figure 5.2: Simulation waveform of ramp signal voltage

The simulation waveform of MOSFET Gate pulse is shown in Figure 5.3

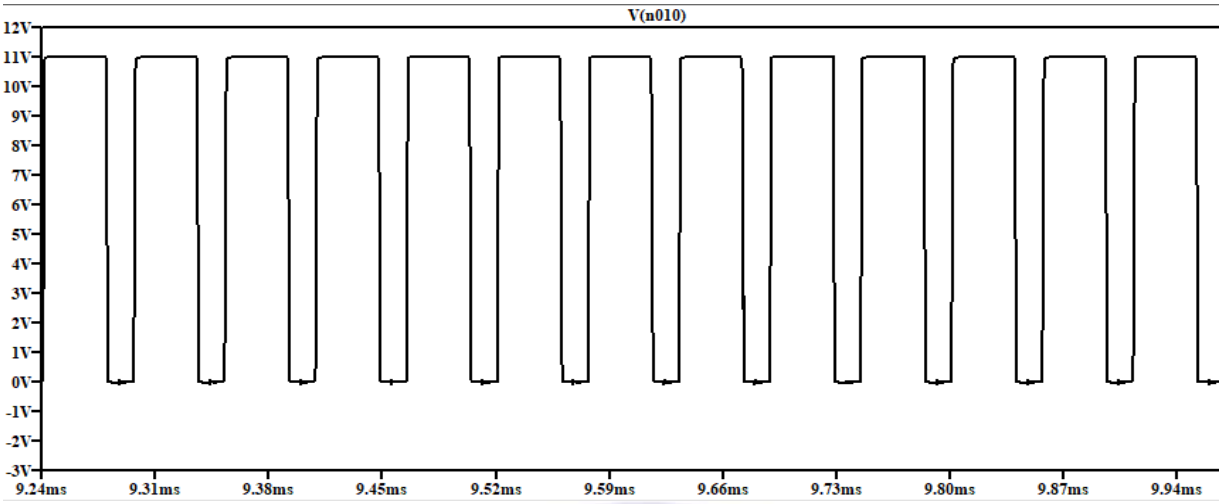


Figure 5.3: Simulation waveform of MOSFET Gate pulse

The transformer primary peak current of 18A is shown in Figure 5.4

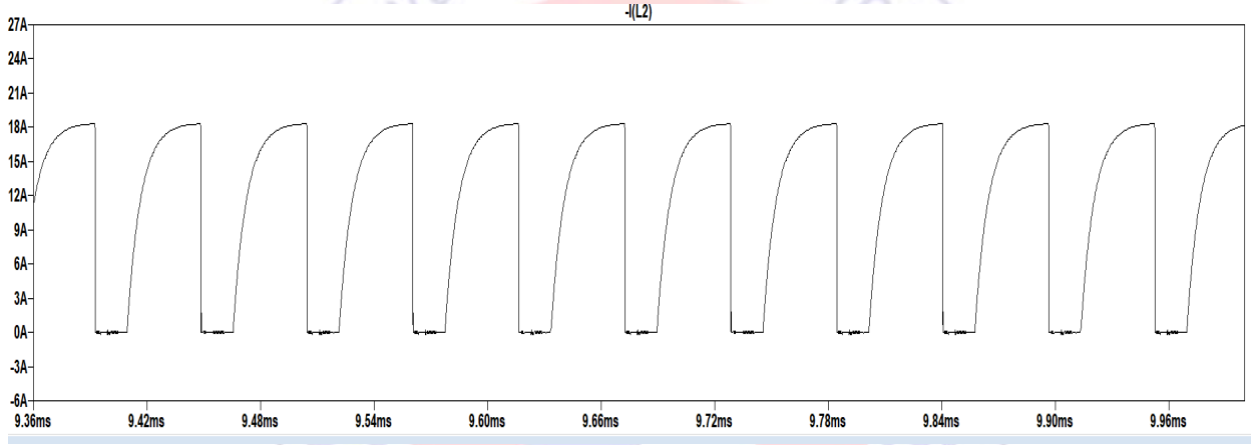


Figure 5.4: Simulation waveform of Transformer Primary peak current

The Output voltage waveform of Forward converter 36V is shown in Figure 5.5

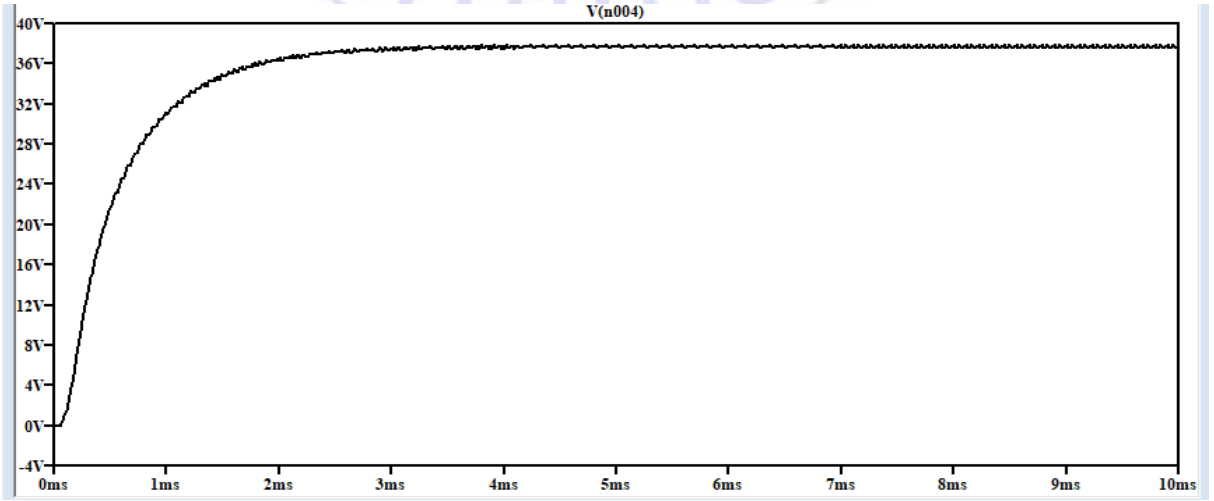


Figure 5.5: Output voltage of Forward converter

- **Synchronous Buck converter**

The voltage across secondary winding of transformer 36V is fed as input to synchronous buck converter to obtain 24V output using LT3845 IC is shown in Figure 5.6

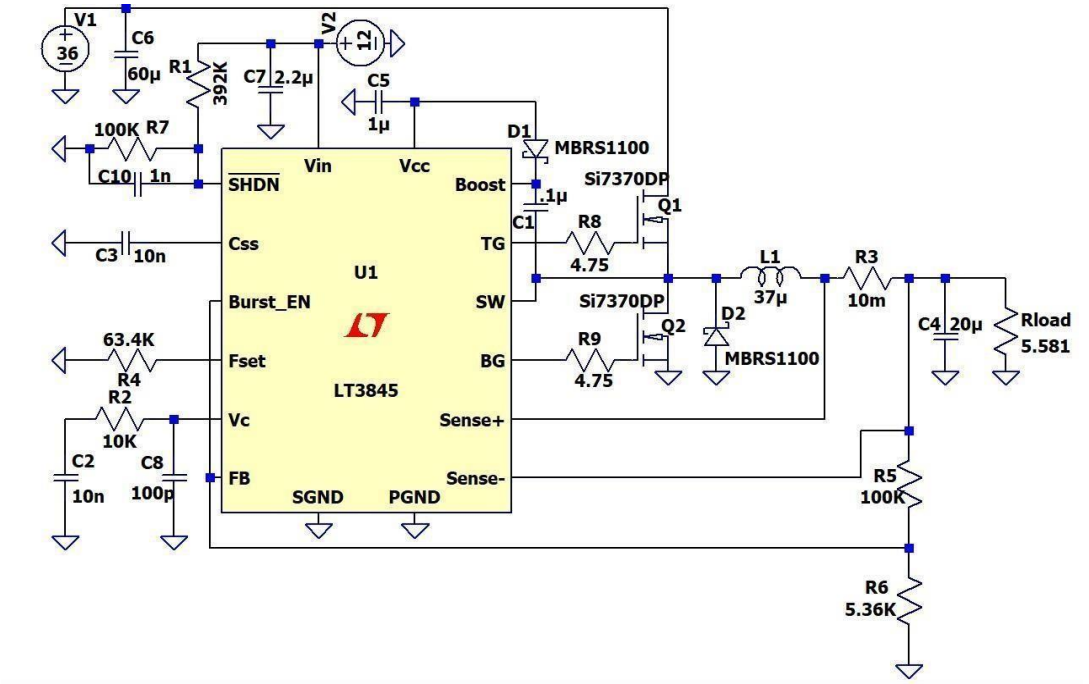


Figure 5.6: Simulation circuit of Synchronous buck converter using LT3845IC

The first output voltage 24V of Multiple output forward converter waveformobtained from the synchronous buck converter is shown in Figure 5.7

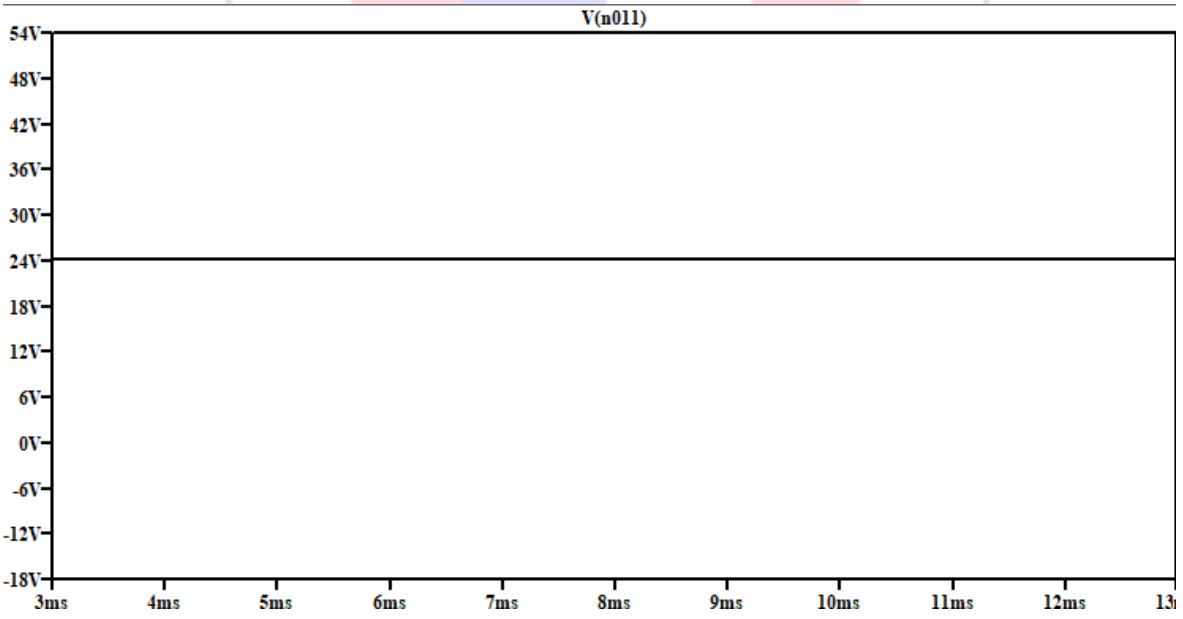


Figure 5.7: Output voltage waveform of Synchronous buck converter

The Output current of synchronous buck converter is shown in Figure 5.8

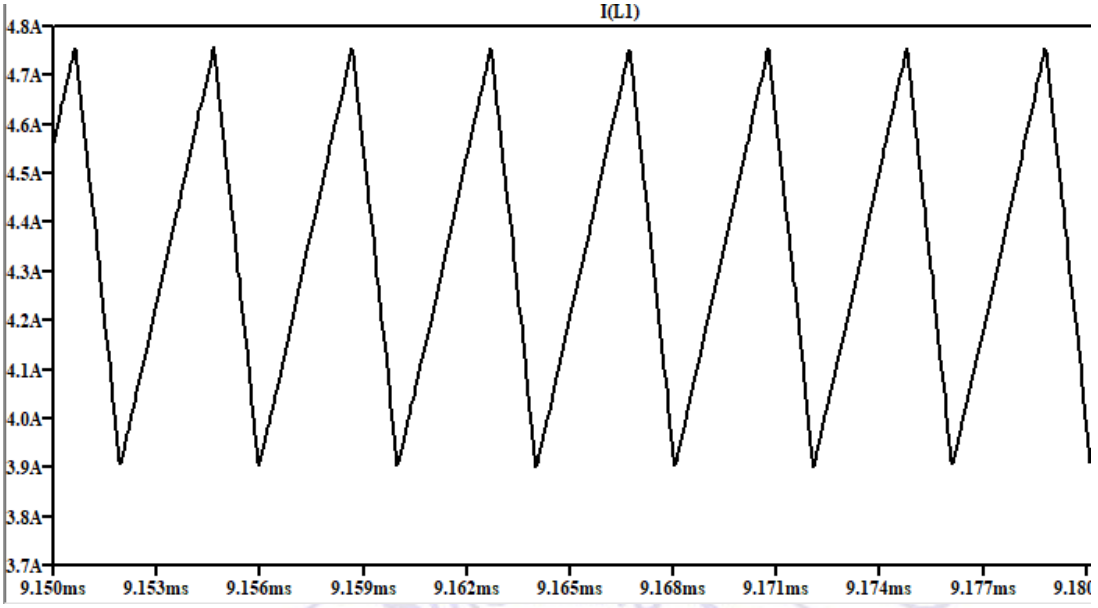


Figure 5.8: Output current waveform of Synchronous buck converter

- **Low drop out regulators**

Low dropout regulators (LDOs) are a simple inexpensive way to regulate an output voltage that is powered from a higher voltage input. The secondaries of the forward transformer are designed to get voltages of 14V,6V and 4V further connected to LDO regulators to regulate these voltages to 12.7 V, 5.6V and 3.8V respectively. Here p-channel MOSFET is used as series pass element along with an error amplifier. The LDO 1 simulationcircuit to regulate the output voltage to 12.7V is shown in Figure 5.9

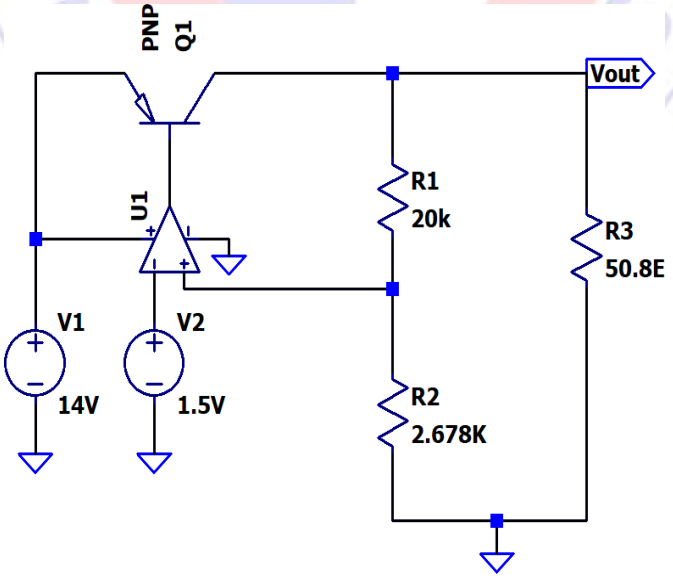


Figure 5.9: Simulation circuit of LDO 1

The waveform of Output voltage 12.7V from LDO 1 is shown in Figure 5.10

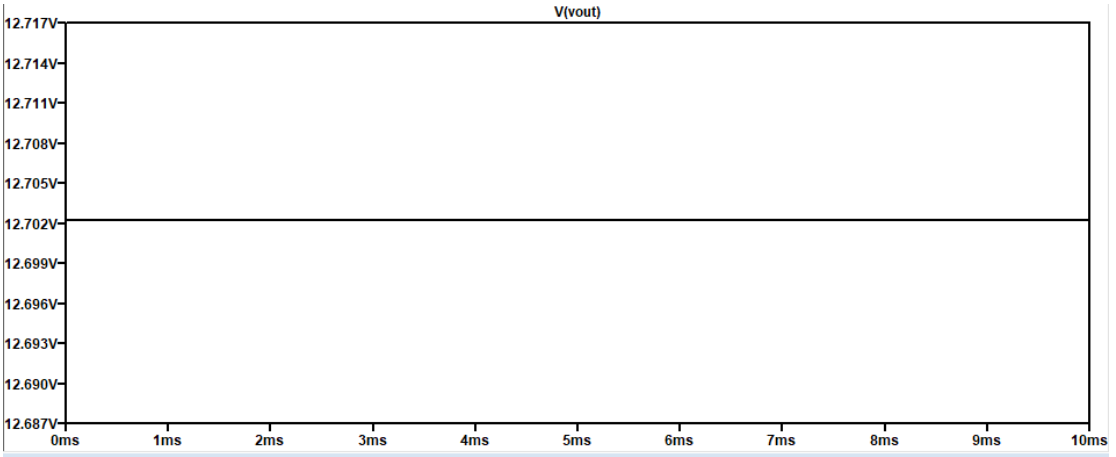


Figure 5.10: Output voltage waveform of LDO 1

The LDO 2 simulation circuit to regulate the output voltage to 12.7V is shown in Figure 5.11

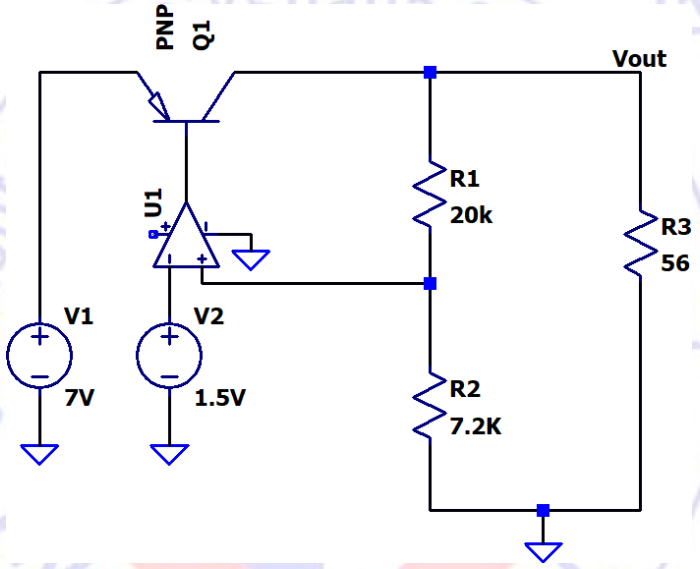


Figure 5.11: Simulation circuit of LDO 2

The waveform of Output voltage 5.6V from LDO2 is shown in Figure 5.12

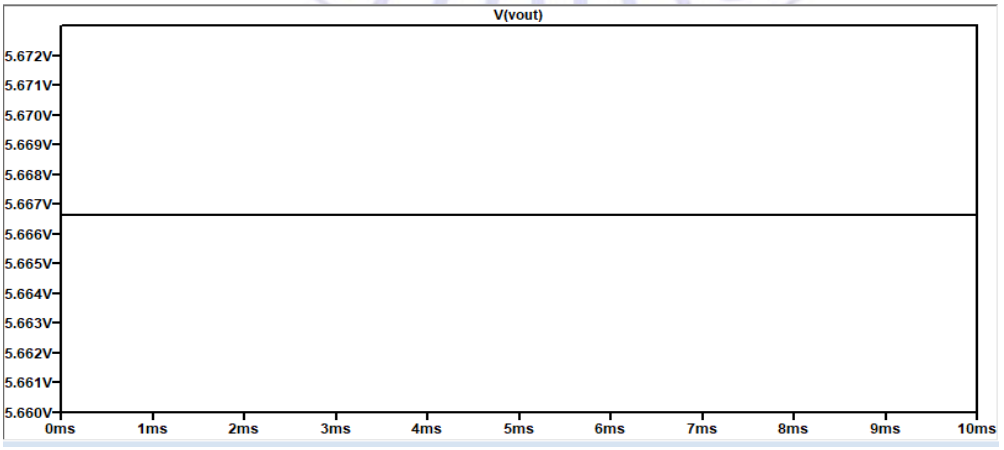


Figure 5.12: Output voltage waveform of LDO 2

The LDO 3 simulation circuit to regulate the output voltage to 12.7V is shown in Figure 5.13

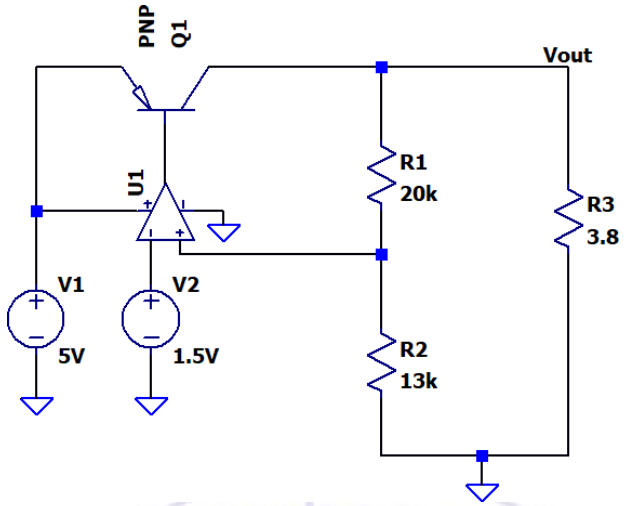


Figure 5.13: Simulation circuit of LDO 3

The waveform of Output voltage 3.8V from LDO 3 is shown in Figure 5.14

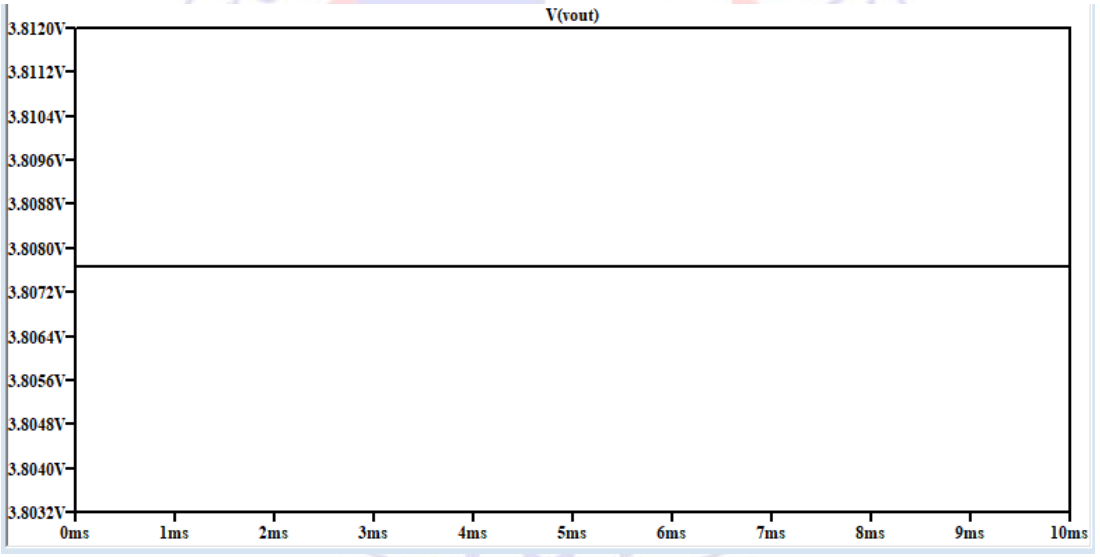


Figure 5.14: Output voltage waveform of LDO 3

- **Sync circuit**

The main function of sync circuit is to synchronize the switching frequency of Main MOSFET in primary with the synchronous buck converter MOSFET at the secondary to 250kHz

The simulation of Sync circuit is shown in Figure 5.15

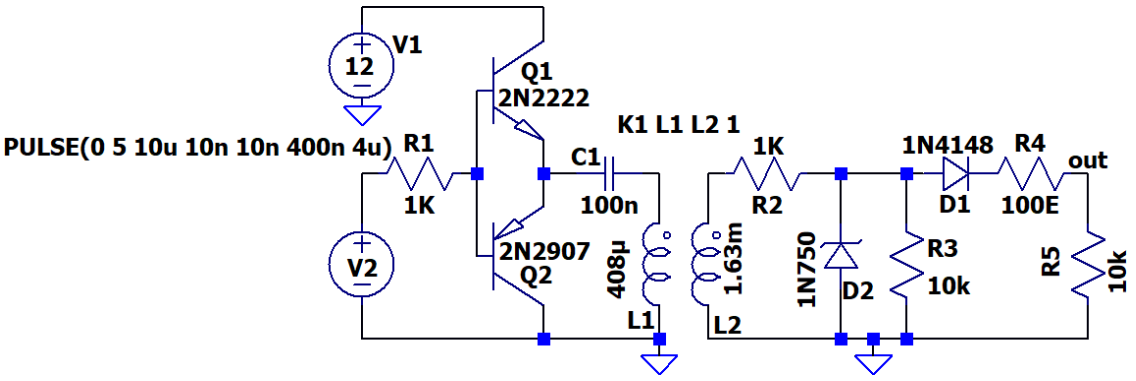


Figure 5.15: Simulation of Sync Circuit

The output voltage waveform of sync circuit of frequency 250kHz is shown in Figure5.15

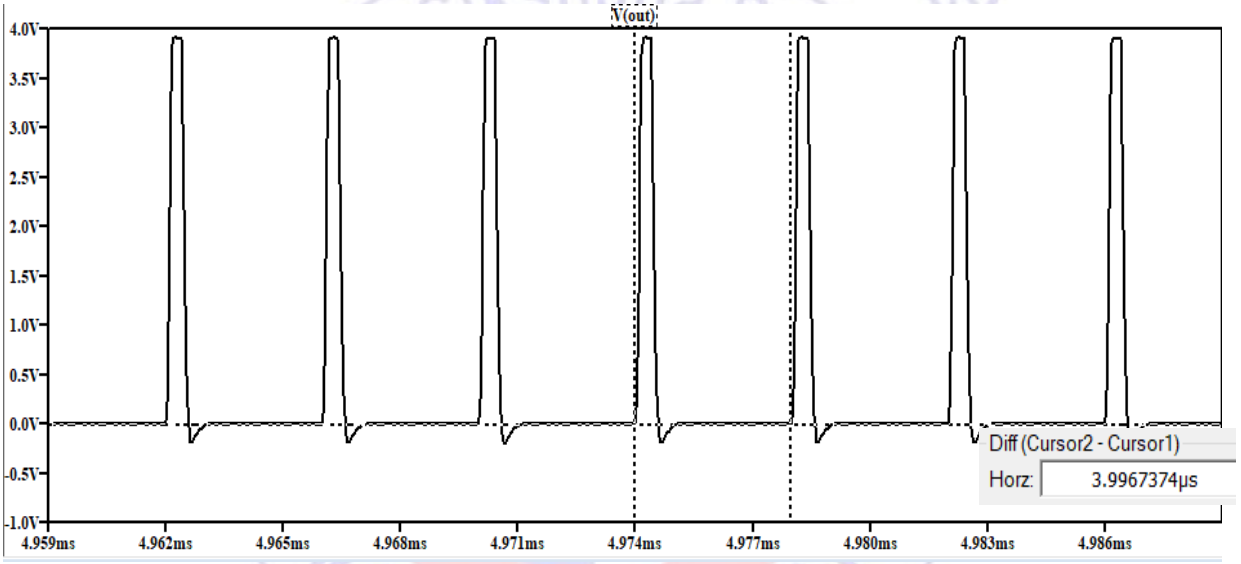


Figure 5.16: waveform of Sync circuit

- **Output Overvoltage Protection Circuit**

Over voltage protection is designed to operate only if any of the three output voltages exceeds 125% of the rated output voltage. In case of an over voltage, the output of the over voltage protection circuit becomes high and this high signal is connected to the shutdown pinof the PWM IC turns off the converter. On the secondary side, opto isolator (4N25A) is used toprovide isolation between input and output sections. If over voltage exists, then the latch up point obtain high. The simulation circuit of Overvoltage protection circuit is shown in Figure 5.17

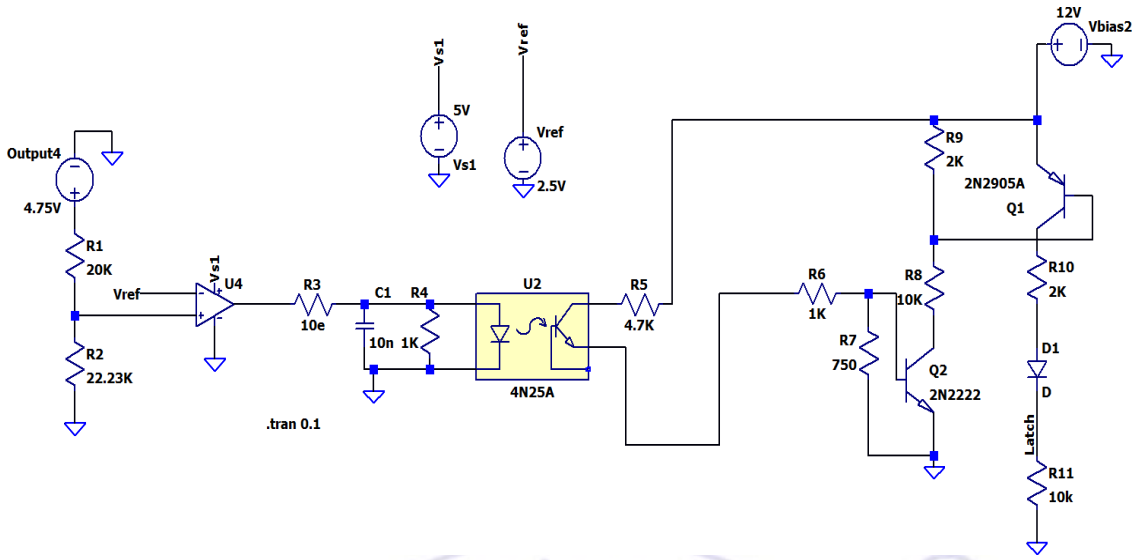


Figure 5.17: Overvoltage protection simulation Circuit

The latch pin is of high value as overvoltage protection is triggered for 125% of output voltage is shown in Figure 5.18

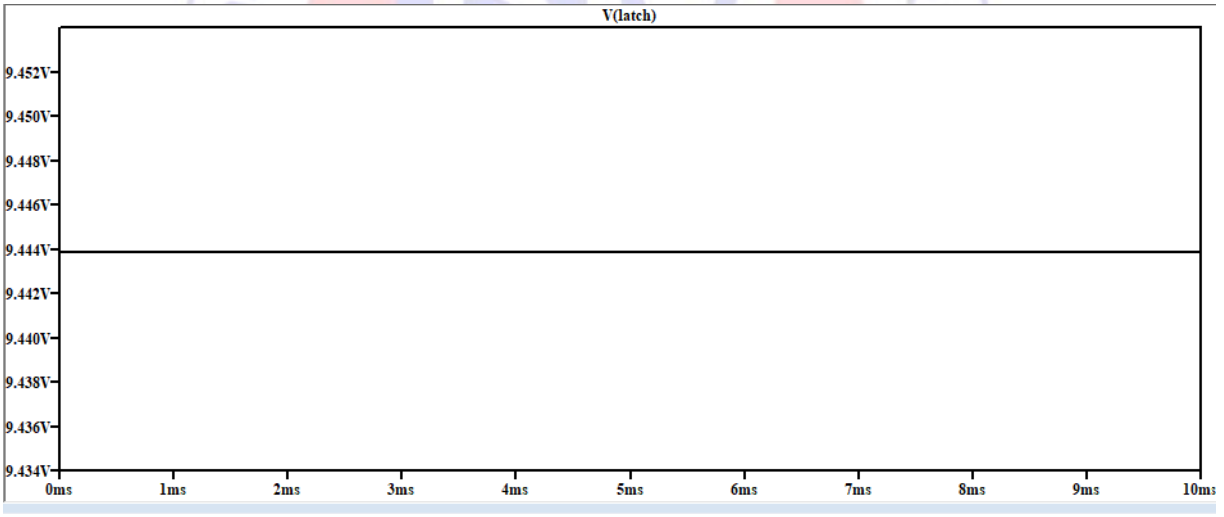


Figure 5.18: Output voltage waveform of Overvoltage protection Circuit

- **Input undervoltage Protection Circuit**

The input undervoltage protection is triggered for the voltage less than 20V is shown in Figure 5.19. The input voltage is fed to the voltage divider network consisting of resistors R1 and R2 and the voltage appearing across R2 appears across the inverting terminal of the opamp. This error signal is fed to the non-inverting terminal of the op-amp. Inverting terminal of this op-amp is maintained at 2.5V.

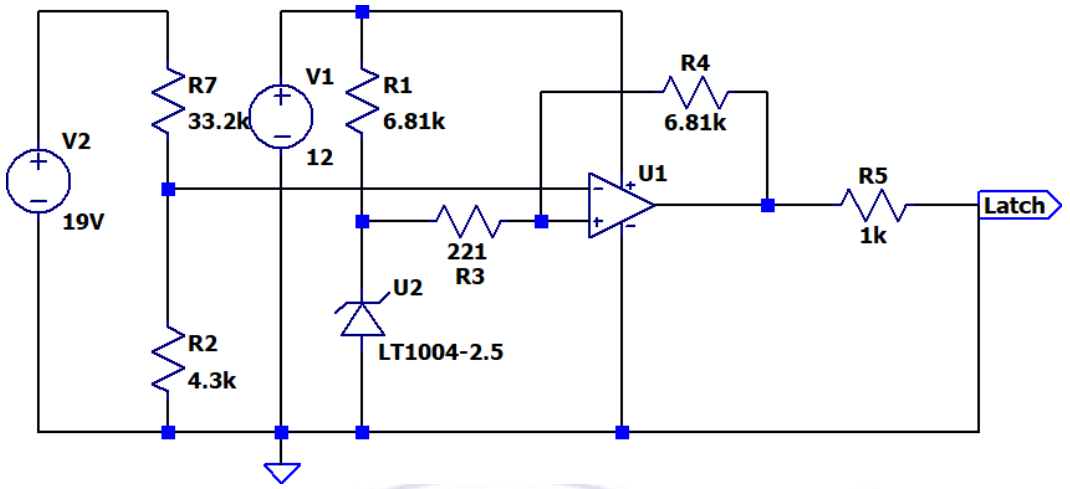


Figure 5.19: Undervoltage protection Circuit

The latch pin is of high value as input undervoltage protection is triggered for less than input voltage of 20V is shown in Figure 5.20

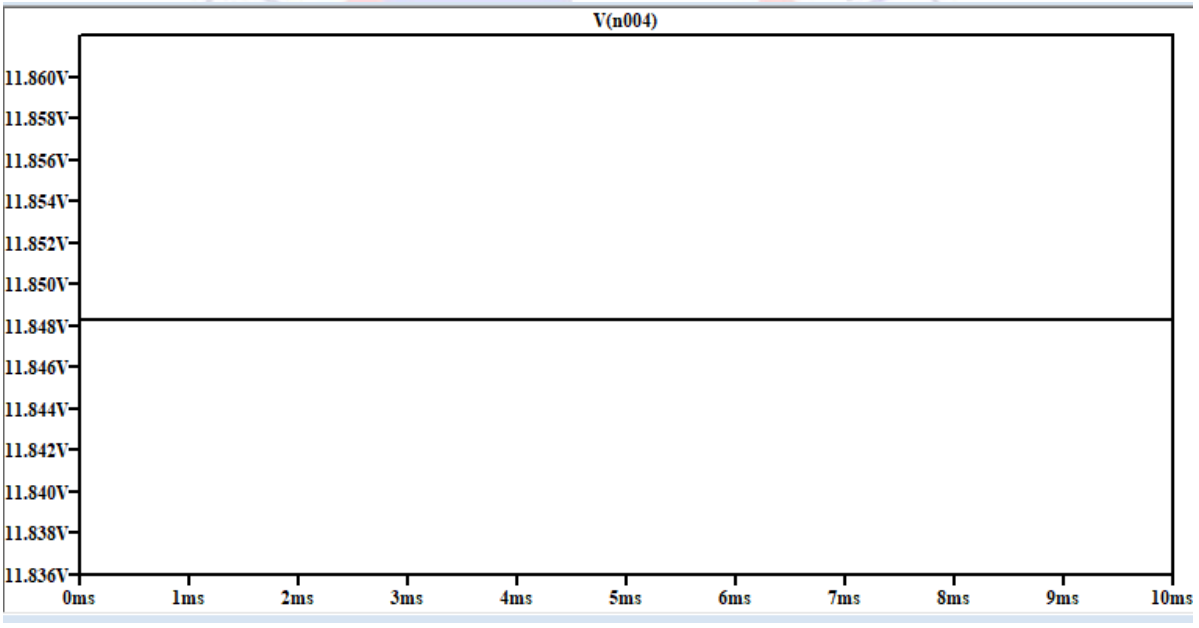


Figure 5.20: Output voltage waveform of Input Undervoltage Circuit

- **External Disable Circuit**

The converter is turned off by manually operated switch through grounding the resistor R3, transistor Q1 drives the base current is turned ON is shown in Figure 5.21, D1 is forward biased allow latch pin to be high, shutdowns the converter.

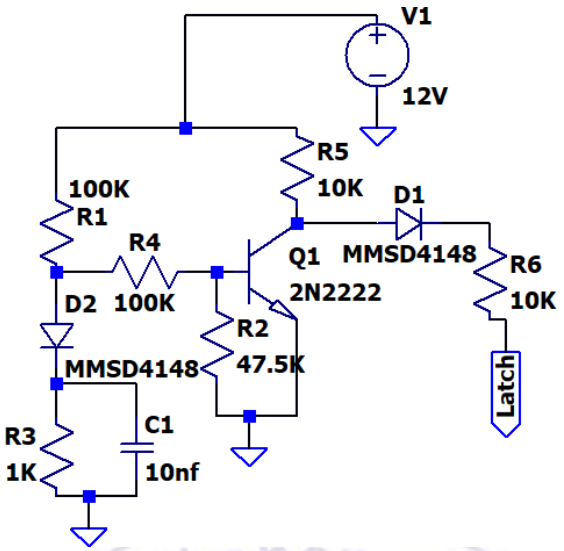


Figure 5.21: Output External disable Circuit

The output voltage waveform of high latch pin is shown in Figure 5.22

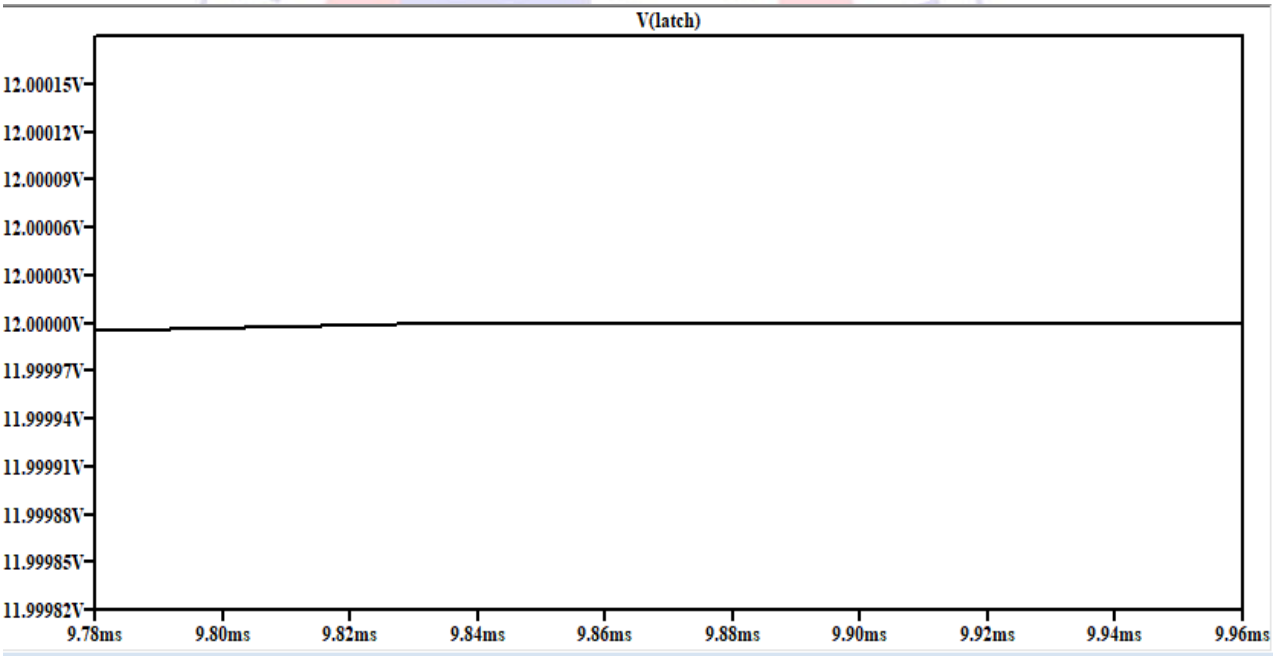


Figure 5.22: Output voltage waveform of External disable circuit

5.1 Hardware Implementation

Experimental results that depict line regulation, load regulation, cross regulation, efficiency and ripple voltage measured at different outputs are tabulated. Various waveforms like Output voltage, Output current, drain voltage, Gate pulse, Output ripple waveforms of Forward converter are presented.

The hardware implementation of the converter includes various parts

A. PWM IC (UC2825DWTR)

B. MOSFET

C. Transformer

D. Differential-mode filter inductor

E. Common-mode filter inductor

F. Output Diodes

G. Diode Rectifier.

5.2.1 Implementation

From the designed values various components are selected. According to the Schematic representation the selected components like capacitor, inductor, resistors, MOSFET, windings of transformers, PWM controller IC's are mounted on the printed circuit board. MOSFET is provided with heat sink, to absorb the heat dissipated by the MOSFET and the switch is provided by the snubber circuit, to reduce the voltage stress on the switch. The snubber comprises ofthree components snubbing capacitor, resistor and diode. The instantaneous change in the dutycycle, the overshoot of the output voltage caused by the input voltage in voltage mode control technique is reduced. Current sense circuitry senses the input current and provide the over current protection. Input under voltage protection is also provided.

Hardware layout of Forward Converter (Top view) is shown in the Figure 5.23. It consists Input connector, EMI filter includes differential mode and common mode filter, Primary side MOSFET, Forward transformer, three LDO, Output Inductor Coupled inductor, Diode rectifier, Current transformer.

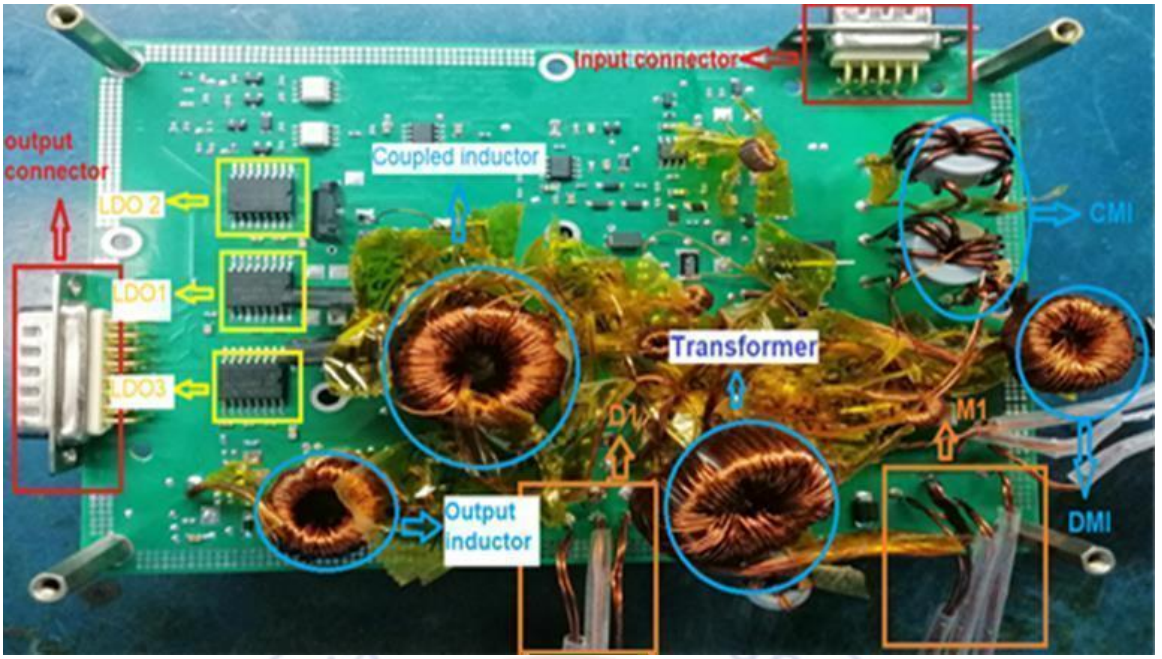


Figure 5.23: Hardware Layout of Forward Converter (Top view)

Hardware Layout of Forward Converter (Bottom view) is shown in the figure 5.24. It consists of Protection circuits like Over Voltage Protection, Under Voltage Protection Circuit, Over Power Protection Circuit and Feed-Forward circuit. Secondary side MOSFET's M2(control switch) and M3 (synchronous switch) of Buck regulator LT3845 IC, Diode's D2, D3, D4 for secondary side LDO's, Gate driver IC, two PWM IC's, one to generate switching frequency and another for Feed forward control of the converter.

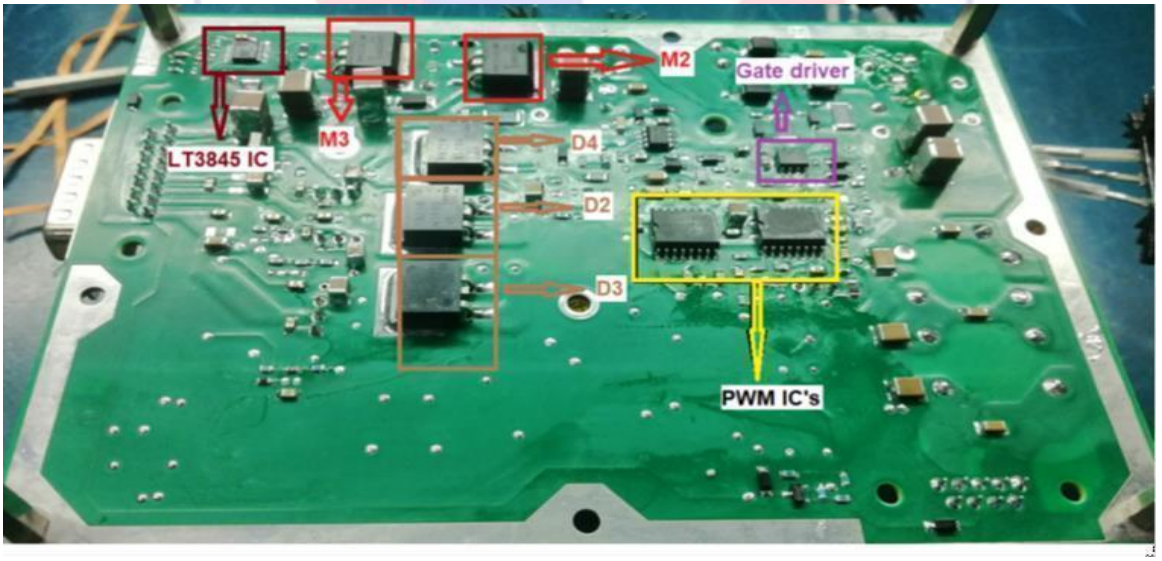


Figure 5.24: Hardware Layout of Forward Converter (Top view)

5.2.2 Tested Waveforms of Forward Converter

The converter topology performance is evaluated by conducting various electrical tests like input parameter measurement, efficiency measurement, ripple measurement, line regulation, load regulation and cross regulation. The converter is tested for input voltage range from 26V to 45V operating at 250 KHz. Output voltages are measured for different load conditions.

Waveform of the output voltage 1 from the synchronous buck converter 24V is shown in Figure 5.25 by using the DSO. For changes in the input voltages ranging from 26 V to 45V, the output voltage is regulated.

Figure 5.25: Output voltage Waveform 1

Waveform of the output voltage 2 from the LDO 1 regulator 12.7V is shown in Figure 5.26 by using the DSO. For changes in the input voltages ranging from 26 V to 45 V, the output voltage is regulated.

Figure 5.26: Output voltage Waveform 2

Waveform of the output voltage 3 from the LDO 2 regulator 5.6V is shown in Figure 5.27 by using the DSO. For changes in the input voltages ranging from 26 V to 45 V, the output voltage is regulated.

Figure 5.27: Output voltage Waveform 3

Waveform of the output voltage 4 from the LDO 3 regulator is shown in Figure 5.28 by using the DSO. For changes in the input voltages ranging from 26 V to 45 V, the output voltage is regulated.

Figure 5.28: Output voltage Waveform 4

The waveform of the ramp signal generated from PWM controller is shown in Figure 5.29

Figure 5.29: Ramp voltage waveform

The duty cycle of gate pulse varies according to the input voltage. As inputvoltage increases, the width of the duty pulse decreases.

The waveform of gate pulse for 26V with the duty cycle of 45% is shown in Figure 5.30

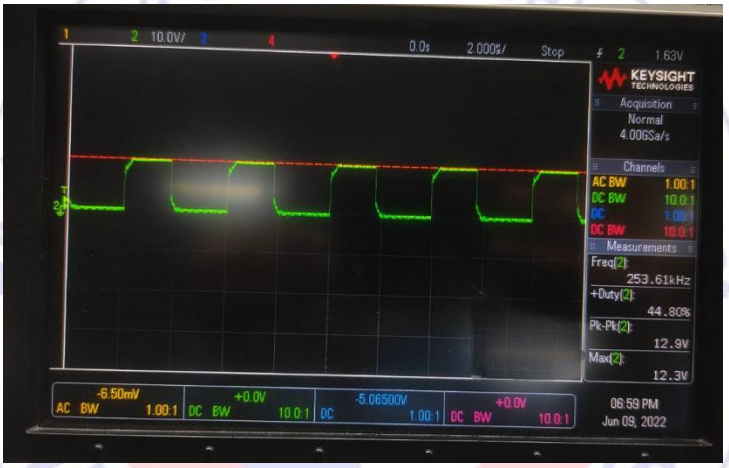


Figure 5.30: Gate pulse waveform for 26V

The waveform of gate pulse for 37V with the duty cycle of 30% is shown in Figure 5.31

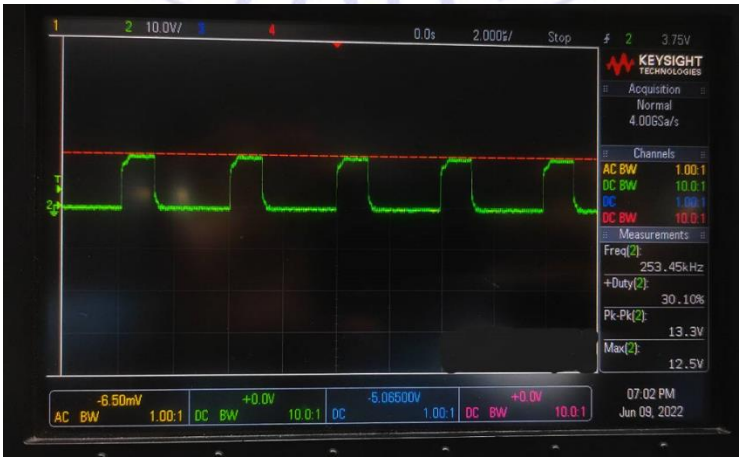


Figure 5.31: Gate pulse waveform for 37V

The waveform of gate pulse for 45V with the duty cycle of 30% is shown in Figure 5.32

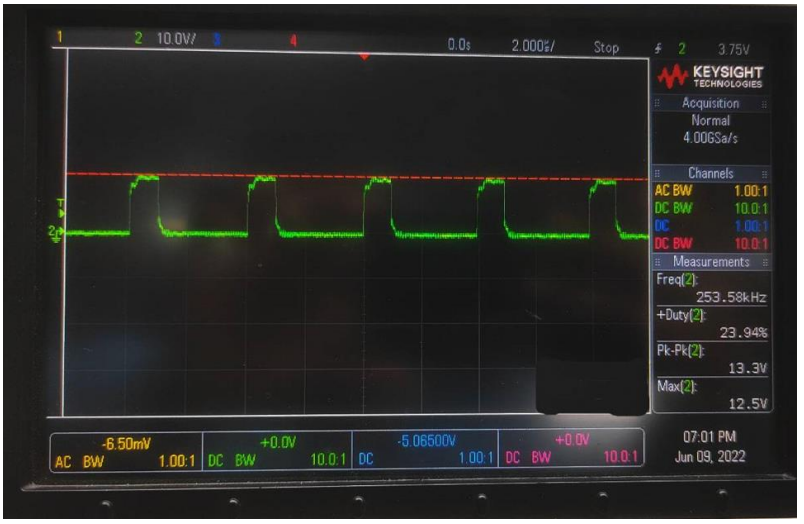


Figure 5.32: Gate pulse waveform for 45V

The drain to source voltage waveform of MOSFET is shown in the Figure 5.33. The stress on the switch is reduced by snubber circuit, so the losses are reduced. The voltages tress on the MOSFET is less than the two times the supply voltage. The switching frequency maintained is 250 KHz.

Figure 5.33: Mosfet Voltage waveform

Waveform of Transformer primary current is shown by using the DSO. For changes in the input voltage 26 V. Waveform of transformer primary peak current is shown in Figure 5.34.

Figure 5.34: Transformer Primary current

Waveform of Output Current 1 from the synchronous buck converter is shown by using the DSO. For changes in the input voltages ranging from 26 V to 45 V, the output voltage is regulated. Waveform of output current 1 is shown in Figure 5.35.

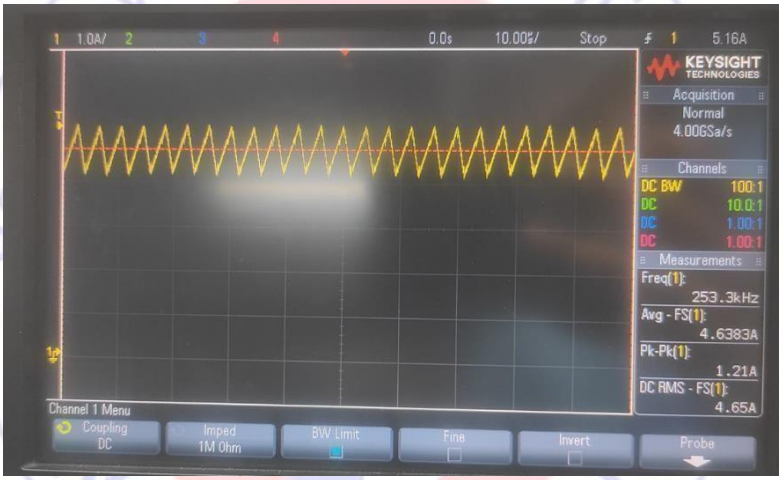


Figure 5.35: Output current of Synchronous buck converter

5.2 Summary

The simulations of the circuits were performed and waveforms for the same wasobtained. The designed components mounted on the PCB and hardware implementation was carried out. The readings and waveforms for the circuit were noted.

CHAPTER 6

RESULTS AND DISCUSSIONS

The chapter includes the results for the Multiple Output Forward Converter with Feed-Forward Control for Space Applications. Load regulation denotes the variation of output voltage that the load changes from no minimum load to maximum load.

6.1 Simulation Results

The obtained simulation results of regulated output voltages are 24V, 12.7 V 5.6 V and 3.8 V, the output currents are 4.3A,0.25A, 0.1A and 1A respectively. The results obtained from the simulation analysis are similar to the hardware implemented results.

6.2 Hardware Results

Line regulation denotes the variation of output voltage with respect to variation in the input voltage with the output load held constant.

$$\%\ Line\ regulation = \left(\frac{V_{out}\ at\ 26V - V_{out}\ at\ 45V}{V_{out}\ at\ 37V}\right) X\ 100 \qquad (6.1)$$

The specification for line regulation is less than 1%. Table 6.1 Shows Line regulation for different Input Voltage Ranges.

Table 6.1: Shows Line Regulation for Different Input Voltage Ranges

Load Condition	Output1 (+24V)	Output2 (+12.7V)	Output3 (+5.6V)	Output4 (+3.8V)
10% Load	0.03	0.02	0.03	0.02
50% Load	0.01	0.14	0.02	0.01
100% Load	0.02	0.17	0.01	0.03

Load regulation denotes the variation of the input voltage with respect to load variation

$$\%\ Load\ regulation = \left(\frac{V_{out}\ at\ 10\%\ load - V_{out}\ at\ 100\%\ load}{V_{out}\ at\ 100\%\ load}\right) X\ 100 \qquad (6.2)$$

The specification for line regulation is less than 1%. Table 6.2 Shows Load Regulation for Load Variation.

Table 6.2: Shows Line Regulation for Different Input Voltage Ranges

Load Variation	Input Voltage(V)	Output1 (+24V)	Output2 (+12.7V)	Output3 (+5.6V)	Output4 (+3.8V)
10% to 100% load (Spec < ±1%)	26V	0.04	0.13	0.05	0.39
	37V	0.45	0.31	0.01	0.47
	45V	0.43	0.31	0.01	0.42
No load to 10% load (Spec < ±3%)	26V	0.03	0.01	0.03	0.1
	37V	0.01	0.03	0.04	0.08
	45V	0.02	0.02	0.04	0.05

Cross regulation is measured by keeping the measuring output at full load and other outputs at 10% load and is tabulated in Table 6.3

$$\%\ Cross\ regulation = \left(\frac{Measured\ output\ at\ 100\%\ load\ with\ remaining\ outputs\ at\ 10\%\ load \_ Measured\ output\ at\ 100\%\ load\ with\ remaining\ outputs\ at\ 100\%\ load}{Measured\ output\ at\ 100\%\ load\ with\ remaining\ outputs\ at\ 10\%\ load} \right) X\ 100 \qquad (6.3)$$

Table 6.3: Shows Line Regulation for Different Input Voltage Ranges

Input Voltage	Parameter	A*	B*
+24V	Voltage	23.931	23.909
	cross Regulation	0.09	
+12.7V	Voltage	12.722	12.693
	cross Regulation	0.23	
+3.8V	Voltage	3.805	3.802
	cross Regulation	0.08	
+5.6V	Voltage	5.613	5.616
	cross Regulation	-0.05	

A*= Measured output in 100% load condition & remaining outputs are in 10% load condition

B*= Measured output in 100% load condition & remaining outputs are in 100% load condition

Results are shown for the Multiple output Forward Converter with Feed-Forward Control for Space Applications. The specified Output Voltage, Current, Output Voltage ripple and Drain to Source Voltage of MOSFET is obtained for the switching frequency of 250 KHz. The output voltage waveform for varying input voltages ranging from 26 V to 45 V are obtained. The output voltages are regulated for changing input voltage ranges. The practical values for Output Voltage, Output Current, Output Voltage ripple are shown in the Table 6.3 for 100% Loading Conditions for 26V Input Voltage.

Table 6.3: 100% Loading Conditions for 26V Input Voltage.

Parameter	**Output1 (+24V)**	**Output2 (+12.7V)**	**Output3 (+3.8V)**	**Output4 (+5.6V)**
Input Current (A)	5.132			
Output Voltage (V)	23.918	12.712	3.804	5.618
Load Current (A)	4.30	0.25	1.00	0.10
Output Power (W)	102.8	3.2	3.8	0.6
Total Output Power (W)	110.4			
Input Power (W)	133.4			
Total Loss (W)	23.0			
Efficiency (%)	82.7			
Ripple(mV)	98.0	60.0	31.2	45.0

Ripple voltage is the ac component presented in DC voltage. Ripple voltage is the important factor that decides the quality of the DC output voltage. Ripple voltages are measured for different load conditions at different input voltage ranges.

Snubber circuits are used to protect the switch. RCD snubber has losses due to the presence of resistive element. Energy regenerative snubber is lossless and helps in improving efficiency.

The input voltage applied here is 37V. For this the all the four outputs are regulated. Table 6.4 shows 100% Loading Conditions for 45 V Input Voltage. The readings of output voltage, output current, output ripple voltage and the calculated efficiency is obtained and the output voltage ripple obtained is within the specification.

Table 6.4: 100% Loading Conditions for 37 V Input Voltage.

Parameter	Output1 (+24V)	Output2 (+12.7V)	Output3 (+3.8V)	Output4 (+5.6V)
Input Current (A)	3.641			
Output Voltage (V)	23.909	12.693	3.802	5.616
Load Current (A)	4.30	0.25	1.00	0.10
Output Power (W)	102.8	3.2	3.8	0.6
Total Output Power (W)	110.3			
Input Power (W)	134.7			
Total Loss (W)	24.4			
Efficiency (%)	81.9			
Ripple(mV)	92.0	82.0	33.6	42.0

The input voltage applied here is 45V. For this the all the four outputs are regulated. Table 6.4 shows 100% Loading Conditions for 45V Input Voltage. The readings of output voltage, output current, output ripple voltage and the calculated efficiency is obtained. And the output voltage ripple obtained is within the specification

Table 6.4: 100% Loading Conditions for 45 V Input Voltage.

Parameter	Output1 (+24V)	Output2 (+12.7V)	Output3 (+3.8V)	Output4 (+5.6V)
Input Current (A)	3.027			
Output Voltage (V)	23.917	12.691	3.804	5.616
Load Current (A)	4.30	0.25	1.00	0.10
Output Power (W)	102.8	3.2	3.8	0.6
Total Output Power (W)	110.4			
Input Power (W)	136.2			
Total Loss (W)	25.8			
Efficiency (%)	81.0			
Ripple(mV)	90.0	60.0	31	42.0

6.1 Summary

Simulation of the circuits were carried out and obtained the waveforms for the same circuits. Hardware implementation is carried out and readings for various input voltages were noted down.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

Linear power supplies has drawbacks like low efficiency, difficulties in thermal management and boosting the output voltage. These drawbacks are overcome by Switch Mode Power Supplies (SMPS). Space applications require power supplies include lighter, smaller, more efficient and highly reliable. SMPS is best suited for space applications as they have all the required qualities. Multiple output DC-DC converters are used in space applications because of the requirement of different voltage levels. Regulation of individual outputs is the problem with multiple output DC-DC converter. Post regulators are used to regulate the output. Linear regulators, independent switches are used as post regulators, but they have drawbacks like increased number of components, power loss, lower efficiency, increase in cost and size. Conventional voltage mode control uses feedback technique to control the output voltage by controlling the duty cycle. In this control technique, the loop isslow and thus transient response is slow. Current mode control is difficult to design because of the requirement of two control loops to regulate the output.

In order to overcome the problems, a forward converter with two outputs followed by Feed-Forward Control with Voltage Mode is designed. Voltage feed forward control technique isused to control the duty cycle. This control technique is simple to design and results in betterline regulation. The converter has been designed with 250kHz switching frequency using UC15252VTD1 PWM controller. It has functional benefits such as reduction in transformersize and better efficiency Various protection features such as short circuit protection, outputover voltage protection and input under voltage protection have been implemented.

7.1 Conclusion

Multiple Output Forward Converter with Feed-Forward Control for Space Application has been designed. The selected topology is Forward Converter. The main components include PWM Controller IC, Driver Circuit, MOSFET Switch and Transformer. The software analysis has been carried out by using LT Spice. The simulation results shown that the Multiple Output Voltages obtained were 24 V,12.7, 3.8 V & 5.6 V and the Output Currents obtained were 4.3 A,0.25A, 1A & 0.1 A respectively. The same results are obtainedfor Hardware Implementation. The obtained efficiency is more than 80%, and obtained Output Voltage Ripple is less than 50 mVp-p.

7.2 Future Scope

There is scope for future improvement of the converter. They are as listed are

- Further GaN (Gallium Nitride) material switch can be used instead of Silicon material MOSFET Switch to reduce losses and to improve the efficiency of the Converter.
- The frequency of operation can be further increased to reduce the size of magnetic components.
- Efforts to increase the efficiency can be made by implementing synchronous rectifiers at the output side instead of using diodes

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APPENDIX A

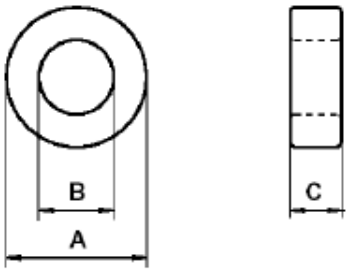
MAGNETICS ®
A Division of Spang & Company

Specification for:

ZP42207TC

110 Delta Drive
Pittsburgh, PA 15238
Phone: 412/696-1333
Fax: 412/696-0333
Email:magnetics@spang.com

DIMENSIONS



(mm)	Uncoated Nominal:	Coated Min:	Coated Max:
O.D. (A)	22.1	21.84	22.86
I.D. (B)	13.7	12.95	13.95
Ht. (C)	7.8	7.84	8.56

Eff. Parameters		
A_e mm^2	l_e mm	V_e mm^3
32.1	54.1	1740

INDUCTANCE

AL value (nH/T^2)	Test conditions
1875 ± 25%	10 kHz, 0.5 mT (For N = 5, use 1 mA), 25°C

CORE LOSSES

P_L max	Production lot limit Max avg	Test conditions
217 mW (124 mW/cm^3)	197 mW (113 mW/cm^3)	100 kHz, 100 mT, 100°C

COATING

Epoxy rated for 200°C continuous operation.
Voltage breakdown rating 1500 V_{DC} Min Wire-to-Wire.

NOTE

Spec. Modifications	Previous	Revised
2006.06.22	Bare Nom Ht = 7.92 Losses: General P material Breakdown voltage > 1,000 V	Bare Nom Ht = 7.8 Losses: Detail as indicated Breakdown voltage > 1,500 V_{DC}

LINEAR TECHNOLOGY

LT3845

High Voltage Synchronous Current Mode Step-Down Controller with Adjustable Operating Frequency

FEATURES

- **High Voltage Operation: Up to 60V**
- **Synchronizable Up to 600kHz**
- **Adjustable Constant Frequency: 100kHz to 500kHz**
- **Output Voltages Up to 36V**
- Adaptive Nonoverlap Circuitry Prevents Switch Shoot-Through
- Reverse Inductor Current Inhibit for Discontinuous Operation Improves Efficiency with Light Loads
- Programmable Soft-Start
- 120µA No Load Quiescent Current
- 10µA Shutdown Supply Current
- 1% Regulation Accuracy
- Standard Gate N-Channel Power MOSFETs
- Current Limit Unaffected by Duty Cycle
- Reverse Overcurrent Protection
- 16-Lead Thermally Enhanced TSSOP Package, 16-Pin PDIP

APPLICATIONS

- 12V and 42V Automotive and Heavy Equipment
- 48V Telecom Power Supplies
- Avionics and Industrial Control Systems
- Distributed Power Converters

DESCRIPTION

The LT®3845 is a high voltage, synchronous, current mode controller used for medium to high power, high efficiency supplies. It offers a wide 4V to 60V input range (7.5V minimum start-up voltage). An onboard regulator simplifies the biasing requirements by providing IC power directly from V_{IN}.

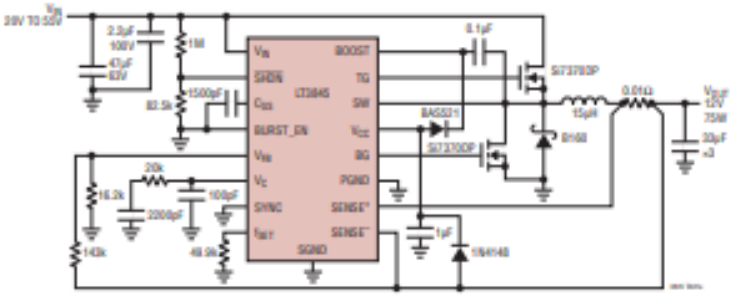
Burst Mode® operation maintains high efficiency at light loads by reducing IC quiescent current to 120µA. Light load efficiency is also improved with the reverse inductor current inhibit function which supports discontinuous operation.

Additional features include adjustable fixed operating frequency that can be synchronized to an external clock for noise sensitive applications, gate drivers capable of driving large N-channel MOSFETs, a precision undervoltage lockout, 10µA shutdown current, short-circuit protection and a programmable soft-start.

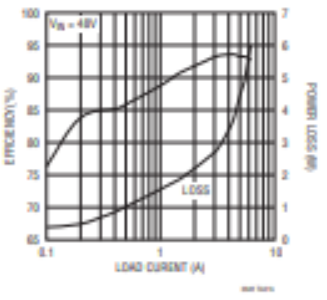
The LT3845 is available in a 16-lead thermally enhanced TSSOP package and 16-pin through hole N package.

TYPICAL APPLICATION

High Voltage Step-Down Regulator 48V to 12V at 75W



Efficiency and Power Loss vs Load Current



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JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

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Implementation of Multiple Output Forward Control with Voltage Feed Forward Control for Space Application

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Abstract: This paper describes the Hardware design and implementation of Forward converter with multiple outputs for remote sensing and image pay load application. The converter is designed to operate at 250kHz by PWM controller. Input Voltage Feed forward control technique is incorporated to attain ±1% line regulation. Synchronous buck converter at secondary side improves efficiency of the converter and low drop regulator is used to regulate output voltage and minimize cross regulation. Converter has Inherent features such as over voltage protection, Input undervoltage protection, short circuit protection and external disable circuit. Under ambient temperature, the electrical test is carried out to validate the design results.

Key Words **- Forward converter, PWM controller, synchronous buck converter, Low drop out regulator, cross regulation**

I. INTRODUCTION

Switched Mode power supplies has become conventional in space grade application [1] than linear power supplies, because of higher efficiency as switching elements avoids operation in active region but operates either in saturation or cut-off region, reduces power losses. The other critical aspects are compact size, lightweight and high reliability to operate under intense temperature conditions [2]. The main applications of SMPS are battery charging, Military, biomedical equipment and electronic devices [3]. Among switch mode power supplies, DC-DC isolated converters are significant to obtain regulated outputs, provides electrical isolation with multiple outputs and are widely used in computer power supplies, uninterrupted power supplies and telecommunication [4]. Forward converter is most used for space application among DC-DC converter because of its high transformer utilization, more efficient and is often chosen for output power under 200W and voltage range of 60V-200V[5].

1.1 Forward converter

Forward converter is magnetically coupled, provides isolation between source and load also it is an isolated version of buck converter. Forward transformer does not store energy hence, ferrite core is most widely used as core material, transforms energy instantly from primary to secondary winding for high power application with

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high voltage conversion ratio[5]. Reset winding has to be provided on the primary side to restore flux to zero vale in every cycle to avoid saturation. The conventional Forward Converter is shown in Fig1.1

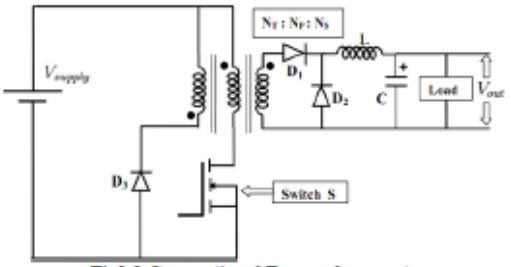

Fig1.1 Conventional Forward converter

Input voltage is applied to primary winding at the time switch S is turned ON. Secondary voltage is reflected based on turns ratio. Diode D1 rectifies voltage and energy is stored in inductance L, is delivered to load during switch S is in OFF condition. freewheeling diode D2 provides path for load current and constant voltage is maintained by output capacitance C.

1.2 Input Voltage Feed forward control Technique

The common voltage mode control technique comprises mainly error amplifier and PWM modulator, an error signal is caused due to difference between sensed output signal through voltage divider with constant reference voltage. Error signal is compared with fixed slope sawtooth signal generates larger error signal as the input voltage is varied and fed back to PWM controller to generate gate pulse for switch operation, increases the response time [7].

In order to improve transient response, input voltage feed forward control technique is incorporated [8] wherein, varying sawtooth signal corresponding to the input voltage is compared with the error signal in response to output voltage to generate gate pulse for the variation in duty cycle in accordance to changes in input voltage to achieve ±1% line regulation [9].

II. Block diagram

The design and realization of 110W with four outputs DC-DC converter is based on the detailed requirements obtained from space application center. The block diagram of converter is shown in Fig.2.1

The Input EMI filter eliminates common mode and differential mode noise generated from switching of power MOSFET and mutual inductance between wires and radiated electromagnetic interferences to meet EMI regulation. The current transformer CT1 sense the primary current. Start up circuit comprise Darlington pair amplifier generates initial voltage of 11V for PWM controller circuit of forward converter to turn ON the MOSFET during first cycle. Bias winding power up all the active components in the circuit and acts as feedback for PWM controller to generate gate pulses for MOSFET at 250kHz. with the switching action of MOSFET, the filtered input voltage is applied to primary side of transformer and transfers energy to secondary side to obtain output voltage according to turns ratio.

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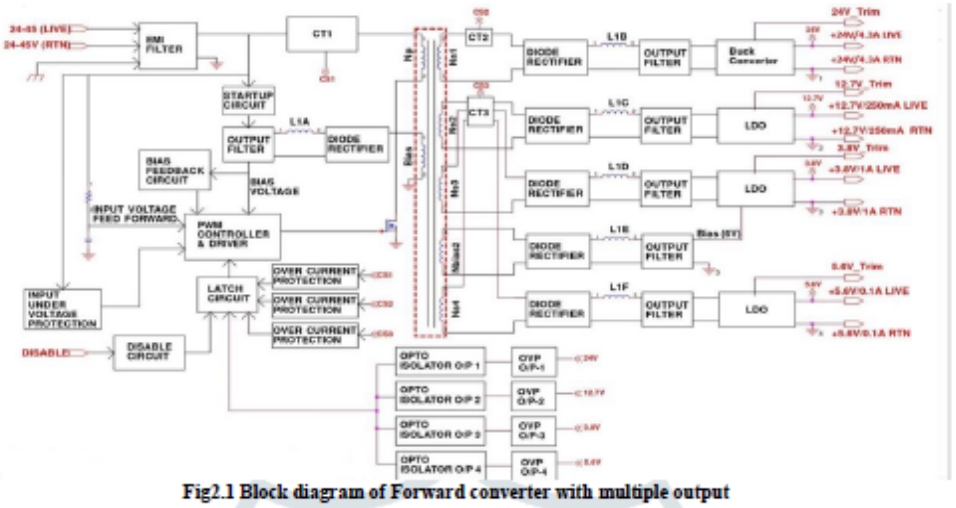

Fig2.1 Block diagram of Forward converter with multiple output

Voltage Feed forward control adjust the duty ratio with the variation in the input voltage to maintain the constant output voltage. The secondary windings generate raw voltage and are coupled using coupled inductor. Secondary raw voltages are rectified by diode rectifier also filtered out by individual output filter and connected to synchronous buck converter for improved efficiency and three LDO to maintain regulated output voltage. All the four outputs 24V,12.7V,5.6V and 3.8V are equipped with the protection circuits such as output overvoltage, Input under voltage, output short circuit, overcurrent and external disable circuit. Current Transformer CT2 sense the secondary output current of synchronous buck converter of 4.3A, one current transformer CT3 for all three LDO since load currents are of low value 0.25A,0.1 and 1A. sync circuit is used to synchronize the switching frequency of main MOSFET and synchronous buck converter MOSFET[7].

2.1Methodology

Forward converters are primarily used for protection purpose due to their isolation and to maintain a regulated output voltage (24V,12.7V,5.6V and 3.8V) over changes in the input voltage from 26V to 45V.The converter is designed to operate at switching frequency of 250kHz to optimize switching losses, mass and size of transformer and output filter. The PWM IC UC2825 is selected because of its high switching frequency, controller is designed for voltage mode with input voltage feedforward capability. It has advantages of soft start, maximum duty cycle control and requires low start up current.

The converter includes EMI Filter, Main Transformer winding, bias winding Coupled Inductors, Diode rectifier, output filter, Snubber Resistor and Capacitor and protection circuit components. components are selected UC2825 DWTR Controller IC, SOIC 16, Diode Rectifier HF40A060ACDV 600V, 30A.The MOSFET Switch BUY25CS45B 250V, 45A, 0.05ohm Rds is selected based on the low Drain to Source on State resistance, low Conduction and Switching losses.

The selected components are embedded on the Printed circuit board using lead and a soldering gun. MOSFET switches are mounted with heat sink that absorbs the heat dissipated by the switch. The printed circuit board (PCB) is connected to a power source using wires. The converter is loaded with 10% to 100% conditions over the input voltage range 26V to 45V, and as the input voltage changes, the output voltage is adjusted by

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feedback from the feedforward voltage mode control that sends the signal to the PWM controller. The controller changes duty cycle to generate gate pulse to MOSFET for the operation of converter. output voltage, current, drain to source voltage are viewed in digital storage oscilloscope.

III. Converter Design

Design of the converter is carried out based on specification obtained from space application centre mainly includes transformer core selection, PWM controller IC, synchronous buck converter IC, Linear drop out regulator IC, MOSFET Switch, diode rectifier, Filter Inductor, Filter Capacitor. Filter Inductor reduces the Output Current Ripple, Filter Capacitor reduces the Output Voltage Ripple.

- Input Voltage Range: 26 V to 45 V
- Output Parameters: 24V /4.3 A: 12.7V /0.25 A: 5.6V/ 0.1A: 3.8V/1A
- Output Power: 110W
- Maximum Duty cycle: 0.6
- Efficiency: ≥80%
- Line regulation: < 1%
- Load regulation: <1%
- Cross regulation: <2%
- Ripple: < 100mV for 24V&12.7V, < 50 mV for 5.6V&3.8V

3.1Transformer Core selection:

Power handling capability and area product of transformer are the two major criteria for the selection of core transformer.

Forward converter Area product is calculated as follows

$$A_p = \frac{\sqrt{D_{max}*(P_{out}+P_{bias})*(1+\frac{1}{Eff})}}{k_w*J*10^{-6}*B_m*f_{sw}} = 4272.89mm^2 \quad (3.1)$$

P_{out} is 110W, total output power of the converter

P_{bias} is power required by bias winding.

An appropriate core is selected to have area product greater than the calculated Ap. Area product (Ap) is provided as the product of the core cross section (Ac) and the window area (Aw).

Selected Toroid Core: ZP-42207TC, Material, Ur:2500, AL: 1875nH/1000T

Turns ratio is calculated as follows

$$T_{ratio\ bias} = \frac{(V_{bias}+V_{LDB})+V_{DB}*D_{max}}{D_{max}*V_{in}} = 0.981 \quad (3.2)$$

V_{bias} is the voltage required for bias winding

$V_{LDB}$is the extra voltage required for regulator

V_{DB} is the voltage drop across diode rectifier

The primary turns of the converter is calculated as follows

$$Np = V_{in(min)} * D_{max} * B_m * A_c * 10^{-6} * f_{sw} = 10 \text{ turns} \quad (3.3)$$

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The calculation of primary winding inductance

$$L_p = {N_p}^2 * A_L = 10^2 * 1875 * 10^{-9} = 188\text{uH} \quad (3.4)$$

3.2 MOSFET selection

MOSFET selection is depending on the Drain to Source voltage (Vds), Drain current (Id), Drain to Source ON state resistance (Rds), Gate charge (Qg), conduction loss, switching loss and Output Capacitance loss (Coss)

$$\text{Conduction loss, } P_{conduction} = 1.25 * R_{ds} * {I_{prms}}^2 \quad (3.5)$$

$$\text{Gate charge loss, } P_{gate} = Q_{gate} * V_{gate} * f_{sw} \quad (3.6)$$

The selected MOSFET is BUY25CS45B, 250V, 45A, 0.05 Ohm

3.3 Low drop out regulator

Low drop out regulator are a simple inexpensive way to regulate an output voltage is powered from a higher voltage input. LDO operates with very small input-output differential voltage called drop out voltage [10]. Constant input voltage is applied to LDO to regulate output voltage for the changes in load. The feedback loop controls the drain to source resistance $R_{ds(on)}$ by varying the gate source voltage, with increased gate source voltage reduces $R_{ds(on)}$ results more drop out voltage to maintain constant output voltage as required. circuit diagram of low drop out regulator circuit is shown in Fig3.1

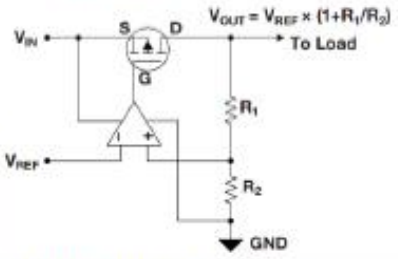

Fig3.1 LDO circuit

IV. Hardware Implementation

Hardware layout of Forward Converter is shown in the Fig4.1. It consists Input connector, EMI filter includes differential mode and common mode filter, Primary side MOSFET, Forward transformer, three LDO, Output Inductor Coupled inductor, Current transformer and output connector.

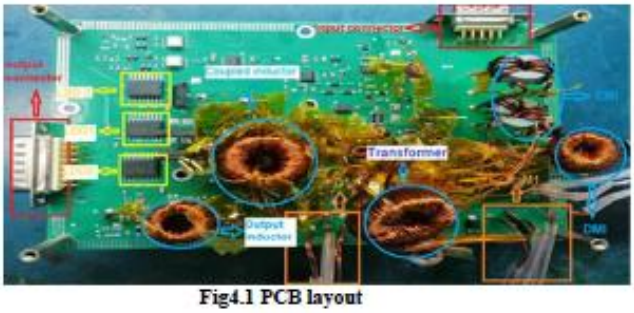

Fig4.1 PCB layout

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4.1Tested waveforms of converter

The converter topology performance is evaluated by observing waveforms of all four output voltages, Mosfet gate pulse to adjust duty ratio for input voltage variation from 26V to 45V, Transformer primary current, output current, ripple voltage is measured for different load conditions from 10% to 100%. The waveform of the ramp signal generated from PWM controller is of 250kHz is shown in Fig4.2

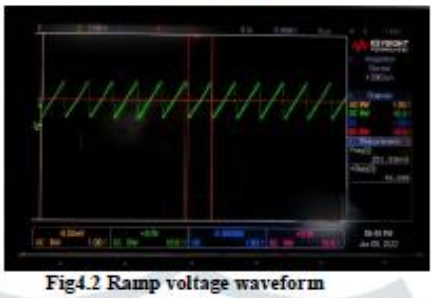
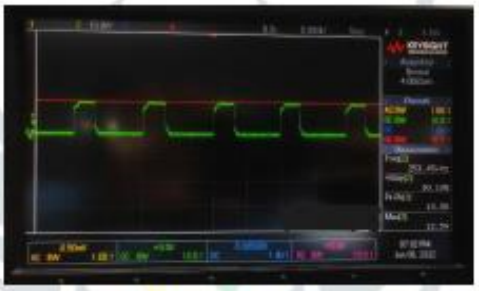


Fig4.2 Ramp voltage waveform

The duty cycle of gate pulse varies according to the input voltage. As input voltage increases, the width of the duty pulse decreases. waveform of gate pulse for 37V with the duty cycle of 30% is shown in Fig4.3

Fig4.3 Gate pulse waveform for 37V



The waveform of drain to source voltage waveform of MOSFET is shown in the Fig4.4. stress on the switch is high without snubber circuit.

Fig4.4 Mosfet drain to source voltage Vds

The secondary side of the forward transformer are designed to get output voltage of 24V from synchronous buck converter with input raw voltage of 36V and other raw voltages of 14V,6V and 4V further connected to LDO regulators to regulate these voltages to 12.7 V, 5.6V and 3.8V respectively is shown in Fig4.5

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Fig4.5 Multiple outputs of forward converter

24V 12.7V 5.6V 3.8V

V. Hardware Experimental Results

The practical values for Output Voltage, Output Current, Output Voltage ripple are shown in the Table 5.1 for 100% Loading Conditions for 37V Input Voltage

Table5.1:100 % Loading conditions for Nominal input voltage 37V

Parameter	Output1 (+24V)	Output2 (+12.7V)	Output3 (+3.8V)	Output4 (+5.6V)
Input Current (A)	3.641			
Output Voltage (V)	23.909	12.693	3.802	5.616
Load Current (A)	4.30	0.25	1.00	0.10
Output Power (W)	102.8	3.2	3.8	0.6
Total Output Power(W)	110.3			
Input Power (W)	134.7			
Total Loss (W)	24.4			
Efficiency (%)	81.9			
Ripple(mV)	75.0	82.0	33.6	42.0

VI. Conclusion

Multiple Output Forward Converter with Feed-Forward Control has been designed and implemented for space application. The main components include PWM Controller IC, Driver Circuit, MOSFET Switch, Transformer, LT3845 IC synchronous buck converter to obtain 24V output and Three UC2834 IC LDO's to regulate output voltage to 12.7V,5.6V and 3.8V. Hardware implementation results ±1% line and load regulation also 80% efficiency was found to be within specified norms

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